THE DATASHEET OF

MAX5040EUB+T

19-2461; Rev 1; 12/03

EVALUATION KIT AVAILABLE

Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

General Description

The MAX5039/MAX5040 provide intelligent control to power systems where two supply voltages need tracking. These cases include PowerPC®, DSP, and ASIC systems, which require a lower CORE voltage supply and a higher I/O voltage supply.

The MAX5039/MAX5040 control the output voltage of the CORE and I/O supplies during power-up, power-down, and brownout situations. They ensure that the two power supplies rise or fall at the same rate, limiting the voltage difference between the CORE and I/O supplies. This eliminates stresses on the processor. The MAX5039/MAX5040 shut down both the CORE and I/O supplies if either one is shorted or otherwise fails to come up.

The MAX5040 provides a power-OK (POK) signal that signals the processor if the CORE supply, the I/O supply, and the system bus supply (V_{CC}) are above their respective specified levels. The MAX5039/MAX5040 are targeted for nominal bus V_{CC} voltages from 4V to 5.5V. The MAX5039/MAX5040 work with CORE voltages ranging from 800mV to about 3V (depending on the gate-to-source turn-on threshold of the external N-channel MOSFET) and I/O voltages ranging from V_{CORE} to 4V. The MAX5039/MAX5040 provide tracking control of the I/O and CORE voltages using a single external N-channel MOSFET connected across them. This MOSFET is not in series with the power paths and does not dissipate any additional power during normal system operation. The external MOSFET is only on for brief periods during power-up/power-down cycling so a low-cost, small-size MOSFET with a rating of 1/4th to 1/8th of the normal supply current is suitable.

The MAX5039/MAX5040 are offered in space-saving 8-pin µMAX and 10-pin µMAX packages, respectively.

Applications

PowerPC Systems

Embedded DSPs and ASICs

Embedded 16- and 32-Bit Controller Systems

Telecom/Base Station/Networking

Typical Operating Circuit and Pin Configurations appear at end of data sheet.

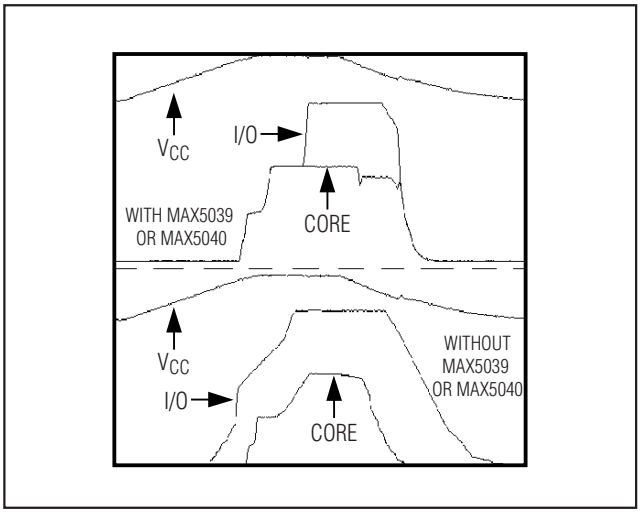
PowerPC is a registered trademark of IBM Corp.

Features

- **Provide Tracking of Two External Power Supplies During Power-Up and Power-Down**
- **Compatible with a Wide Range of External Power Supplies Independent of Output Power**
- **Bus Voltage Undervoltage Lockout Enables/Disables CORE and I/O Supplies Together**
- **Detect Short Circuit on V_{CORE} and $V_{I/O}$, Disable CORE and I/O Supplies in Either Case**
- **Output Undervoltage Monitoring**
- **POK Status (MAX5040)**
- **Operating V_{CC} Supply Voltage Range: 2.5V to 5.5V**
- **I/O Voltage Range: V_{CORE} to 4V**
- **CORE Voltage Range: 0.8V to $V_{I/O}$**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5039EUA-T	-40°C to +85°C	8 µMAX
MAX5040EUB-T	-40°C to +85°C	10 µMAX



Power-On and Power-Off With and Without Voltage Tracking

Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND)
V_{CC}, NDRV, $\overline{SDO}$, and POK .....-0.3V to +14V
CORE_FB, UVLO, I/O_SENSE, I/O, CORE.....-0.3V to +4.25V
All Pins to V_{CC} (except POK)..... +0.3V
NDRV Continuous Current 50mA
Continuous Current, All Other Pins 20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.5mW/°C above +70°C).....362mW
10-Pin µMAX (derate 5.6mW/°C above +70°C).....444mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V to 5.5V, V_{UVLO} = 2V, V_{CORE} = 1.8V, $V_{I/O}$ = 2.5V, V_{CORE_FB} = 1V, V_{I/O_SENSE} = 2V (MAX5040 only), T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EXTERNAL SUPPLY CONDITIONS							
V_{CC}	V_{CC}	(Note 1)		2.5		5.5	V
V_{CC} Supply Current	I_{CC}				1.3	2.25	mA
Lowest V_{CC} Where $\overline{SDO}$ Is Valid	V_{CCLO}	(Note 2)				0.9	V
$\overline{SDO}$ Output Low Voltage at V_{CC} = V_{CCLO}		V_{UVLO} = V_{CC} = V_{CCLO}, $I_{\overline{SDO}}$ = 50µA, measure $V_{\overline{SDO}}$ (Note 2)				0.4	V
V_{CC} IC Turn-On Voltage Threshold (Note 3)		V_{CC} rising			2.43	2.5	V
		Hysteresis			0.05		
CORE Voltage Range	V_{CORE}	I/O and CORE valid, V_{CC} = 5.5V (Notes 4, 5)		0.8		$V_{I/O}$	V
I/O Voltage Range	$V_{I/O}$	I/O and CORE valid (Note 5) V_{CC} > 4V		V_{CORE}		4.0	V
		I/O and CORE valid (Note 5), 2.5V ≤ V_{CC} ≤ 4V		V_{CORE}		V_{CC}	
USER-PROGRAMMABLE UNDERVOLTAGE LOCKOUT							
UVLO Trip Threshold	V_{UVCC}	V_{UVLO} rising		1.200	1.230	1.260	V
		Hysteresis			110		mV
UVLO Input Bias Current		V_{UVLO} = 2V				250	nA
CORE AND I/O REGULATION							
CORE Feedback, CORE_FB, and Reference Voltage	V_{C_REF}			784	800	816	mV
CORE Regulator Large-Signal Gain	A_V	CORE_FB to NDRV			60		dB
CORE Regulator Crossover Frequency		CORE_FB to NDRV			400		kHz
NDRV Output Resistance		Pullup strength, $V_{I/O}$ = 1V, V_{CORE} = 2V, I_{NDRV} = -10mA	V_{CC} ≥ 3V		40	80	Ω
			V_{CC} ≥ 2.5V		50	100	
		Pulldown strength, $V_{I/O}$ = 2V, V_{CORE} = 1V, I_{NDRV} = 10mA	V_{CC} ≥ 3V		13	27	
			V_{CC} ≥ 2.5V		17	35	
I/O-CORE Comparator Trip Threshold (Note 6)	V_{TH}	V_{CORE} - $V_{I/O}$, $V_{I/O}$ falling		60	90	130	mV
		V_{CORE} - $V_{I/O}$, $V_{I/O}$ rising		-15	0	+15	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.5V to 5.5V, V_{UVLO} = 2V, V_{CORE} = 1.8V, $V_{I/O}$ = 2.5V, V_{CORE_FB} = 1V, V_{I/O_SENSE} = 2V (MAX5040 only), T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Amp Gain	A_{VOL}			4000		V/V
CORE Pulldown Resistance		V_{CORE} = 1.8V, V_{UVLO} = 1V, V_{CC} = 2.5V		20	50	Ω
MONITOR OUTPUTS						
$\overline{SDO}$ Output Low Voltage	V_{OLSDO}	$I_{\overline{SDO}}$ = 1.8mA, V_{UVLO} = 1V, V_{CC} = 2.5V			0.4	V
$\overline{SDO}$ Output High Voltage	V_{OHSDO}	$I_{\overline{SDO}}$ = -1.0mA, V_{CC} = 4V	V_{CC} - 0.4V			V
		$I_{\overline{SDO}}$ = -1.0mA, V_{CC} = 2.5V	V_{CC} - 0.55V			
I/O_SENSE Trip Threshold	V_{I/O_REF}	V_{I/O_SENSE} rising	1.200	1.230	1.260	V
		Hysteresis		25		mV
POK Output Low Voltage	V_{OLPOK}	I_{POK} = 1.8mA			0.4	V
POK Leakage Current	I_{LPOK}	V_{POK} = V_{CC}			1.0	µA
POK Glitch Rejection Time	t_{POK}	(Note 7)		50		µs
Fault Time	t_{FAULT}	(Note 8)	10	15	20	ms
I/O and CORE INPUTS						
I/O Input Bias Current		$V_{I/O}$ = 1V			20	µA
CORE Input Bias Current		V_{CORE} = 1V			20	µA
I/O_SENSE Input Bias Current		V_{I/O_SENSE} = 0.8V			250	nA
CORE_FB Input Bias Current		V_{CORE_FB} = 1.2V			300	nA

Note 1: V_{CC} slew-rate limited to 30V/µs.

Note 2: $\overline{SDO}$ automatically goes low when the UVLO pin drops below its threshold (or V_{CC} drops below 2.5V). $\overline{SDO}$ remains low as V_{CC} falls. For some V_{CC} below V_{CCLO} $\overline{SDO}$ may float.

Note 3: This undervoltage lockout disables the MAX5039/MAX5040 at V_{CC} voltages below which the device cannot effectively operate. When V_{CC} drops below the threshold, $\overline{SDO}$ goes low, the bleeder turns off, and POK is high impedance.

Note 4: In order to regulate correctly, V_{CC} must be higher than V_{CORE} plus the turn-on voltage of the external N-channel MOSFET.

Note 5: I/O and CORE valid mean the voltages on these pins have settled within their target specifications for normal operation.

Note 6: CORE and I/O supplies rise and fall rates must be limited to less than 6.6V/µs.

Note 7: POK does not deassert for glitches less than t_{POK}.

Note 8: A fault condition is latched when either of the two following conditions maintains for longer than t_{FAULT}:

$V_{CORE\_FB} < V_{C\_REF}$ (i.e., V_{CORE} is less than its set point)

$V_{I/O} < V_{CORE}$

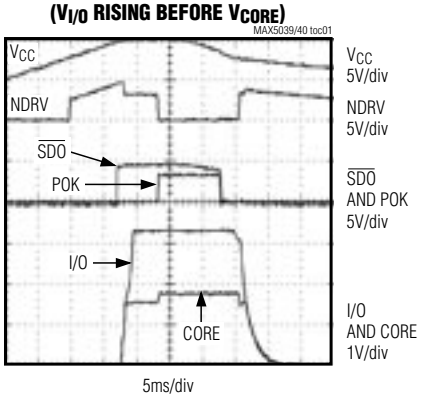
A FAULT condition forces $\overline{SDO}$ and POK (MAX5040 only) low. CORE discharges to GND through 20Ω while V_{CC} > 2.5V. Cycle UVLO or V_{CC} low, then high, to clear a FAULT.

Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

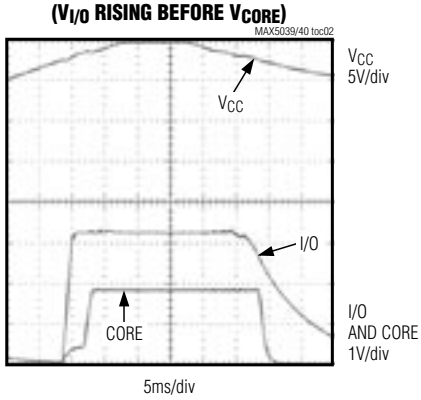
Typical Operating Characteristics

(V_{CC} = 5V, V_{CORE} = 1.8V, $V_{I/O}$ = 3.3V, T_A = +25°C, unless otherwise specified.)

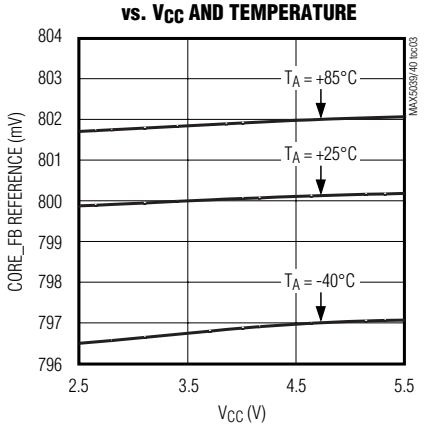
SYSTEM POWER-UP/POWER-DOWN ($V_{I/O}$ RISING BEFORE V_{CORE})



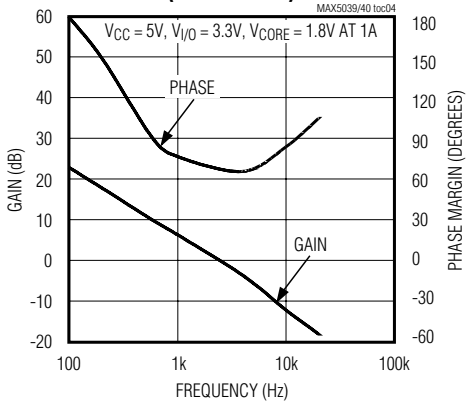
SYSTEM POWER-UP/POWER-DOWN WITHOUT MAX5039/MAX5040 ($V_{I/O}$ RISING BEFORE V_{CORE})



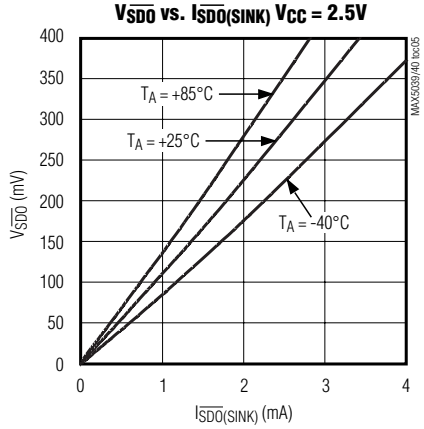
CORE_FB REFERENCE (V_{C_REF}) vs. V_{CC} AND TEMPERATURE



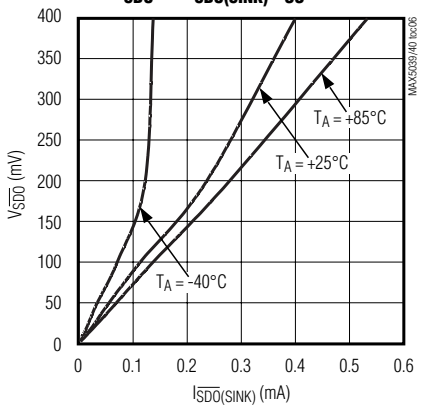
CORE REGULATOR LOOP BODE PLOT (SEE FIGURE 9)



$V_{\overline{SDO}}$ vs. $I_{\overline{SDO}(SINK)}$ V_{CC} = 2.5V



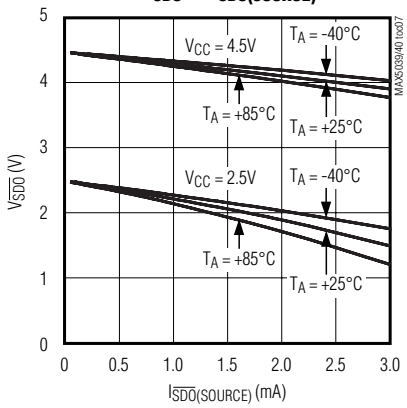
$V_{\overline{SDO}}$ vs. $I_{\overline{SDO}(SINK)}$ V_{CC} = 0.9V



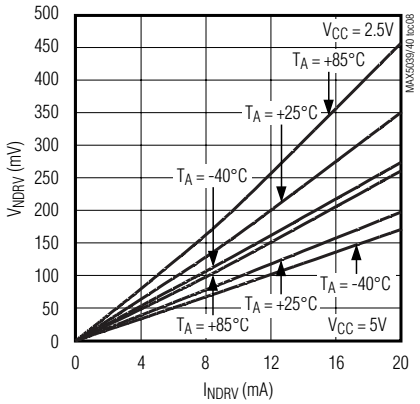
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CORE} = 1.8V, $V_{I/O}$ = 3.3V, T_A = +25°C, unless otherwise specified.)

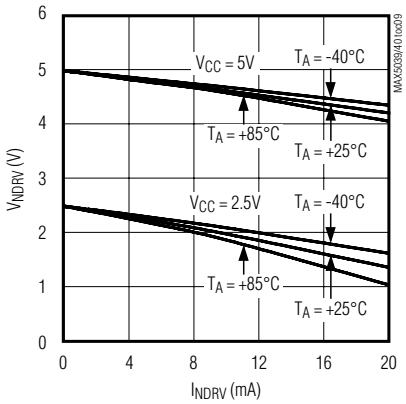
$V_{\overline{SDO}}$ vs. $I_{\overline{SDO}(SOURCE)}$



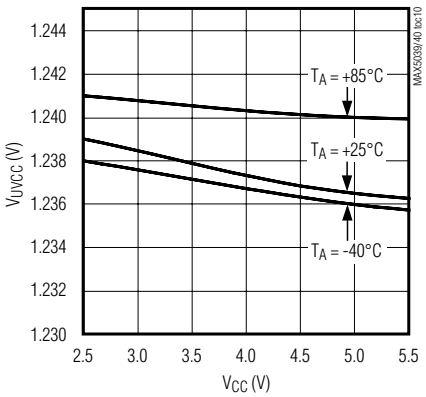
NDRV PULLDOWN STRENGTH



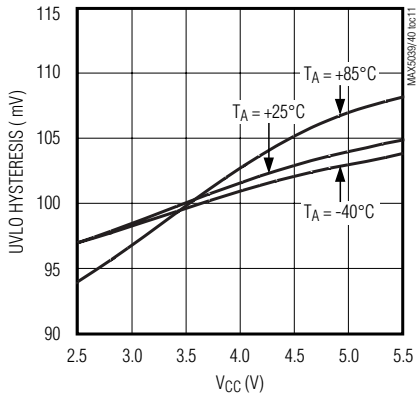
NDRV PULLUP STRENGTH



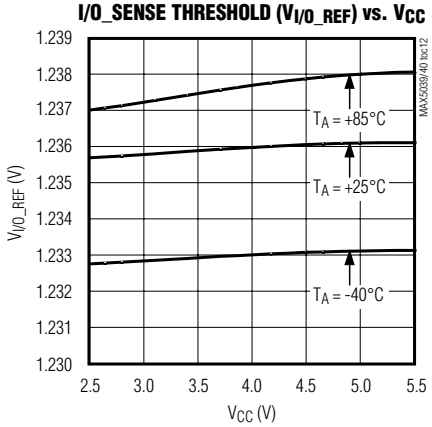
UVLO RISING THRESHOLD vs. V_{CC}



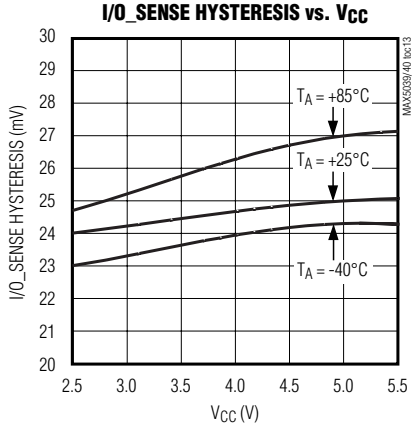
UVLO HYSTERESIS vs. V_{CC}



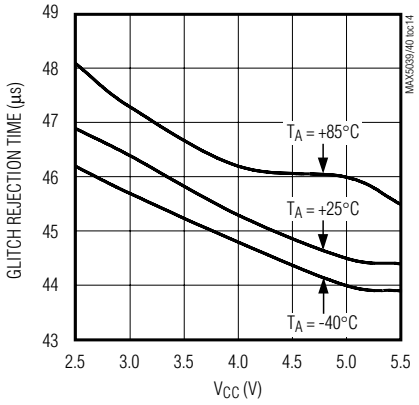
I/O_SENSE THRESHOLD (V_{I/O_REF}) vs. V_{CC}



I/O_SENSE HYSTERESIS vs. V_{CC}



POK GLITCH REJECTION vs. V_{CC}



Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

Pin Description

PIN		NAME	FUNCTION
MAX5039	MAX5040		
1	1	$\overline{SDO}$	Active-Low Shutdown Output. Connect $\overline{SDO}$ to active-low shutdown input of both CORE and I/O supplies. $\overline{SDO}$ is high when $V_{UVLO} \geq V_{UVCC}$ and $V_{CC} \geq 2.5V$ and if there is no fault.
2	2	V_{CC}	Supply Voltage Input. Connect V_{CC} to the supply voltage that powers the CORE and I/O supplies. Bypass V_{CC} to GND with a 1µF capacitor.
3	3	UVLO	User-Programmable Undervoltage Lockout. Connect to midpoint of the voltage-divider from V_{CC} to GND. Set trip point below minimum V_{CC} voltage. $V_{UVLO} \leq V_{UVCC}$ forces $\overline{SDO}$ and POK (MAX5040 only) low. Use UVLO as an active-low shutdown input to turn on/off the CORE and I/O supplies if desired.
4	4	GND	Ground
5	7	CORE_FB	CORE Feedback Input. Connect CORE_FB to the midpoint of the voltage-divider from CORE to GND. The MAX5039/MAX5040 keep CORE_FB from dropping below V_{C_REF} by controlling NDRV. Any time V_{CORE_FB} falls below V_{C_REF}, NDRV rises above ground to a voltage sufficient to maintain $V_{CORE\_FB} = V_{C\_REF}$. If V_{CORE_FB} remains below V_{C_REF} for longer than t_{FAULT}, a latched FAULT is generated. During a FAULT, MAX5039/MAX5040 continue to regulate CORE_FB. Three things halt regulation of CORE_FB: • If V_{CC} falls below 2.5V, NDRV goes to GND. • If I/O falls below CORE, NDRV goes to V_{CC}. • If V_{CORE_FB} rises above V_{C_REF}, NDRV goes to GND.
6	8	CORE	CORE Supply Sense Input. Connect CORE to the core output voltage. If $V_{CORE} > V_{I/O}$, NDRV goes to V_{CC}, POK (MAX5040 only) goes low. FAULT is latched if this condition lasts longer than t_{FAULT}. A 20Ω bleeder discharges CORE to GND whenever $\overline{SDO}$ is low and $V_{CC} > 2.5V$.
7	9	I/O	I/O Supply Sense Input. Connect to I/O output voltage. If $V_{CORE} > V_{I/O}$, NDRV goes to V_{CC}, POK (MAX5040 only) drives low. A FAULT is latched if this condition lasts longer than t_{FAULT}.
8	10	NDRV	N-Channel MOSFET Gate Driver. Connect NDRV to the gate of the external N-channel MOSFET that shunts I/O to CORE.
—	5	I/O_SENSE	I/O Feedback Input. Use a resistor-divider to divide $V_{I/O}$ and apply to this pin. When $V_{I/O\_SENSE} \leq V_{I/O\_REF}$, POK drives low. I/O_SENSE can also be used to monitor any other voltage.
—	6	POK	Open-Drain Power-OK Output. POK drives low when any condition below is true: • $V_{CC} \leq 2.5V$ • $V_{UVLO} \leq V_{UVCC}$ • $V_{CORE\_FB} \leq V_{C\_REF}$ • $V_{I/O} \leq V_{CORE}$ • $V_{I/O\_SENSE} \leq V_{I/O\_REF}$ • MAX5039/MAX5040 latches a FAULT

Performance During Typical Operation

Scope shots are of the MAX5040 EV kit. Figures 1 through 8 demonstrate system performance of the MAX5040 under various power-up, power-down, and fault conditions. In some cases (described in detail below), startup or shutdown of the I/O and CORE supplies were purposely delayed with respect to each other to simulate possible system operating conditions.

In Figure 1 (with MAX5040), V_{CC} ramps up slowly and the I/O supply comes up before the CORE supply. As soon as V_{CC} rises above 2.5V (at about 7.5ms) NDRV goes to V_{CC} shorting the I/O and CORE supplies together. When V_{CC} rises above 4.5V (bringing V_{UVLO} above V_{UVCC}), $\overline{SDO}$ goes high enabling the I/O and CORE supplies. Although the CORE PWM supply turns on 5ms after the I/O PWM supply, both supply voltages come up together because NDRV is held at V_{CC}, shorting the supplies together through the N-channel FET. The I/O supply supports both the I/O line and the CORE line. Once V_{CORE} rises close to its set point, NDRV falls to around 2.8V to regulate V_{CORE} at its set point. At around 22ms, the CORE supply comes up, NDRV goes to GND, and POK goes high. On power-down, when V_{CC} drops low enough to bring V_{UVLO} below V_{UVCC}, $\overline{SDO}$ immediately falls, turning the I/O and CORE supplies off. Simultaneously, POK falls, indicating power-down to the processor. When the I/O voltage drops below the CORE voltage, NDRV goes to V_{CC} (at around 36ms), shorting the supplies together. NDRV remains at V_{CC} until V_{CC} falls below 2.5V and then it returns to GND.

In Figure 2 (without MAX5040), V_{CC} ramps up slowly and the CORE and I/O supplies are turned on when V_{CC} exceeds 2.5V. The I/O voltage comes up before the CORE voltage. There is a 3.3V difference between the I/O and CORE supplies for about 4ms before the CORE supply finally comes up. When V_{CC} powers down, I/O remains high for about 10ms after CORE reaches GND.

In Figure 3 (with MAX5040), V_{CC} ramps up slowly and the CORE supply comes up before the I/O supply. As soon as V_{CC} rises above 2.5V (at about 7.5ms), NDRV goes to V_{CC}, shorting the I/O and CORE supplies together. When V_{CC} rises above 4.5V (bringing V_{UVLO} above V_{UVCC}), $\overline{SDO}$ goes high, enabling the I/O and CORE supplies. Although the I/O PWM supply turns on 8ms after the CORE PWM supply, both supply voltages come up together because NDRV is held at V_{CC}, shorting the supplies together through the N-channel FET. The CORE supply supports both the CORE line and the I/O line until the I/O supply comes up. At around 23ms, the I/O supply turns on, pulling the I/O voltage above the CORE voltage. At this point, the MAX5040 brings NDRV to GND and POK goes high. On power-down, when V_{CC} drops low enough to bring V_{UVLO} below V_{UVCC}, $\overline{SDO}$ immediately falls, turning the I/O and CORE supplies off. Simultaneously POK falls, indicating power-down to the processor. When the CORE voltage drops below its regulation point, NDRV begins to regulate it (at around 30ms). When I/O falls below CORE, NDRV is pulled up to V_{CC} to short the two supplies together.

In Figure 4 (without MAX5040), V_{CC} ramps up slowly and the CORE voltage comes up before the I/O voltage. It takes about 8ms before the I/O supply finally comes up above the CORE supply. When V_{CC} powers down, the supplies do not turn off together. CORE remains high for around 14ms after I/O falls.

In Figure 5 (with MAX5040), the system power-up is attempted with the CORE supply held in shutdown. As soon as V_{CC} rises above 2.5V, NDRV goes to V_{CC}, shorting the I/O and CORE supplies together. Next, when V_{CC} rises above 4.5V (bringing V_{UVLO} above V_{UVCC}), $\overline{SDO}$ goes high, enabling the I/O and CORE supplies. Both supplies come up together because NDRV is high. Note that the CORE supply is still off; CORE is held up through the N-channel FET shunt. Once V_{CORE} rises close to its set point, the linear regulator holds V_{CORE} to its set point by regulating NDRV to around 2.8V. After 15ms of regulating CORE, the MAX5040 latches a fault. $\overline{SDO}$ goes low, NDRV goes to V_{CC}, and both supplies power down together. POK remains low throughout because a valid operating state was not achieved.

In Figure 6 (with MAX5040), V_{CC} is set to 5V. Toggling UVLO from low to high controls system startup. While UVLO is low and the V_{CC} is 5V, NDRV is high, causing the supplies to be shorted together. When UVLO goes high, $\overline{SDO}$ also goes high, turning on the CORE and I/O supplies (at around 3ms). In this example, the I/O supply comes up before the CORE supply. The MAX5040 regulates CORE by driving NDRV to about 2.8V until the CORE supply comes up (at around 7ms), then NDRV falls to GND and POK goes high. When UVLO is driven low, $\overline{SDO}$ goes low, disabling the CORE and I/O supplies. NDRV goes to V_{CC} and both supplies power down together.

In Figure 7 (with MAX5040), V_{CC} is set to 5V. Toggling UVLO from low to high controls system startup. While UVLO is low and the V_{CC} is 5V, NDRV is high, shorting the supplies together while they are both off. When UVLO does go high, $\overline{SDO}$ also goes high, turning on the CORE and I/O supplies (at around 8ms). In this example, the CORE supply comes up before the I/O

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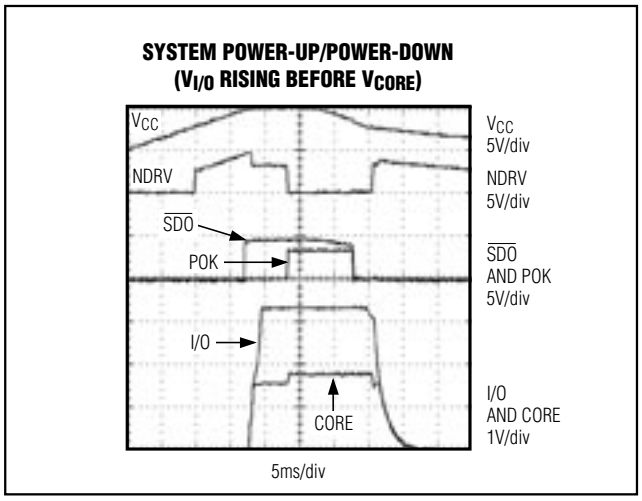

Figure 1. System Power-Up/Power-Down ($V_{I/O}$ Rising Before V_{CORE})

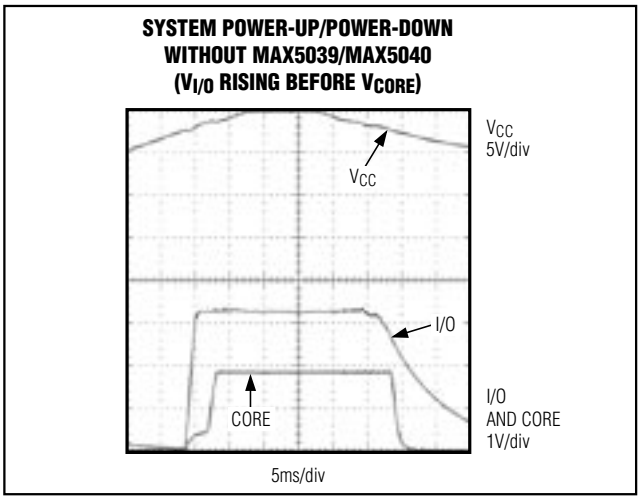

Figure 2. System Power-Up/Power-Down Without MAX5039/MAX5040 ($V_{I/O}$ Rising Before V_{CORE})

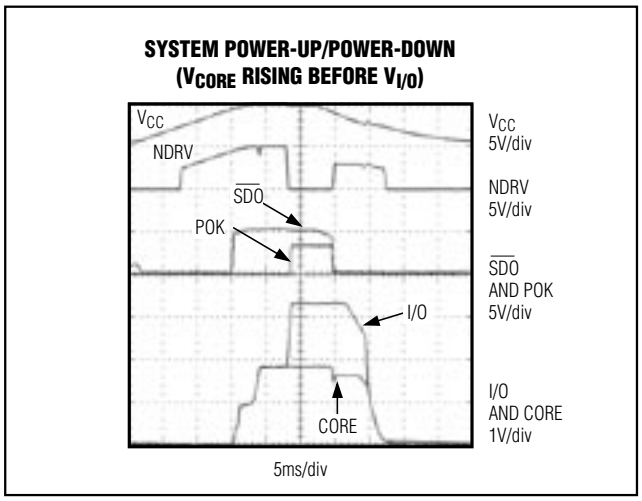

Figure 3. System Power-Up/Power-Down (V_{CORE} Rising Before $V_{I/O}$)

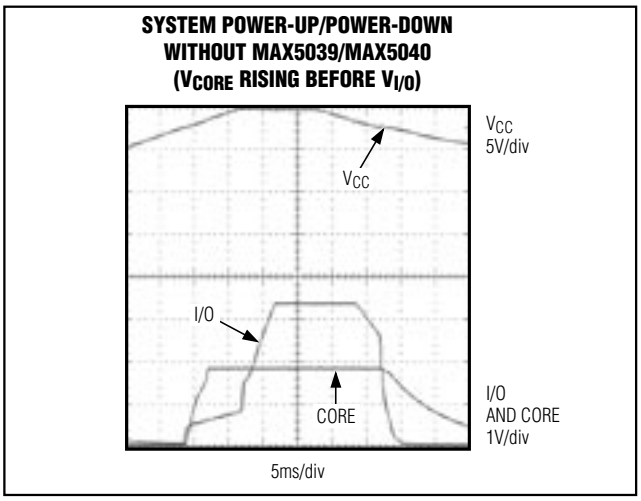

Figure 4. System Power-Up/Power-Down Without MAX5039/MAX5040 (V_{CORE} Rising Before $V_{I/O}$)

supply. The MAX5040 holds up I/O by driving NDRV to V_{CC} (because the I/O voltage is less than the CORE voltage) until the I/O supply comes up (at around 16ms). At this point, NDRV goes to GND and POK goes high. UVLO is driven low (at around 22ms), causing $\overline{SDO}$ to go low, disabling the CORE and I/O supplies. The CORE supply powers down at about 23ms and NDRV goes to 2.8V to regulate the CORE supply until I/O falls. Then NDRV goes to V_{CC} when the I/O voltage falls to the CORE voltage (at around 36ms).

Figure 8 (with MAX5040) starts out with the supplies in their normal range. At 3ms, CORE is shorted to GND. NDRV goes high, and POK goes low immediately. NDRV shorts the I/O supply to the CORE supply, bringing the supplies down together. After 15ms, the MAX5040 latches a fault and $\overline{SDO}$ goes low turning off the supplies.

Detailed Description

The MAX5039/MAX5040 voltage-tracking controllers limit the maximum differential voltage between two power supplies during power-up, power-down, and brownout conditions. The devices provide a shutdown output control signal, $\overline{SDO}$, which is used to turn on

and off the CORE and I/O power supplies. The MAX5039/MAX5040 monitor and compare the CORE and I/O voltages as follows.

When the I/O voltage is greater than or equal to the CORE voltage, MAX5039/MAX5040 regulate the external N-channel MOSFET as a linear regulator by controlling NDRV. The linear regulator regulates the CORE voltage to the value set by the external resistor-divider connected from CORE to CORE_FB and GND (see Figures 9 and 10). If the CORE_FB voltage is far less than its regulation point, V_{C_REF} (800mV), NDRV drives high to V_{CC}, effectively shorting CORE and I/O together through the external MOSFET. If the CORE_FB voltage equals V_{C_REF}, NDRV goes into regulation mode. If the CORE_FB voltage is higher than V_{C_REF}, the linear regulator goes into standby mode and pulls NDRV low, turning off the external N-channel MOSFET.

When the I/O voltage is lower than the CORE voltage by V_{TH} (90mV), the MAX5039/MAX5040 turn the external N-channel MOSFET on by driving NDRV high to V_{CC}.

Whenever $\overline{SDO}$ is high, the MAX5039/MAX5040 track the time that NDRV is in regulation mode or driven high. If NDRV is in regulation mode or driven high for longer than t_{FAULT} (15ms), a fault occurs and $\overline{SDO}$ is pulled low.

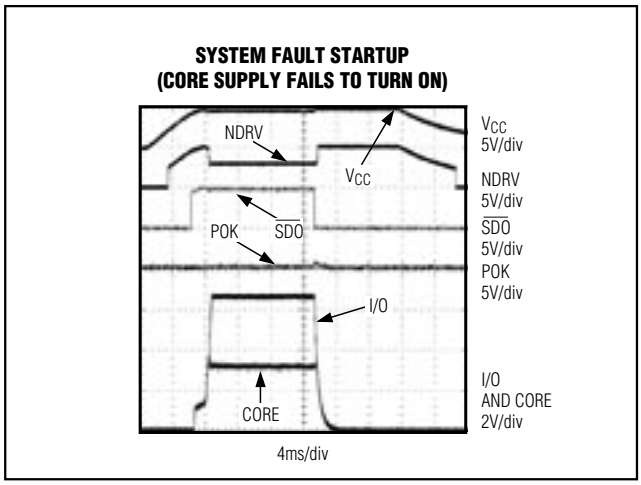

Figure 5. System Power-Up/Power-Down, Fault Startup (CORE Supply Fails to Turn On)

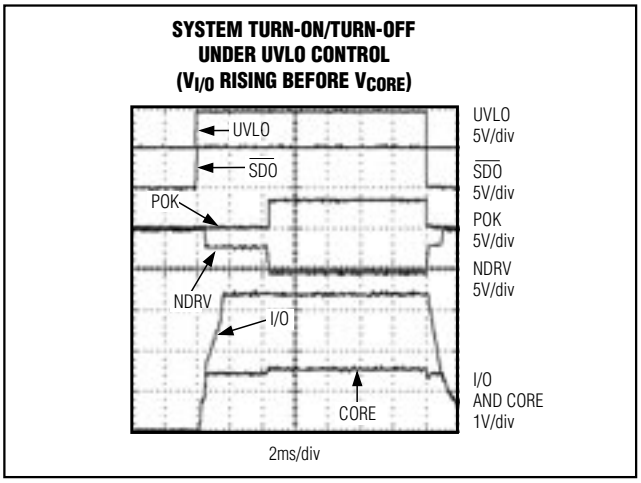

Figure 6. System Turn-On/Turn-Off Under UVLO Control (VI/O Rising Before VCORE)

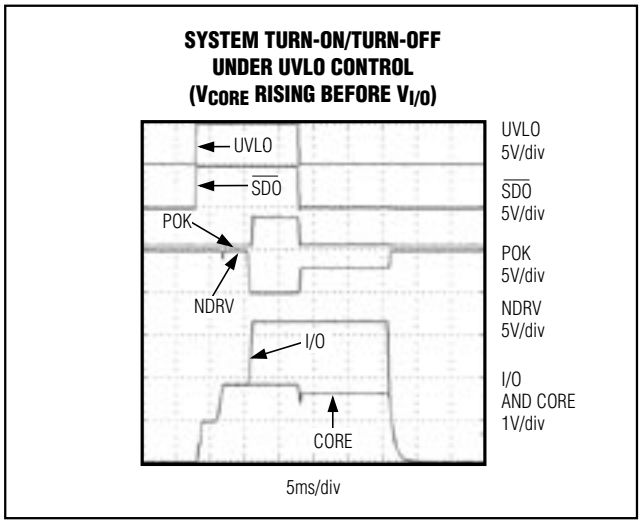

Figure 7. System Turn-On/Turn-Off Under UVLO Control (VCORE Rising Before VI/O)

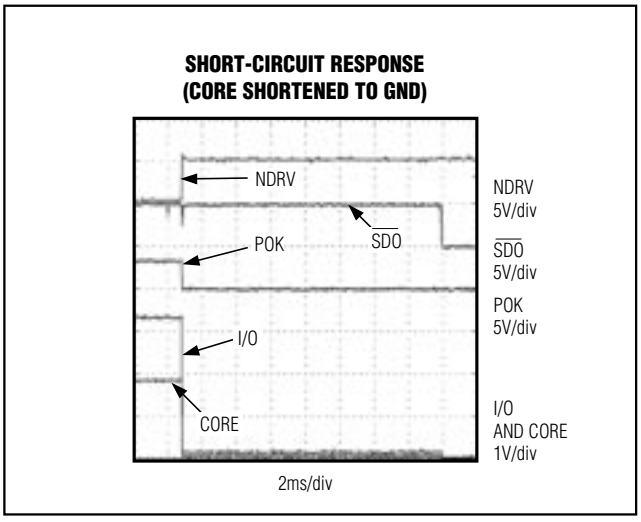

Figure 8. Short-Circuit Response (CORE Shorted to GND)

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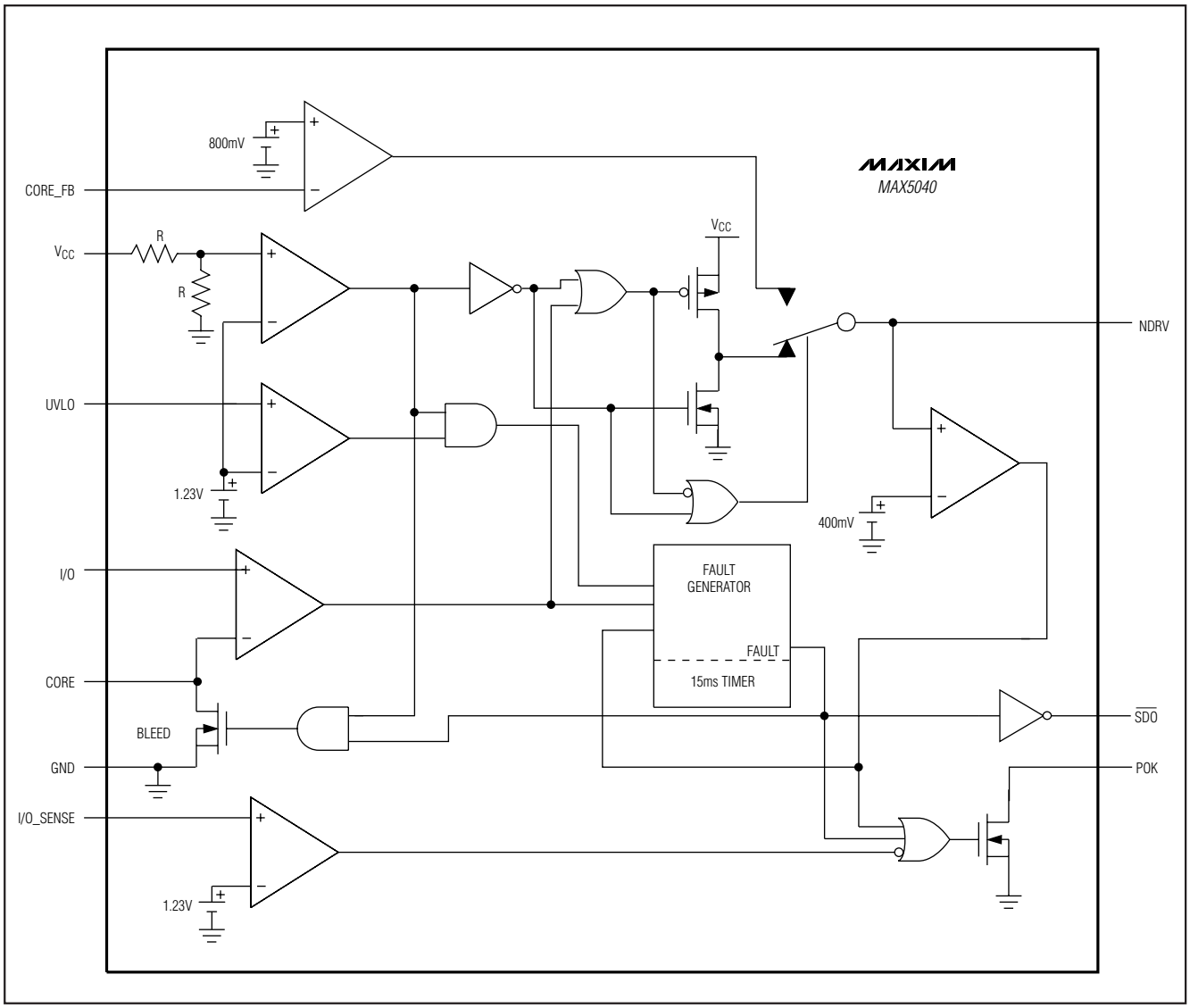
Functional Diagram



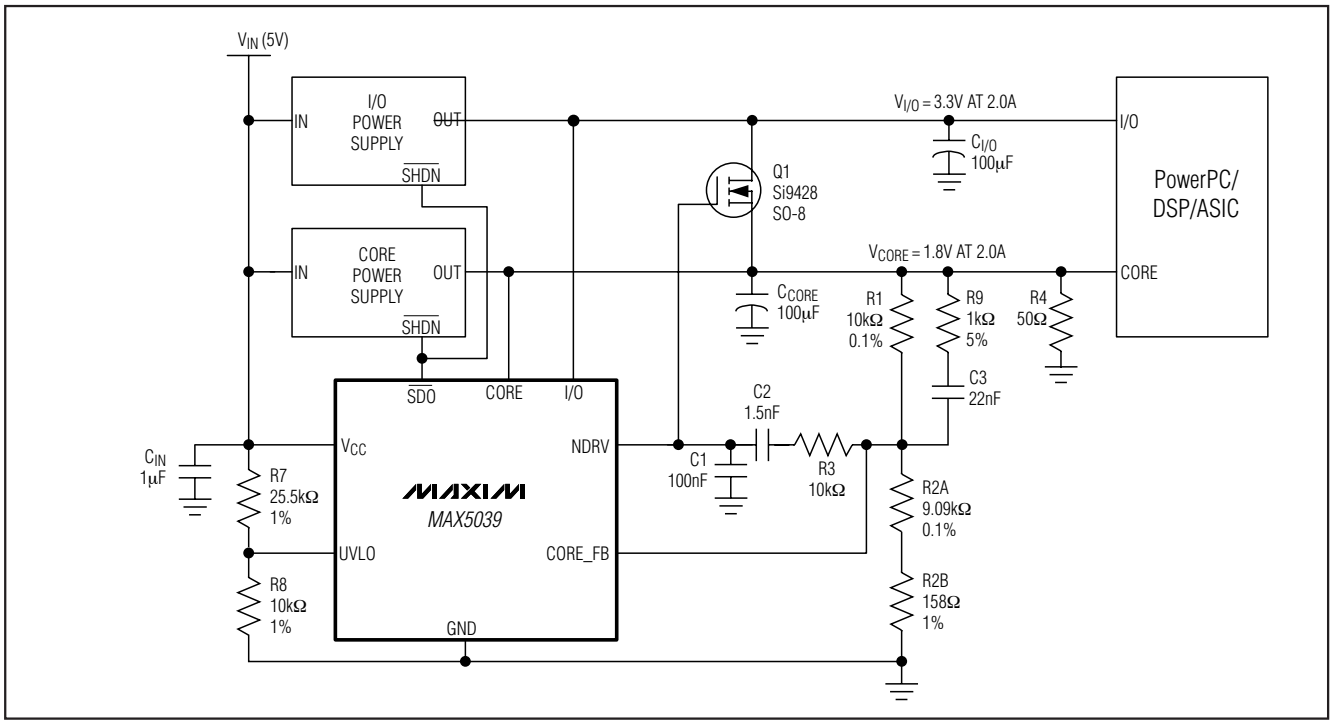


Figure 9. Typical Application Circuit for the MAX5039

Designing with MAX5039/MAX5040

The MAX5039/MAX5040 provide intelligent control to power systems where two power supplies need tracking. Follow the steps below for designing with the MAX5039/MAX5040:

1) Select an appropriate external N-channel MOSFET (see the *N-Channel MOSFET Selection* section).
2) Set the CORE regulation voltage (see the *Programming the CORE Voltage* section).
3) Set the UVLO voltage trip threshold (see the *Programming UVLO Voltage* section).
4) Compensate the CORE linear regulator loop (see the *Linear Regulator Compensation* section).
5) Set the POK voltage trip threshold (MAX5040 only, see the *Programming I/O_SENSE Voltage* section).

Figures 9 and 10 show an application example.

Functional Description

$\overline{SDO}$

$\overline{SDO}$ is the shutdown signal output. Connect $\overline{SDO}$ to the CORE and I/O power-supply shutdown pins. $\overline{SDO}$ allows the MAX5039/MAX5040 to control the turning on and off of the external switching regulators or linear regulators that supply the CORE and I/O voltages. Using this single control signal, the MAX5039/MAX5040 turn the CORE and I/O power supplies on and off together, minimizing the voltage differential between them.

$\overline{SDO}$ is low when:

- The voltage on the UVLO pin is below V_{UVCC} (1.230V).
- V_{CC} is below the IC turn-on voltage threshold (2.43V).
- A fault condition is detected.

The MAX5039/MAX5040 prevent premature turn-on of the CORE and I/O power supplies during power-up by actively holding $\overline{SDO}$ low as soon as V_{CC} rises above 0.9V, provided the condition for $\overline{SDO}$ to stay low is valid.

NDRV

NDRV controls the gate of the external N-channel MOSFET (which is connected between the I/O and CORE voltages), as needed, as long as V_{CC} is within its operating range.

NDRV is driven high to V_{CC} when $V_{I/O} < V_{CORE}$.

NDRV regulates the external MOSFET as a linear regulator when $V_{I/O} > V_{CORE}$ and $V_{CORE\_FB} < V_{C\_REF}$.

NDRV is driven low when $V_{I/O} > V_{CORE}$ and $V_{CORE\_FB} > V_{C\_REF}$.

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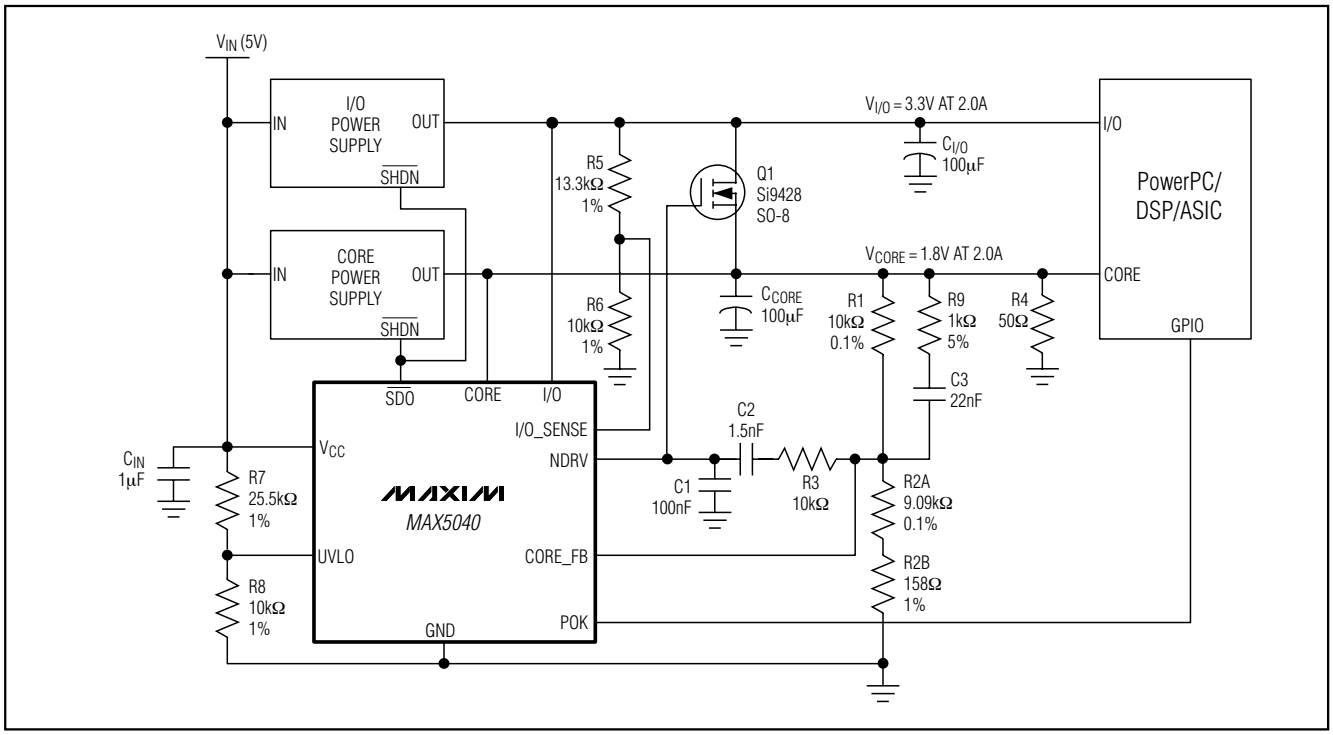

Figure 10. Typical Application Circuit for the MAX5040

UVLO

UVLO is a user-programmable undervoltage lockout input. When the UVLO voltage is above V_{UVCC}, the MAX5039/MAX5040 hold $\overline{SDO}$ high, given that V_{CC} is within its operating range and there is no fault condition present. When the UVLO voltage falls below V_{UVCC}, $\overline{SDO}$ is pulled low. Use a resistor-divider from the input of the CORE and I/O power supplies to UVLO to GND to set the undervoltage lockout (see the *Typical Application Circuit*). The MAX5039/MAX5040 keep the CORE and I/O power supplies off (through the $\overline{SDO}$) until their input voltage is within its operating range.

UVLO can be used to turn off the CORE and I/O power supplies through $\overline{SDO}$. Pull the UVLO pin low with an open-collector driver to assert $\overline{SDO}$, which turns off the power supplies.

Active Bleeder

The MAX5039/MAX5040 contain an internal 20Ω N-channel MOSFET bleeder that connects CORE to ground. The bleeder turns on whenever the MAX5039/MAX5040 hold $\overline{SDO}$ low and V_{CC} is above the V_{CC} IC turn-on voltage threshold (2.43V). This bleeder assists in discharging the output capacitor(s) during power-down/brownout conditions. The MAX5039/MAX5040 maintain tight voltage tracking of the CORE and I/O voltages, as long as V_{CC} is within its operating voltage range. It is important to discharge the output capacitors to ground before V_{CC} drops out of its range. Figure 11 illustrates a method to prolong V_{CC} after a power-down/brownout condition.

The hold-up capacitor, C_{HD}, holds the voltage at V_{CC} up and provides the power to the MAX5039/MAX5040 to keep them in operation even after V_{IN} has gone down.

Power-Up

The MAX5039/MAX5040 prevent premature turning on of the CORE and I/O power supplies during power-up by actively holding $\overline{SDO}$ low as soon as V_{CC} rises above 0.9V, provided the condition for $\overline{SDO}$ to stay low is valid. The MAX5039/MAX5040 completely turn on and NDRV is operational when V_{CC} rises above the V_{CC} IC turn-on voltage threshold (2.43V). In this state, the MAX5039/MAX5040 maintain tight tracking of the CORE and I/O output voltages. The MAX5039/MAX5040 continue to hold $\overline{SDO}$ low until the UVLO voltage rises above V_{UVCC} (1.230V).

Once the UVLO voltage rises above V_{UVCC}, $\overline{SDO}$ goes high, enabling the CORE and I/O power supplies at the same time. Without voltage tracking, depending on the

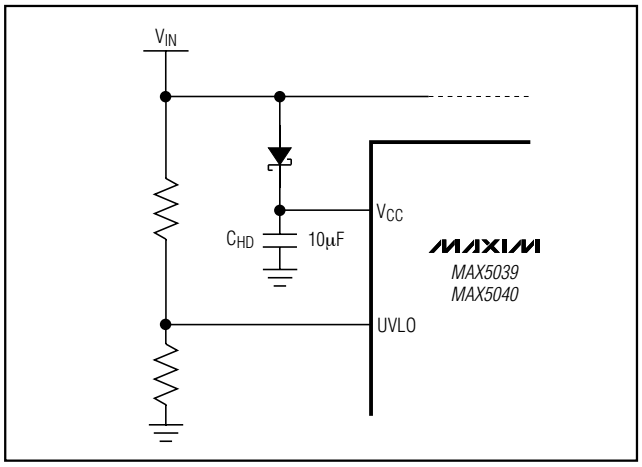

Figure 11. Circuit Prolongs V_{CC} After a Brownout/Power-Down Condition

power supplies startup delay and/or soft-start timing, which are specific to each of the power supplies, CORE and I/O outputs may not rise at the same time or at the same rate. Output loading and capacitance further separate the two output's rise time. The MAX5039/MAX5040 help the system to overcome these differences and keeps CORE and I/O voltages tracking together by controlling NDRV, dynamically driving NDRV high, low, or in regulation mode, depending on the CORE and I/O voltage condition.

Normal Operation

After the power-up period is over, CORE and I/O output voltages settle to their respective regulated values. The linear regulator formed by MAX5039/MAX5040 and the external MOSFET is turned off. During normal operation, the linear regulator goes into a standby mode and NDRV is driven low.

The resistor-divider from CORE to CORE_FB to GND must be set so that the linear regulator regulation voltage is less than the CORE power-supply regulation voltage. See the *Programming the CORE Voltage* section.

During normal operation, the MAX5039/MAX5040 constantly monitor the CORE, I/O, and CORE_FB voltages. NDRV responds as needed, according to the conditions described in the *NDRV* section.

Power-Down/Brownout or Shutdown

The MAX5039/MAX5040 continue to provide tracking for the CORE and I/O output voltages during power-down/brownout or shutdown.

During shutdown (UVLO is pulled below V_{UVCC}), $\overline{SDO}$ is pulled low, disabling the CORE and I/O power supplies together. The CORE and I/O output voltages start to fall. Without voltage tracking, depending on the output capacitance and loading, CORE and I/O voltages may not fall at the same rate. Similar to the power-up condition, the MAX5039/MAX5040 keep CORE and I/O voltages tracking together by controlling NDRV, dynamically driving NDRV high, low, or in regulation mode, depending on the CORE and I/O voltage condition.

During power-down/brownout, V_{CC} is dropping and the UVLO voltage is also dropping. When the UVLO voltage falls below V_{UVCC}, $\overline{SDO}$ is pulled low, disabling the CORE and I/O power supplies. Similar to the shutdown condition, the MAX5039/MAX5040 keep CORE and I/O voltages together. It is important that V_{CC} remains in its operating voltage range in order to keep the MAX5039/MAX5040 operating to provide tracking until the output voltages have discharged to a safe level. Figure 11 illustrates a method to prolong V_{CC} after a power-down/brownout condition. The bleeder circuitry is helpful in this power-down/brownout condition because the bleeder helps speed up the discharge process.

FAULT Condition

While $\overline{SDO}$ is high, the MAX5039/MAX5040 keep track of the time NDRV is driven high or in regulation mode. In a typical system during power-up, power-down/brownout, and normal operation, the time NDRV is driven high or in regulation mode should last for only a few milliseconds. If this time exceeds t_{FAULT} (15ms), indicating an abnormal condition, a fault is generated. During a fault condition, $\overline{SDO}$ is driven low and NDRV continues its operation as described in the *NDRV* section.

A fault condition is latched. To clear a fault, toggle V_{CC} and/or UVLO to unlatch and restart the system.

Output Short-Circuit Condition

If any of the outputs are shorted to ground, NDRV is driven high to keep the CORE and I/O voltages tracking each other. The current through the external MOSFET is limited by the current limit provided by the external power supply. If the short-circuit condition lasts more than t_{FAULT}, a fault is generated, $\overline{SDO}$ is driven low (which turns off the CORE and I/O power supplies), and NDRV continues its operation as described in the *NDRV* section.

Applications Information

N-Channel MOSFET Selection

The external N-channel MOSFET connected between CORE and I/O power supplies is expected to turn on briefly during power-up and power-down/brownout conditions. During normal operation, this MOSFET is turned off. In general, only a small size MOSFET is needed. A MOSFET capable of carrying 1/4th to 1/8th

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of the maximum output current rating of the CORE or I/O power supplies is adequate. However, care should be taken when selecting this MOSFET to make sure it is capable of sustaining all of the worst-case conditions, as well as riding through all of the fault conditions. The following are guidelines for selecting the external N-channel MOSFET:

1) MOSFET drain-to-source maximum voltage rating: V_{DS} rating > $V_{I/O}$ maximum voltage.
2) MOSFET gate-to-source maximum voltage rating: V_{GS} rating > V_{CC} maximum.
3) MOSFET gate turn-on threshold voltage: $V_{GS(th)}$ < minimum operating voltage of (V_{CC} - V_{CORE}). For example, if V_{CC} minimum operating voltage is 4.5V, CORE voltage is 1.8V, then $V_{GS(th)}$ < (4.5V - 1.8V) = 2.7V. A MOSFET with logic-level gate turn-on threshold voltage is appropriate for this application.
4) Determine the maximum current that can go through the MOSFET during power-up, power-down/brownout, or output short-circuit conditions. In most cases, this maximum current is the current limit of the CORE or the I/O power supplies, whichever is larger. Choose the MOSFET with pulse current rating sufficiently higher than this current. Note that typical MOSFET pulse current rating is much larger than its continuous current rating.
5) Determine the MOSFET maximum R_{DSON} such that under worst-case current, the voltage drop across its drain-to-source is within the tracking limit (approximately 400mV for most PowerPCs, ASICs, and DSPs).
6) Determine the maximum single-shot power dissipation in the MOSFET during power-up, or during an output short-circuit condition. Considering the following cases:
   - When either the I/O or CORE is shorted to GND, NDRV is driven high to V_{CC}, turning the MOSFET on. The current through the MOSFET is the maximum current that the supply not shorted can produce (the CORE supply maximum current if I/O is shorted or vice versa). Depending on which supply is shorted, take the maximum short-circuit current that either the I/O or CORE supplies produce. Call this current I_{PSLIM}. In this case, the power dissipation in the MOSFET is $I_{PSLIM}^2 \times R_{DS(ON)}$.
   - During power-up, the I/O voltage comes up first, and the CORE power supply fails to turn on. The MOSFET is in linear regulator mode, supporting the CORE full-load current, as well as the charging of the CORE output capacitor. For most practical cases, the power charging the CORE output capacitor can be ignored. The power dissipation in the MOSFET for this case is ($V_{I/O}$ - V_{CORE}) x I_{CORE}, where $V_{I/O}$ is the regulated I/O voltage, V_{CORE} is the regulated CORE voltage, and I_{CORE} is the CORE full-load current.
   - During power-up, the CORE voltage comes up first, and the I/O power supply fails to turn on. The MOSFET turns on hard, keeping the I/O voltage close to the CORE voltage. The MOSFET in this case supports the I/O load current, as well as the charging of the I/O output capacitor. For most practical cases, the power charging the I/O output capacitor can be ignored. Since the I/O voltage never reaches its final value, the I/O load current might be off and the power dissipation in the MOSFET is minimal. However, assuming the worst-case condition that the I/O load draws its full-load current, the power dissipation in the MOSFET would be $I_{I/O}^2 \times R_{DS(ON)}$, where $I_{I/O}$ is the I/O full-load current.

   The worst-case single-shot power dissipation in the MOSFET is the maximum value from the steps above and for a maximum duration of t_{FAULT}.
7) Next, select the MOSFET that can take this single pulse energy without going over its maximum junction temperature rating. The maximum MOSFET junction temperature can be calculated as follows:

$$T_J = T_{AMB} + P_{PULSE} \times Z_{\theta JA}$$

   where T_J is the junction temperature, T_{AMB} is the ambient temperature, P_{PULSE} is the single-shot power dissipation calculated in step 6 above, and $Z_{\theta JA}$ is the junction-to-ambient thermal impedance of the selected MOSFET for a single pulse of t_{FAULT} duration. $Z_{\theta JA}$ is specified in all typical MOSFET data sheets.

Example: I/O = 3.3V, I/O power supply has a current limit ($I_{I/O(LIM)}$) of 6A, I/O full-load current is 3A. CORE is 1.8V, CORE power supply has a current limit ($I_{CORE(LIM)}$) of 6A, CORE full-load current is 4A. V_{CC} = 5V + 0.5V. CORE and I/O voltages must track to within 400mV.

Choose a Si9428DY (N-channel MOSFET, V_{DS} max = 20V, $R_{DS(ON)}$ at +25°C = 0.04Ω at V_{GS} = 2.5V, $R_{DS(ON)}$ at +125°C = 1.5 x $R_{DS(ON)}$ at 25°C, from the MOSFET data sheet, V_{GS} max = 8V).

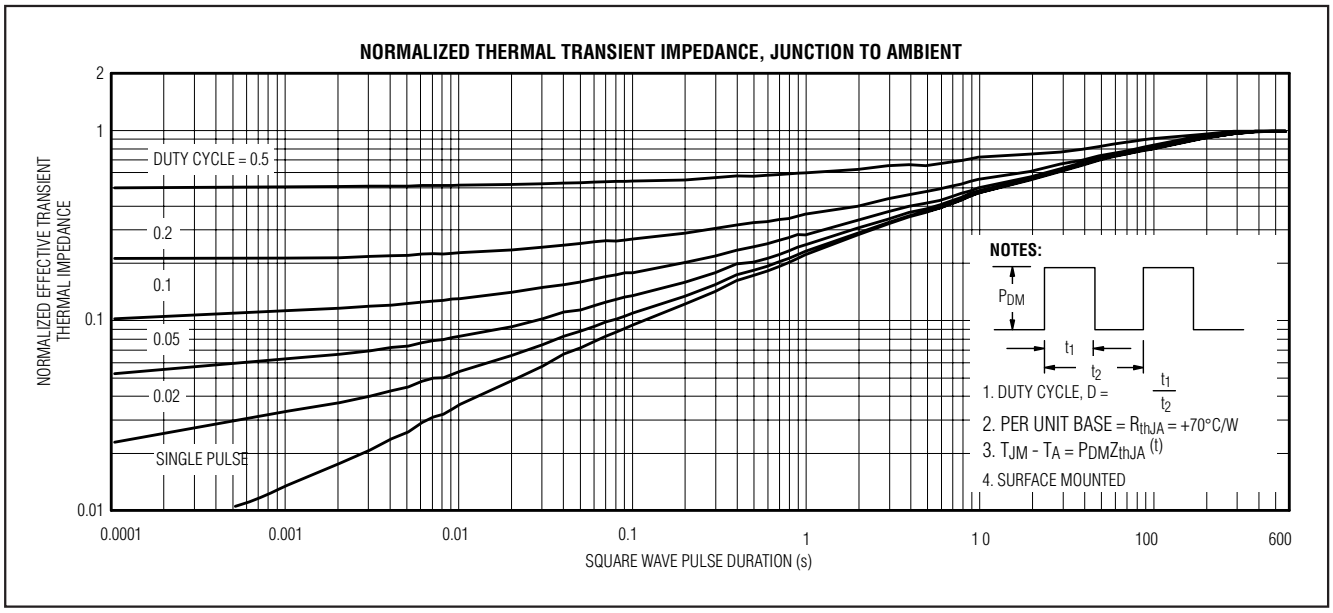

Figure 12. Normalized Thermal Transient Impedance

From step 5: the maximum $V_{I/O}$ and V_{CORE} differential voltage = ($I_{CORE(LIM)}$) x ($R_{DS(ON)}$) = 6A x 0.04Ω x 1.5 = 360mV.

From step 6 (first bullet): power dissipation = I_{PSLIM}^2 x $R_{DS(ON)}$ = $(6A)^2$ x 0.04Ω x 1.5 = 2.16W.

From step 6 (second bullet): power dissipation = ($V_{I/O}$ - V_{CORE}) x I_{CORE} = (3.3V - 1.8V) x 4A = 6W.

From step 6 (third bullet): power dissipation = $I_{I/O}^2$ x $R_{DS(ON)}$ = $(3A)^2$ x 0.04Ω x 1.5 = 0.54W.

So, the worst-case power dissipation in the MOSFET is 6W for a maximum duration of 20ms. From the Si9428DY data sheet, under the normalized thermal transient impedance curve (Figure 12), the $Z_{\theta JA}$ is 0.05 x +70°C/W for a single pulse. The worst-case junction temperature of the MOSFET at +85°C ambient temperature is:

$$T_J = T_{AMB} + P_{PULSE} \times Z_{\theta JA}$$
$$= +85°C + 6W \times 0.05 \times +70°C/W = +106°C$$

Programming the CORE Voltage

See the application circuit examples in Figures 9 and 10. The following explains constraints on the CORE voltage.

The high-side constraint requires that the CORE regulator maintain a minimum voltage during normal operation. The low-side limit requires that the CORE regulator hold the CORE voltage such that the voltage difference from I/O to CORE does not exceed the processor's maximum allowable voltage difference:

To calculate the high-side limit, set the maximum CORE voltage set point at the minimum system CORE voltage minus the total system tolerance:

$$CORESET_{MAX} = CORE_{MIN} - TOL$$

(TOL = Total Tolerance)

Calculate the low-side constraint by taking the maximum system I/O voltage, subtracting the maximum allowable I/O to CORE difference and adding the total system tolerance.

$$CORESET_{MIN} = I/O_{MAX} - \Delta V_{I/OC} + TOL$$

The following comprise the sources for the total system tolerance:

- Resistor resolution error
- Resistor tolerance error
- Resistor temperature drift (TCR) error
- MAX5039/MAX5040 reference error
- Loop-gain error

For example:

- V_{CORE} = 1.800 ±5%
- $V_{I/O}$ = 3.300 ±5%
- Maximum voltage that I/O can exceed CORE without damage to the processor:

$$\Delta V_{I/OC} = (V_{I/O} - V_{CORE})_{MAX} = 2V$$

- System minimum gain = 1000V/V

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Resistor tolerance error:

$$ERROR_{RESTOL}(\%) = RES\_TOL\ (\%) \times 2 \times (1\text{-}Ratio)$$

where:

$$Ratio = \frac{V_{C\_REF}}{V_{REGNOM}} = \frac{800mV}{V_{REGNOM}}$$

If the nominal CORE set point is 1.6V, the ratio is 800mV/1600mV = 0.5. With 1% resistors, the resistor error is:

$$ERROR_{RESTOL}(\%) = \pm 1\% \times \{2 \times (1 - 0.5)\} = \pm 1\%$$

Resistor temperature coefficient error:

$$ERROR_{RES\text{-}TCR} = 100 \left(Ratio \left\{ 1 + \frac{R1\left[1+\left(TCR \times \Delta T\right)\right]}{R2\left[1-\left(TCR \times \Delta T\right)\right]} \right\} - 1 \right)$$

A similar value applies when the (+) and (-) are reversed in the above quotient. TCR is expressed in parts per million. One-percent chip resistors are typically specified at ±100ppm while 0.1% resistors are specified at ±25ppm.

Resistor Resolution Error: This error can be negligible when R2 is split into two parts, a high-value 0.1% resistor in series with a low-value 1% resistor to trim the final value.

MAX5039/MAX5040 reference error: ±2.0% by specification.

Loop-gain error: This error is due to the finite system gain.

$$ERROR_{GAIN} = 100 \left(\frac{A_{OL} \times Ratio}{\left(A_{OL} \times Ratio\right)+1} - 1 \right)$$

$$= 100 \left(\frac{1000 \times 0.5}{\left(1000 \times 0.5\right)+1} - 1 \right)$$

Table 1. Error Summation

ERROR SOURCE	AMOUNT (1% Res.) (%)	AMOUNT (0.1% Res.) (%)
Resistor Tolerance	±1.0	±0.1
Resistor TCR (-40°C/+85°C)	±0.55	±0.14
Reference Voltage	±2.0	±2.0
Loop-Gain Error	0 to -0.2	0 to -0.2
Total = TOL	+3.55/-3.75	+2.24/-2.44

A minimum but unspecified loop gain of 1000 yields a -0.2% gain error. No positive gain error is possible.

Calculate the maximum and minimum regulator core voltage set point as follows:

$$CORESET_{MAX} = CORE_{MIN} - TOL = (1.8V - 5\%) - 2.5\%$$
$$= 1.8V \times 92.5\% = 1.665V$$

$$CORESET_{MIN} = I/O_{MAX} - \Delta V_{I/OC} + TOL$$
$$= ((3.3V + 5\%) - 2V) + 2.5\%$$
$$= (3.465V - 2V) \times 102.5\%$$
$$= 1.465V \times 102.5\% = 1.5016V$$

Set the CORE voltage set point (V_{REGNOM}) between 1.5016V and 1.665V and as close to the upper value (1.665V) as possible.

Connect the midpoint of a voltage-divider between CORE and GND to CORE_FB, as shown in Figure 10. Set the midpoint voltage to 800mV for a maximum CORE voltage set point of 1.665V.

Choose a value for R1 of 10kΩ.

Calculate R2 with the following equation:

$$R2 = \frac{R1}{\frac{V_{REGNOM}}{V_{C\_REF}} - 1}$$

Example:

$$R2 = R1 = \frac{R2 \times V_{C\_REF}}{V_{REGNOM\ -1}} = \left(\frac{0.8V}{1.665V - 0.8V}\right) 10k\Omega$$
$$= 9.24855k\Omega$$

Using a standard 9.09kΩ (±0.1%) resistor in series with a 158Ω (1%) resistor yields negligible resolution error.

Programming UVLO Voltage

See the application circuit examples in Figures 9 and 10.

The MAX5039/MAX5040 provide a user-programmable undervoltage lockout feature through the UVLO pin. When using a resistor-divider, R7 and R8, from an input voltage rail (V_{IN}) to UVLO to GND, the user-programmable UVLO feature allows V_{IN} to get to a certain value before MAX5039/MAX5040 turn the system power supplies on together. V_{IN} is usually the input voltage to the system power supplies and it can be the same as V_{CC}. The UVLO pin also provides the system a way to turn on/off the system power supplies (see the *UVLO* section). Choose the UVLO trip point such that the minimum V_{IN} voltage exceeds the maximum UVLO rising

threshold. Follow the guidelines below to program the UVLO voltage:

1) Determine the V_{IN} tolerance; ±5% is common.
2) Determine the V_{UVLO} rising threshold tolerance:

   Undervoltage lockout rising trip threshold, V_{UVCC}, tolerance: 1.230V ±2.5%

   Programming resistor tolerance: pick a ±1% resistor or better (±1.6% over temperature from Table 1)

   Resistor-divider ratio tolerance: ±1% maximum for ±1% resistors

   Resistor value resolution: ±0.5% (can be zero if exact resistor value is available)

   Extra margin: ±1%

   Total = ±6.6%
3) Set V_{UVLO} nominal value to:

   V_{IN} nominal value - (V_{IN} tolerance + V_{UVLO} tolerance)
4) Calculate R7 using the equation:

$$R7 = \left(\frac{V_{UVLONOM}}{V_{UVCC}} - 1\right) R8$$

where R8 is typically 10kΩ.

Example: V_{IN} nominal value = 5V, V_{IN} tolerance = ±5V%; set the V_{UVLO} nominal value to 5V - (5% + 6.6%) = 4.42V.

Choose R8 = 10.0kΩ, ±1%:

$$R7 = \left(\frac{V_{UVLONOM}}{V_{UVCC}} - 1\right) R8 = \left(\frac{4.42V}{1.230V} - 1\right) 10k\Omega = 25.93k\Omega$$

Use the next-lower value: R7 = 25.5kΩ.

Linear Regulator Compensation

See the application circuit examples in Figures 9 and 10.

The external MOSFET, together with the feedback resistor-divider, R1 and R2, from CORE to CORE_FB to GND, and NDRV form a linear regulator loop. This linear regulator should be compensated for stable operation.

Note: The linear regulator spends most of its time in idle mode. It operates in transient mode and regulation mode only during system power-up/power-down, brownout, and occasional system load transient conditions. Loop stability applies when the linear regulator is in the regulation mode. Follow these simple guidelines to stabilize the linear loop: (see the Core Regulator Loop Bode Plot in the *Typical Operating Characteristics*).

1) Place C1, a 100nF ceramic capacitor (X5R, X7R type or better) from NDRV to GND.
2) Select R1 and R2, a resistor-divider from CORE to CORE_FB to GND to set the linear regulator output regulation voltage (see the *Programming Core Voltage* section).
3) Place R3 and C2, an RC network from CORE_FB to NDRV. Set R3 = R1 and calculate C2 as follows:

$$C2 = \frac{1}{2\pi \times 10kHz \times R3}$$

4) Place R4, a preload resistor, from CORE to GND.

   Calculate R4 as follows:

$$R4 \le \frac{V_{CORE}}{0.03A}$$

5) Place R9 and C3, a lead network, from V_{CORE} to CORE_FB. Set R9 = R1/10, and calculate C3 as follows:

$$C3 = \frac{1}{2\pi \times 7227Hz \times R9}$$

Example: CORE power supply = 1.8V, V_{REGNOM} = 1.6V, C_{CORE} = 100µF, Q_1 = Si9428 (Vishay Siliconix):

$$R1 = R3 = 10.0k\Omega, 1\%$$

$$C2 = \frac{1}{(2\pi \times 10kHz \times 10k\Omega)} = 1.6nF$$

Use a 1.5nF standard value.

$$R4 \le \frac{1.6V}{0.03A} = 53\Omega$$

Use a 51Ω standard value.

$$C3 = \frac{1}{2\pi \times 7227Hz \times R5} = \frac{1}{2\pi \times 7227Hz \times 1k\Omega} = 22nF$$

Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

Programming I/O_SENSE Voltage (MAX5040 Only)

See the application circuit examples in Figures 9 and 10.

I/O_SENSE is used to monitor the I/O output voltage or any other voltage. The result is reported by the POK output signal. Choose the I/O_SENSE trip point such that the minimum monitored voltage at I/O_SENSE exceeds the maximum I/O_SENSE rising threshold.

Follow the guidelines below to program the I/O_SENSE voltage:

1) Determine the tolerance of the output voltage to be monitored, V_O: 5% is common.
2) Determine V_{I/O_SENSE} rising threshold tolerance:

   I/O sense trip-point threshold, V_{IO_REF}, tolerance: 1.230V ±2.5%

   Resistor error tolerance build-up is the same as that calculated in the *Programming UVLO Voltage* section.

   Total = ±6.6%.
3) Set V_{I/O_SENSE} rising nominal value to: V_O nominal value - (V_O tolerance + V_{I/O_SENSE} tolerance).
4) Calculate using the following equation:

$$R5 = \left(\frac{V_{I/O\_SENSENOM}}{V_{I/O\_REF}} - 1 \right) R6$$

where R6 is typically 10kΩ.

Example: $V_{I/O}$ nominal value = 3.3V, set V_{I/O_SENSE} nominal value to 3.3V - (5% + 6.6%) = 2.9172V.

Choose R6 = 10.0kΩ, 1%:

$$R5 = \left(\frac{V_{I/O\_SENSENOM}}{V_{I/O\_REF}} - 1 \right) R6$$

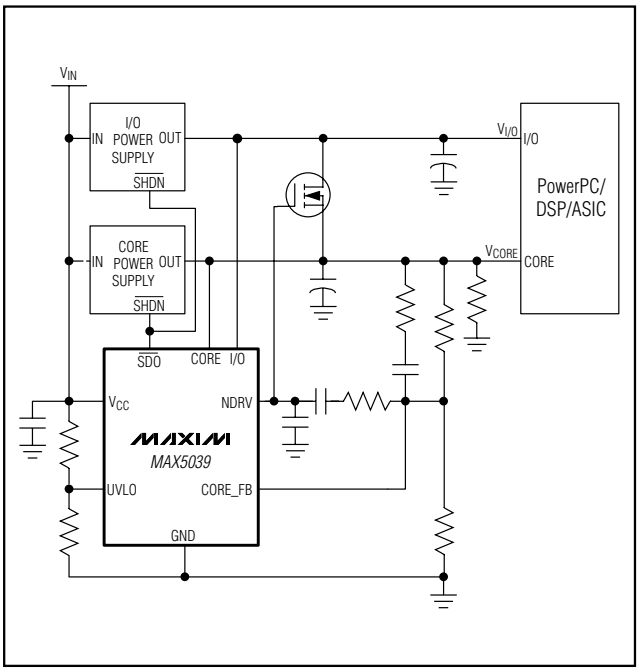
$$R5 = \left(\frac{2.9172V}{1.230V} - 1 \right) 10k\Omega = 13.72k\Omega$$

Use the next lower 13.7kΩ standard value.

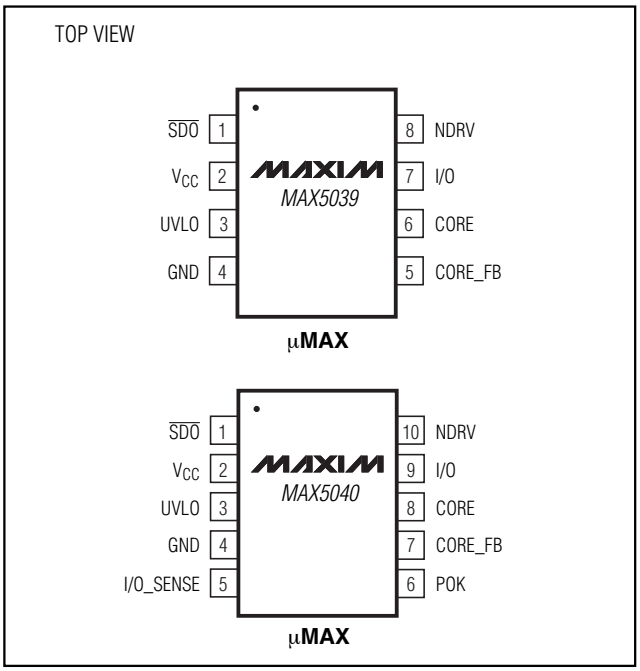
Calculating Component Values

For more detailed information, go to Maxim's website for the Application Note, "Dual Voltage Tracking Circuit for I/O, Microprocessor, and DSP Core Voltages." A link in the application note has a downloadable component selection spreadsheet for calculating component values. This spreadsheet calculates values for all passive components in Figure 10 and lists the resulting min/max values of V_{REGNOM} for standard PowerPC core voltages. DIY options are included for other core and I/O voltages.

Typical Operating Circuit



Pin Configurations



Chip Information

TRANSISTOR COUNT: 1272

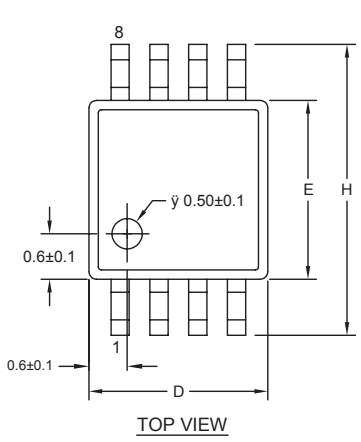
PROCESS: BiCMOS

Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs

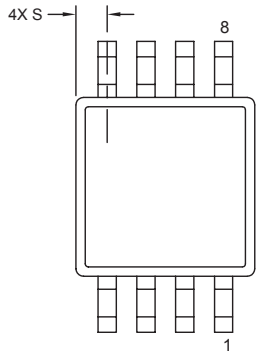
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS

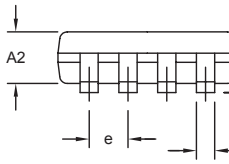


TOP VIEW

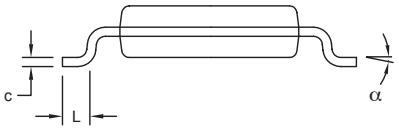


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1

Package Information (continued)

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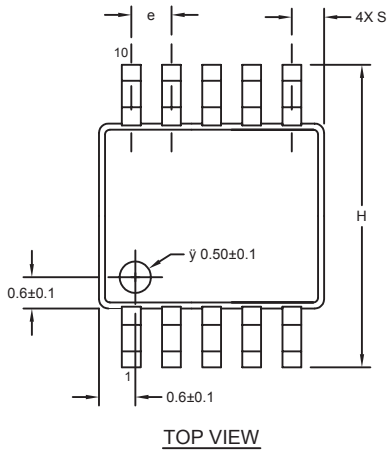
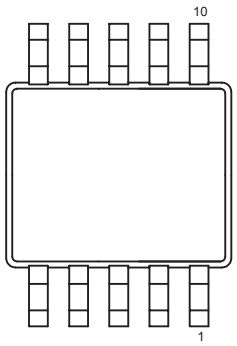
10LUMAX.EPS



TOP VIEW



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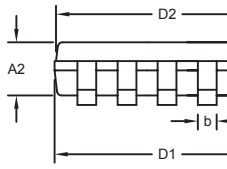
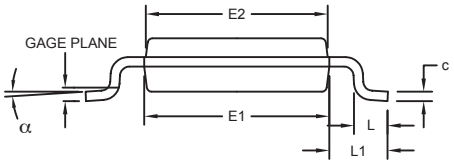
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



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DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management