THE DATASHEET OF

MAX20735EPL+

MAX20735

Integrated, Step-Down Switching Regulator

General Description

The MAX20735 is a fully integrated, highly efficient switching regulator for applications operating from 4.5V to 16V and requiring up to 40A maximum load. This single-chip regulator provides extremely compact, high-efficiency power-delivery solutions with high-precision output voltages and excellent transient response for networking, datacom, and telecom equipment.

The IC offers a broad range of programmable features through capacitors and resistors connected to dedicated programming pins. Using this feature, the operation can be optimized for a specific application, reducing the component count- and/or setting-appropriate trade-offs between the regulator's performance and system cost. Ease of programming enables using the same design for multiple applications.

The MAX20735 includes protection capabilities. Positive and negative cycle-by-cycle overcurrent protection and overtemperature protection ensure a rugged design. Input undervoltage lockout shuts down the device to prevent operation when the input voltage is out of specification. A status pin provides an output signal to show that the output voltage is within range and the system is regulating.

Applications

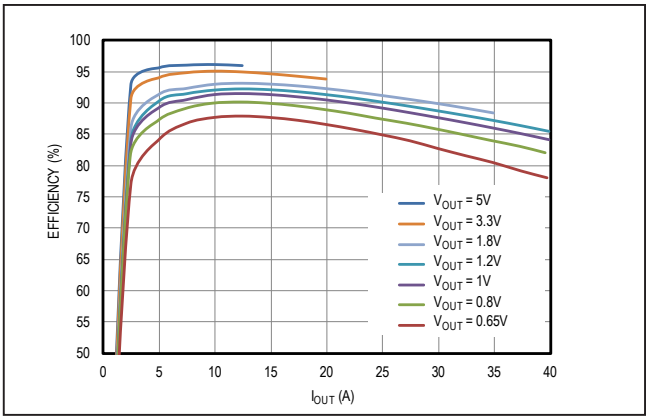
- Communications Equipment
- Networking Equipment
- Servers and Storage Equipment
- Point-of-Load Voltage Regulators
- µP Chipsets
- Memory VDDQ
- I/O

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- High Power Density and Low Component Count
  - Overall Solution Size: 509mm^2 Including Inductor and Output Capacitors
  - 90.7% Peak Efficiency: V_{DDH} = 12V and V_{OUT} = 1V
  - Fast Transient Response: Supports Up to 300A/µs Load Step Transients
- Optimized Component Performance and Efficiency with Reduced Design-In Time
- Increased Power-Supply Reliability with System and IC Self-Protection Features
  - Differential Remote Sense with Open-Circuit Detection
  - Hiccup Overcurrent Protection
  - Programmable Thermal Shutdown

Typical System Efficiency vs. Load Current (V_{DDH} = 12V)



DESCRIPTION	CURRENT RATING*	INPUT VOLTAGE	OUTPUT VOLTAGE
Electrical Rating	40A	4.5V to 16V	0.6484V to 5.5V
Thermal Rating T_A = 55°C, 200 LFM	35A	12V	1V
Thermal Rating T_A = 85°C, 0 LFM	22A		

**For specific operating conditions, refer to the SOA curves in the Typical Operating Characteristics section.*

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Absolute Maximum Ratings

Input Pin Voltage (V_{DDH}) (Note 1) .....-0.3V to +18V
V_{CC}.....-0.3V to +2V
STAT and OE Pin Voltages .....-0.3V to +4V
PGM1, PGM2, PGM3, V_{SENSE+} and V_{SENSE-} Pin Voltages.....-0.3V to +2V
Switching Node Voltage (VX) DC.....-0.3V to +18V
Switching Node Voltage (VX) 25ns (Note 2).....-10V to +23V
(BST - VX) Pin Differential .....-0.3 to +2.5V
Junction Temperature (T_J).....+150°C
Storage Temperature Range..... -65°C to +150°C
Peak Reflow Temperature Lead-Free .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Operating Ratings

Input Voltage (V_{DDH}).....4.5V to 16V
Junction Temperature (T_J)..... -40°C to +125°C
Maximum Average Input Current (I_{VDDH_MAX}) (Note 3).....6A
Maximum Average Output Current (I_{MAX}) 40A
Peak Output Current (I_{PK}).....90A

Package Information

PACKAGE TYPE: 15 FCQFN	
Package Code	P154A9F+1
Outline Number	**21-100027**
Land Pattern Number	**90-100025**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	12°C/W (typ) (Note 4) (still air, no heatsink)
Junction to Case (θ_{JC})	.42°C/W (max)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed informa¬tion on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Note 1: As measured at the V_{DDH} pin referenced to GND pin immediately adjacent using a high frequency scope probe with I_{LOAD} at I_{MAX}. A high-frequency input bypass capacitor must be located less than 60 mils from the V_{DDH} pin per our design guidelines.
Note 2: The 25ns rating is the allowable voltage on the VX node in excess of the -0.3V to +18V DC ratings. The VX voltage can exceed the DC rating in either the positive or negative direction for up to 25ns per cycle.
Note 3: See *Average Input Current Limit* section.
Note 4: Data taken using Maxim's evaluation kit, MAX20735EVKIT#. The PCB has four layers of 2oz copper.

Electrical Characteristics

(Circuit of Figure 6, V_{DDH} = 4.5V to 16V, T_A = +25°C, unless otherwise specified. Typical values are at T_A = +25°C. All devices are tested at T_A = +25°C. Limits over temperature are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE							
Supply Voltage Range	V_{DDH}	(Note 5)		4.5		16	V
OUTPUT VOLTAGE (NOTE 6)							
Output Voltage Range	V_{OUT}	(Note 5)		0.65		5.5	V
V_{REF}							
V_{REF} Values	V_{REF}	Selected by C_SEL1 (Note 7)			0.6484		V
					0.8984		
					1.0		
V_{REF} Tolerance		Referred to V_{SENSE} pins (Note 5)	0.6484V V_{REF}	-1.0		+1.0	%
			0.8984V V_{REF}	-1.0		+1.0	
			1V V_{REF}	-1.0		+1.0	
FEEDBACK LOOP							
Integrator Recovery Time Constant	t_{REC}				20		µs
Gain (see the *Control Loop* section for details)	R_{GAIN}	Selected by R_SEL3 (Notes 5 and 7)			0.8		mV/A
					1.6		
					3.2		
Gain Accuracy		(Notes 5, 8, 9)		-20		+20	%
SWITCHING FREQUENCY							
Switching Frequency	f_{SW}	Selected by C_SEL2 and C_SEL3 (see Tables 5, 6) (Note 7)			400		kHz
					500		
					600		
					700		
					800		
					900		
Switching Frequency Accuracy		(Notes 5, 8, 9)		-20		+20	%
INPUT PROTECTION							
Rising V_{DDH} UVLO Threshold	V_{DDH_UVLO}	(Note 5)			4.25	4.47	V
Falling V_{DDH} UVLO Threshold		(Note 5)		3.7	3.9		
Hysteresis					350		mV

Electrical Characteristics (continued)

(Circuit of Figure 6, V_{DDH} = 4.5V to 16V, T_A = +25°C, unless otherwise specified. Typical values are at T_A = +25°C. All devices are tested at T_A = +25°C. Limits over temperature are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT-VOLTAGE PROTECTION (OVP)							
Overvoltage Protection Rising Threshold	OVP	Relative to programmed V_{OUT}		9.7	13	16.3	%
OVP Deglitch Filter Time					8		µs
Power Good Protection Falling Threshold	PWRGD	Relative to programmed V_{OUT}		6	9	12	%
Power Good Protection Rising Threshold				3	6	9	%
Power Good Deglitch Filter Time					8		µs
OVERCURRENT PROTECTION (OCP)							
Positive OCP Inception Threshold (Inductor Valley Current)	OCP	Selected by R_SEL3 (Notes 5, 7, 8, 9)	Setting 0	16.3	21	26.1	A
			Setting 1	20.8	27	33.0	
			Setting 2	24.6	32	39.9	
			Setting 3	30.6	38	45.5	
Hysteresis of Positive OCP					20		%
Negative OCP Inception Threshold (Inductor Valley Current)		Selected by R_SEL3	Setting 0		-28.1		
			Setting 1		-33.2		
			Setting 2		-38.6		
			Setting 3		-43.8		
Hysteresis of Negative OCP					0		%
OVERTEMPERATURE PROTECTION (OTP)							
OTP Inception Threshold	OTP	Selected by R_SEL2 (Notes 7, 8, 9)		120	130	140	°C
				140	150	160	
Hysteresis					10		°C
OE MAXIMUM VOLTAGE							
OE Max Voltage	OE					V_{DDH} - 2.5	V
Rising Threshold		Measured at OE pin (Note 5)		0.83	0.9	0.97	V
Hysteresis					0.2		
OE Pin Input Resistance				200	275	350	kΩ
OE Deglitch Filter Time		(Note 9)		0.9		2.2	µs
STARTUP TIMING							
Enable Time from OE Rise to Start of BST Charge	t_{OE}	After t_{INIT}			16		µs
Soft-Start Ramp Time	t_{SS}	Set by R_SEL1 (Note 7)			1.5		ms
					3		ms
BST Charging Time	t_{BST}				8		µs

Electrical Characteristics (continued)

(Circuit of Figure 6, V_{DDH} = 4.5V to 16V, T_A = +25°C, unless otherwise specified. Typical values are at T_A = +25°C. All devices are tested at T_A = +25°C. Limits over temperature are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STAT PIN						
Allowable Pullup Voltage	VOH_{STAT}				3.6	V
Status Output Low	VOL_{STAT}	I_{STAT} = 2.5mA			0.4	V
		I_{STAT} = 0.2mA, 0V < V_{CC} < UVLO and 0V < V_{DDH} < UVLO (Note 5)			0.65	
		I_{STAT} = 1.3mA, 0V < V_{CC} < UVLO and 0V < V_{DDH} < UVLO (Note 5)			0.75	
Status Output High Leakage Current		STAT pulled up to 3.3V through 20kΩ			7	µA
Time from V_{OUT} Ramp Completion to STAT Pin Released	t_{STAT}	STAT output low to high, set by R_SEL2 (Note 7)		125		µs
				2000		
PGM1–PGM3 PINS (ALSO SEE TABLES 2–7)						
Allowable R_SEL Resistor Range		12 resistor values detected	1.78		162	kΩ
R_SEL Resistor Required Accuracy		EIA standard resistor values only		±1		%
Allowable C_SEL Capacitor Range		Three options (0, 220, or 1000pF)	0		1000	pF
C_SEL Capacitor Required Accuracy		Use X7R or better		±20		%
External Capacitance		Load and stray capacitance in addition to C_SELA/B			20	pF
SYSTEM SPECIFICATIONS (NOTE 10)						
Line Regulation	V_{OUT}			±0.2		%
Load Regulation (Static)		I_{OUT} = 0 - I_{MAX}		±0.7		
Efficiency (V_{DDH} = 12V, V_{OUT} = 1V)	η	Peak		90.7		%
		Full load (40A)		84.3		

Note 5: Specification applies over the temperature range of T_J = -40° to +125°C.

Note 6: For proper regulation, it is required that V_{DDH} > (V_{OUT} + 2V). If V_{OUT} is set greater than (UVLO - 2V), the IC can come out of UVLO, but regulation is not guaranteed while V_{DDH} is below (V_{OUT} + 2V). To avoid this condition, OE can be held low until V_{DDH} is greater than (V_{OUT} + 2V).

Note 7: Parameters that are programmable.

Note 8: Min/max limits are ≥ 4σ about the mean.

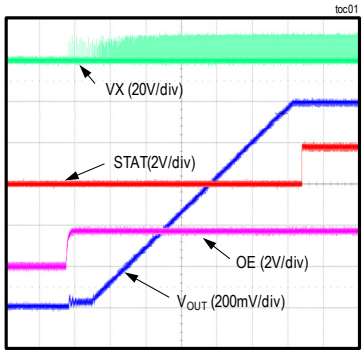
Note 9: Guaranteed by design; not prodcution tested.

Note 10: These specifications refer to the operation of the system and are based on the circuit shown in the reference schematic. Tolerance of external components can affect these parameters. System performance numbers are measured using the Maxim evaluation board for this product with BOM as shown on the MAX20735 EV kit data sheet. If a different PCB layout and different external components are used, these values can change.

Typical Operating Characteristics

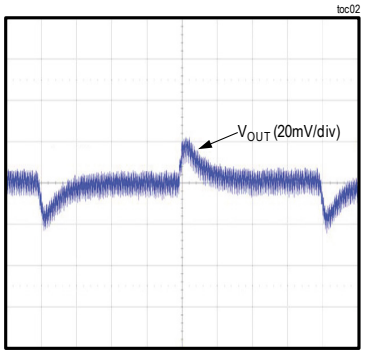
(Unless otherwise noted: Tested on the MAX20735EVKIT# with component values per Table 8; V_{DDH} = 12V, V_{OUT} = 1V, f_{SW} = 400kHz, T_A = 25°C, Still Air, No Heatsink.)

STARTUP RESPONSE



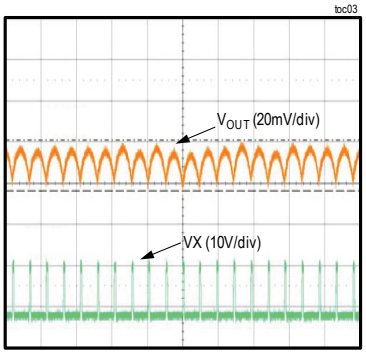
TIME: 500µs/div

TRANSIENT RESPONSE



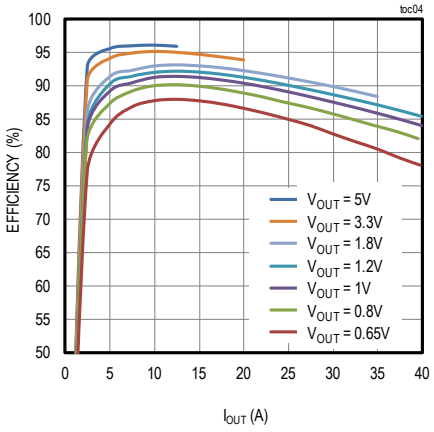
TIME: 50µs/div
CONDITIONS: I_{OUT} = 20A to 30A STEP at 1A/µs

TYPICAL V_{OUT} RIPPLE



TIME: 5µs/div
CONDITIONS: I_{OUT} = 40A

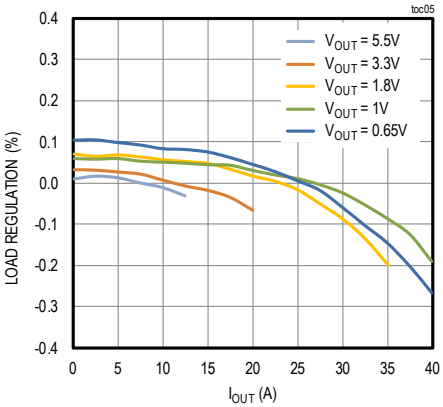
SYSTEM EFFICIENCY vs. OUTPUT LOAD



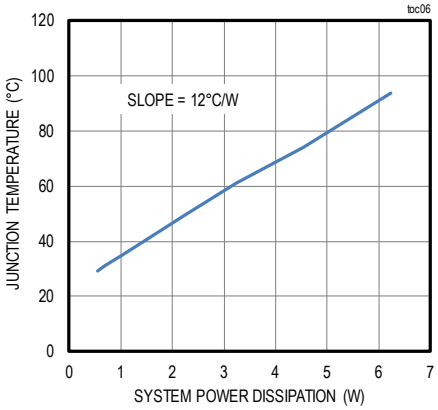
Typical Operating Characteristics (continued)

(Unless otherwise noted: Tested on the MAX20735EVKIT# with component values per Table 8; V_{DDH} = 12V, V_{OUT} = 1V, f_{SW} = 400kHz, T_A = 25°C, Still Air, No Heatsink.)

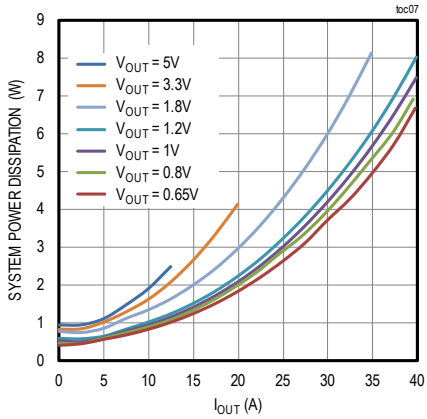
LOAD REGULATION



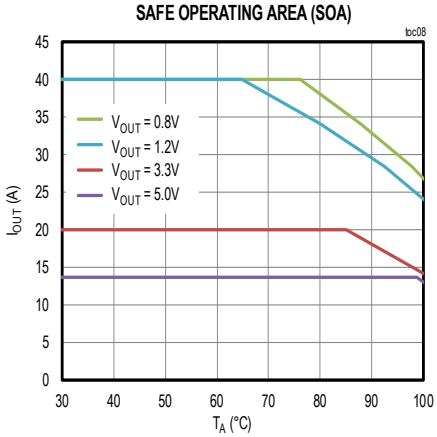
JUNCTION TEMPERATURE vs. SYSTEM POWER DISSIPATION



SYSTEM POWER DISSIPATION



SAFE OPERATING AREA (SOA)



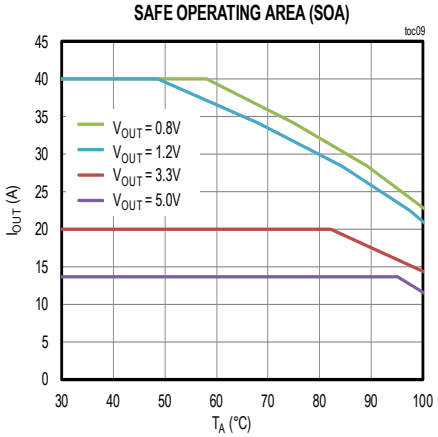
CONDITIONS: 400LFM

CURVE INDICATES T_J = 125°C, $I_{OUT} = I_{MAX}$, or $I_{VDDH} = I_{VDDH_MAX}$, WHICHEVER HAPPENS FIRST

Typical Operating Characteristics (continued)

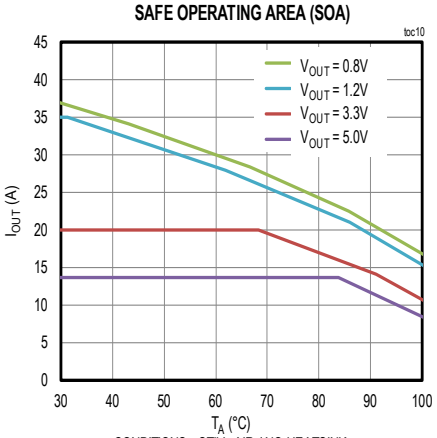
(Unless otherwise noted: Tested on the MAX20735EVKIT# with component values per Table 8; V_{DDH} = 12V, V_{OUT} = 1V, f_{SW} = 400kHz, T_A = 25°C, Still Air, No Heatsink.)

SAFE OPERATING AREA (SOA)



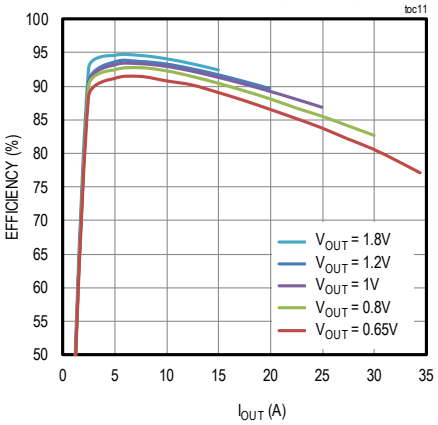
CONDITIONS: 200LFM
CURVE INDICATES T_J = 125°C, I_{OUT} = I_{MAX}, or I_{VDDH} = I_{VDDH_MAX}, WHICHEVER HAPPENS FIRST

SAFE OPERATING AREA (SOA)

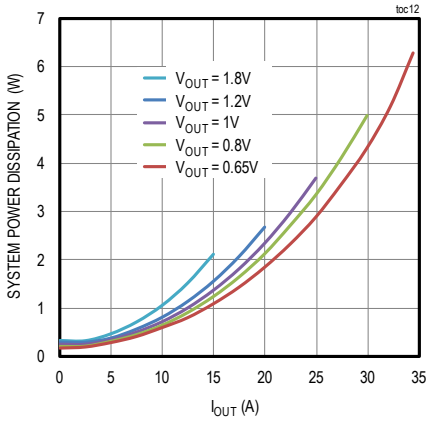


CONDITIONS: STILL AIR / NO HEATSINK
CURVE INDICATES T_J = 125°C, I_{OUT} = I_{MAX}, or I_{VDDH} = I_{VDDH_MAX}, WHICHEVER HAPPENS FIRST

SYSTEM EFFICIENCY vs. OUTPUT LOAD (V_{DDH} = 5V)



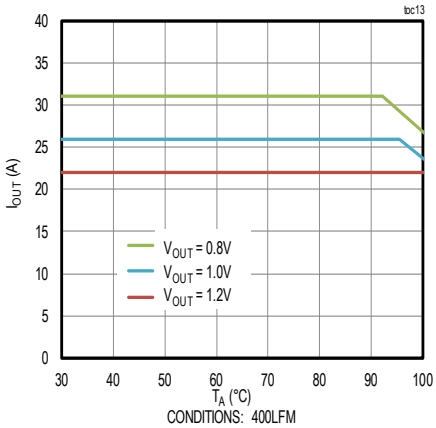
SYSTEM POWER DISSIPATION (V_{DDH} = 5V)



Typical Operating Characteristics (continued)

(Unless otherwise noted: Tested on the MAX20735EVKIT# with component values per Table 8; V_{DDH} = 12V, V_{OUT} = 1V, f_{SW} = 400kHz, T_A = 25°C, Still Air, No Heatsink.)

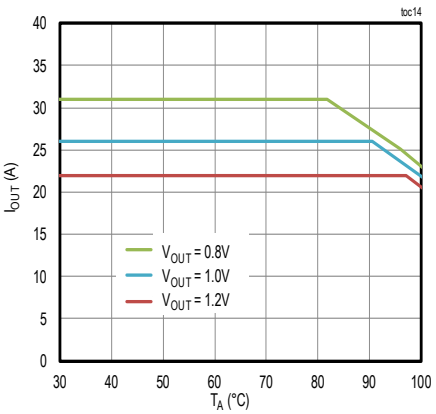
SAFE OPERATING AREA (SOA) (V_{DDH} = 5V)



CONDITIONS: 400LFM

CURVE INDICATES T_J = 125°C, I_{OUT} = I_{MAX}, or I_{VDDH} = I_{VDDH_MAX}, WHICHEVER HAPPENS FIRST

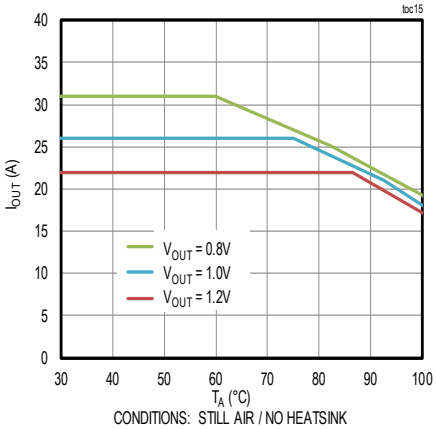
SAFE OPERATING AREA (SOA) (V_{DDH} = 5V)



CONDITIONS: 200LFM

CURVE INDICATES T_J = 125°C, I_{OUT} = I_{MAX}, or I_{VDDH} = I_{VDDH_MAX}, WHICHEVER HAPPENS FIRST

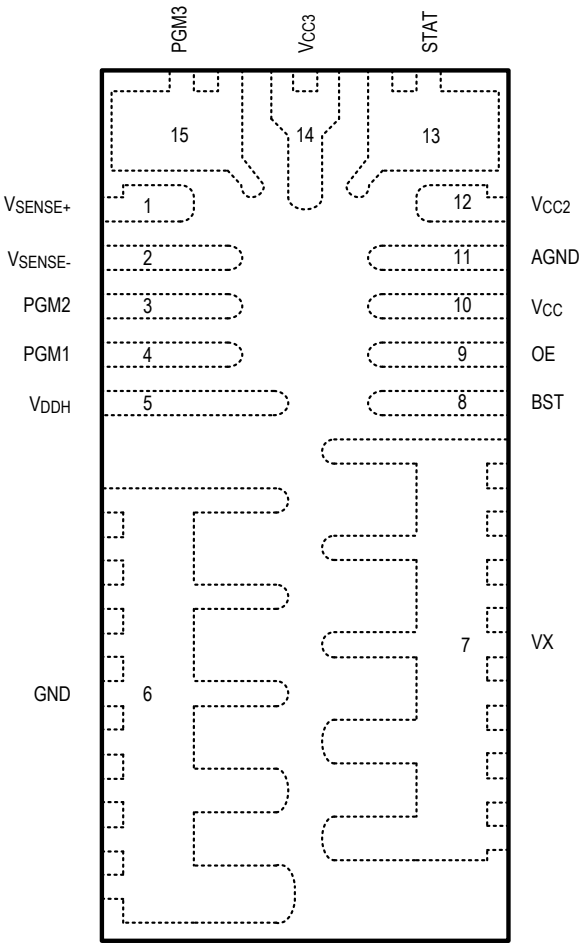
SAFE OPERATING AREA (SOA) (V_{DDH} = 5V)



CONDITIONS: STILL AIR / NO HEATSINK

CURVE INDICATES T_J = 125°C, I_{OUT} = I_{MAX}, or I_{VDDH} = I_{VDDH_MAX}, WHICHEVER HAPPENS FIRST

Pin Configuration

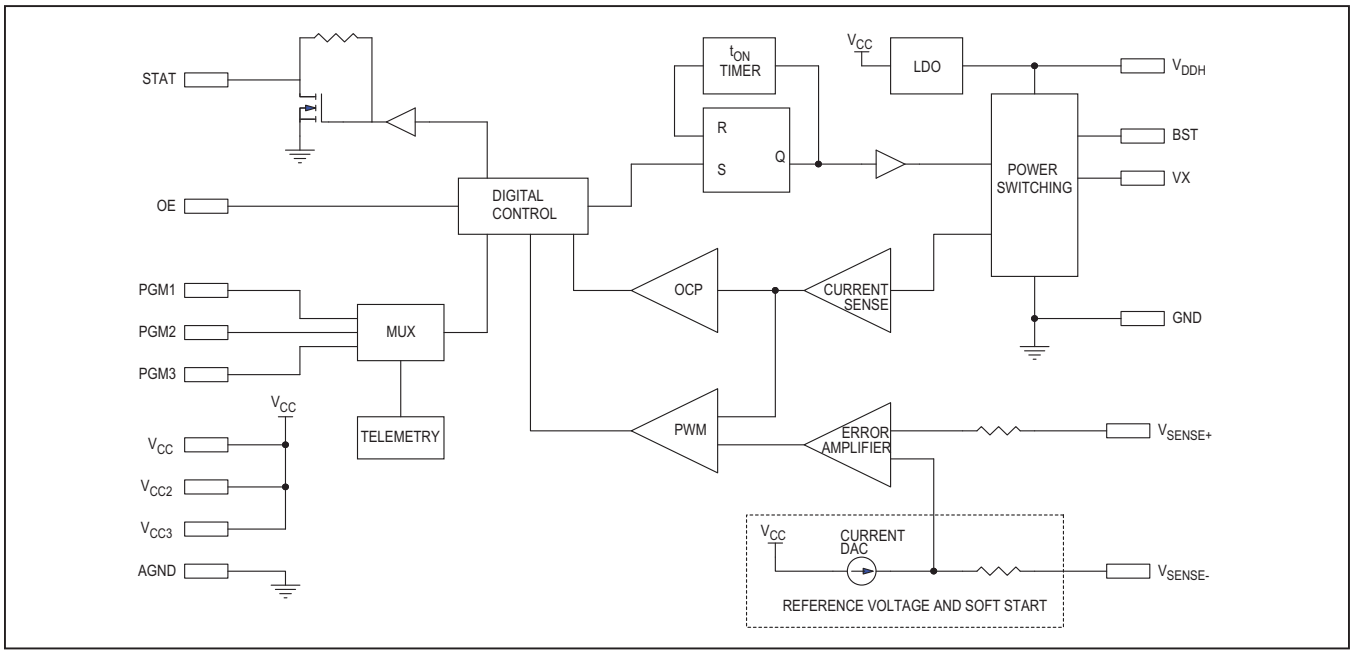


(TOP VIEW)

Pin Description

PIN	NAME	FUNCTION
1	V_{SENSE+}	Remote-Sense Positive Node. Connect this node to V_{OUT} at the load. A resistive voltage-divider can be used to regulate the output above the reference voltage.
2	V_{SENSE-}	Remote-Sense Negative Node. Connect this node to ground at the load using a Kelvin connection.
3, 4	PGM2, PGM1	Program Node. Connect this node to ground through a programming resistor and capacitor.
5	V_{DDH}	Power Input Voltage. The high-side MOSFET switch is connected to this node. See the *Input Capacitor* section for decoupling requirements.
6	GND	Power Ground Node. The low-side MOSFET switch is connected to this node.
7	VX	Power-Switching Node. Connect this node to the inductor.
8	BST	Bootstrap for High-Side Switch. Connect a 0.22µF ceramic capacitor between BST and VX.
9	OE	Output-Enable Node. This node is used to enable the regulator and has a precisethreshold to allow sequencing of multiple regulators. There is an internal 275kΩ (typ) pulldown on this pin.
10	V_{CC}	Analog/Gate-Drive Supply for the IC from Internal 1.85V (typ) LDO. This node MUST be connected to three 10µF X5R or better decoupling capacitors with a very short, wide trace. V_{CC} can be connected to 20kΩ pullups for STAT and OE as shown in Figure 6. Do not connect V_{CC} to other external loads. Do not overdrive V_{CC} from an external source.
11	AGND	Analog/Signal Ground. See the *PCB Layout* section for layout information.
12, 14	V_{CC2}, V_{CC3}	Connect to V_{CC}. Digital factory test input. Must be connected high for normal operation.
13	STAT	Open-Drain Power-Good/Fault-Status Indication. Connect a pullup resistor to 1.8V or 3.3V.
15	PGM3	Program Node. Connect this node to ground through a programming resistor and capacitor.

Block Diagram



Operation

Control Architecture

The MAX20735 provides an extremely compact, high-efficiency regulator solution with minimal external components and circuit design required. The monolithic solution includes the top and bottom power switches, gate drives, precision DAC reference, PWM controller, and fault protections (see the *Block Diagram*). An external bootstrap capacitor is used to provide the drive voltage for the top switch. Other external components include the input and output filter capacitors, buck inductor, and a few Rs and Cs to set the operating mode.

The IC implements an advanced valley current-mode control algorithm that supports all multilayer ceramic chip (MLCC) output capacitors and fast transient response. In steady-state, it operates at a fixed switching frequency. During loading transients, the switching frequency speeds up to minimize the output-voltage undershoot. Likewise, during unloading transients, the switching frequency slows down to minimize the output-voltage overshoot.

The switching frequency can be set to 400kHz, 500kHz, 600kHz, 700kHz, 800kHz, or 900kHz using C_SEL2 and C_SEL3.

Voltage regulation is achieved by modulating the low-side on-time, comparing the difference between the feedback and reference voltages with the low-side current-sense signal using Maxim's proprietary integrated current-sense technology. Once the PWM modulator forces a low-to-high transition, the high-side switch is enabled for a fixed time after which the low-side switch is turned on again. An error amplifier with an integrator is used to maintain zero-droop operation. The integrator has a transient recovery time constant of 20µs (typ).

During regulation, the differential voltage between the V_{SENSE+} and V_{SENSE-} pins tracks the reference voltage which can be set to 0.6484V, 0.8984V or 1V via C_SEL1. The sense pins can be connected to the output voltage through a voltage divider so V_{OUT} can be higher than the reference voltage.

The switching frequency is determined by the high-side ontime as shown in Equation 1.

Equation 1:

$$f_{SW} = \frac{1}{t_{H_ON}} \times \frac{V_{OUT}}{V_{DDH}}$$

where:

f_{SW} = Switching frequency (MHz)

t_{H_ON} = On period for high-side switch (µs)

V_{OUT} = Output voltage (V)

V_{DDH} = Input voltage (V)

The t_{H_ON} high-side on-time is controlled by the IC to be proportional to the duty cycle so that the resulting switching frequency is independent of supply voltage and output voltage.

Equation 2:

$$t_{H_ON} \alpha \frac{V_{OUT}}{V_{DDH}}$$

The t_{H_ON} pulse-width is clamped to a minimum of 50ns (after t_{SS}) and a maximum of 2µs to prevent any unexpected operation during extreme V_{OUT} conditions.

Voltage Regulator Enable and Turn-On Sequencing

The startup timing is shown in Figure 1. After V_{DDH} is applied, the IC goes through an initialization time (t_{INIT}) that takes up to 308µs. After initialization, OE is read. Once OE is high for more than the 16µs OE filter time (t_{OE}), BST charging starts and is performed for 8µs (t_{BST}), and then the soft-start ramp begins. The soft-start ramp time (t_{SS}) is 3ms or 1.5ms, depending on the user's programmed value. V_{OUT} ramps up linearly during the soft-start ramp time. If there are no faults, the STAT pin is released from being held low after the completion of the soft-start ramp time plus the user-programmable STAT blanking time (t_{STAT}) of 125µs or 2ms. If OE is pulled low, the IC shuts down.

Soft-Start Control

The initial output-voltage behavior is determined by a linear ramp of the internal reference voltage from zero to the final value (t_{SS} in Figure 1). The ramp time t_{SS} is programmable from to 1.5ms or 3ms.

If the regulator is enabled when the output voltage has a residual voltage, the system will not regulate until the reference voltage ramps above this residual value. In this case, the t_{OE} (OE valid to onset of regulation) specification is extended by the time required for the desired voltage startup ramp to reach the actual residual output voltage, but the time to reach the steady-state output voltage is unchanged.

If the residual voltage is higher than the set output voltage, neither the high-side nor the low-side switch turns on by the end of t_{SS}. Under these conditions, switching begins after t_{SS}.

Remote Output-Voltage Sensing

To ensure the most accurate sensing of the output voltage, a differential voltage-sense topology is used, with a negative remote-sense pin provided. Point-of-load sensing compensates for voltage drops between the output of the regulator and its load and provides the highest regulation accuracy. The voltage-sensing circuit features excellent common-mode rejection to further improve load-voltage regulation.

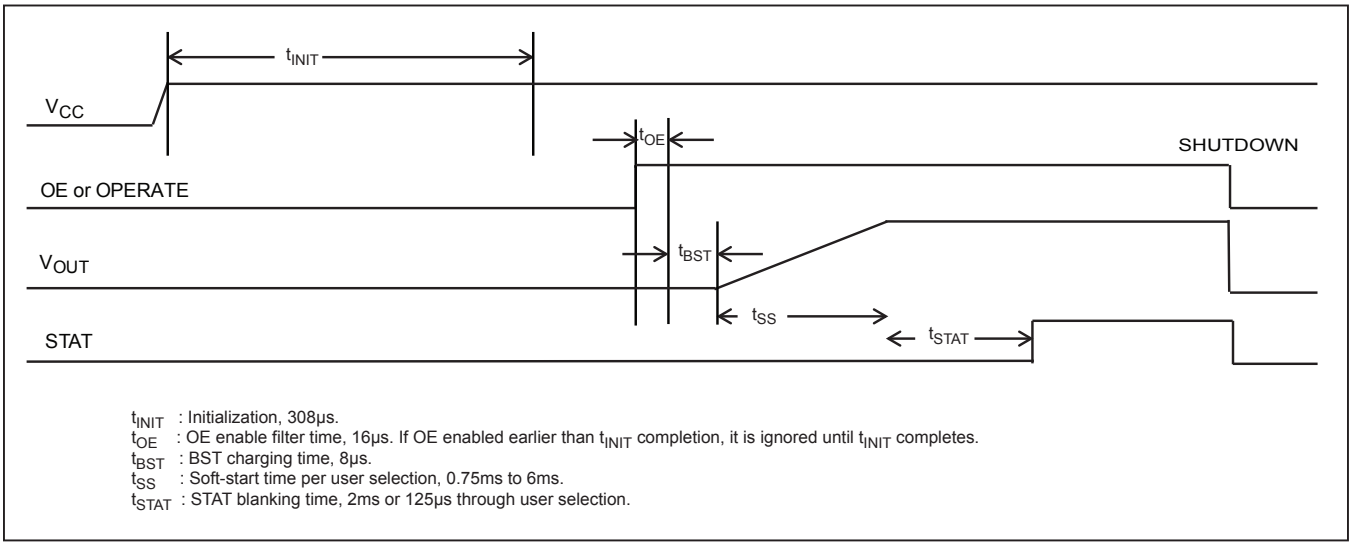


Figure 1. Startup Timing

Protection and Status Operation

Output-Voltage Protection

The feedback voltage is continuously monitored for both undervoltage and overvoltage conditions. The typical fault-detection threshold is 13% above and 9% below the reference voltage (see *Electrical Characteristics* table). If the output voltage falls below the power-good protection (PWRGD) threshold beyond the filter time, the regulator status (STAT) output goes low but the system continues to operate, attempting to maintain regulation.

If the output voltage rises above the overvoltage-protection (OVP) threshold beyond the filter time, the STAT pin is lower and the system shuts down until the output voltage falls within the valid range.

Current Limiting and Short-Circuit Protection

The regulator's valley current-mode control architecture provides inherent current limiting and short-circuit protection. The bottom switch's instantaneous current is monitored using integrated current sensing and controlled on a cycle-by-cycle basis within the control block.

Current clamping occurs when the minimum instantaneous ("valley") low-side switch-current level exceeds the OCP threshold current, as shown in Figure 2. In this situation, turn-on of the high-side switch is prevented until the current falls below the threshold level. Since the inductor valley current is the controlled parameter, the average current delivered during positive current clamping remains a function of several system-level parameters. Note that I_{OCP} has hysteresis and the value drops down to I_{OCP2} once it has been triggered as shown in Figure 2.

Undervoltage Lockout (UVLO)

The regulator internally monitors V_{DDH} with an undervoltage-lockout (UVLO) circuit. When the input supply voltage is below the UVLO threshold, the regulator stops switching, and the STAT pin is driven low. For UVLO levels, refer to the *Electrical Characteristics* table.

Overtemperature Protection (OTP)

The overtemperature-protection level can be set to 150°C or 130°C through R_SEL2. If the die temperature reaches the OTP level during operation, the regulator is disabled and the STAT pin is driven low. Overtemperature is a nonlatching fault, with the hysteresis shown in the *Electrical Characteristics* table.

Regulator Status

The regulator status (STAT) signal provides an open-drain output, consistent with CMOS logic levels, that indicates whether the regulator is functioning properly. An external pullup resistor is required for connecting STAT to V_{CC} or another 1.8V or 3.3V supply.

Table 1. Summary of Fault Actions

FAULT	ACTION
Power Good (Output Undervoltage)	STAT LOW
Output OVP	STAT LOW, Shutdown and Restart
Overtemperature	STAT LOW, Shutdown and Restart
Supply Fault (V_{DDH_UVLO}; V_{CC_UVLO})	STAT LOW, Shutdown and Restart
BST Fault	STAT LOW, Shutdown and Restart

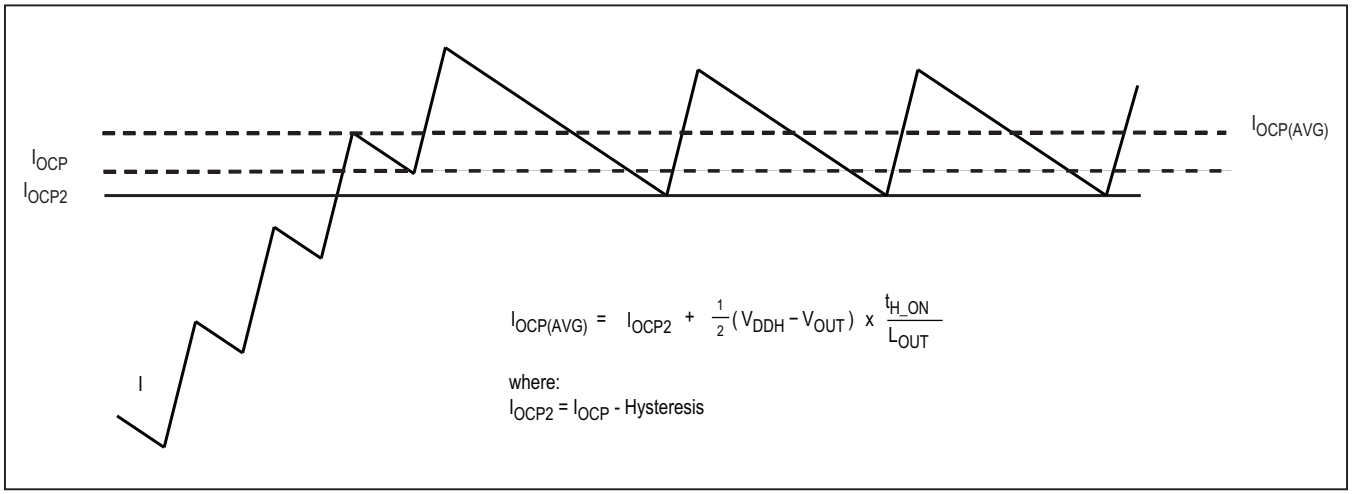


Figure 2. Inductor Current During Current Limiting

The STAT pin is low while the regulator is disabled. The STAT pin goes high after the startup ramp is completed plus the programmed t_{STAT} blanking interval, if the output voltage is within the PWRGD/OVP regulation window. The STAT pin is an open-drain output and is 3.3V tolerant. The pin will remain low when V_{DDH} is not present.

The STAT pin is driven low when one or more of the following conditions exists:

- A PWRGD fault (see the *Output-Voltage Protection* section).
- The V_{SENSE-} pin is left unconnected or shorted to V_{DDH}.
- The die temperature has exceeded the temperature-shutdown threshold shown in the *Electrical Characteristics* table.
- The OVP circuit has detected that the output voltage is above the tolerance limit.
- The supply voltage has dropped below the UVLO threshold.
- A fault is detected on the BST node such as shorted or open bootstrap capacitor.

The ensuing startup follows the same timing as shown in Figure 1.

Table 2. PGM1 Pin R_SEL1 Values

R(kΩ) ±1%	SOFT-START TIME (ms)
1.78	3
46.4	1.5

Table 3. PGM1 Pin C_SEL1 Values

C (pF) ±20%	V_{REF} (V)
Open	0.6484
220	0.8984
1000	1

Table 4. PGM2 Pin R_SEL2 Values

R(kΩ) ±1%	OTP (°C)	t_{STAT} (µs)
1.78	150	2000
2.67	150	125
4.02	130	2000
6.04	130	125

PGM1, 2 and 3 Pin Functionality

The PGM1:PGM3 pins are used to set up some of the key programmable features of the regulator IC. A resistor and capacitor are connected to the PGM pins and their values are read during power up initialization (e.g., power must be cycled to re-read the values).

The parasitic loading on the PGM1:PGM3 pins must be limited to less than 20pF and greater than 20MΩ to avoid interfering with the R_SEL and C_SEL decoding.

Table 5. PGM2 Pin C_SEL2 Values

C(pF) ±20%	f_{SW} FREQUENCY BAND
Open	Even
220	Odd

Table 6. PGM3 Pin C_SEL3 Values

C(pF) ±20%	EVEN BAND f_{SW} FREQUENCY (kHz)	ODD BAND f_{SW} FREQUENCY (kHz)
Open	400	500
220	600	700
1000	800	900

Table 7. PGM3 Pin R_SEL3 Values

R (kΩ) ±1%	R_{GAIN} (mΩ)	OCP*
1.78	0.8	Setting 0
2.67	0.8	Setting 1
4.02	0.8	Setting 2
6.04	0.8	Setting 3
9.09	3.2	Setting 0
13.3	3.2	Setting 1
20	3.2	Setting 2
30.9	3.2	Setting 3
46.4	1.6	Setting 0
71.5	1.6	Setting 1
107	1.6	Setting 2
162	1.6	Setting 3

**See the Electrical Characteristics table for values.*

Reference Design

The typical application schematic is shown in Figure 3 and Table 8 shows optimum component values for common output voltages.

Average Input Current Limit

The input current of V_{DDH} is given by Equation 3. V_{OUT}, I_{OUT} and V_{DDH} should be properly chosen so that the average input current does not exceed 6A (I_{VDDH_MAX}).

Equation 3:

$$I_{VDDH} = \frac{V_{OUT} \times I_{OUT}}{V_{DDH} \times \eta}$$

where:

V_{OUT} = Output voltage

I_{OUT} = Output current

V_{DDH} = Input voltage

η = Efficiency (refer to the *Typical Operating Characteristics* section)

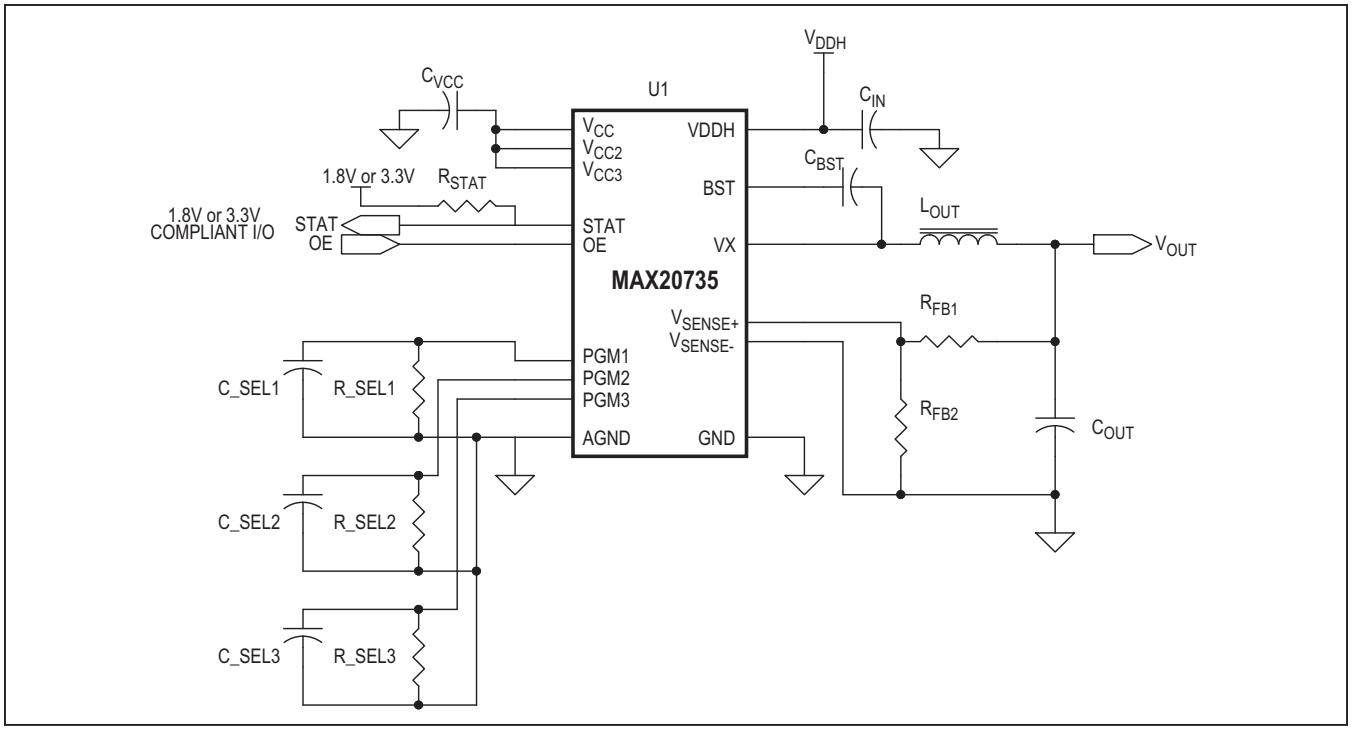


Figure 3. Typical Application Circuit

Table 8. Reference Design Component Values

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	R_SELA (kΩ)	C_SELA (pF)	R_SELB (kΩ)	C_SELB (pF)	R_{GAIN} (mΩ)	V_{REF} (V)	f_{SW} (kHz)	L_{OUT} (nH)	C_{OUT}
0.6484	1	Open	1.78	Open	107	Open	1.6	0.6484	400	170	12 x 100µF + 1 x 22µF
0.8	1.37	5.9	1.78	Open	71.5	Open	1.6	0.6484	400	170	10 x 100µF + 1 x 22µF
1	1.87	3.48	1.78	Open	71.5	Open	1.6	0.6484	400	170	9 x 100µF + 1 x 22µF
1.2	1.74	2.05	1.78	Open	71.5	Open	1.6	0.6484	400	170	9 x 100µF + 1 x 22µF
1.8	3.09	1.74	1.78	Open	71.5	220	1.6	0.6484	600	170	9 x 100µF + 1 x 22µF
3.3	5.62	1.37	1.78	Open	162	220	1.6	0.6484	600	210	9 x 100µF + 1 x 22µF
5.0	7.15	1.07	1.78	Open	107	220	1.6	0.6484	600	210	9 x 100µF + 1 x 22µF

Note: *For input caps, see the Input Capacitor Selection section.*

Output-Voltage Setting

If an output voltage not listed in Table 8 is required, calculate new values for R_{FB1} and R_{FB2} (as discussed below) and use the other circuit values of the closest output voltage in Table 8, or calculate them as shown below.

The output voltage is set by the V_{REF} DAC and divider ratio of resistors R_{FB1} and R_{FB1} per Equation 4. The IC regulates the V_{SENSE+} pin to the reference voltage (V_{REF}), which is set by the DAC. Upon powerup, the DAC voltage initializes to one of the user-selectable V_{REF} voltages. The divider resistors are chosen to give the correct output voltage and to have an approximate parallel resistance of R_{PAR} = 1kΩ for best common-mode rejection of the error amplifier. In applications requiring less than 10mV peak-to-peak output-voltage ripple, setting a lower DAC reference voltage such as 0.6484V is recommended because the part will have less DAC voltage noise.

Equation 4:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where:

V_{REF} = 0.6484V, 0.8984V, or 1.0V (set by C_SEL1).

The divider resistors are then given by Equation 5.

Equation 5:

$$R_{FB1} = V_{OUT} \times \left(\frac{R_{PAR}}{V_{REF}}\right)$$

$$R_{FB2} = R_{FB1} \times \left(\frac{R_{PAR}}{R_{FB1} - R_{PAR}}\right)$$

where:

R_{FB1} = Top divider resistor

R_{FB2} = Bottom divider resistor

R_{PAR} = Desired parallel resistance of R_{FB1} and R_{FB2}

V_{OUT} = Output voltage

V_{REF} = 0.6484V, 0.8984V, or 1.0V (set by C_SEL1)

Control-Loop Stability

The IC uses valley current-mode control that is stabilized by selecting appropriate values of C_{OUT} and R_{GAIN}. No compensation network is required. For stability, the loop bandwidth (BW) should be 100kHz or less. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The loop bandwidth can be approximated by breaking the loop into gain terms as outlined below.

1) The IC's valley current-mode control scheme has an effective transconductance gain of $1/R_{GAIN}$.
2) For MLCC capacitors, the output capacitors contribute an impedance gain of $1/(2 \times \pi \times C_{OUT} \times f)$.
3) The feedback-divider contributes an attenuation of $K_{DIV} = R_{FB2}/(R_{FB1} + R_{FB2})$.
4) An inherent high-frequency pole located at 150kHz.

When the BW is 100kHz or less, the high-frequency pole can be ignored and the approximate loop gain and BW are given by Equation 6.

Equation 6:

$$|LOOP_GAIN\ (f)| = \frac{K_{DIV}}{2 \times \pi \times R_{GAIN} \times C_{OUT} \times f}$$

$$BW = \frac{K_{DIV}}{2 \times \pi \times R_{GAIN} \times C_{OUT}}$$

OR

$$BW = \frac{1}{2 \times \pi \times R_{GAIN_EFF} \times C_{OUT}}$$

where:

$R_{GAIN_EFF} = R_{GAIN}/K_{DIV}$

For stability, R_{GAIN} and C_{OUT} should be chosen so that BW < 100kHz.

The available R_{GAIN} settings are shown in Table 7. When choosing which R_{GAIN} setting to use, one should consider that while higher R_{GAIN} allows the loop to be stabilized with less C_{OUT}, less C_{OUT} generally results in higher ripple and larger transient overshoot and undershoot, so there needs to be a balance.

Integrator

The IC has an integrator included in its error amplifier that was ignored in the above equations for simplicity. The integrator only adds gain at low frequencies, so it does not really effect the loop BW calculation. The purpose of the integrator is to improve load regulation. The integrator adds a factor of $(1/t_{REC} + s)/s$ to the loop gain.

Step Response

R_{GAIN_EFF} is important since it determines the small-signal transient response of the regulator. When a load step is applied that does not exceed the slew-rate capability of the inductor current, the regulator responds linearly and V_{OUT} temporarily changes by the amount of V_{OUT_ERROR} (see Equation 7).

Equation 7:

$$V_{OUT_ERROR} = I_{STEP} \times R_{GAIN_EFF}$$

The integrator causes V_{OUT} to recover to the nominal value with a time constant of t_{REC} = 20µs. The regulator can be modeled to a first-order by the averaged small-signal equivalent circuit shown in Figure 4. Here, V_{EQ} is an ideal voltage source, R_{EQ} is an equivalent lossless resistance created by the control-loop action, and L_{EQ} is an equivalent inductance. Note that L_{EQ} is not the same as the actual L_{OUT} inductor which has been absorbed into the model. C_{OUT} is the actual output capacitance.

Output-Capacitor ESR

In the above control-loop discussion, the case of MLCC output capacitors has been considered. Another case worth mentioning is the use of output capacitors with more significant ESR. This can be considered as long as the capacitors are rated to handle the inductor current ripple and expected surge currents. Thus far, it has been assumed that C_{OUT} is comprised of MLCCs and the net ESR is negligible compared to R_{GAIN}/K_{DIV}. If the net ESR of the C_{OUT} bank is not negligible compared to R_{GAIN}/K_{DIV}, the inductor current ripple is effectively sensed by the ESR and adds to the R_{GAIN_EFF} as shown in Equation 8.

Equation 8:

$$R_{GAIN_EFF} = \frac{R_{GAIN}}{K_{DIV}} + ESR$$

The capacitor's ESR also introduces a zero into the loop gain. The inherent high-frequency pole helps to compensate this zero. For a more in-depth view of the effect of circuit values on regulator performance, the Maxim Simplis model and evaluation kit can be used. It is recommended to simulate and/or test regulator performance when using values other than the recommended component values.

The performance data shown in the *Typical Operating Characteristics* section was taken using the Maxim EV kit and component values in Table 8. For most applications, these are the optimum values to use. Table 9 through Table 11 show suitable part numbers for input and output capacitors and the inductor.

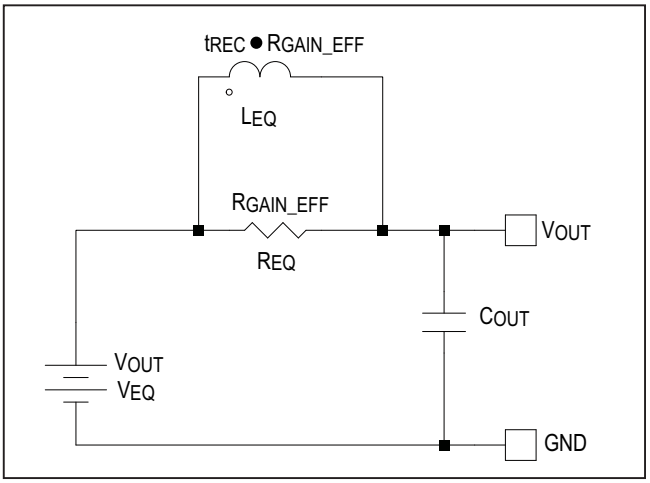


Figure 4. Averaged Small-Signal Equivalent Circuit of Regulator

***Note:** The large-signal transient response is approximately the larger between the V_{OUT_ERROR} and the Unloading Transient.*

Table 9. Recommended Inductors

COMPANY	VALUE (nH)	I_{SAT} (A)	R_{DC} (mΩ)	FOOTPRINT (mm)	HEIGHT (mm)	PART NUMBER	WEBSITE
Cooper	170	60	0.29	10.4 x 8.0	7.5	FP1007R3-R17-R	www.cooperindustries.com
Pulse	210	64	0.32	13.5 x 13.0	8.0	PA0513.211NLT	www.pulseelectronics.com
Pulse	260	55	0.32	13.5 x 13.0	8.0	PA0513.261NLT	www.pulseelectronics.com
Pulse	320	45	0.32	13.5 x 13.0	8.0	PA0513.321NLT	www.pulseelectronics.com
Pulse	440	30	0.32	13.5 x 13.0	8.0	PA0513.441NLT	www.pulseelectronics.com

Table 10. MLCC Input Capacitors

CASE SIZE	VALUE (µF)	TEMPERATURE RATING	VOLTAGE RATING	T (NOTE 1)	COMPANY	PART NUMBER
0603	1	X7S X7R	16V	0.8 (Note 2)	Murata TDK	GRM188C71C105KA12D C1608X7R1C105K
0805	2.2	X7R	25V 16V 16V	1.25 1.25 1.25	Murata TDK AVX	GRM21BR71E225KA73L C2012X7R1C225M 0805YC225MAT
0805	4.7	X7R	16V	1.25	Murata	GRM21BR71C475K
1206	4.7	X7R	16V	1.65	AVX Murata	1206YC475MAT GRM31CR71C475KA01L
1206	10	X7R	16V	1.65	Murata TDK AVX	GRM31CR71C106KAC7L C3216X7R1C106M 1206YC106MAT
1210	10	X7R	16V 25V	2.0 2.5	Murata TDK	GRM32DR71C106KA01L C3225X7R1E106M
1210	22	X7R	16V	2.45 2.5 2.5	AVX Murata TDK	1210YC226MAT GRM32ER71A476K C3225X7R1C226M

***Note 1**: T indicates nominal thickness in mm.*

***Note 2:** Indicates capacitors with nominal thickness smaller than the minimum FCQFN package thickness.*

Table 11. Recommended Output Capacitors

COMPANY	VALUE (µF)	PART NUMBER	TEMP. RATING	VOLT. RATING	CASE SIZE	T (NOTE)	WEBSITE
AVX	22 22	08054D226MAT2A 12066D226MAT2A	X5R X5R	4V 6.3V	0805 1206	1.3 1.65	www.avxcorp.com
Murata	22 22 22	GRM21BR60J226ME39L GRM31CR60J226KE19L GRM32DR60J226KA01L	X5R X5R X5R	6.3V 6.3V 6.3V	0805 1206 1210	1.25 1.6 2.0	www.murata.co.jp
Panasonic	22 22 22	ECJ3YB0J226M ECJHVB0J226M ECJ3Y70J226M	X5R X5R X7R	6.3V 6.3V 6.3V	1206 1206 1206	1.6 0.85 1.65	www.panasonic.com
Taiyo Yuden	22 22 22	AMK212BJ226MG JMK316BJ226ML JMK325BJ226MY	X5R X5R X5R	4V 6.3V 6.3V	0805 1206 1210	1.25 1.6 1.9	www.taiyo-yuden.com
TDK	22 22 22 22	C2012X5R0J226M C3216X5R0J226M C3225X5R0J226M C3216X6S0J226M	X5R X5R X5R X6S	6.3V 6.3V 6.3V 6.3V	0805 1206 1210 1206	1.25 1.6 1.6 1.6	www.component.tdk.com

***Note:** T indicates nominal thickness in mm.*

Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitors needed to maintain transient tolerances.

For any buck regulator, the maximum current slew rate through the output inductor is given by Equation 9.

Equation 9:

$$SlewRate = \frac{dI_L}{dt} = \frac{V_L}{L_{OUT}}$$

where:

I_L = Inductor current

L_{OUT} = Output inductance

V_L = V_{DDH} - V_{OUT} during high-side FET conduction and -V_{OUT} during low-side FET conduction

Equation 9 shows that larger inductor values limit the regulator's ability to slew current through the output inductor in response to step-load transients. Consequently, more output capacitors are required to supply (or store) sufficient charge to maintain regulation while the inductor current ramps up to supply the load.

In contrast, smaller inductor values increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak ripple current is given by Equation 10.

Equation 10:

$$I_{OUTRIPPLE} = \frac{t_{H_ON} \times (V_{DDH} - V_{OUT})}{L_{OUT}}$$

where:

t_{H_ON} = High-side switch on-time (based on nominal V_{OUT}) (see Equation 1)

L_{OUT} = Output inductance

V_{DDH} = Input voltage

V_{OUT} = Output voltage

From Equation 10, for the same switching frequency, ripple current increases as L decreases. This increased ripple current results in increased AC losses, larger peak current, and for the same output capacitance, results in increased output-voltage ripple.

$I_{OUTRIPPLE}$ should be set to 25% to 50% of the IC's rated output current. A suitable inductor value can then be found by solving Equation 10 for inductance as in Equation 11 and Equation 12.

Equation 11:

$$L_{OUT} = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{OUTRIPPLE} \times f_{SW}}$$

And assuming $I_{OUTRIPPLE}$ = 0.25 x I_{OUT} for a typical inductor value, see Equation 12.

Equation 12:

$$L_{OUT} = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times (0.25 \times I_{OUT}) \times f_{SW}}$$

So, for a 35A regulator running at 400kHz with V_{DDH} = 12V and V_{OUT} = 1V, Equation 13 shows the target value for the inductor.

Equation 13:

$$L_{OUT} = \frac{1 \times (12 - 1)}{12 \times 0.25 \times 35 \times 400{,}000}$$

$$= 262nH$$

The saturation current rating of the inductor is another important consideration. At current limit, the peak inductor current is given Equation 14.

Equation 14:

$$I_{PK} = I_{OCP} + I_{OUTRIPPLE}$$

where:

I_{OCP} = Overcurrent-protection trip point (see *Electrical Characteristics* and *Current Limiting and Short-Circuit Protection* sections)

$I_{OUTRIPPLE}$ = Peak-to-peak inductor current ripple, defined above

For proper OCP operation of the regulator, it is important that I_{PK} never exceeds the saturation current rating of the inductor (I_{SAT}). It is recommended that a margin of at least 20% is included between I_{PK} and I_{SAT} as shown in Equation 15.

Equation 15:

$$I_{SAT} > 1.2 \times I_{PK}$$

Also, note that during a hard V_{OUT} short circuit, $I_{OUTRIPPLE}$ increases because V_{OUT} went to zero in Equation 10.

Finally, the power dissipation of the inductor influences the regulation efficiency. Losses in the inductor include core loss, DC resistance loss and AC resistance loss. For the best efficiency, use inductors with core material exhibiting low loss in the range of 0.5MHz to 2MHz and low-winding resistance.

Table 9 provides a summary of recommended inductor suppliers and part numbers.

Output Capacitor Selection

The minimum recommended output capacitance for stability is given in the *Control-Loop Stability* section and is normally implemented using several 100µF 1206 (or similar) MLCCs. For low slew rate transient loads, R_{GAIN_EFF} determines the V_{OUT_ERROR} for a given load step per the small-signal model as discussed above. In this case, C_{OUT} has no effect on the V_{OUT_ERROR}.

However, in the event that the slew rate of the load transient greatly exceeds the slew rate of the inductor current, the transient V_{OUT} error can be larger than predicted by the small-signal model. In this case, the V_{OUT} loading and unloading transients can be approximated by taking the larger result between Equation 7 and Equation 16.

Equation 16:

$$LOADING\,TRANSIENT(V) = \frac{L_{OUT} \times \left(I_{STEP} + \frac{I_{OUTRIPPLE}}{2}\right)^2}{2 \times C_{OUT} \times (V_{DDH} - V_{OUT})}$$

$$UNLOADING\,TRANSIENT(V) = \frac{L_{OUT} \times \left(I_{STEP} + \frac{I_{OUTRIPPLE}}{2}\right)^2}{2 \times C_{OUT} \times V_{OUT}} + I_{STEP} \times \frac{t_{H_ON}}{C_{OUT}}$$

In order to meet an aggressive transient specification, C_{OUT} may have to be increased and/or L_{OUT} may have to be decreased. However, note that decreasing L_{OUT} results in larger inductor ripple current and thus decreased efficiency and increased output ripple.

Output voltage ripple is another important consideration in the selection of output capacitors. For a buck regulator operating in CCM, the total voltage ripple across the output capacitor bank can be approximated as the sum of three voltage waveforms: 1) the triangle wave that results from multiplying the AC ripple current by the ESR, 2) the square wave that results from multiplying the ripple current slew rate by the ESL and 3) the piece wise quadratic waveform that results from charging and discharging the output capacitor. Although the phasing of these three components does impact the total output ripple, a common approximation is to ignore the phasing and to find the upper bound of the peak-to-peak ripple by summing all three components, as shown in Equation 17.

Equation 17:

$$V_{PP} = ESR(I_{OUTRIPPLE}) + ESL\left(\frac{V_{DDH}}{L_{OUT}}\right) + \left(\frac{I_{OUTRIPPLE}}{8 \times f_{SW} \times C_{OUT}}\right)$$

where:

ESR = Equivalent series resistance at the output

$I_{OUTRIPPLE}$ = Peak-to-peak inductor current ripple

ESL = High-frequency equivalent series inductance at output

V_{DDH} = Input voltage

L_{OUT} = Output inductance

f_{SW} = Switching frequency

C_{OUT} = Output capacitance

In a typical MAX20735 application with a bank of 0805, X5R, 6.3V, and 22µF output capacitors, these three components are roughly equal.

The ESL effect of an output capacitor on output-voltage ripple cannot be easily estimated from the resonant frequency; the high-frequency (10MHz or above) impedance of that capacitor should be used. PCB traces and vias in the V_{OUT}/GND loop contribute additional parasitic inductance.

The final considerations in the selection of output capacitors are ripple current rating and power dissipation. Using a conservative design approach, the output capacitors should be designed to handle the maximum peak-to-peak AC ripple current experienced in the worst-case scenario. Because the recommended output capacitors have extremely low-ESR values, they are typically rated well above the current and power stresses seen here. For the triangular AC ripple current at the output, the total RMS current and power is given by Equation 18 and Equation 19.

Equation 18:

$$I_{RMS_COUT} = \frac{I_{OUTRIPPLE}}{\sqrt{12}}$$

where:

$I_{OUTRIPPLE}$ = Peak-to peak ripple current value.

Equation 19:

$$P_{COUT} = I_{RMS_COUT}^2 \times ESR$$

where ESR is the equivalent series resistance of the entire output capacitor bank

Input Capacitor Selection

The selection and placement of input capacitors are important considerations. High-frequency input capacitors serve to control switching noise. Bulk input capacitors are designed to filter the pulsed DC current drawn by the regulator. For the best performance, lowest cost and smallest size of the MAX20735 systems, MLCC capacitors with 1210 or smaller case sizes, capacitance values of 47µF or smaller, 16V or 25V voltage ratings and X5R or better temperature characteristics are recommended as bulk. The minimum recommended value of capacitance are 2 x 47µF (bulk) and 1.0µF + 0.1µF (high frequency). Smaller values of bulk capacitance can be used in direct proportion to the maximum load current.

It is recommended to choose the main MLCC input capacitance to control the peak-to-peak input voltage ripple to 2% to 3% of its DC value in accordance with Equation 20.

Equation 20:

$$C_{IN} = \frac{I_{MAX} \times V_{OUT} \times (V_{DDH} - V_{OUT})}{\left(f_{SW} \times V_{DDH}^2 \times V_{INPP}\right)}$$

where:

C_{IN} = Input capacitance (MLCC)

I_{MAX} = Maximum load current

V_{DDH} = DC input voltage

V_{OUT} = DC output voltage

f_{SW} = Switching frequency (CCM)

V_{INPP} = Target peak-to-peak input voltage ripple

Because the bulk input capacitors must source the pulsed DC input current of the regulator, the power dissipation and ripple current rating for these capacitors are far more important than that for the output capacitors. The RMS current that the input capacitor must withstand can be approximated using Equation 21.

Equation 21:

$$I_{RMS_CIN} = \frac{I_{LOAD}\sqrt{V_{OUT}(V_{DDH} - V_{OUT})}}{V_{DDH}}$$

where I_{LOAD} is the output DC load current.

With an equivalent series resistance of the bulk input capacitor bank (ESR_{CIN}), the total power dissipation in the input capacitors is given by Equation 22.

Equation 22:

$$P_{CIN} = I_{RMS_CIN}^2 \times ESR_{CIN}$$

Resistor Selection and its Effect on DC Output Voltage Accuracy

R_{FB1} and R_{FB2} set the output voltage as described in Equation 4. The tolerance of these resistors affects the accuracy of the set output voltage. Due to the form of Equation 4, the effect is higher at higher output voltages. Figure 5 shows the effect of 0.1% tolerance resistors over a range of output voltages. For different tolerance resistors, multiply the output-voltage error by the resistors' tolerances divided by 0.1%. For example, for 0.5% tolerance resistors, multiply the output error shown by 5. To obtain accuracy overtemperature, for a worst case, the temperature coefficients multiplied by the temperature range should be added to the tolerance (i.e., for 25ppm/°C resistors over a 50°C excursion, add 0.125% to the 25°C tolerance).The error due to the voltage feedback resistors' tolerance, R_{FB1} and R_{FB2} should be added to the output-voltage tolerance due to the IC's feedback-voltage accuracy shown in the *Electrical Characteristics* table.

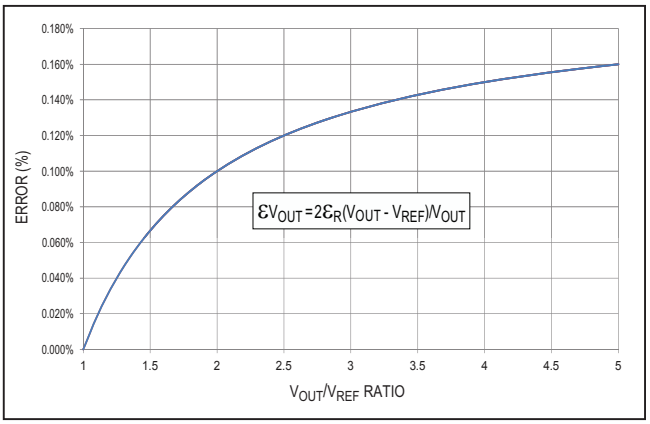


Figure 5. DC Accuracy Impact Showing Effect of 0.1% Tolerance for R_{FB1} and R_{FB2}

PCB Layout

PCB layout can dramatically affect the performance of the regulator. A poorly designed board can degrade efficiency, noise performance, and even control loop stability. At higher switching frequencies, layout issues are especially critical.

As a general guideline, the input capacitors and the output inductor should be placed in close proximity to the regulator IC, while the output capacitors should be lumped together as close as possible to the load. Traces to these components should be kept as short and wide as possible in order to minimize parasitic inductance and resistance. Traces connecting the input capacitors and V_{DDH} (power input node) on the IC require particular attention since they carry currents with the largest RMS values and fastest slew rates. According to best practice, the input capacitors should be placed as close as possible to the input supply pins with the smallest package high-frequency capacitor being the closest to the IC and no more than 60 mils from the IC pins. Preferably, there should be an uninterrupted ground plane located immediately underneath these high-frequency current paths, with the ground plane located no more than 8 mils below the top layer. By keeping the flow of this high-frequency AC current localized to a tight loop at the regulator, electromagnetic interference (EMI) can be minimized.

Voltage sense lines should be routed differentially directly from the load points. The ground plane can be used as a shield for these or other sensitive signals to protect them from capacitive or magnetic coupling of high-frequency noise.

For remote-sense applications where the load and regulator IC are separated by a significant distance or impedance, it is important to place the majority of the output capacitors directly at the load. Ideally, for system stability, all of the output capacitors should be placed as close as possible to the load. In remote-sense applications, common-mode filtering is necessary to filter high-frequency noise in the sense lines.

The following layout recommendations should be used for optimal performance:

- It is essential to have a low-impedance and uninterrupted ground plane under the IC and extended out underneath the inductor and output capacitor bank.
- Multiple vias are recommended for all paths that carry high currents (i.e., GND, V_{DDH}, VX). Vias should be placed close to the chip to create the shortest possible current loops. Via placement must not obstruct the flow of currents or mirror currents in the ground plane.
- A single via in close proximity to the chip should be used to connect the top layer A_{GND} trace to the second layer ground plane, it must not be connected to the top power ground area.
- The feedback divider and compensation network should be close to the IC to minimize the noise on the IC side of the divider.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative.

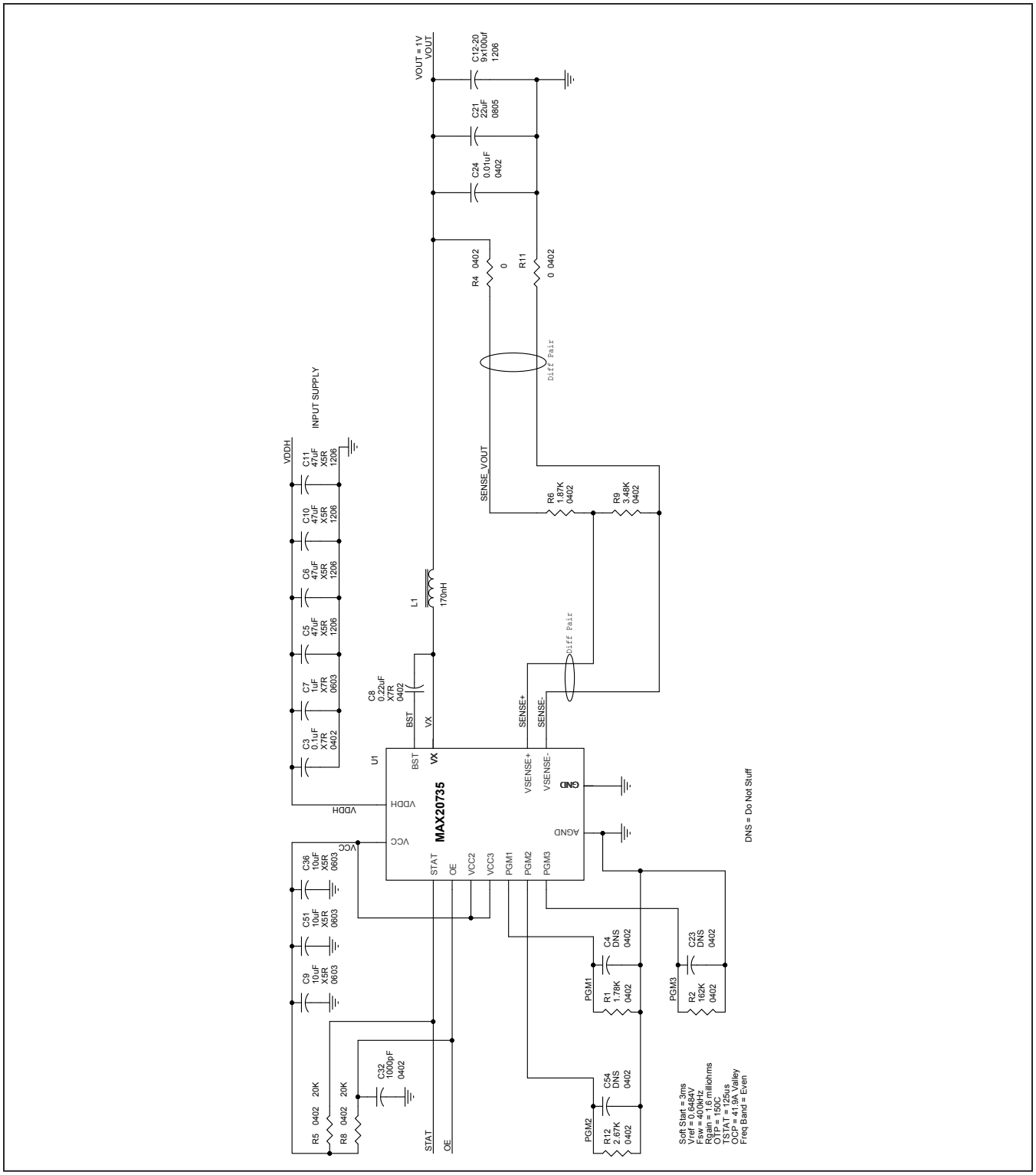


Figure 6. Reference Schematic (V_{DDH} = 4.5V to 16V, V_{OUT} = 1V)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20735EPL+	-40°C to +125°C	15 FCQFN
MAX20735EPL+T	-40°C to +125°C	15 FCQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/16	Initial release	—
1	5/17	Updated *Electrical Ratings* in table and *Typical System Efficiency vs. Load Current* chart on first page. Updated *Package Information* table, *Operating Ratings*, *Electrical Characteristics* table, Table 7, and *Typical Operating Characteristics*. Added *Average Input Current Limit* section and new Equation 3. Renumbered Equations 4 to 22.	1–9 15–16

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