



**THE DATASHEET OF
TMS320F28377SPZPT**



TMS320F2837xS Delfino™ Microcontrollers

1 Device Overview

1.1 Features

- TMS320C28x 32-Bit CPU
 - 200 MHz
 - IEEE 754 Single-Precision Floating-Point Unit (FPU)
 - Trigonometric Math Unit (TMU)
 - Viterbi/Complex Math Unit (VCU-II)
- Programmable Control Law Accelerator (CLA)
 - 200 MHz
 - IEEE 754 Single-Precision Floating-Point Instructions
 - Executes Code Independently of Main CPU
- On-Chip Memory
 - 512KB (256KW) or 1MB (512KW) of Flash (ECC-Protected)
 - 132KB (66KW) or 164KB (82KW) of RAM (ECC-Protected or Parity-Protected)
 - Dual-Zone Security Supporting Third-Party Development
 - Unique Identification Number
- Clock and System Control
 - Two Internal Zero-Pin 10-MHz Oscillators
 - On-Chip Crystal Oscillator
 - Windowed Watchdog Timer Module
 - Missing Clock Detection Circuitry
- 1.2-V Core, 3.3-V I/O Design
- System Peripherals
 - Two External Memory Interfaces (EMIFs) With ASRAM and SDRAM Support
 - 6-Channel Direct Memory Access (DMA) Controller
 - Up to 169 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins With Input Filtering
 - Expanded Peripheral Interrupt Controller (ePIE)
 - Multiple Low-Power Mode (LPM) Support With External Wakeup
- Communications Peripherals
 - USB 2.0 (MAC + PHY)
 - Support for 12-Pin 3.3 V-Compatible Universal Parallel Port (uPP) Interface
 - Two Controller Area Network (CAN) Modules (Pin-Bootable)
 - Three High-Speed (up to 50-MHz) SPI Ports (Pin-Bootable)
 - Two Multichannel Buffered Serial Ports (McBSPs)
 - Four Serial Communications Interfaces (SCI/UART) (Pin-Bootable)
 - Two I2C Interfaces (Pin-Bootable)
- Analog Subsystem
 - Up to Four Analog-to-Digital Converters (ADCs)
 - 16-Bit Mode
 - 1.1 MSPS Each (up to 4.4-MSPS System Throughput)
 - Differential Inputs
 - Up to 12 External Channels
 - 12-Bit Mode
 - 3.5 MSPS Each (up to 14-MSPS System Throughput)
 - Single-Ended Inputs
 - Up to 24 External Channels
 - Single Sample-and-Hold (S/H) on Each ADC
 - Hardware-Integrated Post-Processing of ADC Conversions
 - Saturating Offset Calibration
 - Error From Setpoint Calculation
 - High, Low, and Zero-Crossing Compare, With Interrupt Capability
 - Trigger-to-Sample Delay Capture
 - Eight Windowed Comparators With 12-Bit Digital-to-Analog Converter (DAC) References
 - Three 12-Bit Buffered DAC Outputs
- Enhanced Control Peripherals
 - 24 PWM Channels With Enhanced Features
 - 16 High-Resolution Pulse Width Modulator (HRPWM) Channels
 - High Resolution on Both A and B Channels of 8 PWM Modules
 - Dead-Band Support (on Both Standard and High Resolution)
 - Six Enhanced Capture (eCAP) Modules
 - Three Enhanced Quadrature Encoder Pulse (eQEP) Modules
 - Eight Sigma-Delta Filter Module (SDFM) Input Channels, 2 Parallel Filters per Channel
 - Standard SDFM Data Filtering
 - Comparator Filter for Fast Action for Out of Range
- Configurable Logic Block (CLB)
 - Augments Existing Peripheral Capability
 - Supports Position Manager Solutions



- Package Options:
 - Lead-Free, Green Packaging
 - 337-Ball New Fine Pitch Ball Grid Array (nFBGA) [ZWT Suffix]
 - 176-Pin PowerPAD™ Thermally Enhanced Low-Profile Quad Flatpack (HLQFP) [PTP Suffix]
 - 100-Pin PowerPAD Thermally Enhanced Thin Quad Flatpack (HTQFP) [PZP Suffix]
- Temperature Options:
 - T: –40°C to 105°C Junction
 - S: –40°C to 125°C Junction
 - Q: –40°C to 125°C Free-Air (AEC Q100 Qualification for Automotive Applications)

1.2 Applications

- [Advanced Driver Assistance Systems \(ADAS\)](#)
- [Building Automation](#)
- [Electronic Point of Sale](#)
- [Electric Vehicle/Hybrid Electric Vehicle \(EV/HEV\) Powertrain](#)
- [Factory Automation](#)
- [Grid Infrastructure](#)
- [Industrial Transport](#)
- [Medical, Healthcare, and Fitness](#)
- [Motor Drives](#)
- [Power Delivery](#)
- [Telecom Infrastructure](#)
- [Test and Measurement](#)

1.3 Description

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in [real-time control applications](#) such as [industrial motor drives](#); [solar inverters and digital power](#); [electrical vehicles and transportation](#); [motor control](#); and [sensing and signal processing](#). The C2000 line includes the [Delfino™ Premium Performance](#) family and the [Piccolo™ Entry Performance](#) family.

The Delfino™ TMS320F2837xS is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as [industrial motor drives](#); [solar inverters and digital power](#); [electrical vehicles and transportation](#); and [sensing and signal processing](#). Complete development packages for digital power and industrial drives are available as part of the [powerSUITE](#) and [DesignDRIVE](#) initiatives.

The real-time control subsystem is based on TI's 32-bit C28x floating-point CPU, which provides 200 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations; and the VCU accelerator, which reduces the time for complex math operations common in encoded applications.

The F2837xS microcontroller family features a CLA real-time control coprocessor. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics.

The TMS320F2837xS supports up to 1MB (512KW) of onboard flash memory with error correction code (ECC) and up to 164KB (82KW) of SRAM. Two 128-bit secure zones are also available on the CPU for code protection.

Performance analog and control peripherals are also integrated on the F2837xS MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. The new sigma-delta filter module (SDFM) works in conjunction with the sigma-delta modulator to enable isolated current shunt measurements. The Comparator Subsystem (CMPSS) with windowed comparators allows for protection of power stages when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

Peripherals such as EMIFs, CAN modules (ISO 11898-1/CAN 2.0B-compliant), and a new uPP interface extend the connectivity of the F2837xS. The uPP interface is a new feature of the C2000™ MCUs and supports high-speed parallel connection to FPGAs or other processors with similar uPP interfaces. Lastly, a USB 2.0 port with MAC and PHY lets users easily add universal serial bus (USB) connectivity to their application.

To learn more about the C2000 MCUs, visit the C2000 Overview at www.ti.com/c2000.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE |
|------------------|-------------|-------------------|
| TMS320F28379SZWT | nFBGA (337) | 16.0 mm x 16.0 mm |
| TMS320F28377SZWT | nFBGA (337) | 16.0 mm x 16.0 mm |
| TMS320F28376SZWT | nFBGA (337) | 16.0 mm x 16.0 mm |
| TMS320F28375SZWT | nFBGA (337) | 16.0 mm x 16.0 mm |
| TMS320F28374SZWT | nFBGA (337) | 16.0 mm x 16.0 mm |
| TMS320F28379SPTP | HLQFP (176) | 24.0 mm x 24.0 mm |
| TMS320F28378SPTP | HLQFP (176) | 24.0 mm x 24.0 mm |
| TMS320F28377SPTP | HLQFP (176) | 24.0 mm x 24.0 mm |
| TMS320F28376SPTP | HLQFP (176) | 24.0 mm x 24.0 mm |
| TMS320F28375SPTP | HLQFP (176) | 24.0 mm x 24.0 mm |
| TMS320F28374SPTP | HLQFP (176) | 24.0 mm x 24.0 mm |
| TMS320F28379SPZP | HTQFP (100) | 14.0 mm x 14.0 mm |
| TMS320F28378SPZP | HTQFP (100) | 14.0 mm x 14.0 mm |
| TMS320F28377SPZP | HTQFP (100) | 14.0 mm x 14.0 mm |
| TMS320F28376SPZP | HTQFP (100) | 14.0 mm x 14.0 mm |
| TMS320F28375SPZP | HTQFP (100) | 14.0 mm x 14.0 mm |
| TMS320F28374SPZP | HTQFP (100) | 14.0 mm x 14.0 mm |

(1) For more information on these devices, see [Mechanical, Packaging, and Orderable Information](#).

1.4 Functional Block Diagram

Figure 1-1 shows the CPU system and associated peripherals.

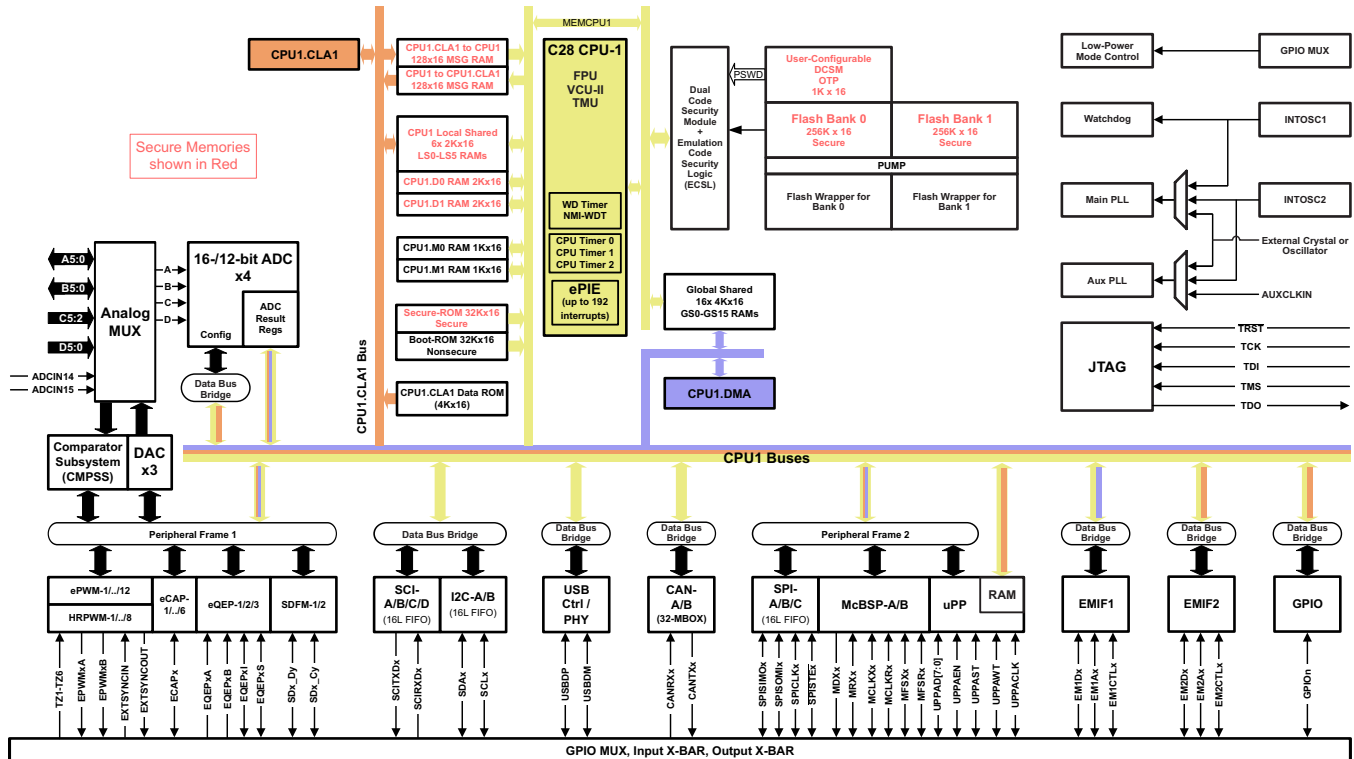


Figure 1-1. Functional Block Diagram

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2 Revision History

| Changes from May 8, 2018 to November 16, 2018 (from F Revision (May 2018) to G Revision) | Page |
|---|---------------------|
| • Global: Added TMS320F28378S..... | 1 |
| • Global: Replaced controlSUITE with C2000Ware. | 1 |
| • Section 1.3 (Description): Updated section. | 2 |
| • Figure 1-1 (Functional Block Diagram): Removed device numbers from the "Flash Bank 1" block and the "Flash Wrapper for Bank 1" block. | 4 |
| • Table 3-1 (Device Comparison): Added data for 28378S. | 7 |
| • Section 3.1 (Related Products): Updated section. | 9 |
| • Table 4-1 (Signal Descriptions): Updated DESCRIPTION of $\overline{\text{XRS}}$ and V_{DD} | 17 |
| • Table 4-7 (Connections for Unused Pins): Updated ACCEPTABLE PRACTICE column of GPIOx, V_{DDA} , and V_{SSA} | 48 |
| • Section 5.9.1 (Power Sequencing): Updated section. | 59 |
| • Figure 5-5 (Power-on Reset): Updated "The $\overline{\text{XRS}}$ pin can be driven externally ..." footnote..... | 61 |
| • Table 5-12 (Internal Clock Frequencies): Removed "Lower LSPCLK will reduce device power consumption. The default at reset is SYSCLK/4." footnote. | 65 |
| • Figure 5-50 (ePWM Trip Input Connectivity): Added PWMSYNC output. | 126 |
| • Figure 5-51 (Synchronization Chain Architecture): Updated figure. | 127 |
| • Section 5.11.5.1 (SDFM Electrical Data and Timing (Using ASYNC)): Changed section title from "SDFM Electrical Data and Timing" to "SDFM Electrical Data and Timing (Using ASYNC)". Updated section. | 136 |
| • Section 5.11.5.1: Added WARNING about glitches and ringing noise on SDFM clock inputs (SDx_Cy pins). | 136 |
| • Table 5-66 (SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option): Changed table title from "SDFM Timing Requirements" to "SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option". | 136 |
| • Section 5.11.5.2 (SDFM Electrical Data and Timing (Using 3-Sample GPIO Input Qualification)): Added section. . | 138 |
| • Section 5.12.1 (Controller Area Network (CAN)): Updated section. | 139 |
| • Table 6-8 (Device Identification Registers): Added PARTIDH for TMS320F28378S. | 186 |
| • Section 6.10 (Dual Code Security Module): Added Code Security Module Disclaimer..... | 197 |
| • Section 8.4 (Documentation Support): Updated section. | 205 |
| • Section 9.1 (Packaging Information): Removed paragraph about the MECHANICAL DATA figure showing a generic thermal pad without dimensions..... | 207 |

3 Device Comparison

Table 3-1 lists the features of each 2837xS device.

Table 3-1. Device Comparison

| FEATURE ⁽¹⁾ | | 28379S | | | 28378S | | 28377S | | | 28376S | | | 28375S | | | 28374S | | | |
|--|--------------------------------|---------------------|--------------------|--------------------|---------------------|--------------------|---------------------|--------------------|--------------------|---------------------|--------------------|--------------------|---------------------|--------------------|--------------------|---------------------|--------------------|--------------------|--|
| Package Type (ZWT is an nFBGA package. PTP is an HLQFP package. PZP is an HTQFP package.) | | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | |
| Processor and Accelerators | | | | | | | | | | | | | | | | | | | |
| C28x | Number | 1 | | | | | | | | | | | | | | | | | |
| | Frequency (MHz) | 200 | | | | | | | | | | | | | | | | | |
| | Floating-Point Unit (FPU) | Yes | | | | | | | | | | | | | | | | | |
| | VCU-II | Yes | | | | | | | | | | | | | | | | | |
| | TMU – Type 0 | Yes | | | | | | | | | | | | | | | | | |
| CLA – Type 1 | Number | 1 | | | | | | | | | | | | | | | | | |
| | Frequency (MHz) | 200 | | | | | | | | | | | | | | | | | |
| 6-Channel DMA – Type 0 | | 1 | | | | | | | | | | | | | | | | | |
| Memory | | | | | | | | | | | | | | | | | | | |
| Flash (16-bit words) | | 1MB (512KW) | | | 1MB (512KW) | | 1MB (512KW) | | | 512KB (256KW) | | | 1MB (512KW) | | | 512KB (256KW) | | | |
| RAM (16-bit words) | Dedicated and Local Shared RAM | 36KB (18KW) | | | | | | | | | | | | | | | | | |
| | Global Shared RAM | 128KB (64KW) | | | 128KB (64KW) | | 128KB (64KW) | | | 96KB (48KW) | | | 128KB (64KW) | | | 96KB (48KW) | | | |
| | Total RAM | 164KB (82KW) | | | 164KB (82KW) | | 164KB (82KW) | | | 132KB (66KW) | | | 164KB (82KW) | | | 132KB (66KW) | | | |
| Code security for on-chip flash, RAM, and OTP blocks | | Yes | | | | | | | | | | | | | | | | | |
| Boot ROM | | Yes | | | | | | | | | | | | | | | | | |
| System | | | | | | | | | | | | | | | | | | | |
| Configurable Logic Block (CLB) | | Yes | | | | | | No | | | | | | | | | | | |
| 32-bit CPU timers | | 3 | | | | | | | | | | | | | | | | | |
| Watchdog timers | | 1 | | | | | | | | | | | | | | | | | |
| Nonmaskable Interrupt Watchdog (NMIWD) timers | | 1 | | | | | | | | | | | | | | | | | |
| Crystal oscillator/External clock input | | 1 | | | | | | | | | | | | | | | | | |
| 0-pin internal oscillator | | 2 | | | | | | | | | | | | | | | | | |
| I/O pins (shared) | GPIO | 169 | 97 | 41 | 97 | 41 | 169 | 97 | 41 | 169 | 97 | 41 | 169 | 97 | 41 | 169 | 97 | 41 | |
| External interrupts | | 5 | | | | | | | | | | | | | | | | | |
| EMIF | EMIF1 (16-bit or 32-bit) | 1 | – | 1 | – | 1 | – | 1 | – | 1 | – | 1 | – | 1 | – | 1 | – | – | |
| | EMIF2 (16-bit) | 1 | – | – | – | – | 1 | – | – | 1 | – | – | 1 | – | – | 1 | – | – | |

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the [C2000 Real-Time Control Peripherals Reference Guide](#).

Table 3-1. Device Comparison (continued)

| FEATURE ⁽¹⁾ | | 28379S | | | 28378S | | | 28377S | | | 28376S | | | 28375S | | | 28374S | | | |
|--|-------------------------------------|---------------------|--------------------|--------------------|--------------------|--------------------|---------------------|--------------------|--------------------|---------------------|--------------------|--------------------|---------------------|--------------------|--------------------|---------------------|--------------------|--------------------|----|--|
| Package Type (ZWT is an nFBGA package. PTP is an HLQFP package. PZP is an HTQFP package.) | | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | 337- Ball ZWT | 176- Pin PTP | 100- Pin PZP | | |
| Analog Peripherals | | | | | | | | | | | | | | | | | | | | |
| ADC 16-bit mode | MSPS | 1.1 | | | – | | | 1.1 | | | – | | | | | | | | | |
| | Conversion Time (ns) ⁽²⁾ | 915 | | | – | | | 915 | | | – | | | | | | | | | |
| | Input pins | 24 | 20 | 14 | – | | | 24 | 20 | 14 | 24 | 20 | 14 | – | | | | | | |
| | Channels (differential) | 12 | 9 | 7 | – | | | 12 | 9 | 7 | 12 | 9 | 7 | – | | | | | | |
| ADC 12-bit mode | MSPS | 3.5 | | | | | | | | | | | | | | | | | | |
| | Conversion Time (ns) ⁽²⁾ | 280 | | | | | | | | | | | | | | | | | | |
| | Input pins | 24 | 20 | 14 | 20 | 14 | 24 | 20 | 14 | 24 | 20 | 14 | 24 | 20 | 14 | 24 | 20 | 14 | | |
| | Channels (single-ended) | 24 | 20 | 14 | 20 | 14 | 24 | 20 | 14 | 24 | 20 | 14 | 24 | 20 | 14 | 24 | 20 | 14 | | |
| Number of 16-bit or 12-bit ADCs | 4 | | 2 | | – | | | 4 | | 2 | | 4 | | | 2 | | – | | | |
| Number of 12-bit only ADCs | – | | | 4 | | 2 | | – | | | 4 | | 2 | | 4 | | 2 | | | |
| Temperature sensor | 1 | | | | | | | | | | | | | | | | | | | |
| CMPSS (each CMPSS has two comparators and two internal DACs) | 8 | | 4 | | 8 | | 4 | | 8 | | 4 | | 8 | | 4 | | 8 | | 4 | |
| Buffered DAC | 3 | | | | | | | | | | | | | | | | | | | |
| Control Peripherals⁽³⁾ | | | | | | | | | | | | | | | | | | | | |
| eCAP inputs – Type 0 | 6 | | | | | | | | | | | | | | | | | | | |
| Enhanced Pulse Width Modulator (ePWM) channels – Type 4 | 24 | | 15 | | 24 | | 15 | | 24 | | 15 | | 24 | | 15 | | 24 | | 15 | |
| eQEP modules – Type 0 | 3 | | 2 | | 3 | | 2 | | 3 | | 2 | | 3 | | 2 | | 3 | | 2 | |
| High-resolution ePWM channels – Type 4 | 16 | | 9 | | 16 | | 9 | | 16 | | 9 | | 16 | | 9 | | 16 | | 9 | |
| SDFM channels – Type 0 | 8 | | 6 | | 8 | | 6 | | 8 | | 6 | | 8 | | 6 | | 8 | | 6 | |
| Communication Peripherals⁽³⁾ | | | | | | | | | | | | | | | | | | | | |
| Controller Area Network (CAN) – Type 0 ⁽⁴⁾ | 2 | | | | | | | | | | | | | | | | | | | |
| Inter-Integrated Circuit (I2C) – Type 0 | 2 | | | | | | | | | | | | | | | | | | | |
| Multichannel Buffered Serial Port (McBSP) – Type 1 | 2 | | | | | | | | | | | | | | | | | | | |
| Serial Communications Interface (SCI) – Type 0 | 4 | | 3 | | 4 | | 3 | | 4 | | 3 | | 4 | | 3 | | 4 | | 3 | |
| Serial Peripheral Interface (SPI) – Type 2 | 3 | | | | | | | | | | | | | | | | | | | |
| Universal Serial Bus (USB) – Type 0 | 1 | | | | | | | | | | | | | | | | | | | |
| uPP – Type 0 | 1 | | | | | | | | | | | | | | | | | | | |
| Temperature and Qualification | | | | | | | | | | | | | | | | | | | | |
| Junction Temperature (T _J) | T: –40°C to 105°C | Yes | | | No | | | Yes | | | | | | | | | | | | |
| | S: –40°C to 125°C | Yes | | | | | | | | | | | | | | | | | | |
| | Q: –40°C to 150°C ⁽⁵⁾ | No | | | No | | | Yes | | | No | | | No | | Yes | | No | | |
| Free-Air Temperature (T _A) | Q: –40°C to 125°C ⁽⁵⁾ | | No | | No | | Yes | | No | | No | | Yes | | No | | | | | |

- (2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
- (3) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has less device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number. See [Section 4](#) to identify which peripheral instances are accessible on pins in the smaller package.
- (4) The CAN module uses the IP known as *D_CAN*. This document uses the names *CAN* and *D_CAN* interchangeably to reference this peripheral.
- (5) The letter Q refers to AEC Q100 qualification for automotive applications.

3.1 Related Products

For information about other devices in the [Delfino](#) family of products, see the following links:

[TMS320F2837xD Delfino™ Microcontrollers](#)

The F2837xD series sets a new standard for performance with dual subsystems. Each subsystem consists of a C28x CPU and a parallel control law accelerator (CLA), each running at 200 MHz. Enhancing performance are TMU and VCU [accelerators](#). New capabilities include multiple 16-bit/12-bit mode ADCs, DAC, Sigma-Delta filters, USB, configurable logic block (CLB), on-chip oscillators, and enhanced versions of all peripherals. The F2837xD is available with up to 1MB of Flash. It is available in a 176-pin QFP or 337-pin BGA package.

[TMS320F2837xS Delfino™ Microcontrollers](#)

The F2837xS series is a pin-to-pin compatible version of F2837xD but with only one C28x-CPU-and-CLA subsystem enabled. It is also available in a 100-pin QFP to enable compatibility with the [Piccolo™ TMS320F2807x](#) series.

4 Terminal Configuration and Functions

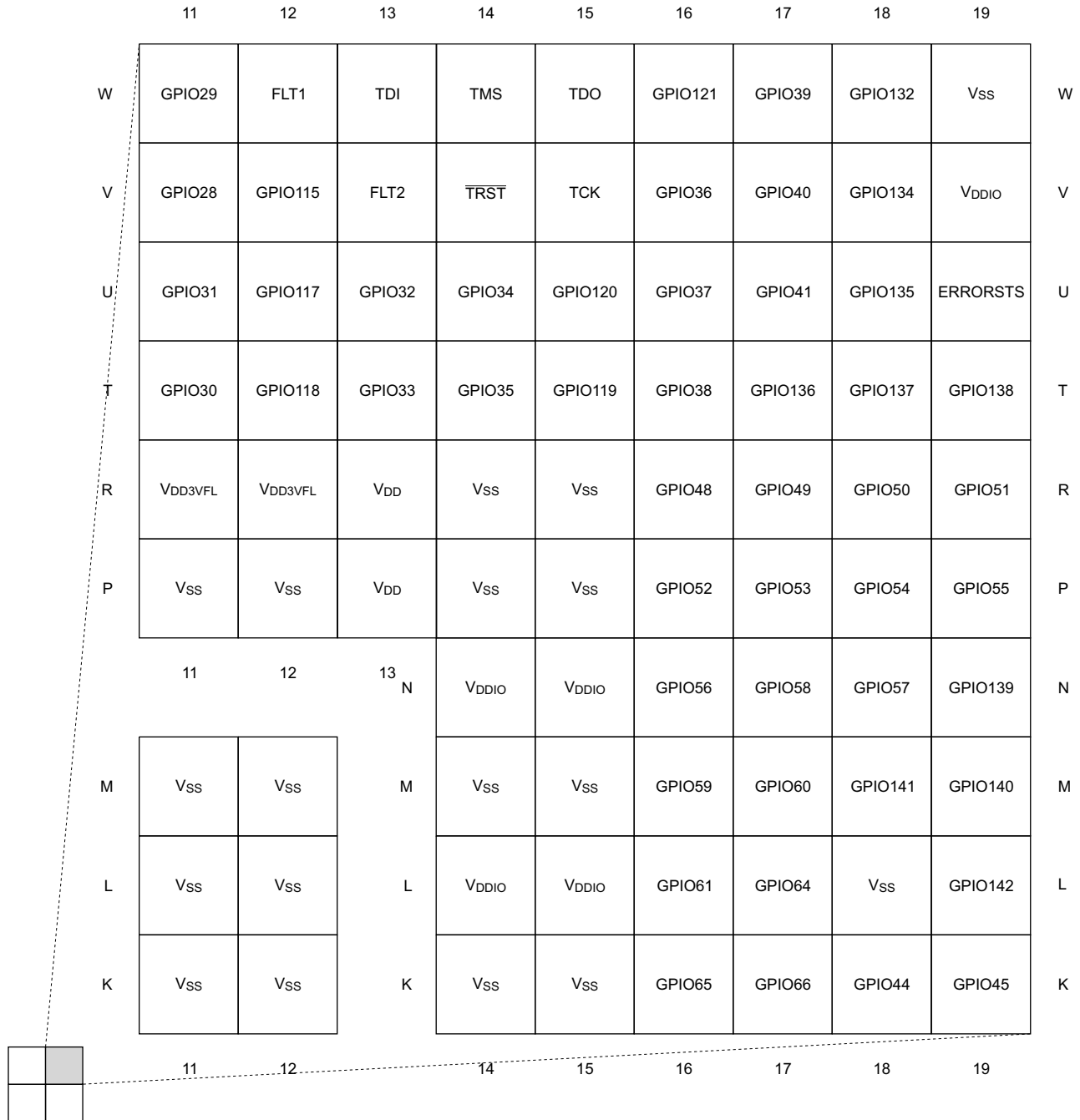
4.1 Pin Diagrams

Figure 4-1 to Figure 4-4 show the terminal assignments on the 337-ball ZWT New Fine Pitch Ball Grid Array. Each figure shows a quadrant of the terminal assignments. Figure 4-5 shows the pin assignments on the 176-pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack. Figure 4-6 shows the pin assignments on the 100-pin PZP PowerPAD Thermally Enhanced Thin Quad Flatpack.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---------------------|---------------------|---------|---------|---------------------|---------------------|------------------|-------------------|-------------------|-----------------|---|
| W | V _{SSA} | ADCINB1 | ADCINB3 | ADCINB5 | V _{REFHIB} | V _{REFLOD} | V _{SS} | V _{DDIO} | GPIO128 | GPIO116 | W |
| V | V _{REFHIA} | ADCINB0 | ADCINB2 | ADCINB4 | V _{REFHID} | V _{REFLOB} | V _{SSA} | GPIO124 | GPIO127 | GPIO131 | V |
| U | ADCINA0 | ADCINA2 | ADCINA4 | ADCIN15 | ADCIND1 | ADCIND3 | ADCIND5 | GPIO123 | GPIO126 | GPIO130 | U |
| T | ADCINA1 | ADCINA3 | ADCINA5 | ADCIN14 | ADCIND0 | ADCIND2 | ADCIND4 | GPIO122 | GPIO125 | GPIO129 | T |
| R | V _{REFHIC} | V _{REFLOA} | ADCINC2 | ADCINC4 | V _{SSA} | V _{DDA} | V _{SS} | V _{SS} | V _{DDIO} | V _{DD} | R |
| P | V _{SSA} | V _{REFLOC} | ADCINC3 | ADCINC5 | V _{SSA} | V _{DDA} | V _{SS} | V _{SS} | V _{DDIO} | V _{DD} | P |
| N | V _{SS} | GPIO109 | GPIO114 | GPIO113 | V _{SS} | V _{SS} | 7 N | 8 | 9 | 10 | N |
| M | V _{DDIO} | GPIO110 | GPIO112 | GPIO111 | V _{DDIO} | V _{DDIO} | M | V _{SS} | V _{SS} | V _{SS} | M |
| L | GPIO27 | GPIO106 | GPIO107 | GPIO108 | V _{SS} | V _{SS} | L | V _{SS} | V _{SS} | V _{SS} | L |
| K | GPIO26 | GPIO25 | GPIO24 | GPIO23 | V _{DD} | V _{DD} | K | V _{SS} | V _{SS} | V _{SS} | K |
| | 1 | 2 | 3 | 4 | 5 | 6 | | 8 | 9 | 10 | |

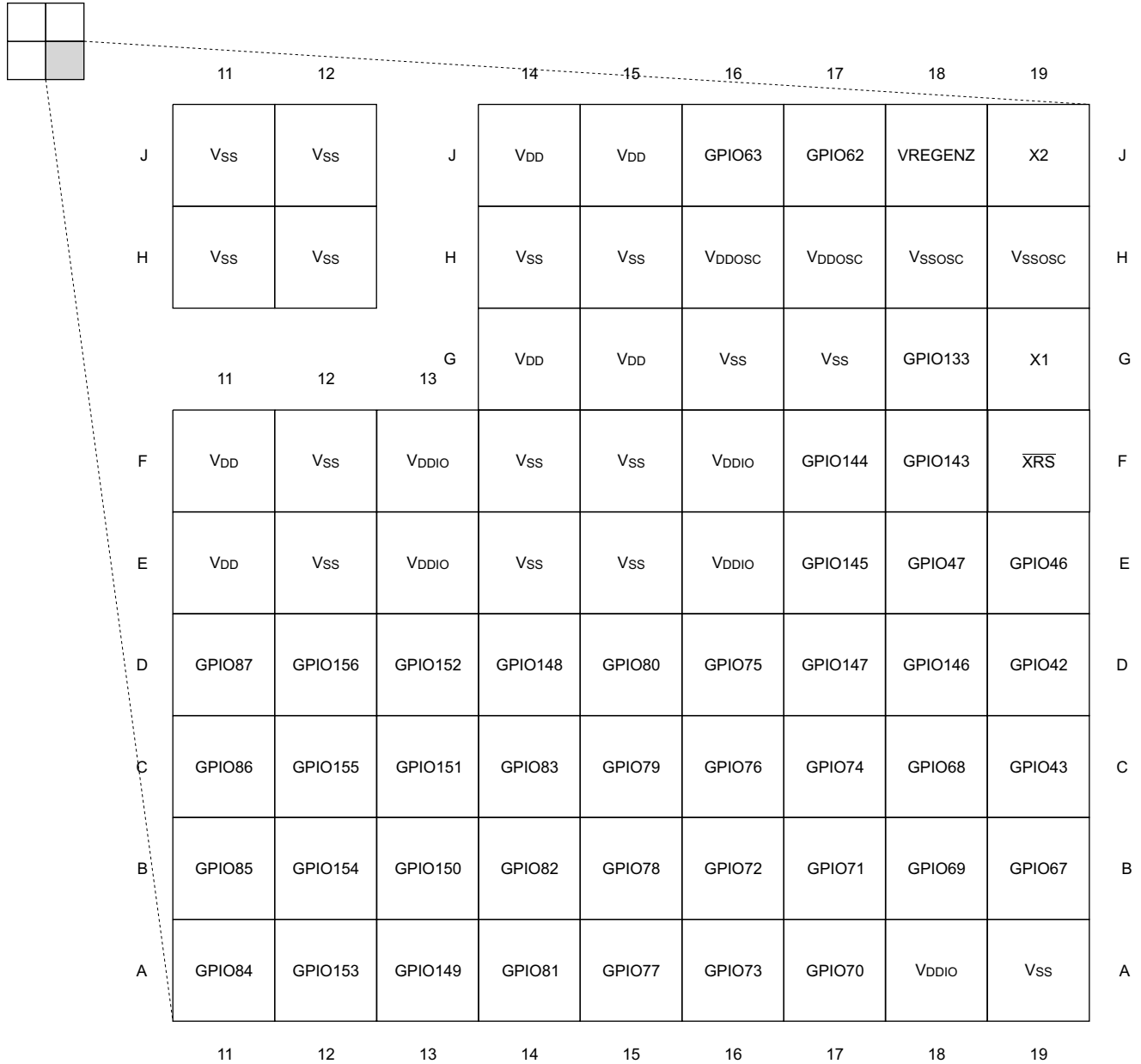
A. Only the GPIO function is shown on GPIO terminals. See Table 4-1 for the complete, muxed signal name.

Figure 4-1. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant A]



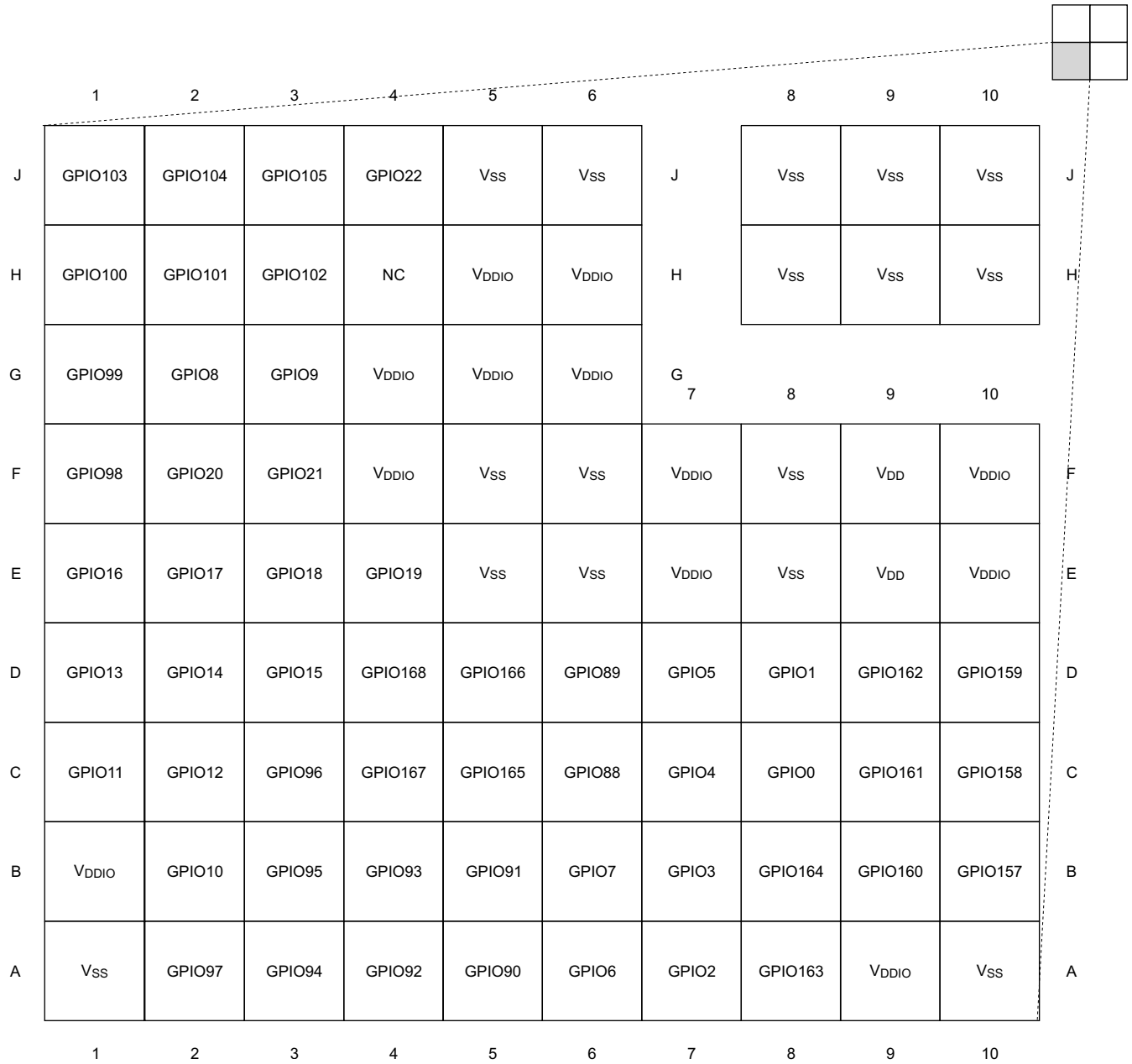
A. Only the GPIO function is shown on GPIO terminals. See [Table 4-1](#) for the complete, muxed signal name.

Figure 4-2. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant B]



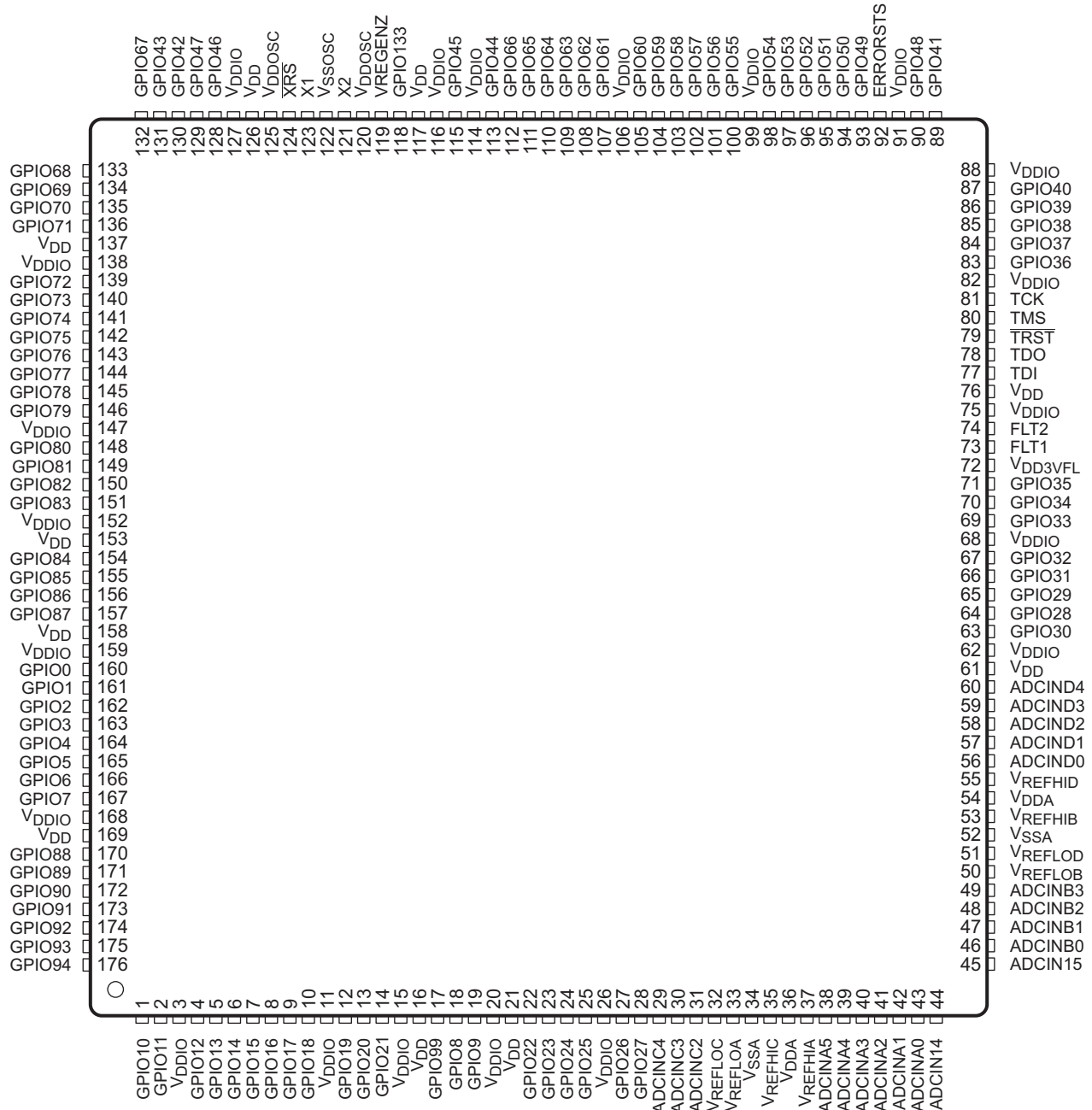
A. Only the GPIO function is shown on GPIO terminals. See [Table 4-1](#) for the complete, muxed signal name.

Figure 4-3. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant C]



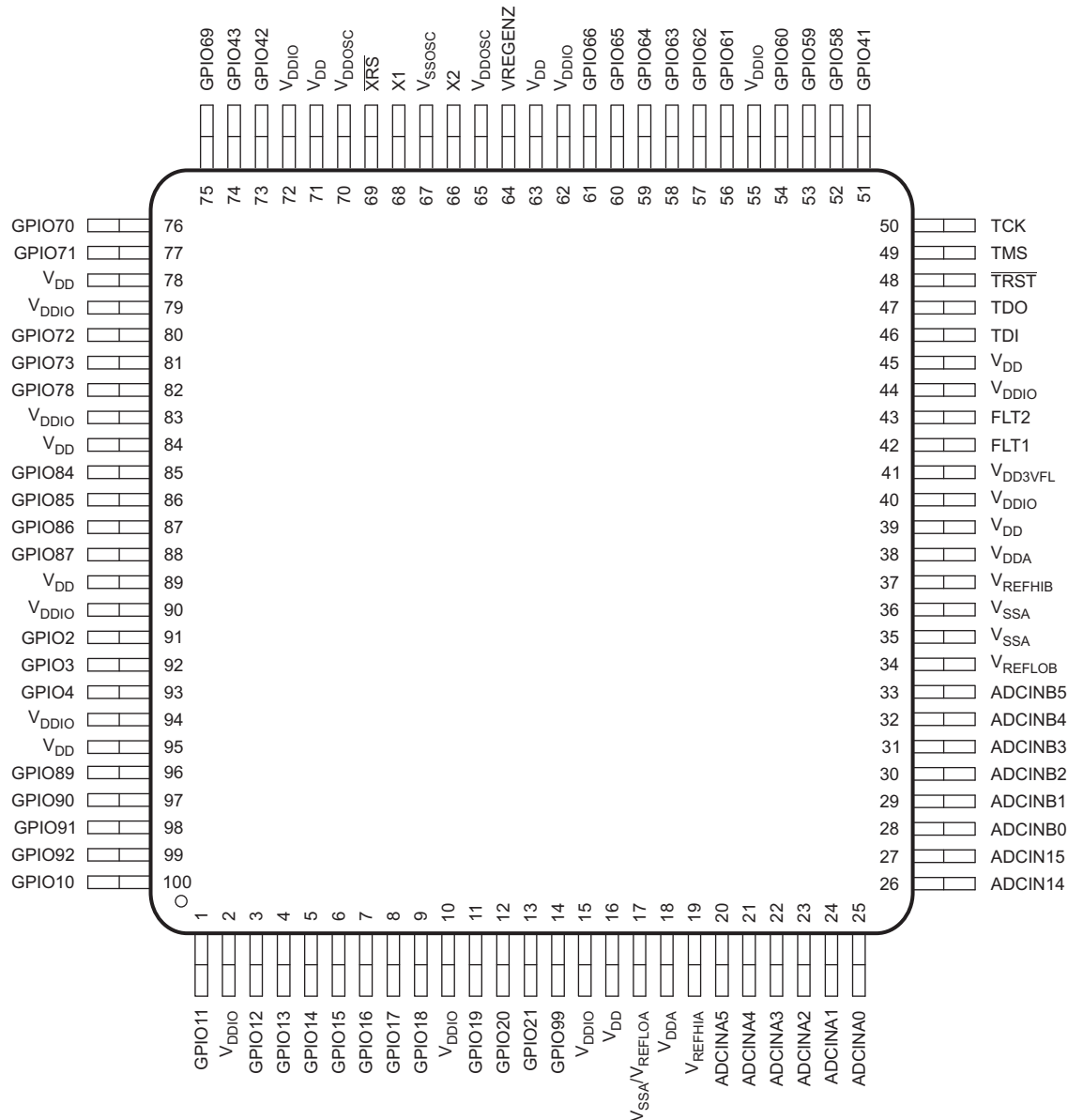
A. Only the GPIO function is shown on GPIO terminals. See [Table 4-1](#) for the complete, muxed signal name.

Figure 4-4. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant D]



A. Only the GPIO function is shown on GPIO pins. See [Table 4-1](#) for the complete, muxed signal name.

Figure 4-5. 176-Pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO pins. See [Table 4-1](#) for the complete, muxed signal name.

Figure 4-6. 100-Pin PZP PowerPAD HTQFP (Top View)

NOTE

The exposed lead frame die pad of the PowerPAD™ package serves two functions: to remove heat from the die and to provide ground path for the digital ground (analog ground is provided through dedicated pins). Thus, the PowerPAD should be soldered to the ground (GND) plane of the PCB because this will provide both the digital ground path and good thermal conduction path. To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD. The thermal land should be soldered to the exposed lead frame die pad of the PowerPAD package; the thermal land should be as large as needed to dissipate the required heat. An array of thermal vias should be used to connect the thermal pad to the internal GND plane of the board. See [PowerPAD™ Thermally Enhanced Package](#) for more details on using the PowerPAD package.

NOTE

PCB footprints and schematic symbols are available for download in a vendor-neutral format, which can be exported to the leading EDA CAD/CAE design tools. See the CAD/CAE Symbols section in the product folder for each device, under the Packaging section. These footprints and symbols can also be searched for at <http://webench.ti.com/cad/>.

4.2 Signal Descriptions

Table 4-1 describes the signals. The GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 3-1 for details. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups are not enabled at reset.

Table 4-1. Signal Descriptions

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|---|--------------|--------------|-------------|-------------|----------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| ADC, DAC, AND COMPARATOR SIGNALS | | | | | | |
| V _{REFHIA} | | V1 | 37 | 19 | I | ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1- μ F capacitor on this pin for the 12-bit mode, or at least a 22- μ F capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V _{REFHIA} and V _{REFLOA} pins. NOTE: Do not load this pin externally. |
| V _{REFHIB} | | W5 | 53 | 37 | I | ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1- μ F capacitor on this pin for the 12-bit mode, or at least a 22- μ F capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V _{REFHIB} and V _{REFLOB} pins. NOTE: Do not load this pin externally. |
| V _{REFHIC} | | R1 | 35 | – | I | ADC-C high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1- μ F capacitor on this pin for the 12-bit mode, or at least a 22- μ F capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V _{REFHIC} and V _{REFLOC} pins. NOTE: Do not load this pin externally. |
| V _{REFHID} | | V5 | 55 | – | I | ADC-D high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1- μ F capacitor on this pin for the 12-bit mode, or at least a 22- μ F capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V _{REFHID} and V _{REFLOD} pins. NOTE: Do not load this pin externally. |
| V _{REFLOA} | | R2 | 33 | 17 | I | ADC-A low reference. On the PZP package, pin 17 is double-bonded to V _{SSA} and V _{REFLOA} . On the PZP package, pin 17 must be connected to V _{SSA} on the system board. |
| V _{REFLOB} | | V6 | 50 | 34 | I | ADC-B low reference |
| V _{REFLOC} | | P2 | 32 | – | I | ADC-C low reference |
| V _{REFLOD} | | W6 | 51 | – | I | ADC-D low reference |
| ADCIN14 | | T4 | 44 | 26 | I | Input 14 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference. |
| CMPIN4P | | | | | I | Comparator 4 positive input |
| ADCIN15 | | U4 | 45 | 27 | I | Input 15 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference. |
| CMPIN4N | | | | | I | Comparator 4 negative input |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|--------------------|--------------|--------------|-------------|-------------|----------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| ADCINA0 DACOUTA | | U1 | 43 | 25 | I O | ADC-A input 0. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled. DAC-A output |
| ADCINA1 DACOUTB | | T1 | 42 | 24 | I O | ADC-A input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled. DAC-B output |
| ADCINA2 CMPIN1P | | U2 | 41 | 23 | I I | ADC-A input 2 Comparator 1 positive input |
| ADCINA3 CMPIN1N | | T2 | 40 | 22 | I I | ADC-A input 3 Comparator 1 negative input |
| ADCINA4 CMPIN2P | | U3 | 39 | 21 | I I | ADC-A input 4 Comparator 2 positive input |
| ADCINA5 CMPIN2N | | T3 | 38 | 20 | I I | ADC-A input 5 Comparator 2 negative input |
| ADCINB0 VDAC | | V2 | 46 | 28 | I I | ADC-B input 0. There is a 100-pF capacitor to V _{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-μF capacitor on this pin. Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to V _{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-μF capacitor on this pin. |
| ADCINB1 DACOUTC | | W2 | 47 | 29 | I O | ADC-B input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled. DAC-C output |
| ADCINB2 CMPIN3P | | V3 | 48 | 30 | I I | ADC-B input 2 Comparator 3 positive input |
| ADCINB3 CMPIN3N | | W3 | 49 | 31 | I I | ADC-B input 3 Comparator 3 negative input |
| ADCINB4 | | V4 | – | 32 | I | ADC-B input 4 |
| ADCINB5 | | W4 | – | 33 | I | ADC-B input 5 |
| ADCINC2 CMPIN6P | | R3 | 31 | – | I I | ADC-C input 2 Comparator 6 positive input |
| ADCINC3 CMPIN6N | | P3 | 30 | – | I I | ADC-C input 3 Comparator 6 negative input |
| ADCINC4 CMPIN5P | | R4 | 29 | – | I I | ADC-C input 4 Comparator 5 positive input |
| ADCINC5 CMPIN5N | | P4 | – | – | I I | ADC-C input 5 Comparator 5 negative input |
| ADCIND0 CMPIN7P | | T5 | 56 | – | I I | ADC-D input 0 Comparator 7 positive input |
| ADCIND1 CMPIN7N | | U5 | 57 | – | I I | ADC-D input 1 Comparator 7 negative input |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|------------------------------------|--------------|--------------|-------------|-------------|----------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| ADCIND2 | | T6 | 58 | – | I | ADC-D input 2 |
| CMPIN8P | | | | | I | Comparator 8 positive input |
| ADCIND3 | | U6 | 59 | – | I | ADC-D input 3 |
| CMPIN8N | | | | | I | Comparator 8 negative input |
| ADCIND4 | | T7 | 60 | – | I | ADC-D input 4 |
| ADCIND5 | | U7 | – | – | I | ADC-D input 5 |
| GPIO AND PERIPHERAL SIGNALS | | | | | | |
| GPIO0 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 0 |
| EPWM1A | 1 | C8 | 160 | – | O | Enhanced PWM1 output A (HRPWM-capable) |
| SDAA | 6 | | | | I/OD | I2C-A data open-drain bidirectional port |
| GPIO1 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 1 |
| EPWM1B | 1 | D8 | 161 | – | O | Enhanced PWM1 output B (HRPWM-capable) |
| MFSRB | 3 | | | | I/O | McBSP-B receive frame synch |
| SCLA | 6 | | | | I/OD | I2C-A clock open-drain bidirectional port |
| GPIO2 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 2 |
| EPWM2A | 1 | A7 | 162 | 91 | O | Enhanced PWM2 output A (HRPWM-capable) |
| OUTPUTXBAR1 | 5 | | | | O | Output 1 of the output XBAR |
| SDAB | 6 | | | | I/OD | I2C-B data open-drain bidirectional port |
| GPIO3 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 3 |
| EPWM2B | 1 | | | | O | Enhanced PWM2 output B (HRPWM-capable) |
| OUTPUTXBAR2 | 2 | | | | O | Output 2 of the output XBAR |
| MCLKRB | 3 | B7 | 163 | 92 | I/O | McBSP-B receive clock |
| OUTPUTXBAR2 | 5 | | | | O | Output 2 of the output XBAR |
| SCLB | 6 | | | | I/OD | I2C-B clock open-drain bidirectional port |
| GPIO4 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 4 |
| EPWM3A | 1 | C7 | 164 | 93 | O | Enhanced PWM3 output A (HRPWM-capable) |
| OUTPUTXBAR3 | 5 | | | | O | Output 3 of the output XBAR |
| CANTXA | 6 | | | | O | CAN-A transmit |
| GPIO5 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 5 |
| EPWM3B | 1 | D7 | 165 | – | O | Enhanced PWM3 output B (HRPWM-capable) |
| MFSRA | 2 | | | | I/O | McBSP-A receive frame synch |
| OUTPUTXBAR3 | 3 | | | | O | Output 3 of the output XBAR |
| CANRXA | 6 | | | | I | CAN-A receive |
| GPIO6 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 6 |
| EPWM4A | 1 | A6 | 166 | – | O | Enhanced PWM4 output A (HRPWM-capable) |
| OUTPUTXBAR4 | 2 | | | | O | Output 4 of the output XBAR |
| EXTSYNCOUT | 3 | | | | O | External ePWM synch pulse output |
| EQEP3A | 5 | | | | I | Enhanced QEP3 input A |
| CANTXB | 6 | | | | O | CAN-B transmit |
| GPIO7 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 7 |
| EPWM4B | 1 | | | | O | Enhanced PWM4 output B (HRPWM-capable) |
| MCLKRA | 2 | B6 | 167 | – | I/O | McBSP-A receive clock |
| OUTPUTXBAR5 | 3 | | | | O | Output 5 of the output XBAR |
| EQEP3B | 5 | | | | I | Enhanced QEP3 input B |
| CANRXB | 6 | | | | I | CAN-B receive |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-------------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO8 | 0, 4, 8, 12 | G2 | 18 | - | I/O | General-purpose input/output 8 |
| EPWM5A | 1 | | | | O | Enhanced PWM5 output A (HRPWM-capable) |
| CANTXB | 2 | | | | O | CAN-B transmit |
| ADCSOCAO | 3 | | | | O | ADC start-of-conversion A output for external ADC |
| EQEP3S | 5 | | | | I/O | Enhanced QEP3 strobe |
| SCITXDA | 6 | | | | O | SCI-A transmit data |
| GPIO9 | 0, 4, 8, 12 | G3 | 19 | - | I/O | General-purpose input/output 9 |
| EPWM5B | 1 | | | | O | Enhanced PWM5 output B (HRPWM-capable) |
| SCITXDB | 2 | | | | O | SCI-B transmit data |
| OUTPUTXBAR6 | 3 | | | | O | Output 6 of the output XBAR |
| EQEP3I | 5 | | | | I/O | Enhanced QEP3 index |
| SCIRXDA | 6 | | | | I | SCI-A receive data |
| GPIO10 | 0, 4, 8, 12 | B2 | 1 | 100 | I/O | General-purpose input/output 10 |
| EPWM6A | 1 | | | | O | Enhanced PWM6 output A (HRPWM-capable) |
| CANRXB | 2 | | | | I | CAN-B receive |
| ADCSOCBO | 3 | | | | O | ADC start-of-conversion B output for external ADC |
| EQEP1A | 5 | | | | I | Enhanced QEP1 input A |
| SCITXDB | 6 | | | | O | SCI-B transmit data |
| UPP-WAIT | 15 | | | | I/O | Universal parallel port wait. Receiver asserts to request a pause in transfer. |
| GPIO11 | 0, 4, 8, 12 | C1 | 2 | 1 | I/O | General-purpose input/output 11 |
| EPWM6B | 1 | | | | O | Enhanced PWM6 output B (HRPWM-capable) |
| SCIRXDB | 2, 6 | | | | I | SCI-B receive data |
| OUTPUTXBAR7 | 3 | | | | O | Output 7 of the output XBAR |
| EQEP1B | 5 | | | | I | Enhanced QEP1 input B |
| UPP-START | 15 | | | | I/O | Universal parallel port start. Transmitter asserts at start of DMA line. |
| GPIO12 | 0, 4, 8, 12 | C2 | 4 | 3 | I/O | General-purpose input/output 12 |
| EPWM7A | 1 | | | | O | Enhanced PWM7 output A (HRPWM-capable) |
| CANTXB | 2 | | | | O | CAN-B transmit |
| MDXB | 3 | | | | O | McBSP-B transmit serial data |
| EQEP1S | 5 | | | | I/O | Enhanced QEP1 strobe |
| SCITXDC | 6 | | | | O | SCI-C transmit data |
| UPP-ENA | 15 | | | | I/O | Universal parallel port enable. Transmitter asserts while data bus is active. |
| GPIO13 | 0, 4, 8, 12 | D1 | 5 | 4 | I/O | General-purpose input/output 13 |
| EPWM7B | 1 | | | | O | Enhanced PWM7 output B (HRPWM-capable) |
| CANRXB | 2 | | | | I | CAN-B receive |
| MDRB | 3 | | | | I | McBSP-B receive serial data |
| EQEP1I | 5 | | | | I/O | Enhanced QEP1 index |
| SCIRXDC | 6 | | | | I | SCI-C receive data |
| UPP-D7 | 15 | | | | I/O | Universal parallel port data line 7 |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-----------------------------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO14 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 14 |
| EPWM8A | 1 | | | | O | Enhanced PWM8 output A (HRPWM-capable) |
| SCITXDB | 2 | D2 | 6 | 5 | O | SCI-B transmit data |
| MCLKXB | 3 | | | | I/O | McBSP-B transmit clock |
| OUTPUTXBAR3 | 6 | | | | O | Output 3 of the output XBAR |
| UPP-D6 | 15 | | | | I/O | Universal parallel port data line 6 |
| GPIO15 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 15 |
| EPWM8B | 1 | | | | O | Enhanced PWM8 output B (HRPWM-capable) |
| SCIRXDB | 2 | D3 | 7 | 6 | I | SCI-B receive data |
| MFSXB | 3 | | | | I/O | McBSP-B transmit frame synch |
| OUTPUTXBAR4 | 6 | | | | O | Output 4 of the output XBAR |
| UPP-D5 | 15 | | | | I/O | Universal parallel port data line 5 |
| GPIO16 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 16 |
| SPISIMOA | 1 | | | | I/O | SPI-A slave in, master out |
| CANTXB | 2 | | | | O | CAN-B transmit |
| OUTPUTXBAR7 | 3 | E1 | 8 | 7 | O | Output 7 of the output XBAR |
| EPWM9A | 5 | | | | O | Enhanced PWM9 output A |
| SD1_D1 | 7 | | | | I | Sigma-Delta 1 channel 1 data input |
| UPP-D4 | 15 | | | | I/O | Universal parallel port data line 4 |
| GPIO17 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 17 |
| SPISOMIA | 1 | | | | I/O | SPI-A slave out, master in |
| CANRXB | 2 | | | | I | CAN-B receive |
| OUTPUTXBAR8 | 3 | E2 | 9 | 8 | O | Output 8 of the output XBAR |
| EPWM9B | 5 | | | | O | Enhanced PWM9 output B |
| SD1_C1 | 7 | | | | I | Sigma-Delta 1 channel 1 clock input |
| UPP-D3 | 15 | | | | I/O | Universal parallel port data line 3 |
| GPIO18 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 18 |
| SPICLKA | 1 | | | | I/O | SPI-A clock |
| SCITXDB | 2 | | | | O | SCI-B transmit data |
| CANRXA | 3 | E3 | 10 | 9 | I | CAN-A receive |
| EPWM10A | 5 | | | | O | Enhanced PWM10 output A |
| SD1_D2 | 7 | | | | I | Sigma-Delta 1 channel 2 data input |
| UPP-D2 | 15 | | | | I/O | Universal parallel port data line 2 |
| GPIO19 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 19 |
| $\overline{\text{SPISTEA}}$ | 1 | | | | I/O | SPI-A slave transmit enable |
| SCIRXDB | 2 | | | | I | SCI-B receive data |
| CANTXA | 3 | E4 | 12 | 11 | O | CAN-A transmit |
| EPWM10B | 5 | | | | O | Enhanced PWM10 output B |
| SD1_C2 | 7 | | | | I | Sigma-Delta 1 channel 2 clock input |
| UPP-D1 | 15 | | | | I/O | Universal parallel port data line 1 |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-------------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO20 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 20 |
| EQEP1A | 1 | | | | I | Enhanced QEP1 input A |
| MDXA | 2 | | | | O | McBSP-A transmit serial data |
| CANTXB | 3 | F2 | 13 | 12 | O | CAN-B transmit |
| EPWM11A | 5 | | | | O | Enhanced PWM11 output A |
| SD1_D3 | 7 | | | | I | Sigma-Delta 1 channel 3 data input |
| UPP-D0 | 15 | | | | I/O | Universal parallel port data line 0 |
| GPIO21 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 21 |
| EQEP1B | 1 | | | | I | Enhanced QEP1 input B |
| MDRA | 2 | | | | I | McBSP-A receive serial data |
| CANRXB | 3 | F3 | 14 | 13 | I | CAN-B receive |
| EPWM11B | 5 | | | | O | Enhanced PWM11 output B |
| SD1_C3 | 7 | | | | I | Sigma-Delta 1 channel 3 clock input |
| UPP-CLK | 15 | | | | I/O | Universal parallel port transmit clock |
| GPIO22 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 22 |
| EQEP1S | 1 | | | | I/O | Enhanced QEP1 strobe |
| MCLKXA | 2 | | | | I/O | McBSP-A transmit clock |
| SCITXDB | 3 | J4 | 22 | – | O | SCI-B transmit data |
| EPWM12A | 5 | | | | O | Enhanced PWM12 output A |
| SPICKLB | 6 | | | | I/O | SPI-B clock |
| SD1_D4 | 7 | | | | I | Sigma-Delta 1 channel 4 data input |
| GPIO23 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 23 |
| EQEP1I | 1 | | | | I/O | Enhanced QEP1 index |
| MFSXA | 2 | | | | I/O | McBSP-A transmit frame synch |
| SCIRXDB | 3 | K4 | 23 | – | I | SCI-B receive data |
| EPWM12B | 5 | | | | O | Enhanced PWM12 output B |
| SPISTEB | 6 | | | | I/O | SPI-B slave transmit enable |
| SD1_C4 | 7 | | | | I | Sigma-Delta 1 channel 4 clock input |
| GPIO24 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 24 |
| OUTPUTXBAR1 | 1 | | | | O | Output 1 of the output XBAR |
| EQEP2A | 2 | | | | I | Enhanced QEP2 input A |
| MDXB | 3 | K3 | 24 | – | O | McBSP-B transmit serial data |
| SPISIMOB | 6 | | | | I/O | SPI-B slave in, master out |
| SD2_D1 | 7 | | | | I | Sigma-Delta 2 channel 1 data input |
| GPIO25 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 25 |
| OUTPUTXBAR2 | 1 | | | | O | Output 2 of the output XBAR |
| EQEP2B | 2 | | | | I | Enhanced QEP2 input B |
| MDRB | 3 | K2 | 25 | – | I | McBSP-B receive serial data |
| SPISOMIB | 6 | | | | I/O | SPI-B slave out, master in |
| SD2_C1 | 7 | | | | I | Sigma-Delta 2 channel 1 clock input |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-------------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO26 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 26 |
| OUTPUTXBAR3 | 1 | | | | O | Output 3 of the output XBAR |
| EQEP2I | 2 | | | | I/O | Enhanced QEP2 index |
| MCLKXB | 3 | K1 | 27 | – | I/O | McBSP-B transmit clock |
| OUTPUTXBAR3 | 5 | | | | O | Output 3 of the output XBAR |
| SPICLKB | 6 | | | | I/O | SPI-B clock |
| SD2_D2 | 7 | | | | I | Sigma-Delta 2 channel 2 data input |
| GPIO27 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 27 |
| OUTPUTXBAR4 | 1 | | | | O | Output 4 of the output XBAR |
| EQEP2S | 2 | | | | I/O | Enhanced QEP2 strobe |
| MFSXB | 3 | L1 | 28 | – | I/O | McBSP-B transmit frame synch |
| OUTPUTXBAR4 | 5 | | | | O | Output 4 of the output XBAR |
| SPISTEB | 6 | | | | I/O | SPI-B slave transmit enable |
| SD2_C2 | 7 | | | | I | Sigma-Delta 2 channel 2 clock input |
| GPIO28 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 28 |
| SCIRXDA | 1 | | | | I | SCI-A receive data |
| EM1CS4 | 2 | V11 | 64 | – | O | External memory interface 1 chip select 4 |
| OUTPUTXBAR5 | 5 | | | | O | Output 5 of the output XBAR |
| EQEP3A | 6 | | | | I | Enhanced QEP3 input A |
| SD2_D3 | 7 | | | | I | Sigma-Delta 2 channel 3 data input |
| GPIO29 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 29 |
| SCITXDA | 1 | | | | O | SCI-A transmit data |
| EM1SDCKE | 2 | W11 | 65 | – | O | External memory interface 1 SDRAM clock enable |
| OUTPUTXBAR6 | 5 | | | | O | Output 6 of the output XBAR |
| EQEP3B | 6 | | | | I | Enhanced QEP3 input B |
| SD2_C3 | 7 | | | | I | Sigma-Delta 2 channel 3 clock input |
| GPIO30 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 30 |
| CANRXA | 1 | | | | I | CAN-A receive |
| EM1CLK | 2 | T11 | 63 | – | O | External memory interface 1 clock |
| OUTPUTXBAR7 | 5 | | | | O | Output 7 of the output XBAR |
| EQEP3S | 6 | | | | I/O | Enhanced QEP3 strobe |
| SD2_D4 | 7 | | | | I | Sigma-Delta 2 channel 4 data input |
| GPIO31 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 31 |
| CANTXA | 1 | | | | O | CAN-A transmit |
| EM1WE | 2 | U11 | 66 | – | O | External memory interface 1 write enable |
| OUTPUTXBAR8 | 5 | | | | O | Output 8 of the output XBAR |
| EQEP3I | 6 | | | | I/O | Enhanced QEP3 index |
| SD2_C4 | 7 | | | | I | Sigma-Delta 2 channel 4 clock input |
| GPIO32 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 32 |
| SDAA | 1 | U13 | 67 | – | I/OD | I2C-A data open-drain bidirectional port |
| EM1CS0 | 2 | | | | O | External memory interface 1 chip select 0 |
| GPIO33 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 33 |
| SCLA | 1 | T13 | 69 | – | I/OD | I2C-A clock open-drain bidirectional port |
| EM1RNW | 2 | | | | O | External memory interface 1 read not write |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|--|----------------------------------|--------------|-------------|-------------|-------------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO34 OUTPUTXBAR1 $\overline{\text{EM1CS2}}$ SDAB | 0, 4, 8, 12 1 2 6 | U14 | 70 | – | I/O O O I/OD | General-purpose input/output 34 Output 1 of the output XBAR External memory interface 1 chip select 2 I2C-B data open-drain bidirectional port |
| GPIO35 SCIRXDA $\overline{\text{EM1CS3}}$ SCLB | 0, 4, 8, 12 1 2 6 | T14 | 71 | – | I/O I O I/OD | General-purpose input/output 35 SCI-A receive data External memory interface 1 chip select 3 I2C-B clock open-drain bidirectional port |
| GPIO36 SCITXDA EM1WAIT CANRXA | 0, 4, 8, 12 1 2 6 | V16 | 83 | – | I/O O I I | General-purpose input/output 36 SCI-A transmit data External memory interface 1 Asynchronous SRAM WAIT CAN-A receive |
| GPIO37 OUTPUTXBAR2 $\overline{\text{EM1OE}}$ CANTXA | 0, 4, 8, 12 1 2 6 | U16 | 84 | – | I/O O O O | General-purpose input/output 37 Output 2 of the output XBAR External memory interface 1 output enable CAN-A transmit |
| GPIO38 EM1A0 SCITXDC CANTXB | 0, 4, 8, 12 2 5 6 | T16 | 85 | – | I/O O O O | General-purpose input/output 38 External memory interface 1 address line 0 SCI-C transmit data CAN-B transmit |
| GPIO39 EM1A1 SCIRXDC CANRXB | 0, 4, 8, 12 2 5 6 | W17 | 86 | – | I/O O I I | General-purpose input/output 39 External memory interface 1 address line 1 SCI-C receive data CAN-B receive |
| GPIO40 EM1A2 SDAB | 0, 4, 8, 12 2 6 | V17 | 87 | – | I/O O I/OD | General-purpose input/output 40 External memory interface 1 address line 2 I2C-B data open-drain bidirectional port |
| GPIO41 EM1A3 SCLB | 0, 4, 8, 12 2 6 | U17 | 89 | 51 | I/O O I/OD | General-purpose input/output 41. For applications using the Hibernate low-power mode, this pin serves as the GPIOHIBWAKE signal. For details, see the Low Power Modes section of the System Control chapter in the TMS320F2837xS Delfino Microcontrollers Technical Reference Manual . External memory interface 1 address line 3 I2C-B clock open-drain bidirectional port |
| GPIO42 SDAA SCITXDA USB0DM | 0, 4, 8, 12 6 15 Analog | D19 | 130 | 73 | I/O I/OD O I/O | General-purpose input/output 42 I2C-A data open-drain bidirectional port SCI-A transmit data USB PHY differential data |
| GPIO43 SCLA SCIRXDA USB0DP | 0, 4, 8, 12 6 15 Analog | C19 | 131 | 74 | I/O I/OD I I/O | General-purpose input/output 43 I2C-A clock open-drain bidirectional port SCI-A receive data USB PHY differential data |
| GPIO44 EM1A4 | 0, 4, 8, 12 2 | K18 | 113 | – | I/O O | General-purpose input/output 44 External memory interface 1 address line 4 |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|---|--------------------------------------|--------------|-------------|-------------|--------------------------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO45 EM1A5 | 0, 4, 8, 12 2 | K19 | 115 | – | I/O O | General-purpose input/output 45 External memory interface 1 address line 5 |
| GPIO46 EM1A6 SCIRXDD | 0, 4, 8, 12 2 6 | E19 | 128 | – | I/O O I | General-purpose input/output 46 External memory interface 1 address line 6 SCI-D receive data |
| GPIO47 EM1A7 SCITXDD | 0, 4, 8, 12 2 6 | E18 | 129 | – | I/O O O | General-purpose input/output 47 External memory interface 1 address line 7 SCI-D transmit data |
| GPIO48 OUTPUTXBAR3 EM1A8 SCITXDA SD1_D1 | 0, 4, 8, 12 1 2 6 7 | R16 | 90 | – | I/O O O O I | General-purpose input/output 48 Output 3 of the output XBAR External memory interface 1 address line 8 SCI-A transmit data Sigma-Delta 1 channel 1 data input |
| GPIO49 OUTPUTXBAR4 EM1A9 SCIRXDA SD1_C1 | 0, 4, 8, 12 1 2 6 7 | R17 | 93 | – | I/O O O I I | General-purpose input/output 49 Output 4 of the output XBAR External memory interface 1 address line 9 SCI-A receive data Sigma-Delta 1 channel 1 clock input |
| GPIO50 EQEP1A EM1A10 SPISIMOC SD1_D2 | 0, 4, 8, 12 1 2 6 7 | R18 | 94 | – | I/O I O I/O I | General-purpose input/output 50 Enhanced QEP1 input A External memory interface 1 address line 10 SPI-C slave in, master out Sigma-Delta 1 channel 2 data input |
| GPIO51 EQEP1B EM1A11 SPISOMIC SD1_C2 | 0, 4, 8, 12 1 2 6 7 | R19 | 95 | – | I/O I O I/O I | General-purpose input/output 51 Enhanced QEP1 input B External memory interface 1 address line 11 SPI-C slave out, master in Sigma-Delta 1 channel 2 clock input |
| GPIO52 EQEP1S EM1A12 SPICLK SD1_D3 | 0, 4, 8, 12 1 2 6 7 | P16 | 96 | – | I/O I/O O I/O I | General-purpose input/output 52 Enhanced QEP1 strobe External memory interface 1 address line 12 SPI-C clock Sigma-Delta 1 channel 3 data input |
| GPIO53 EQEP1I EM1D31 EM2D15 SPISTEC SD1_C3 | 0, 4, 8, 12 1 2 3 6 7 | P17 | 97 | – | I/O I/O I/O I/O I/O I | General-purpose input/output 53 Enhanced QEP1 index External memory interface 1 data line 31 External memory interface 2 data line 15 SPI-C slave transmit enable Sigma-Delta 1 channel 3 clock input |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-------------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO54 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 54 |
| SPISIMOA | 1 | | | | I/O | SPI-A slave in, master out |
| EM1D30 | 2 | | | | I/O | External memory interface 1 data line 30 |
| EM2D14 | 3 | P18 | 98 | – | I/O | External memory interface 2 data line 14 |
| EQEP2A | 5 | | | | I | Enhanced QEP2 input A |
| SCITXDB | 6 | | | | O | SCI-B transmit data |
| SD1_D4 | 7 | | | | I | Sigma-Delta 1 channel 4 data input |
| GPIO55 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 55 |
| SPISOMIA | 1 | | | | I/O | SPI-A slave out, master in |
| EM1D29 | 2 | | | | I/O | External memory interface 1 data line 29 |
| EM2D13 | 3 | P19 | 100 | – | I/O | External memory interface 2 data line 13 |
| EQEP2B | 5 | | | | I | Enhanced QEP2 input B |
| SCIRXDB | 6 | | | | I | SCI-B receive data |
| SD1_C4 | 7 | | | | I | Sigma-Delta 1 channel 4 clock input |
| GPIO56 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 56 |
| SPICKLA | 1 | | | | I/O | SPI-A clock |
| EM1D28 | 2 | | | | I/O | External memory interface 1 data line 28 |
| EM2D12 | 3 | N16 | 101 | – | I/O | External memory interface 2 data line 12 |
| EQEP2S | 5 | | | | I/O | Enhanced QEP2 strobe |
| SCITXDC | 6 | | | | O | SCI-C transmit data |
| SD2_D1 | 7 | | | | I | Sigma-Delta 2 channel 1 data input |
| GPIO57 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 57 |
| SPISTEA | 1 | | | | I/O | SPI-A slave transmit enable |
| EM1D27 | 2 | | | | I/O | External memory interface 1 data line 27 |
| EM2D11 | 3 | N18 | 102 | – | I/O | External memory interface 2 data line 11 |
| EQEP2I | 5 | | | | I/O | Enhanced QEP2 index |
| SCIRXDC | 6 | | | | I | SCI-C receive data |
| SD2_C1 | 7 | | | | I | Sigma-Delta 2 channel 1 clock input |
| GPIO58 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 58 |
| MCLKRA | 1 | | | | I/O | McBSP-A receive clock |
| EM1D26 | 2 | | | | I/O | External memory interface 1 data line 26 |
| EM2D10 | 3 | | | | I/O | External memory interface 2 data line 10 |
| OUTPUTXBAR1 | 5 | N17 | 103 | 52 | O | Output 1 of the output XBAR |
| SPICKLB | 6 | | | | I/O | SPI-B clock |
| SD2_D2 | 7 | | | | I | Sigma-Delta 2 channel 2 data input |
| SPISIMOA | 15 | | | | I/O | SPI-A slave in, master out ⁽²⁾ |
| GPIO59 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 59 ⁽³⁾ |
| MFSRA | 1 | | | | I/O | McBSP-A receive frame synch |
| EM1D25 | 2 | | | | I/O | External memory interface 1 data line 25 |
| EM2D9 | 3 | | | | I/O | External memory interface 2 data line 9 |
| OUTPUTXBAR2 | 5 | M16 | 104 | 53 | O | Output 2 of the output XBAR |
| SPISTEB | 6 | | | | I/O | SPI-B slave transmit enable |
| SD2_C2 | 7 | | | | I | Sigma-Delta 2 channel 2 clock input |
| SPISOMIA | 15 | | | | I/O | SPI-A slave out, master in ⁽²⁾ |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-------------|--------------|--------------|---|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO60 | 0, 4, 8, 12 | M17 | 105 | 54 | I/O | General-purpose input/output 60 |
| MCLKRB | 1 | | | | I/O | McBSP-B receive clock |
| EM1D24 | 2 | | | | I/O | External memory interface 1 data line 24 |
| EM2D8 | 3 | | | | I/O | External memory interface 2 data line 8 |
| OUTPUTXBAR3 | 5 | | | | O | Output 3 of the output XBAR |
| SPISIMOB | 6 | | | | I/O | SPI-B slave in, master out |
| SD2_D3 | 7 | | | | I | Sigma-Delta 2 channel 3 data input |
| SPICLKA | 15 | | | | I/O | SPI-A clock ⁽²⁾ |
| GPIO61 | 0, 4, 8, 12 | L16 | 107 | 56 | I/O | General-purpose input/output 61 ⁽³⁾ |
| MFSRB | 1 | | | | I/O | McBSP-B receive frame synch |
| EM1D23 | 2 | | | | I/O | External memory interface 1 data line 23 |
| EM2D7 | 3 | | | | I/O | External memory interface 2 data line 7 |
| OUTPUTXBAR4 | 5 | | | | O | Output 4 of the output XBAR |
| SPISOMIB | 6 | | | | I/O | SPI-B slave out, master in |
| SD2_C3 | 7 | | | | I | Sigma-Delta 2 channel 3 clock input |
| SPISTEA | 15 | | | | I/O | SPI-A slave transmit enable ⁽²⁾ |
| GPIO62 | 0, 4, 8, 12 | J17 | 108 | 57 | I/O | General-purpose input/output 62 |
| SCIRXDC | 1 | | | | I | SCI-C receive data |
| EM1D22 | 2 | | | | I/O | External memory interface 1 data line 22 |
| EM2D6 | 3 | | | | I/O | External memory interface 2 data line 6 |
| EQEP3A | 5 | | | | I | Enhanced QEP3 input A |
| CANRXA | 6 | | | | I | CAN-A receive |
| SD2_D4 | 7 | | | | I | Sigma-Delta 2 channel 4 data input |
| GPIO63 | 0, 4, 8, 12 | J16 | 109 | 58 | I/O | General-purpose input/output 63 |
| SCITXDC | 1 | | | | O | SCI-C transmit data |
| EM1D21 | 2 | | | | I/O | External memory interface 1 data line 21 |
| EM2D5 | 3 | | | | I/O | External memory interface 2 data line 5 |
| EQEP3B | 5 | | | | I | Enhanced QEP3 input B |
| CANTXA | 6 | | | | O | CAN-A transmit |
| SD2_C4 | 7 | | | | I | Sigma-Delta 2 channel 4 clock input |
| SPISIMOB | 15 | I/O | SPI-B slave in, master out ⁽²⁾ | | | |
| GPIO64 | 0, 4, 8, 12 | L17 | 110 | 59 | I/O | General-purpose input/output 64 ⁽³⁾ |
| EM1D20 | 2 | | | | I/O | External memory interface 1 data line 20 |
| EM2D4 | 3 | | | | I/O | External memory interface 2 data line 4 |
| EQEP3S | 5 | | | | I/O | Enhanced QEP3 strobe |
| SCIRXDA | 6 | | | | I | SCI-A receive data |
| SPISOMIB | 15 | | | | I/O | SPI-B slave out, master in ⁽²⁾ |
| GPIO65 | 0, 4, 8, 12 | K16 | 111 | 60 | I/O | General-purpose input/output 65 |
| EM1D19 | 2 | | | | I/O | External memory interface 1 data line 19 |
| EM2D3 | 3 | | | | I/O | External memory interface 2 data line 3 |
| EQEP3I | 5 | | | | I/O | Enhanced QEP3 index |
| SCITXDA | 6 | | | | O | SCI-A transmit data |
| SPICLKB | 15 | | | | I/O | SPI-B clock ⁽²⁾ |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|----------|--------------|--------------|-------------|-------------|----------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO66 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 66 ⁽³⁾ |
| EM1D18 | 2 | | | | I/O | External memory interface 1 data line 18 |
| EM2D2 | 3 | K17 | 112 | 61 | I/O | External memory interface 2 data line 2 |
| SDAB | 6 | | | | I/OD | I2C-B data open-drain bidirectional port |
| SPISTEB | 15 | | | | I/O | SPI-B slave transmit enable ⁽²⁾ |
| GPIO67 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 67 |
| EM1D17 | 2 | B19 | 132 | – | I/O | External memory interface 1 data line 17 |
| EM2D1 | 3 | | | | I/O | External memory interface 2 data line 1 |
| GPIO68 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 68 |
| EM1D16 | 2 | C18 | 133 | – | I/O | External memory interface 1 data line 16 |
| EM2D0 | 3 | | | | I/O | External memory interface 2 data line 0 |
| GPIO69 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 69 |
| EM1D15 | 2 | B18 | 134 | 75 | I/O | External memory interface 1 data line 15 |
| SCLB | 6 | | | | I/OD | I2C-B clock open-drain bidirectional port |
| SPISIMOC | 15 | | | | I/O | SPI-C slave in, master out ⁽²⁾ |
| GPIO70 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 70 ⁽³⁾ |
| EM1D14 | 2 | | | | I/O | External memory interface 1 data line 14 |
| CANRXA | 5 | A17 | 135 | 76 | I | CAN-A receive |
| SCITXDB | 6 | | | | O | SCI-B transmit data |
| SPISOMIC | 15 | | | | I/O | SPI-C slave out, master in ⁽²⁾ |
| GPIO71 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 71 |
| EM1D13 | 2 | | | | I/O | External memory interface 1 data line 13 |
| CANTXA | 5 | B17 | 136 | 77 | O | CAN-A transmit |
| SCIRXDB | 6 | | | | I | SCI-B receive data |
| SPICLK | 15 | | | | I/O | SPI-C clock ⁽²⁾ |
| GPIO72 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 72. ⁽³⁾ This is the factory default boot mode select pin 1. |
| EM1D12 | 2 | B16 | 139 | 80 | I/O | External memory interface 1 data line 12 |
| CANTXB | 5 | | | | O | CAN-B transmit |
| SCITXDC | 6 | | | | O | SCI-C transmit data |
| SPISTEC | 15 | | | | I/O | SPI-C slave transmit enable ⁽²⁾ |
| GPIO73 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 73 |
| EM1D11 | 2 | | | | I/O | External memory interface 1 data line 11 |
| XCLKOUT | 3 | A16 | 140 | 81 | O/Z | External clock output. This pin outputs a divided-down version of a chosen clock signal from within the device. The clock signal is chosen using the CLKSRCCTL3.XCLKOUTSEL bit field while the divide ratio is chosen using the XCLKOUTDIVSEL.XCLKOUTDIV bit field. |
| CANRXB | 5 | | | | I | CAN-B receive |
| SCIRXDC | 6 | | | | I | SCI-C receive |
| GPIO74 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 74 |
| EM1D10 | 2 | C17 | 141 | – | I/O | External memory interface 1 data line 10 |
| GPIO75 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 75 |
| EM1D9 | 2 | D16 | 142 | – | I/O | External memory interface 1 data line 9 |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|---------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO76 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 76 |
| EM1D8 | 2 | C16 | 143 | – | I/O | External memory interface 1 data line 8 |
| SCITXDD | 6 | | | | O | SCI-D transmit data |
| GPIO77 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 77 |
| EM1D7 | 2 | A15 | 144 | – | I/O | External memory interface 1 data line 7 |
| SCIRXDD | 6 | | | | I | SCI-D receive data |
| GPIO78 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 78 |
| EM1D6 | 2 | B15 | 145 | 82 | I/O | External memory interface 1 data line 6 |
| EQEP2A | 6 | | | | I | Enhanced QEP2 input A |
| GPIO79 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 79 |
| EM1D5 | 2 | C15 | 146 | – | I/O | External memory interface 1 data line 5 |
| EQEP2B | 6 | | | | I | Enhanced QEP2 input B |
| GPIO80 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 80 |
| EM1D4 | 2 | D15 | 148 | – | I/O | External memory interface 1 data line 4 |
| EQEP2S | 6 | | | | I/O | Enhanced QEP2 strobe |
| GPIO81 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 81 |
| EM1D3 | 2 | A14 | 149 | – | I/O | External memory interface 1 data line 3 |
| EQEP2I | 6 | | | | I/O | Enhanced QEP2 index |
| GPIO82 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 82 |
| EM1D2 | 2 | B14 | 150 | – | I/O | External memory interface 1 data line 2 |
| GPIO83 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 83 |
| EM1D1 | 2 | C14 | 151 | – | I/O | External memory interface 1 data line 1 |
| GPIO84 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 84. This is the factory default boot mode select pin 0. |
| SCITXDA | 5 | A11 | 154 | 85 | O | SCI-A transmit data |
| MDXB | 6 | | | | O | McBSP-B transmit serial data |
| MDXA | 15 | | | | O | McBSP-A transmit serial data |
| GPIO85 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 85 |
| EM1D0 | 2 | | | | I/O | External memory interface 1 data line 0 |
| SCIRXDA | 5 | B11 | 155 | 86 | I | SCI-A receive data |
| MDRB | 6 | | | | I | McBSP-B receive serial data |
| MDRA | 15 | | | | I | McBSP-A receive serial data |
| GPIO86 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 86 |
| EM1A13 | 2 | | | | O | External memory interface 1 address line 13 |
| EM1CAS | 3 | | | | O | External memory interface 1 column address strobe |
| SCITXDB | 5 | C11 | 156 | 87 | O | SCI-B transmit data |
| MCLKXB | 6 | | | | I/O | McBSP-B transmit clock |
| MCLKXA | 15 | | | | I/O | McBSP-A transmit clock |
| GPIO87 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 87 |
| EM1A14 | 2 | | | | O | External memory interface 1 address line 14 |
| EM1RAS | 3 | | | | O | External memory interface 1 row address strobe |
| SCIRXDB | 5 | D11 | 157 | 88 | I | SCI-B receive data |
| MFSXB | 6 | | | | I/O | McBSP-B transmit frame synch |
| MFSXA | 15 | | | | I/O | McBSP-A transmit frame synch |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|----------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO88 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 88 |
| EM1A15 | 2 | C6 | 170 | – | O | External memory interface 1 address line 15 |
| EM1DQM0 | 3 | | | | O | External memory interface 1 Input/output mask for byte 0 |
| GPIO89 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 89 |
| EM1A16 | 2 | D6 | 171 | 96 | O | External memory interface 1 address line 16 |
| EM1DQM1 | 3 | | | | O | External memory interface 1 Input/output mask for byte 1 |
| SCITXDC | 6 | | | | O | SCI-C transmit data |
| GPIO90 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 90 |
| EM1A17 | 2 | A5 | 172 | 97 | O | External memory interface 1 address line 17 |
| EM1DQM2 | 3 | | | | O | External memory interface 1 Input/output mask for byte 2 |
| SCIRXDC | 6 | | | | I | SCI-C receive data |
| GPIO91 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 91 |
| EM1A18 | 2 | B5 | 173 | 98 | O | External memory interface 1 address line 18 |
| EM1DQM3 | 3 | | | | O | External memory interface 1 Input/output mask for byte 3 |
| SDAA | 6 | | | | I/OD | I2C-A data open-drain bidirectional port |
| GPIO92 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 92 |
| EM1A19 | 2 | A4 | 174 | 99 | O | External memory interface 1 address line 19 |
| EM1BA1 | 3 | | | | O | External memory interface 1 bank address 1 |
| SCLA | 6 | | | | I/OD | I2C-A clock open-drain bidirectional port |
| GPIO93 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 93 |
| EM1BA0 | 3 | B4 | 175 | – | O | External memory interface 1 bank address 0 |
| SCITXDD | 6 | | | | O | SCI-D transmit data |
| GPIO94 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 94 |
| SCIRXDD | 6 | A3 | 176 | – | I | SCI-D receive data |
| GPIO95 | 0, 4, 8, 12 | B3 | – | – | I/O | General-purpose input/output 95 |
| GPIO96 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 96 |
| EM2DQM1 | 3 | C3 | – | – | O | External memory interface 2 Input/output mask for byte 1 |
| EQEP1A | 5 | | | | I | Enhanced QEP1 input A |
| GPIO97 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 97 |
| EM2DQM0 | 3 | A2 | – | – | O | External memory interface 2 Input/output mask for byte 0 |
| EQEP1B | 5 | | | | I | Enhanced QEP1 input B |
| GPIO98 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 98 |
| EM2A0 | 3 | F1 | – | – | O | External memory interface 2 address line 0 |
| EQEP1S | 5 | | | | I/O | Enhanced QEP1 strobe |
| GPIO99 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 99 |
| EM2A1 | 3 | G1 | 17 | 14 | O | External memory interface 2 address line 1 |
| EQEP1I | 5 | | | | I/O | Enhanced QEP1 index |
| GPIO100 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 100 |
| EM2A2 | 3 | H1 | – | – | O | External memory interface 2 address line 2 |
| EQEP2A | 5 | | | | I | Enhanced QEP2 input A |
| SPISIMOC | 6 | | | | I/O | SPI-C slave in, master out |
| GPIO101 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 101 |
| EM2A3 | 3 | H2 | – | – | O | External memory interface 2 address line 3 |
| EQEP2B | 5 | | | | I | Enhanced QEP2 input B |
| SPISOMIC | 6 | | | | I/O | SPI-C slave out, master in |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|---------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO102 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 102 |
| EM2A4 | 3 | H3 | – | – | O | External memory interface 2 address line 4 |
| EQEP2S | 5 | | | | I/O | Enhanced QEP2 strobe |
| SPICLK | 6 | | | | I/O | SPI-C clock |
| GPIO103 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 103 |
| EM2A5 | 3 | J1 | – | – | O | External memory interface 2 address line 5 |
| EQEP2I | 5 | | | | I/O | Enhanced QEP2 index |
| SPISTEC | 6 | | | | I/O | SPI-C slave transmit enable |
| GPIO104 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 104 |
| SDAA | 1 | | | | I/OD | I2C-A data open-drain bidirectional port |
| EM2A6 | 3 | J2 | – | – | O | External memory interface 2 address line 6 |
| EQEP3A | 5 | | | | I | Enhanced QEP3 input A |
| SCITXDD | 6 | | | | O | SCI-D transmit data |
| GPIO105 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 105 |
| SCLA | 1 | | | | I/OD | I2C-A clock open-drain bidirectional port |
| EM2A7 | 3 | J3 | – | – | O | External memory interface 2 address line 7 |
| EQEP3B | 5 | | | | I | Enhanced QEP3 input B |
| SCIRXDD | 6 | | | | I | SCI-D receive data |
| GPIO106 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 106 |
| EM2A8 | 3 | L2 | – | – | O | External memory interface 2 address line 8 |
| EQEP3S | 5 | | | | I/O | Enhanced QEP3 strobe |
| SCITXDC | 6 | | | | O | SCI-C transmit data |
| GPIO107 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 107 |
| EM2A9 | 3 | L3 | – | – | O | External memory interface 2 address line 9 |
| EQEP3I | 5 | | | | I/O | Enhanced QEP3 index |
| SCIRXDC | 6 | | | | I | SCI-C receive data |
| GPIO108 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 108 |
| EM2A10 | 3 | L4 | – | – | O | External memory interface 2 address line 10 |
| GPIO109 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 109 |
| EM2A11 | 3 | N2 | – | – | O | External memory interface 2 address line 11 |
| GPIO110 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 110 |
| EM2WAIT | 3 | M2 | – | – | I | External memory interface 2 Asynchronous SRAM WAIT |
| GPIO111 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 111 |
| EM2BA0 | 3 | M4 | – | – | O | External memory interface 2 bank address 0 |
| GPIO112 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 112 |
| EM2BA1 | 3 | M3 | – | – | O | External memory interface 2 bank address 1 |
| GPIO113 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 113 |
| EM2CAS | 3 | N4 | – | – | O | External memory interface 2 column address strobe |
| GPIO114 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 114 |
| EM2RAS | 3 | N3 | – | – | O | External memory interface 2 row address strobe |
| GPIO115 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 115 |
| EM2CS0 | 3 | V12 | – | – | O | External memory interface 2 chip select 0 |
| GPIO116 | 0, 4, 8, 12 | | | | I/O | General-purpose input/output 116 |
| EM2CS2 | 3 | W10 | – | – | O | External memory interface 2 chip select 2 |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-------------------------------|------------------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO117 EM2SDCKE | 0, 4, 8, 12 3 | U12 | – | – | I/O O | General-purpose input/output 117 External memory interface 2 SDRAM clock enable |
| GPIO118 EM2CLK | 0, 4, 8, 12 3 | T12 | – | – | I/O O | General-purpose input/output 118 External memory interface 2 clock |
| GPIO119 EM2RNW | 0, 4, 8, 12 3 | T15 | – | – | I/O O | General-purpose input/output 119 External memory interface 2 read not write |
| GPIO120 EM2WE USB0PFLT | 0, 4, 8, 12 3 15 | U15 | – | – | I/O O I/O | General-purpose input/output 120 External memory interface 2 write enable USB external regulator power fault indicator |
| GPIO121 EM2OE USB0EPEN | 0, 4, 8, 12 3 15 | W16 | – | – | I/O O I/O | General-purpose input/output 121 External memory interface 2 output enable USB external regulator enable |
| GPIO122 SPISIMOC SD1_D1 | 0, 4, 8, 12 6 7 | T8 | – | – | I/O I/O I | General-purpose input/output 122 SPI-C slave in, master out Sigma-Delta 1 channel 1 data input |
| GPIO123 SPISOMIC SD1_C1 | 0, 4, 8, 12 6 7 | U8 | – | – | I/O I/O I | General-purpose input/output 123 SPI-C slave out, master in Sigma-Delta 1 channel 1 clock input |
| GPIO124 SPICLK SD1_D2 | 0, 4, 8, 12 6 7 | V8 | – | – | I/O I/O I | General-purpose input/output 124 SPI-C clock Sigma-Delta 1 channel 2 data input |
| GPIO125 SPISTEC SD1_C2 | 0, 4, 8, 12 6 7 | T9 | – | – | I/O I/O I | General-purpose input/output 125 SPI-C slave transmit enable Sigma-Delta 1 channel 2 clock input |
| GPIO126 SD1_D3 | 0, 4, 8, 12 7 | U9 | – | – | I/O I | General-purpose input/output 126 Sigma-Delta 1 channel 3 data input |
| GPIO127 SD1_C3 | 0, 4, 8, 12 7 | V9 | – | – | I/O I | General-purpose input/output 127 Sigma-Delta 1 channel 3 clock input |
| GPIO128 SD1_D4 | 0, 4, 8, 12 7 | W9 | – | – | I/O I | General-purpose input/output 128 Sigma-Delta 1 channel 4 data input |
| GPIO129 SD1_C4 | 0, 4, 8, 12 7 | T10 | – | – | I/O I | General-purpose input/output 129 Sigma-Delta 1 channel 4 clock input |
| GPIO130 SD2_D1 | 0, 4, 8, 12 7 | U10 | – | – | I/O I | General-purpose input/output 130 Sigma-Delta 2 channel 1 data input |
| GPIO131 SD2_C1 | 0, 4, 8, 12 7 | V10 | – | – | I/O I | General-purpose input/output 131 Sigma-Delta 2 channel 1 clock input |
| GPIO132 SD2_D2 | 0, 4, 8, 12 7 | W18 | – | – | I/O I | General-purpose input/output 132 Sigma-Delta 2 channel 2 data input |
| GPIO133/AUXCLKIN SD2_C2 | 0, 4, 8, 12 7 | G18 | 118 | – | I/O I | General-purpose input/output 133. The AUXCLKIN function of this GPIO pin could be used to provide a single-ended 3.3-V level clock signal to the Auxiliary Phase-Locked Loop (AUXPLL), whose output is used for the USB module. The AUXCLKIN clock may also be used for the CAN module. Sigma-Delta 2 channel 2 clock input |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|------------------------------|-----------------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO134 SD2_D3 | 0, 4, 8, 12 7 | V18 | – | – | I/O I | General-purpose input/output 134 Sigma-Delta 2 channel 3 data input |
| GPIO135 SCITXDA SD2_C3 | 0, 4, 8, 12 6 7 | U18 | – | – | I/O O I | General-purpose input/output 135 SCI-A transmit data Sigma-Delta 2 channel 3 clock input |
| GPIO136 SCIRXDA SD2_D4 | 0, 4, 8, 12 6 7 | T17 | – | – | I/O I I | General-purpose input/output 136 SCI-A receive data Sigma-Delta 2 channel 4 data input |
| GPIO137 SCITXDB SD2_C4 | 0, 4, 8, 12 6 7 | T18 | – | – | I/O O I | General-purpose input/output 137 SCI-B transmit data Sigma-Delta 2 channel 4 clock input |
| GPIO138 SCIRXDB | 0, 4, 8, 12 6 | T19 | – | – | I/O I | General-purpose input/output 138 SCI-B receive data |
| GPIO139 SCIRXDC | 0, 4, 8, 12 6 | N19 | – | – | I/O I | General-purpose input/output 139 SCI-C receive data |
| GPIO140 SCITXDC | 0, 4, 8, 12 6 | M19 | – | – | I/O O | General-purpose input/output 140 SCI-C transmit data |
| GPIO141 SCIRXDD | 0, 4, 8, 12 6 | M18 | – | – | I/O I | General-purpose input/output 141 SCI-D receive data |
| GPIO142 SCITXDD | 0, 4, 8, 12 6 | L19 | – | – | I/O O | General-purpose input/output 142 SCI-D transmit data |
| GPIO143 | 0, 4, 8, 12 | F18 | – | – | I/O | General-purpose input/output 143 |
| GPIO144 | 0, 4, 8, 12 | F17 | – | – | I/O | General-purpose input/output 144 |
| GPIO145 EPWM1A | 0, 4, 8, 12 1 | E17 | – | – | I/O O | General-purpose input/output 145 Enhanced PWM1 output A (HRPWM-capable) |
| GPIO146 EPWM1B | 0, 4, 8, 12 1 | D18 | – | – | I/O O | General-purpose input/output 146 Enhanced PWM1 output B (HRPWM-capable) |
| GPIO147 EPWM2A | 0, 4, 8, 12 1 | D17 | – | – | I/O O | General-purpose input/output 147 Enhanced PWM2 output A (HRPWM-capable) |
| GPIO148 EPWM2B | 0, 4, 8, 12 1 | D14 | – | – | I/O O | General-purpose input/output 148 Enhanced PWM2 output B (HRPWM-capable) |
| GPIO149 EPWM3A | 0, 4, 8, 12 1 | A13 | – | – | I/O O | General-purpose input/output 149 Enhanced PWM3 output A (HRPWM-capable) |
| GPIO150 EPWM3B | 0, 4, 8, 12 1 | B13 | – | – | I/O O | General-purpose input/output 150 Enhanced PWM3 output B (HRPWM-capable) |
| GPIO151 EPWM4A | 0, 4, 8, 12 1 | C13 | – | – | I/O O | General-purpose input/output 151 Enhanced PWM4 output A (HRPWM-capable) |
| GPIO152 EPWM4B | 0, 4, 8, 12 1 | D13 | – | – | I/O O | General-purpose input/output 152 Enhanced PWM4 output B (HRPWM-capable) |
| GPIO153 EPWM5A | 0, 4, 8, 12 1 | A12 | – | – | I/O O | General-purpose input/output 153 Enhanced PWM5 output A (HRPWM-capable) |
| GPIO154 EPWM5B | 0, 4, 8, 12 1 | B12 | – | – | I/O O | General-purpose input/output 154 Enhanced PWM5 output B (HRPWM-capable) |
| GPIO155 EPWM6A | 0, 4, 8, 12 1 | C12 | – | – | I/O O | General-purpose input/output 155 Enhanced PWM6 output A (HRPWM-capable) |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-------------------------|------------------|--------------|-------------|-------------|----------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| GPIO156 EPWM6B | 0, 4, 8, 12 1 | D12 | – | – | I/O O | General-purpose input/output 156 Enhanced PWM6 output B (HRPWM-capable) |
| GPIO157 EPWM7A | 0, 4, 8, 12 1 | B10 | – | – | I/O O | General-purpose input/output 157 Enhanced PWM7 output A (HRPWM-capable) |
| GPIO158 EPWM7B | 0, 4, 8, 12 1 | C10 | – | – | I/O O | General-purpose input/output 158 Enhanced PWM7 output B (HRPWM-capable) |
| GPIO159 EPWM8A | 0, 4, 8, 12 1 | D10 | – | – | I/O O | General-purpose input/output 159 Enhanced PWM8 output A (HRPWM-capable) |
| GPIO160 EPWM8B | 0, 4, 8, 12 1 | B9 | – | – | I/O O | General-purpose input/output 160 Enhanced PWM8 output B (HRPWM-capable) |
| GPIO161 EPWM9A | 0, 4, 8, 12 1 | C9 | – | – | I/O O | General-purpose input/output 161 Enhanced PWM9 output A |
| GPIO162 EPWM9B | 0, 4, 8, 12 1 | D9 | – | – | I/O O | General-purpose input/output 162 Enhanced PWM9 output B |
| GPIO163 EPWM10A | 0, 4, 8, 12 1 | A8 | – | – | I/O O | General-purpose input/output 163 Enhanced PWM10 output A |
| GPIO164 EPWM10B | 0, 4, 8, 12 1 | B8 | – | – | I/O O | General-purpose input/output 164 Enhanced PWM10 output B |
| GPIO165 EPWM11A | 0, 4, 8, 12 1 | C5 | – | – | I/O O | General-purpose input/output 165 Enhanced PWM11 output A |
| GPIO166 EPWM11B | 0, 4, 8, 12 1 | D5 | – | – | I/O O | General-purpose input/output 166 Enhanced PWM11 output B |
| GPIO167 EPWM12A | 0, 4, 8, 12 1 | C4 | – | – | I/O O | General-purpose input/output 167 Enhanced PWM12 output A |
| GPIO168 EPWM12B | 0, 4, 8, 12 1 | D4 | – | – | I/O O | General-purpose input/output 168 Enhanced PWM12 output B |
| RESET | | | | | | |
| $\overline{\text{XRS}}$ | | F19 | 124 | 69 | I/OD | Device Reset (in) and Watchdog Reset (out). The devices have a built-in power-on reset (POR) circuit. During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset or NMI watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor with a value from 2.2 k Ω to 10 k Ω should be placed between $\overline{\text{XRS}}$ and V _{DDIO} . If a capacitor is placed between $\overline{\text{XRS}}$ and V _{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V _{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open drain with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|---|--------------|--------------|-------------|-------------|----------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| CLOCKS | | | | | | |
| X1 | | G19 | 123 | 68 | I | On-chip crystal-oscillator input. To use this oscillator, a quartz crystal must be connected across X1 and X2. If this pin is not used, it must be tied to GND. This pin can also be used to feed a single-ended 3.3-V level clock. In this case, X2 is a No Connect (NC). |
| X2 | | J19 | 121 | 66 | O | On-chip crystal-oscillator output. A quartz crystal may be connected across X1 and X2. If X2 is not used, it must be left unconnected. |
| NO CONNECT | | | | | | |
| NC | | H4 | – | – | | No connect. BGA ball is electrically open and not connected to the die. |
| JTAG | | | | | | |
| TCK | | V15 | 81 | 50 | I | JTAG test clock with internal pullup (see Section 5.6) |
| TDI | | W13 | 77 | 46 | I | JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. |
| TDO | | W15 | 78 | 47 | O/Z | JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. ⁽³⁾ |
| TMS | | W14 | 80 | 49 | I | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. |
| $\overline{\text{TRST}}$ | | V14 | 79 | 48 | I | JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-k Ω or smaller resistor generally offers adequate protection. The value of the resistor is application-specific. TI recommends that each target board be validated for proper operation of the debugger and the application. This pin has an internal 50-ns (nominal) glitch filter. |
| INTERNAL VOLTAGE REGULATOR CONTROL | | | | | | |
| VREGENZ | | J18 | 119 | 64 | I | Internal voltage regulator enable with internal pulldown. The internal VREG is not supported and must be disabled. Connect VREGENZ to V _{DDIO} . |

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|---------------------------------------|--------------|--------------|-------------|-------------|----------------------|--|
| NAME | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| ANALOG, DIGITAL, AND I/O POWER | | | | | | |
| V _{DD} | | E9 | 16 | 16 | | 1.2-V digital logic power pins. TI recommends placing a decoupling capacitor near each V _{DD} pin with a minimum total capacitance of approximately 20 uF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution. |
| | | E11 | 21 | 39 | | |
| | | F9 | 61 | 45 | | |
| | | F11 | 76 | 63 | | |
| | | G14 | 117 | 71 | | |
| | | G15 | 126 | 78 | | |
| | | J14 | 137 | 84 | | |
| | | J15 | 153 | 89 | | |
| | | K5 | 158 | 95 | | |
| | | K6 | 169 | – | | |
| | | P10 | – | – | | |
| | | P13 | – | – | | |
| | | R10 | – | – | | |
| | R13 | – | – | | | |
| V _{DD3VFL} | | R11 | 72 | 41 | | 3.3-V Flash power pin. Place a minimum 0.1-μF decoupling capacitor on each pin. |
| | | R12 | – | – | | |
| V _{DDA} | | P6 | 36 | 18 | | 3.3-V analog power pins. Place a minimum 2.2-μF decoupling capacitor to V _{SSA} on each pin. |
| | | R6 | 54 | 38 | | |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|--------------------|--------------|--------------|-------------|-------------|----------------------|---|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| V _{DDIO} | | A9 | 3 | 2 | | 3.3-V digital I/O power pins. Place a minimum 0.1- μ F decoupling capacitor on each pin. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution. |
| | | A18 | 11 | 10 | | |
| | | B1 | 15 | 15 | | |
| | | E7 | 20 | 40 | | |
| | | E10 | 26 | 44 | | |
| | | E13 | 62 | 55 | | |
| | | E16 | 68 | 62 | | |
| | | F4 | 75 | 72 | | |
| | | F7 | 82 | 79 | | |
| | | F10 | 88 | 83 | | |
| | | F13 | 91 | 90 | | |
| | | F16 | 99 | 94 | | |
| | | G4 | 106 | – | | |
| | | G5 | 114 | – | | |
| | | G6 | 116 | – | | |
| | | H5 | 127 | – | | |
| | | H6 | 138 | – | | |
| | | L14 | 147 | – | | |
| | | L15 | 152 | – | | |
| | | M1 | 159 | – | | |
| | | M5 | 168 | – | | |
| | M6 | – | – | | | |
| | N14 | – | – | | | |
| | N15 | – | – | | | |
| | P9 | – | – | | | |
| | R9 | – | – | | | |
| | V19 | – | – | | | |
| | W8 | – | – | | | |
| V _{DDOSC} | | H16 | 120 | 65 | | Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1- μ F (minimum) decoupling capacitor on each pin. |
| | | H17 | 125 | 70 | | |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|-----------------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| V _{SS} | | A1 | PWR PAD | PWR PAD | | Device ground. For Quad Flatpacks (QFPs), the PowerPAD on the bottom of the package must be soldered to the ground plane of the PCB. |
| | | A10 | | | | |
| | | A19 | | | | |
| | | E5 | | | | |
| | | E6 | | | | |
| | | E8 | | | | |
| | | E12 | | | | |
| | | E14 | | | | |
| | | E15 | | | | |
| | | F5 | | | | |
| | | F6 | | | | |
| | | F8 | | | | |
| | | F12 | | | | |
| | | F14 | | | | |
| | | F15 | | | | |
| | | G16 | | | | |
| | | G17 | | | | |
| | | H8 | | | | |
| | | H9 | | | | |
| | | H10 | | | | |
| | | H11 | | | | |
| | | H12 | | | | |
| | | H14 | | | | |
| | | H15 | | | | |
| | | J5 | | | | |
| | | J6 | | | | |
| | | J8 | | | | |
| | | J9 | | | | |
| | | J10 | | | | |
| | | J11 | | | | |
| | J12 | | | | | |
| | K8 | | | | | |
| | K9 | | | | | |
| | K10 | | | | | |
| | K11 | | | | | |
| | K12 | | | | | |
| | K14 | | | | | |
| | K15 | | | | | |
| | L5 | | | | | |
| | L6 | | | | | |
| | L8 | | | | | |
| | L9 | | | | | |

Table 4-1. Signal Descriptions (continued)

| NAME | TERMINAL | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|--------------------|--------------|--------------|-------------|-------------|----------------------|--|
| | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| V _{SS} | | L10 | PWR PAD | PWR PAD | | Device ground. For Quad Flatpacks (QFPs), the PowerPAD on the bottom of the package must be soldered to the ground plane of the PCB. |
| | | L11 | | | | |
| | | L12 | | | | |
| | | L18 | | | | |
| | | M8 | | | | |
| | | M9 | | | | |
| | | M10 | | | | |
| | | M11 | | | | |
| | | M12 | | | | |
| | | M14 | | | | |
| | | M15 | | | | |
| | | N1 | | | | |
| | | N5 | | | | |
| | | N6 | | | | |
| | | P7 | | | | |
| | | P8 | | | | |
| | | P11 | | | | |
| | | P12 | | | | |
| | | P14 | | | | |
| | P15 | | | | | |
| | R7 | | | | | |
| | R8 | | | | | |
| | R14 | | | | | |
| | R15 | | | | | |
| | W7 | | | | | |
| | W19 | | | | | |
| V _{SSOSC} | | H18 | 122 | 67 | | Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground. |
| | | H19 | – | – | | |
| V _{SSA} | | P1 | 34 | 17 | | Analog ground. On the PZP package, pin 17 is double-bonded to V _{SSA} and V _{REFLOA} . This pin must be connect to V _{SSA} . |
| | | P5 | 52 | 35 | | |
| | | R5 | – | 36 | | |
| | | V7 | – | – | | |
| | | W1 | – | – | | |

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | | | | I/O/Z ⁽¹⁾ | DESCRIPTION |
|--------------------------|--------------|--------------|-------------|-------------|----------------------|--|
| NAME | MUX POSITION | ZWT BALL NO. | PTP PIN NO. | PZP PIN NO. | | |
| SPECIAL FUNCTIONS | | | | | | |
| ERRORSTS | | U19 | 92 | – | O | Error status output. This pin has an internal pulldown. |
| TEST PINS | | | | | | |
| FLT1 | | W12 | 73 | 42 | I/O | Flash test pin 1. Reserved for TI. Must be left unconnected. |
| FLT2 | | V13 | 74 | 43 | I/O | Flash test pin 2. Reserved for TI. Must be left unconnected. |

(1) I = Input, O = Output, OD = Open Drain, Z = High Impedance

(2) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

(3) This pin has output impedance that can be as low as 22 Ω. This output could have fast edges and ringing depending on the system PCB characteristics. If this is a concern, the user should take precautions such as adding a 39Ω (10% tolerance) series termination resistor or implement some other termination scheme. It is also recommended that a system-level signal integrity analysis be performed with the provided IBIS models. The termination is not required if this pin is used for input function.

4.3 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. [Table 4-2](#) lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. In order to avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in [Table 4-2](#) with pullups and pulldowns are always on and cannot be disabled.

Table 4-2. Pins With Internal Pullup and Pulldown

| PIN | RESET (XRS = 0) | DEVICE BOOT | APPLICATION SOFTWARE |
|------------|-----------------|--------------------------------|--------------------------------------|
| GPIOx | Pullup disabled | Pullup disabled ⁽¹⁾ | Pullup enable is application-defined |
| TRST | | Pulldown active | |
| TCK | | Pullup active | |
| TMS | | Pullup active | |
| TDI | | Pullup active | |
| XRS | | Pullup active | |
| VREGENZ | | Pulldown active | |
| ERRORSTS | | Pulldown active | |
| Other pins | | No pullup or pulldown present | |

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

4.4 Pin Multiplexing

4.4.1 GPIO Muxed Pins

Table 4-3 shows the GPIO muxed pins. The default for each pin is the GPIO function, secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured prior to the GPyMUXn to avoid transient pulses on GPIO's from alternate mux selections. Columns not shown and blank cells are reserved GPIO Mux settings.

Table 4-3. GPIO Muxed Pins⁽¹⁾⁽²⁾

| GPIO Index | GPIO Mux Selection | | | | | | | |
|---------------------|---|-----------------|-----|-----------------|-----------------|-----------------|------------|-----------------|
| | 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 15 |
| | GPyGMUXn. GPIOz = 00b, 01b, 10b, 11b | 00b | | | 01b | | | 11b |
| GPyMUXn. GPIOz = | 00b | 01b | 10b | 11b | 01b | 10b | 11b | 11b |
| GPIO0 | EPWM1A (O) | | | | | SDAA (I/OD) | | |
| GPIO1 | EPWM1B (O) | | | MFSRB (I/O) | | SCLA (I/OD) | | |
| GPIO2 | EPWM2A (O) | | | | OUTPUTXBAR1 (O) | SDAB (I/OD) | | |
| GPIO3 | EPWM2B (O) | OUTPUTXBAR2 (O) | | MCLKRB (I/O) | OUTPUTXBAR2 (O) | SCLB (I/OD) | | |
| GPIO4 | EPWM3A (O) | | | | OUTPUTXBAR3 (O) | CANTXA (O) | | |
| GPIO5 | EPWM3B (O) | MFSRA (I/O) | | OUTPUTXBAR3 (O) | | CANRXA (I) | | |
| GPIO6 | EPWM4A (O) | OUTPUTXBAR4 (O) | | EXTSYNCOOUT (O) | EQEP3A (I) | CANTXB (O) | | |
| GPIO7 | EPWM4B (O) | MCLKRA (I/O) | | OUTPUTXBAR5 (O) | EQEP3B (I) | CANRXB (I) | | |
| GPIO8 | EPWM5A (O) | CANTXB (O) | | ADCSOCAO (O) | EQEP3S (I/O) | SCITXDA (O) | | |
| GPIO9 | EPWM5B (O) | SCITXDB (O) | | OUTPUTXBAR6 (O) | EQEP3I (I/O) | SCIRXDA (I) | | |
| GPIO10 | EPWM6A (O) | CANRXB (I) | | ADCSOCBO (O) | EQEP1A (I) | SCITXDB (O) | | UPP-WAIT (I/O) |
| GPIO11 | EPWM6B (O) | SCIRXDB (I) | | OUTPUTXBAR7 (O) | EQEP1B (I) | SCIRXDB (I) | | UPP-START (I/O) |
| GPIO12 | EPWM7A (O) | CANTXB (O) | | MDXB (O) | EQEP1S (I/O) | SCITXDC (O) | | UPP-ENA (I/O) |
| GPIO13 | EPWM7B (O) | CANRXB (I) | | MDRB (I) | EQEP1I (I/O) | SCIRXDC (I) | | UPP-D7 (I/O) |
| GPIO14 | EPWM8A (O) | SCITXDB (O) | | MCLKXB (I/O) | | OUTPUTXBAR3 (O) | | UPP-D6 (I/O) |
| GPIO15 | EPWM8B (O) | SCIRXDB (I) | | MFSXB (I/O) | | OUTPUTXBAR4 (O) | | UPP-D5 (I/O) |
| GPIO16 | SPISIMOA (I/O) | CANTXB (O) | | OUTPUTXBAR7 (O) | EPWM9A (O) | | SD1_D1 (I) | UPP-D4 (I/O) |
| GPIO17 | SPISOMIA (I/O) | CANRXB (I) | | OUTPUTXBAR8 (O) | EPWM9B (O) | | SD1_C1 (I) | UPP-D3 (I/O) |
| GPIO18 | SPICLKA (I/O) | SCITXDB (O) | | CANRXA (I) | EPWM10A (O) | | SD1_D2 (I) | UPP-D2 (I/O) |
| GPIO19 | SPISTEA (I/O) | SCIRXDB (I) | | CANTXA (O) | EPWM10B (O) | | SD1_C2 (I) | UPP-D1 (I/O) |
| GPIO20 | EQEP1A (I) | MDXA (O) | | CANTXB (O) | EPWM11A (O) | | SD1_D3 (I) | UPP-D0 (I/O) |
| GPIO21 | EQEP1B (I) | MDRA (I) | | CANRXB (I) | EPWM11B (O) | | SD1_C3 (I) | UPP-CLK (I/O) |
| GPIO22 | EQEP1S (I/O) | MCLKXA (I/O) | | SCITXDB (O) | EPWM12A (O) | SPICLKB (I/O) | SD1_D4 (I) | |
| GPIO23 | EQEP1I (I/O) | MFSXA (I/O) | | SCIRXDB (I) | EPWM12B (O) | SPISTEB (I/O) | SD1_C4 (I) | |
| GPIO24 | OUTPUTXBAR1 (O) | EQEP2A (I) | | MDXB (O) | | SPISIMOB (I/O) | SD2_D1 (I) | |
| GPIO25 | OUTPUTXBAR2 (O) | EQEP2B (I) | | MDRB (I) | | SPISOMIB (I/O) | SD2_C1 (I) | |
| GPIO26 | OUTPUTXBAR3 (O) | EQEP2I (I/O) | | MCLKXB (I/O) | OUTPUTXBAR3 (O) | SPICLKB (I/O) | SD2_D2 (I) | |
| GPIO27 | OUTPUTXBAR4 (O) | EQEP2S (I/O) | | MFSXB (I/O) | OUTPUTXBAR4 (O) | SPISTEB (I/O) | SD2_C2 (I) | |
| GPIO28 | SCIRXDA (I) | EM1CS4 (O) | | | OUTPUTXBAR5 (O) | EQEP3A (I) | SD2_D3 (I) | |
| GPIO29 | SCITXDA (O) | EM1SDCKE (O) | | | OUTPUTXBAR6 (O) | EQEP3B (I) | SD2_C3 (I) | |
| GPIO30 | CANRXA (I) | EM1CLK (O) | | | OUTPUTXBAR7 (O) | EQEP3S (I/O) | SD2_D4 (I) | |
| GPIO31 | CANTXA (O) | EM1WE (O) | | | OUTPUTXBAR8 (O) | EQEP3I (I/O) | SD2_C4 (I) | |
| GPIO32 | SDAA (I/OD) | EM1CS0 (O) | | | | | | |
| GPIO33 | SCLA (I/OD) | EM1RNW (O) | | | | | | |
| GPIO34 | OUTPUTXBAR1 (O) | EM1CS2 (O) | | | | SDAB (I/OD) | | |
| GPIO35 | SCIRXDA (I) | EM1CS3 (O) | | | | SCLB (I/OD) | | |
| GPIO36 | SCITXDA (O) | EM1WAIT (I) | | | | CANRXA (I) | | |
| GPIO37 | OUTPUTXBAR2 (O) | EM1OE (O) | | | | CANTXA (O) | | |
| GPIO38 | | EM1A0 (O) | | | SCITXDC (O) | CANTXB (O) | | |
| GPIO39 | | EM1A1 (O) | | | SCIRXDC (I) | CANRXB (I) | | |

(1) I = Input, O = Output, OD = Open Drain

(2) GPIO Index settings of 9, 10, 11, 13, and 14 are reserved.

Table 4-3. GPIO Muxed Pins⁽¹⁾⁽²⁾ (continued)

| GPIO Index | GPIO Mux Selection | | | | | | | |
|----------------------|-----------------------|-----|--------------|--------------|-----------------|----------------|------------|-------------------------------|
| | 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 15 |
| GPyGMUXn. GPIOz = | 00b, 01b, 10b, 11b | 00b | | | 01b | | | 11b |
| GPyMUXn. GPIOz = | 00b | 01b | 10b | 11b | 01b | 10b | 11b | 11b |
| GPIO40 | | | EM1A2 (O) | | | SDAB (I/OD) | | |
| GPIO41 | | | EM1A3 (O) | | | SCLB (I/OD) | | |
| GPIO42 | | | | | | SDAA (I/OD) | | SCITXDA (O) |
| GPIO43 | | | | | | SCLA (I/OD) | | SCIRXDA (I) |
| GPIO44 | | | EM1A4 (O) | | | | | |
| GPIO45 | | | EM1A5 (O) | | | | | |
| GPIO46 | | | EM1A6 (O) | | | SCIRXDD (I) | | |
| GPIO47 | | | EM1A7 (O) | | | SCITXDD (O) | | |
| GPIO48 | OUTPUTXBAR3 (O) | | EM1A8 (O) | | | SCITXDA (O) | SD1_D1 (I) | |
| GPIO49 | OUTPUTXBAR4 (O) | | EM1A9 (O) | | | SCIRXDA (I) | SD1_C1 (I) | |
| GPIO50 | EQEP1A (I) | | EM1A10 (O) | | | SPISIMOC (I/O) | SD1_D2 (I) | |
| GPIO51 | EQEP1B (I) | | EM1A11 (O) | | | SPISOMIC (I/O) | SD1_C2 (I) | |
| GPIO52 | EQEP1S (I/O) | | EM1A12 (O) | | | SPICLK (I/O) | SD1_D3 (I) | |
| GPIO53 | EQEP1I (I/O) | | EM1D31 (I/O) | EM2D15 (I/O) | | SPISTEC (I/O) | SD1_C3 (I) | |
| GPIO54 | SPISIMOA (I/O) | | EM1D30 (I/O) | EM2D14 (I/O) | EQEP2A (I) | SCITXDB (O) | SD1_D4 (I) | |
| GPIO55 | SPISOMIA (I/O) | | EM1D29 (I/O) | EM2D13 (I/O) | EQEP2B (I) | SCIRXDB (I) | SD1_C4 (I) | |
| GPIO56 | SPICLKA (I/O) | | EM1D28 (I/O) | EM2D12 (I/O) | EQEP2S (I/O) | SCITXDC (O) | SD2_D1 (I) | |
| GPIO57 | SPISTEA (I/O) | | EM1D27 (I/O) | EM2D11 (I/O) | EQEP2I (I/O) | SCIRXDC (I) | SD2_C1 (I) | |
| GPIO58 | MCLKRA (I/O) | | EM1D26 (I/O) | EM2D10 (I/O) | OUTPUTXBAR1 (O) | SPICLKB (I/O) | SD2_D2 (I) | SPISIMOA ⁽³⁾ (I/O) |
| GPIO59 | MFSRA (I/O) | | EM1D25 (I/O) | EM2D9 (I/O) | OUTPUTXBAR2 (O) | SPISTEB (I/O) | SD2_C2 (I) | SPISOMIA ⁽³⁾ (I/O) |
| GPIO60 | MCLKRB (I/O) | | EM1D24 (I/O) | EM2D8 (I/O) | OUTPUTXBAR3 (O) | SPISIMOB (I/O) | SD2_D3 (I) | SPICLKA ⁽³⁾ (I/O) |
| GPIO61 | MFSRB (I/O) | | EM1D23 (I/O) | EM2D7 (I/O) | OUTPUTXBAR4 (O) | SPISOMIB (I/O) | SD2_C3 (I) | SPISTEA ⁽³⁾ (I/O) |
| GPIO62 | SCIRXDC (I) | | EM1D22 (I/O) | EM2D6 (I/O) | EQEP3A (I) | CANRXA (I) | SD2_D4 (I) | |
| GPIO63 | SCITXDC (O) | | EM1D21 (I/O) | EM2D5 (I/O) | EQEP3B (I) | CANTXA (O) | SD2_C4 (I) | SPISIMOB ⁽³⁾ (I/O) |
| GPIO64 | | | EM1D20 (I/O) | EM2D4 (I/O) | EQEP3S (I/O) | SCIRXDA (I) | | SPISOMIB ⁽³⁾ (I/O) |
| GPIO65 | | | EM1D19 (I/O) | EM2D3 (I/O) | EQEP3I (I/O) | SCITXDA (O) | | SPICLKB ⁽³⁾ (I/O) |
| GPIO66 | | | EM1D18 (I/O) | EM2D2 (I/O) | | SDAB (I/OD) | | SPISTEB ⁽³⁾ (I/O) |
| GPIO67 | | | EM1D17 (I/O) | EM2D1 (I/O) | | | | |
| GPIO68 | | | EM1D16 (I/O) | EM2D0 (I/O) | | | | |
| GPIO69 | | | EM1D15 (I/O) | | | SCLB (I/OD) | | SPISIMOC ⁽³⁾ (I/O) |
| GPIO70 | | | EM1D14 (I/O) | | CANRXA (I) | SCITXDB (O) | | SPISOMIC ⁽³⁾ (I/O) |
| GPIO71 | | | EM1D13 (I/O) | | CANTXA (O) | SCIRXDB (I) | | SPICLK ⁽³⁾ (I/O) |
| GPIO72 | | | EM1D12 (I/O) | | CANTXB (O) | SCITXDC (O) | | SPISTEC ⁽³⁾ (I/O) |
| GPIO73 | | | EM1D11 (I/O) | XCLKOUT (O) | CANRXB (I) | SCIRXDC (I) | | |
| GPIO74 | | | EM1D10 (I/O) | | | | | |
| GPIO75 | | | EM1D9 (I/O) | | | | | |
| GPIO76 | | | EM1D8 (I/O) | | | SCITXDD (O) | | |
| GPIO77 | | | EM1D7 (I/O) | | | SCIRXDD (I) | | |
| GPIO78 | | | EM1D6 (I/O) | | | EQEP2A (I) | | |
| GPIO79 | | | EM1D5 (I/O) | | | EQEP2B (I) | | |
| GPIO80 | | | EM1D4 (I/O) | | | EQEP2S (I/O) | | |
| GPIO81 | | | EM1D3 (I/O) | | | EQEP2I (I/O) | | |
| GPIO82 | | | EM1D2 (I/O) | | | | | |
| GPIO83 | | | EM1D1 (I/O) | | | | | |
| GPIO84 | | | | | SCITXDA (O) | MDXB (O) | | MDXA (O) |
| GPIO85 | | | EM1D0 (I/O) | | SCIRXDA (I) | MDRB (I) | | MDRA (I) |
| GPIO86 | | | EM1A13 (O) | EM1CAS (O) | SCITXDB (O) | MCLKXB (I/O) | | MCLKXA (I/O) |
| GPIO87 | | | EM1A14 (O) | EM1RAS (O) | SCIRXDB (I) | MFSXB (I/O) | | MFSXA (I/O) |
| GPIO88 | | | EM1A15 (O) | EM1DQM0 (O) | | | | |
| GPIO89 | | | EM1A16 (O) | EM1DQM1 (O) | | SCITXDC (O) | | |

(3) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

Table 4-3. GPIO Muxed Pins⁽¹⁾⁽²⁾ (continued)

| GPIO Index | GPIO Mux Selection | | | | | | | |
|----------------------|-----------------------|-----|------------|--------------|--------------|----------------|------------|----------|
| | 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 15 |
| GPyGMUXn. GPIOz = | 00b, 01b, 10b, 11b | 00b | | | 01b | | | 11b |
| GPyMUXn. GPIOz = | 00b | 01b | 10b | 11b | 01b | 10b | 11b | 11b |
| GPIO90 | | | EM1A17 (O) | EM1DQM2 (O) | | SCIRXDC (I) | | |
| GPIO91 | | | EM1A18 (O) | EM1DQM3 (O) | | SDAA (I/OD) | | |
| GPIO92 | | | EM1A19 (O) | EM1BA1 (O) | | SCLA (I/OD) | | |
| GPIO93 | | | | EM1BA0 (O) | | SCITXDD (O) | | |
| GPIO94 | | | | | | SCIRXDD (I) | | |
| GPIO95 | | | | | | | | |
| GPIO96 | | | | EM2DQM1 (O) | EQEP1A (I) | | | |
| GPIO97 | | | | EM2DQM0 (O) | EQEP1B (I) | | | |
| GPIO98 | | | | EM2A0 (O) | EQEP1S (I/O) | | | |
| GPIO99 | | | | EM2A1 (O) | EQEP1I (I/O) | | | |
| GPIO100 | | | | EM2A2 (O) | EQEP2A (I) | SPISIMOC (I/O) | | |
| GPIO101 | | | | EM2A3 (O) | EQEP2B (I) | SPISOMIC (I/O) | | |
| GPIO102 | | | | EM2A4 (O) | EQEP2S (I/O) | SPICLK (I/O) | | |
| GPIO103 | | | | EM2A5 (O) | EQEP2I (I/O) | SPISTEC (I/O) | | |
| GPIO104 | SDAA (I/OD) | | | EM2A6 (O) | EQEP3A (I) | SCITXDD (O) | | |
| GPIO105 | SCLA (I/OD) | | | EM2A7 (O) | EQEP3B (I) | SCIRXDD (I) | | |
| GPIO106 | | | | EM2A8 (O) | EQEP3S (I/O) | SCITXDC (O) | | |
| GPIO107 | | | | EM2A9 (O) | EQEP3I (I/O) | SCIRXDC (I) | | |
| GPIO108 | | | | EM2A10 (O) | | | | |
| GPIO109 | | | | EM2A11 (O) | | | | |
| GPIO110 | | | | EM2WAIT (I) | | | | |
| GPIO111 | | | | EM2BA0 (O) | | | | |
| GPIO112 | | | | EM2BA1 (O) | | | | |
| GPIO113 | | | | EM2CAS (O) | | | | |
| GPIO114 | | | | EM2RAS (O) | | | | |
| GPIO115 | | | | EM2CS0 (O) | | | | |
| GPIO116 | | | | EM2CS2 (O) | | | | |
| GPIO117 | | | | EM2SDCKE (O) | | | | |
| GPIO118 | | | | EM2CLK (O) | | | | |
| GPIO119 | | | | EM2RNW (O) | | | | |
| GPIO120 | | | | EM2WE (O) | | | | USB0PFLT |
| GPIO121 | | | | EM2OE (O) | | | | USB0EPEN |
| GPIO122 | | | | | | SPISIMOC (I/O) | SD1_D1 (I) | |
| GPIO123 | | | | | | SPISOMIC (I/O) | SD1_C1 (I) | |
| GPIO124 | | | | | | SPICLK (I/O) | SD1_D2 (I) | |
| GPIO125 | | | | | | SPISTEC (I/O) | SD1_C2 (I) | |
| GPIO126 | | | | | | | SD1_D3 (I) | |
| GPIO127 | | | | | | | SD1_C3 (I) | |
| GPIO128 | | | | | | | SD1_D4 (I) | |
| GPIO129 | | | | | | | SD1_C4 (I) | |
| GPIO130 | | | | | | | SD2_D1 (I) | |
| GPIO131 | | | | | | | SD2_C1 (I) | |
| GPIO132 | | | | | | | SD2_D2 (I) | |
| GPIO133/ AUXCLKIN | | | | | | | SD2_C2 (I) | |
| GPIO134 | | | | | | | SD2_D3 (I) | |
| GPIO135 | | | | | | SCITXDA (O) | SD2_C3 (I) | |
| GPIO136 | | | | | | SCIRXDA (I) | SD2_D4 (I) | |
| GPIO137 | | | | | | SCITXDB (O) | SD2_C4 (I) | |
| GPIO138 | | | | | | SCIRXDB (I) | | |
| GPIO139 | | | | | | SCIRXDC (I) | | |
| GPIO140 | | | | | | SCITXDC (O) | | |

Table 4-3. GPIO Muxed Pins⁽¹⁾⁽²⁾ (continued)

| GPIO Index | GPIO Mux Selection | | | | | | | |
|----------------------|-----------------------|-------------|-----|-----|-----|-------------|-----|-----|
| | 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 15 |
| GPyGMUXn. GPIOz = | 00b, 01b, 10b, 11b | 00b | | | 01b | | | 11b |
| GPyMUXn. GPIOz = | 00b | 01b | 10b | 11b | 01b | 10b | 11b | 11b |
| | GPIO141 | | | | | SCIRXDD (I) | | |
| | GPIO142 | | | | | SCITXDD (O) | | |
| | GPIO143 | | | | | | | |
| | GPIO144 | | | | | | | |
| | GPIO145 | EPWM1A (O) | | | | | | |
| | GPIO146 | EPWM1B (O) | | | | | | |
| | GPIO147 | EPWM2A (O) | | | | | | |
| | GPIO148 | EPWM2B (O) | | | | | | |
| | GPIO149 | EPWM3A (O) | | | | | | |
| | GPIO150 | EPWM3B (O) | | | | | | |
| | GPIO151 | EPWM4A (O) | | | | | | |
| | GPIO152 | EPWM4B (O) | | | | | | |
| | GPIO153 | EPWM5A (O) | | | | | | |
| | GPIO154 | EPWM5B (O) | | | | | | |
| | GPIO155 | EPWM6A (O) | | | | | | |
| | GPIO156 | EPWM6B (O) | | | | | | |
| | GPIO157 | EPWM7A (O) | | | | | | |
| | GPIO158 | EPWM7B (O) | | | | | | |
| | GPIO159 | EPWM8A (O) | | | | | | |
| | GPIO160 | EPWM8B (O) | | | | | | |
| | GPIO161 | EPWM9A (O) | | | | | | |
| | GPIO162 | EPWM9B (O) | | | | | | |
| | GPIO163 | EPWM10A (O) | | | | | | |
| | GPIO164 | EPWM10B (O) | | | | | | |
| | GPIO165 | EPWM11A (O) | | | | | | |
| | GPIO166 | EPWM11B (O) | | | | | | |
| | GPIO167 | EPWM12A (O) | | | | | | |
| | GPIO168 | EPWM12B (O) | | | | | | |

4.4.2 Input X-BAR

The Input X-BAR is used to route any GPIO input to the ADC, eCAP, and ePWM peripherals as well as to external interrupts (XINT) (see Figure 4-7). Table 4-4 shows the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual*.

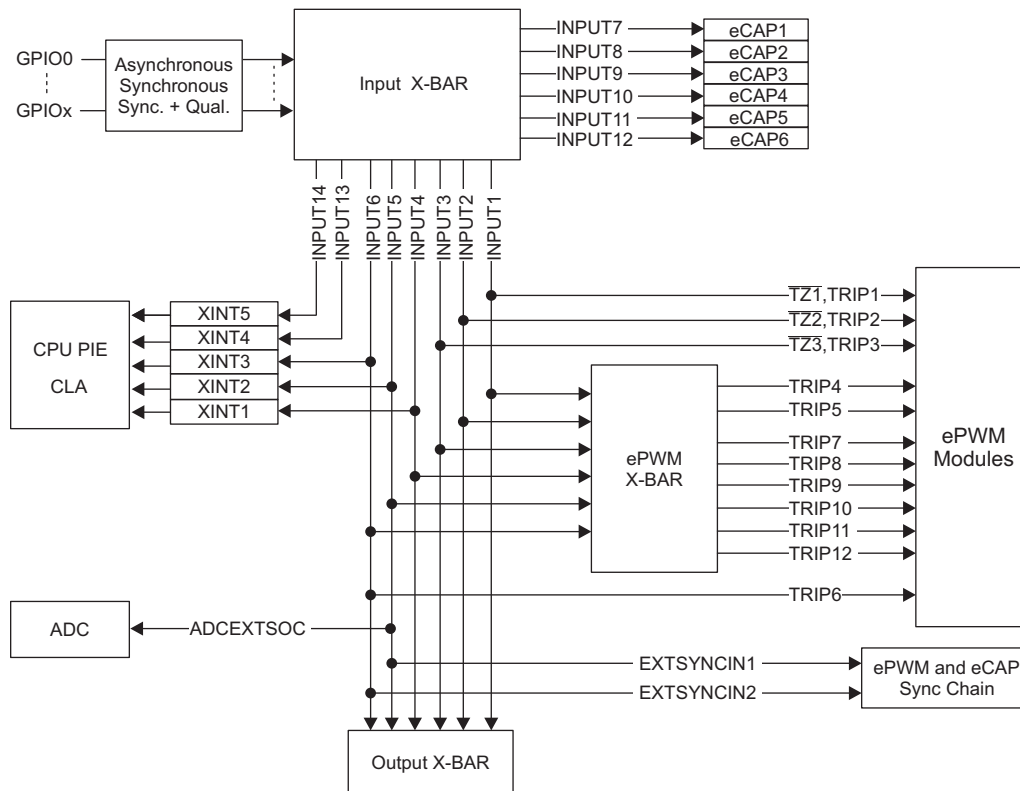


Figure 4-7. Input X-BAR

Table 4-4. Input X-BAR Destinations

| INPUT | DESTINATIONS |
|---------|--|
| INPUT1 | EPWM[TZ1,TRIP1], EPWM X-BAR, Output X-BAR |
| INPUT2 | EPWM[TZ2,TRIP2], EPWM X-BAR, Output X-BAR |
| INPUT3 | EPWM[TZ3,TRIP3], EPWM X-BAR, Output X-BAR |
| INPUT4 | XINT1, EPWM X-BAR, Output X-BAR |
| INPUT5 | XINT2, ADCEXTSOC, EXTSYNCIN1, EPWM X-BAR, Output X-BAR |
| INPUT6 | XINT3, EPWM[TRIP6], EXTSYNCIN2, EPWM X-BAR, Output X-BAR |
| INPUT7 | ECAP1 |
| INPUT8 | ECAP2 |
| INPUT9 | ECAP3 |
| INPUT10 | ECAP4 |
| INPUT11 | ECAP5 |
| INPUT12 | ECAP6 |
| INPUT13 | XINT4 |
| INPUT14 | XINT5 |

4.4.3 Output X-BAR and ePWM X-BAR

The Output X-BAR has eight outputs which can be selected on the GPIO mux as OUTPUTXBARx. The ePWM X-BAR has eight outputs which are connected to the TRIPx inputs of the ePWM. The sources for both the Output X-BAR and ePWM X-BAR are shown in Figure 4-8. For details on the Output X-BAR and ePWM X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual*.

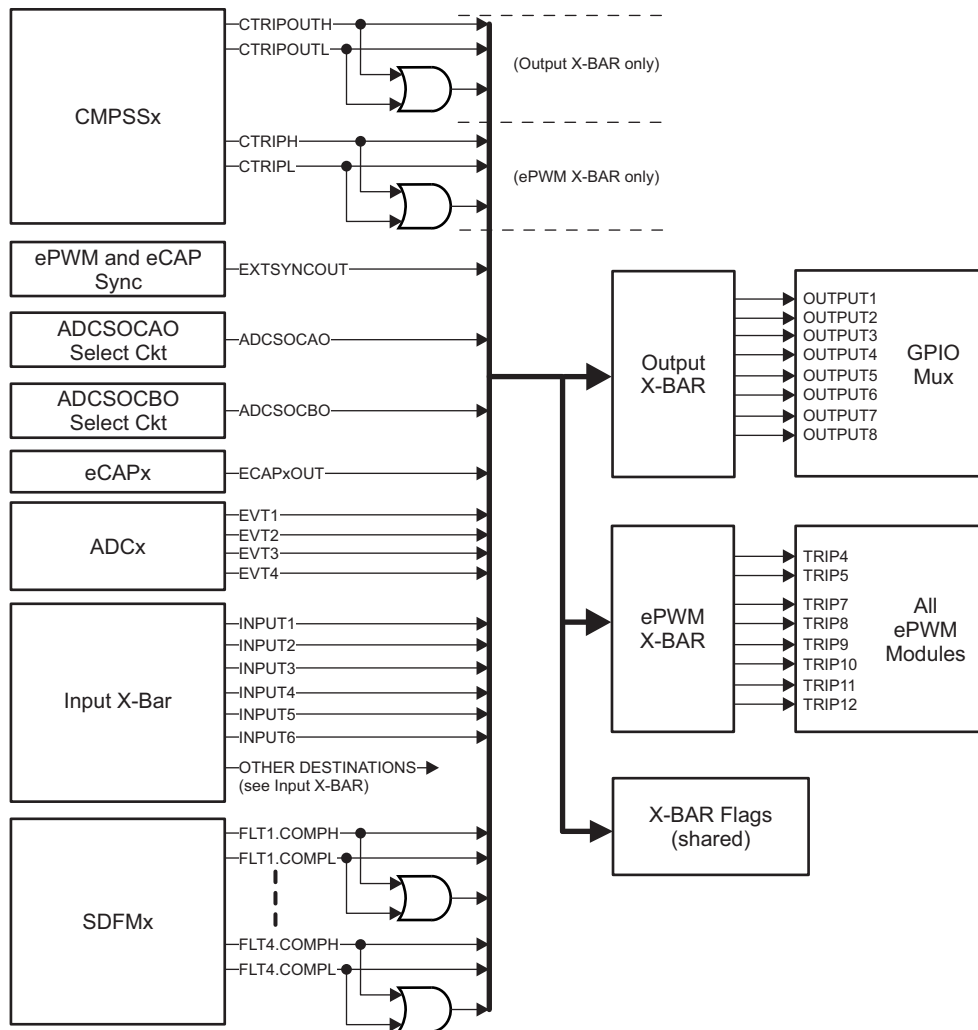


Figure 4-8. Output X-BAR and ePWM X-BAR

4.4.4 USB Pin Muxing

Table 4-5 shows assignment of the alternate USB function mapping. These can be configured with the GPBAMSEL register.

Table 4-5. Alternate USB Function

| GPIO | GPBAMSEL SETTING | USB FUNCTION |
|--------|-------------------|--------------|
| GPIO42 | GPBAMSEL[10] = 1b | USB0DM |
| GPIO43 | GPBAMSEL[11] = 1b | USB0DP |

4.4.5 High-Speed SPI Pin Muxing

The SPI module on this device has a high-speed mode. To achieve the highest possible speed, a special GPIO configuration is used on a single GPIO mux option for each SPI. These GPIOs may also be used by the SPI when not in high-speed mode (HS_MODE = 0).

To select the mux options that enable the SPI high-speed mode, configure the GPyGMUX and GPyMUX registers as shown in Table 4-6.

Table 4-6. GPIO Configuration for High-Speed SPI

| GPIO | SPI SIGNAL | MUX CONFIGURATION | |
|-------------|----------------|---------------------|--------------------|
| SPIA | | | |
| GPIO58 | SPISIMOA | GPBGMUX2[21:20]=11b | GPBMUX2[21:20]=11b |
| GPIO59 | SPISOMIA | GPBGMUX2[23:22]=11b | GPBMUX2[23:22]=11b |
| GPIO60 | SPICLKA | GPBGMUX2[25:24]=11b | GPBMUX2[25:24]=11b |
| GPIO61 | <u>SPISTEA</u> | GPBGMUX2[27:26]=11b | GPBMUX2[27:26]=11b |
| SPIB | | | |
| GPIO63 | SPISIMOB | GPBGMUX2[31:30]=11b | GPBMUX2[31:30]=11b |
| GPIO64 | SPISOMIB | GPCGMUX1[1:0]=11b | GPCMUX1[1:0]=11b |
| GPIO65 | SPICLKB | GPCGMUX1[3:2]=11b | GPCMUX1[3:2]=11b |
| GPIO66 | <u>SPISTEB</u> | GPCGMUX1[5:4]=11b | GPCMUX1[5:4]=11b |
| SPIC | | | |
| GPIO69 | SPISIMOC | GPCGMUX1[11:10]=11b | GPCMUX1[11:10]=11b |
| GPIO70 | SPISOMIC | GPCGMUX1[13:12]=11b | GPCMUX1[13:12]=11b |
| GPIO71 | SPICLKC | GPCGMUX1[15:14]=11b | GPCMUX1[15:14]=11b |
| GPIO72 | <u>SPISTEC</u> | GPCGMUX1[17:16]=11b | GPCMUX1[17:16]=11b |

4.5 Connections for Unused Pins

For applications that do not need to use all functions of the device, [Table 4-7](#) lists acceptable conditioning for any unused pins. When multiple options are listed in [Table 4-7](#), any are acceptable. Pins not listed in [Table 4-7](#) must be connected according to [Table 4-1](#).

Table 4-7. Connections for Unused Pins

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|--------------------------|---|
| Analog | |
| V _{REFHIX} | Tie to V _{DDA} |
| V _{REFLOX} | Tie to V _{SSA} |
| ADCIN _x | <ul style="list-style-type: none"> • No Connect • Tie to V_{SSA} |
| Digital | |
| GPIO _x | <ul style="list-style-type: none"> • No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled) |
| X1 | Tie to V _{SS} |
| X2 | No Connect |
| TCK | <ul style="list-style-type: none"> • No Connect • Pullup resistor |
| TDI | <ul style="list-style-type: none"> • No Connect • Pullup resistor |
| TDO | No Connect |
| TMS | No Connect |
| $\overline{\text{TRST}}$ | Pulldown resistor (2.2 kΩ or smaller) |
| V _{REGENZ} | Tie to V _{DDIO} . V _{REG} is not supported. |
| ERRORSTS | No Connect |
| FLT1 | No Connect |
| FLT2 | No Connect |
| Power and Ground | |
| V _{DD} | All V _{DD} pins must be connected per Table 4-1 . |
| V _{DDA} | If a dedicated analog supply is not used, tie to V _{DDIO} . |
| V _{DDIO} | All V _{DDIO} pins must be connected per Table 4-1 . |
| V _{DD3VFL} | Must be tied to V _{DDIO} |
| V _{DDOSC} | Must be tied to V _{DDIO} |
| V _{SS} | All V _{SS} pins must be connected to board ground. |
| V _{SSA} | If a dedicated analog ground is not used, tie to V _{SS} . |
| V _{SSOSC} | If an external crystal is not used, this pin may be connected to the board ground. |

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------------------------|--|------|-----|------|
| Supply voltage | V_{DDIO} with respect to V_{SS} | -0.3 | 4.6 | V |
| | V_{DD3VFL} with respect to V_{SS} | -0.3 | 4.6 | |
| | V_{DDOSC} with respect to V_{SS} | -0.3 | 4.6 | |
| | V_{DD} with respect to V_{SS} | -0.3 | 1.5 | |
| Analog voltage | V_{DDA} with respect to V_{SSA} | -0.3 | 4.6 | V |
| Input voltage | V_{IN} (3.3 V) | -0.3 | 4.6 | V |
| Output voltage | V_O | -0.3 | 4.6 | V |
| Input clamp current | Digital input (per pin), I_{IK} ($V_{IN} < V_{SS}$ or $V_{IN} > V_{DDIO}$) | -20 | 20 | mA |
| | Analog input (per pin), $I_{IKANALOG}$ ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$) | -20 | 20 | |
| | Total for all inputs, $I_{IKTOTAL}$ ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$) | -20 | 20 | |
| Output current | Digital output (per pin), I_{OUT} | -20 | 20 | mA |
| Free-Air temperature | T_A | -40 | 125 | °C |
| Operating junction temperature | T_J | -40 | 150 | °C |
| Storage temperature ⁽³⁾ | T_{stg} | -65 | 150 | °C |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.4](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS} , unless otherwise noted.
- (3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see [Semiconductor and IC Package Thermal Metrics](#).

5.2 ESD Ratings – Commercial

| | | | VALUE | UNIT |
|---|-------------------------------|--|-------|------|
| TMS320F28379S, TMS320F28376S, TMS320F28375S, and TMS320F28374S in 337-ball ZWT package | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | |
| TMS320F28379S, TMS320F28378S, TMS320F28376S, TMS320F28375S, and TMS320F28374S in 176-pin PTP package | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | |
| TMS320F28379S, TMS320F28378S, TMS320F28376S, and TMS320F28374S in 100-pin PZP package | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings – Automotive

| | | | VALUE | UNIT | |
|---|-------------------------|---|--|-------|---|
| TMS320F28377S in 337-ball ZWT package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner balls on 337-ball ZWT: A1, A19, W1, W19 | ±750 | |
| TMS320F28377S in 176-pin PTP package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176 | ±750 | |
| TMS320F28377S and TMS320F28375S in 100-pin PZP package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 100-pin PZP: 1, 25, 26, 50, 51, 75, 76, 100 | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|--|---|------|-----|------|------|
| Device supply voltage, I/O, $V_{DDIO}^{(1)}$ | | 3.14 | 3.3 | 3.47 | V |
| Device supply voltage, V_{DD} | | 1.14 | 1.2 | 1.26 | V |
| Supply ground, V_{SS} | | | 0 | | V |
| Analog supply voltage, V_{DDA} | | 3.14 | 3.3 | 3.47 | V |
| Analog ground, V_{SSA} | | | 0 | | V |
| Junction temperature, T_J | T version | –40 | | 105 | °C |
| | S version ⁽²⁾ | –40 | | 125 | |
| | Q version (AEC Q100 qualification) ⁽²⁾ | –40 | | 150 | |
| Free-Air temperature, T_A | Q version (AEC Q100 qualification) | –40 | | 125 | °C |

(1) V_{DDIO} , V_{DD3VFL} , and V_{DDOSC} should be maintained within 0.3 V of each other.

(2) Operation above $T_J = 105^\circ\text{C}$ for extended duration will reduce the lifetime of the device. See [Calculating Useful Lifetimes of Embedded Processors](#) for more information.

5.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. [Table 5-1](#) shows the device current consumption at 200-MHz SYSCLK.

Table 5-1. Device Current Consumption at 200-MHz SYSCLK

| MODE | TEST CONDITIONS | I _{DD} | | I _{DDIO} ⁽¹⁾ | | I _{DDA} | | I _{DD3VFL} | |
|------------------------------------|--|--------------------|--------------------|----------------------------------|--------------------|--------------------|--------------------|---------------------|--------------------|
| | | TYP ⁽²⁾ | MAX ⁽³⁾ | TYP ⁽²⁾ | MAX ⁽³⁾ | TYP ⁽²⁾ | MAX ⁽³⁾ | TYP ⁽²⁾ | MAX ⁽³⁾ |
| Operational | <ul style="list-style-type: none"> Code is running out of RAM.⁽⁴⁾ All I/O pins are left unconnected. Peripherals not active have their clocks disabled. FLASH is read and in active state. XCLKOUT is enabled at SYSCLK/4. | 245 mA | 400 mA | 30 mA | | 13 mA | 20 mA | 33 mA | 40 mA |
| IDLE | <ul style="list-style-type: none"> CPU1 is in IDLE mode. Flash is powered down. XCLKOUT is turned off. | 80 mA | 215 mA | 3 mA | 10 mA | 10 μA | 150 μA | 10 μA | 150 μA |
| STANDBY | <ul style="list-style-type: none"> CPU1 is in STANDBY mode. Flash is powered down. XCLKOUT is turned off. | 30 mA | 170 mA | 3 mA | 10 mA | 5 μA | 150 μA | 10 μA | 150 μA |
| HALT | <ul style="list-style-type: none"> CPU1 watchdog is running. Flash is powered down. XCLKOUT is turned off. | 1.5 mA | 120 mA | 750 μA | 2 mA | 5 μA | 150 μA | 10 μA | 150 μA |
| HIBERNATE | <ul style="list-style-type: none"> CPU1.M0 and CPU1.M1 RAMs are in low-power data retention mode. | 300 μA | 5 mA | 750 μA | 2 mA | 5 μA | 75 μA | 1 μA | 50 μA |
| Flash Erase/Program ⁽⁵⁾ | <ul style="list-style-type: none"> CPU1 is running from RAM. All I/O pins are left unconnected. Peripheral clocks are disabled. CPU1 is performing Flash Erase and Programming. XCLKOUT is turned off. | 154 mA | 230 mA | 3 mA | 10 mA | 10 μA | 150 μA | 45 mA | 55 mA |

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.

(2) TYP: V_{nom}, 30°C

(3) MAX: V_{max}, 125°C

(4) The following is executed in a loop on CPU1:

- All of the communication peripherals are exercised in loop-back mode: CAN-A to CAN-B; SPI-A to SPI-C; SCI-A to SCI-D; I2C-A to I2C-B; McBSP-A to McBSP-B; USB
- SDFM1 to SDFM4 active
- ePWM1 to ePWM12 generate 400-kHz PWM output on 24 pins
- CPU TIMERS active
- DMA does 32-bit burst transfers
- CLA1 does multiply-accumulate tasks
- All ADCs perform continuous conversion
- All DACs ramp voltage up/down at 150 kHz
- CMPSS1 to CMPSS8 active
- VCU does complex multiply/accumulate with parallel load
- TMU calculates a cosine
- FPU does multiply/accumulate with parallel load

(5) Brownout events during flash programming can corrupt flash data. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

5.5.1 Current Consumption Graphs

Figure 5-1 and Figure 5-2 are a typical representation of the relationship between frequency and current consumption/power on the device. The operational test from Table 5-1 was run across frequency at V_{max} and high temperature. Actual results will vary based on the system implementation and conditions.

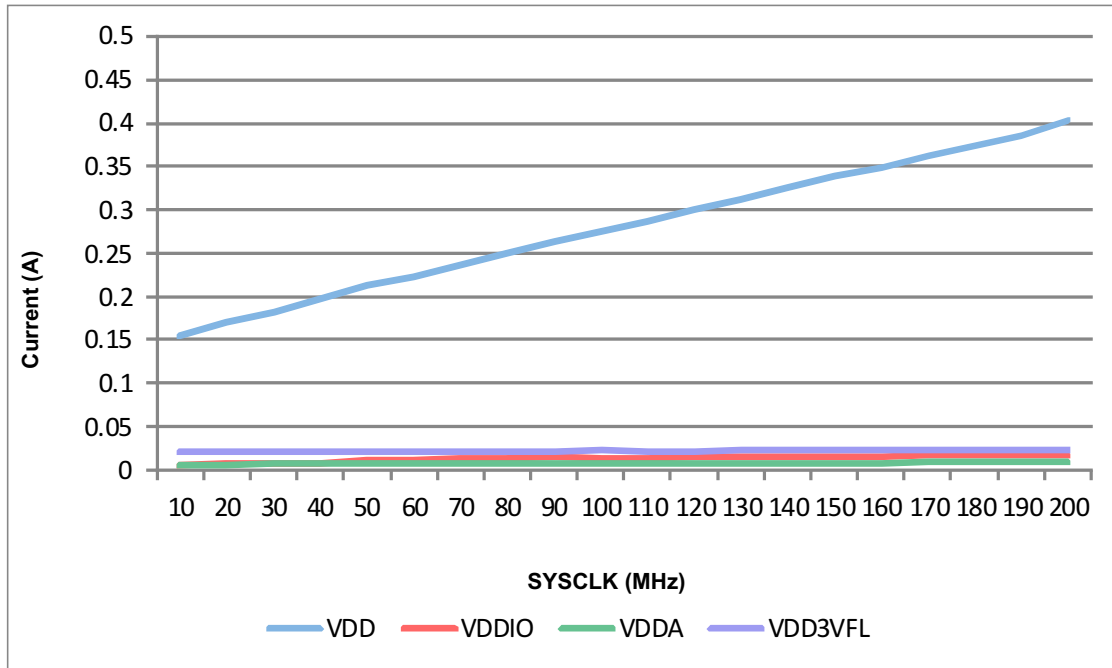


Figure 5-1. Operational Current Versus Frequency

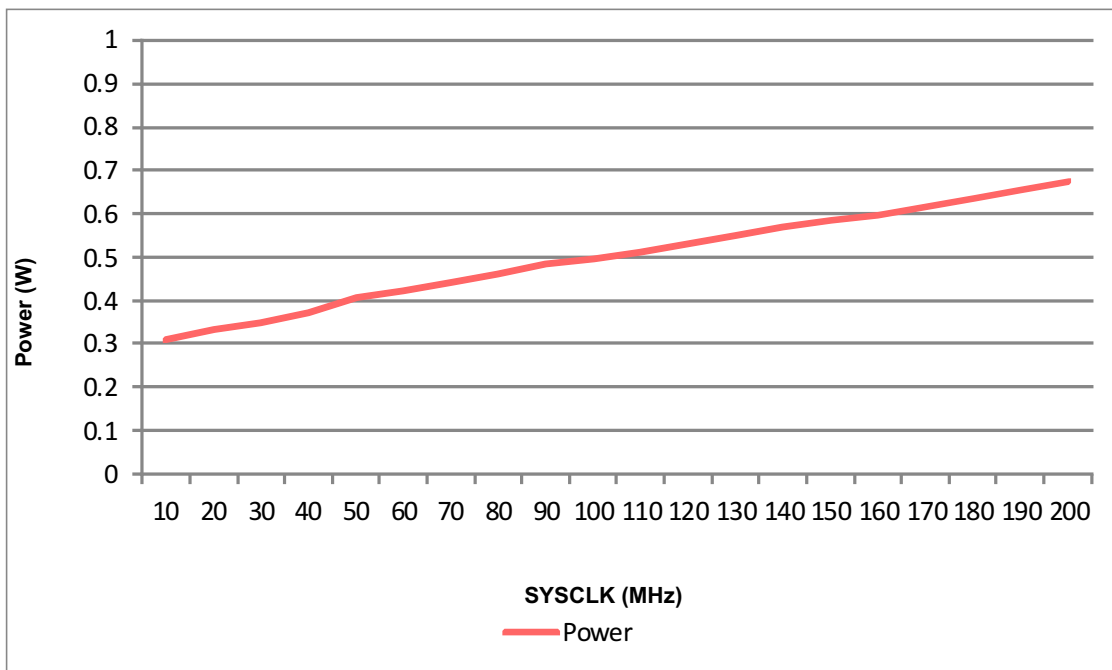


Figure 5-2. Power Versus Frequency

Leakage current will increase with operating temperature in a nonlinear manner. The difference in V_{DD} current between TYP and MAX conditions can be seen in [Figure 5-3](#). The current consumption in HALT mode is primarily leakage current as there is no active switching if the internal oscillator has been powered down.

[Figure 5-3](#) shows the typical leakage current across temperature. The device was placed into HALT mode under nominal voltage conditions.

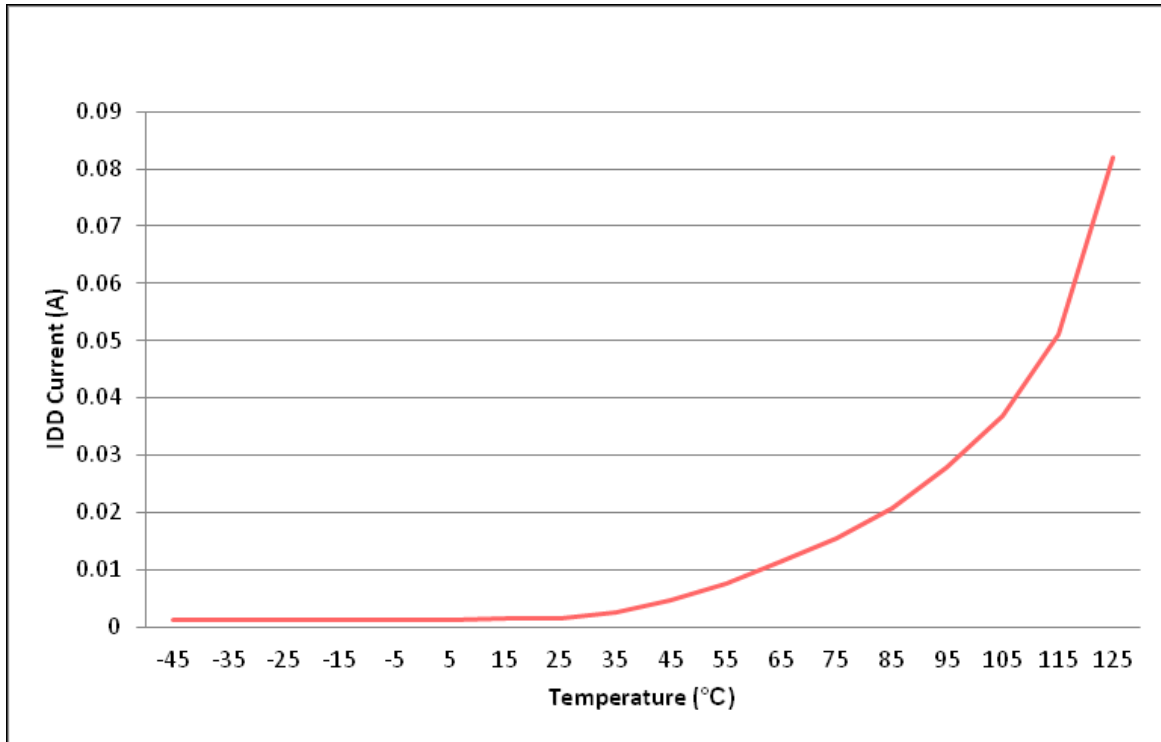


Figure 5-3. I_{DD} Leakage Current Versus Temperature

5.5.2 Reducing Current Consumption

The F2837xS devices provide some methods to reduce the device current consumption:

- Any one of the four low-power modes—IDLE, STANDBY, HALT, and HIBERNATE—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. [Table 5-2](#) indicates the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.

Table 5-2. Current on V_{DD} Supply by Various Peripherals (at 200 MHz)⁽¹⁾

| PERIPHERAL MODULE ⁽²⁾ | I _{DD} CURRENT REDUCTION (mA) |
|----------------------------------|--|
| ADC ⁽³⁾ | 3.3 |
| CAN | 3.3 |
| CLA | 1.4 |
| CMPSS ⁽³⁾ | 1.4 |
| CPUTIMER | 0.3 |
| DAC ⁽³⁾ | 0.6 |
| DMA | 2.9 |
| eCAP | 0.6 |
| EMIF1 | 2.9 |
| EMIF2 | 2.6 |
| ePWM1 to ePWM4 ⁽⁴⁾ | 4.5 |
| ePWM5 to ePWM12 ⁽⁴⁾ | 1.7 |
| HRPWM ⁽⁴⁾ | 1.7 |
| I2C | 1.3 |
| McBSP | 1.6 |
| SCI | 0.9 |
| SDFM | 2 |
| SPI | 0.5 |
| uPP | 7.3 |
| USB and AUXPLL at 60 MHz | 23.8 |

(1) At V_{max} and 125°C.

(2) All peripherals are disabled upon reset. Use the PCLKCRx register to individually enable peripherals. For peripherals with multiple instances, the current quoted is for a single module.

(3) This number represents the current drawn by the digital portion of the ADC, CMPSS, and DAC modules.

(4) The ePWM is at /2 of SYSCLK.

5.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|---|--|-----|-------------------------|------|
| V _{OH} | High-level output voltage | I _{OH} = I _{OH} MIN | V _{DDIO} * 0.8 | | | V |
| | | I _{OH} = -100 μA | V _{DDIO} - 0.2 | | | |
| V _{OL} | Low-level output voltage | I _{OL} = I _{OL} MAX | | | 0.4 | V |
| | | I _{OL} = 100 μA | | | 0.2 | |
| I _{OH} | High-level output source current for all output pins | | -4 | | | mA |
| I _{OL} | Low-level output sink current for all output pins | | | | 4 | mA |
| V _{IH} | High-level input voltage (3.3 V) | GPIO0–GPIO7, GPIO42–GPIO43, GPIO46–GPIO47 | V _{DDIO} * 0.7 | | V _{DDIO} + 0.3 | V |
| | | All other pins | 2.0 | | V _{DDIO} + 0.3 | |
| V _{IL} | Low-level input voltage (3.3 V) | | V _{SS} - 0.3 | | 0.8 | V |
| V _{HYSTERESIS} | Input hysteresis | | | 150 | | mV |
| I _{pulldown} | Input current | Digital inputs with pulldown ⁽¹⁾ | V _{DDIO} = 3.3 V V _{IN} = V _{DDIO} | 120 | | μA |
| I _{pullup} | Input current | Digital inputs with pullup enabled ⁽¹⁾ | V _{DDIO} = 3.3 V V _{IN} = 0 V | 150 | | μA |
| I _{LEAK} | Pin leakage | Digital | Pullups disabled 0 V ≤ V _{IN} ≤ V _{DDIO} | | 2 | μA |
| | | Analog (except ADCINB0 or DACOUTx) | 0 V ≤ V _{IN} ≤ V _{DDA} | | 2 | |
| | | ADCINB0 | | 2 | 11 ⁽²⁾ | |
| | | DACOUTx | | 66 | | |
| C _I | Input capacitance | | | 2 | | pF |

(1) See [Table 4-2](#) for a list of pins with a pullup or pulldown.

(2) The MAX input leakage shown on ADCINB0 is at high temperature.

5.7 Thermal Resistance Characteristics

5.7.1 ZWT Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|-------------------------------|---|---------------------|-------------------------------|
| R _{θJC} | Junction-to-case thermal resistance | 8.3 | N/A |
| R _{θJB} | Junction-to-board thermal resistance | 11.6 | N/A |
| R _{θJA} (High k PCB) | Junction-to-free air thermal resistance | 21.5 | 0 |
| R _{θJMA} | Junction-to-moving air thermal resistance | 19.0 | 150 |
| | | 17.8 | 250 |
| | | 16.5 | 500 |
| Psi _{JT} | Junction-to-package top | 0.2 | 0 |
| | | 0.3 | 150 |
| | | 0.4 | 250 |
| | | 0.5 | 500 |
| Psi _{JB} | Junction-to-board | 11.4 | 0 |
| | | 11.3 | 150 |
| | | 11.2 | 250 |
| | | 11.0 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

5.7.2 PTP Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|-------------------------------|---|---------------------|-------------------------------|
| R _{θJC} | Junction-to-case thermal resistance | 6.97 | N/A |
| R _{θJB} | Junction-to-board thermal resistance | 6.05 | N/A |
| R _{θJA} (High k PCB) | Junction-to-free air thermal resistance | 17.8 | 0 |
| R _{θJMA} | Junction-to-moving air thermal resistance | 12.8 | 150 |
| | | 11.4 | 250 |
| | | 10.1 | 500 |
| Psi _{JT} | Junction-to-package top | 0.11 | 0 |
| | | 0.24 | 150 |
| | | 0.33 | 250 |
| | | 0.42 | 500 |
| Psi _{JB} | Junction-to-board | 6.1 | 0 |
| | | 5.5 | 150 |
| | | 5.4 | 250 |
| | | 5.3 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

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- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

5.7.3 PZP Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|-------------------------------|---|---------------------|-------------------------------|
| R _{θJC} | Junction-to-case thermal resistance | 4.3 | N/A |
| R _{θJB} | Junction-to-board thermal resistance | 5.9 | N/A |
| R _{θJA} (High k PCB) | Junction-to-free air thermal resistance | 19.1 | 0 |
| R _{θJMA} | Junction-to-moving air thermal resistance | 14.3 | 150 |
| | | 12.8 | 250 |
| | | 11.4 | 500 |
| Psi _{JT} | Junction-to-package top | 0.03 | 0 |
| | | 0.09 | 150 |
| | | 0.12 | 250 |
| | | 0.20 | 500 |
| Psi _{JB} | Junction-to-board | 6.0 | 0 |
| | | 5.5 | 150 |
| | | 5.5 | 250 |
| | | 5.3 | 500 |

- (1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
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 - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- (2) lfm = linear feet per minute

5.8 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report [Semiconductor and IC Package Thermal Metrics](#) helps to understand the thermal metrics and definitions.

5.9 System

5.9.1 Power Sequencing

5.9.1.1 Signal Pin Requirements

Before powering the device, no voltage larger than 0.3 V above V_{DDIO} can be applied to any digital pin, and no voltage larger than 0.3 V above V_{DDA} can be applied to any analog pin (including V_{REFHI}).

5.9.1.2 V_{DDIO} , V_{DDA} , V_{DD3VFL} , and V_{DDOSC} Requirements

The 3.3-V supplies should be powered up together and kept within 0.3 V of each other during functional operation.

5.9.1.3 V_{DD} Requirements

The internal VREG is not supported. The VREGENZ pin must be tied to V_{DDIO} and an external source used to supply 1.2 V to V_{DD} . During the ramp, V_{DD} should be kept no more than 0.3 V above V_{DDIO} .

V_{DDOSC} and V_{DD} must be powered on and off at the same time. V_{DDOSC} should not be powered on when V_{DD} is off. For applications not powering V_{DDOSC} and V_{DD} at the same time, see the "INTOSC: V_{DDOSC} Powered Without V_{DD} Can Cause INTOSC Frequency Drift" advisory in the [TMS320F2837xS Delfino™ MCUs Silicon Errata](#).

There is an internal 12.8-mA current source from V_{DD3VFL} to V_{DD} when the flash banks are active. When the flash banks are active and the device is in a low-activity state (for example, a low-power mode), this internal current source can cause V_{DD} to rise to approximately 1.3 V. There will be zero current load to the external system V_{DD} regulator while in this condition. This is not an issue for most regulators; however, if the system voltage regulator requires a minimum load for proper operation, then an external 82Ω resistor can be added to the board to ensure a minimal current load on V_{DD} . See the "Low-Power Modes: Power Down Flash or Maintain Minimum Device Activity" advisory in the [TMS320F2837xS Delfino™ MCUs Silicon Errata](#).

5.9.1.4 Supply Ramp Rate

The supplies should ramp to full rail within 10 ms. [Table 5-3](#) shows the supply ramp rate.

Table 5-3. Supply Ramp Rate

| | | MIN | MAX | UNIT |
|------------------|---|-----|--------|------|
| Supply ramp rate | V_{DDIO} , V_{DD} , V_{DDA} , V_{DD3VFL} , V_{DDOSC} with respect to V_{SS} | 330 | 10^5 | V/s |

5.9.1.5 Supply Supervision

An internal power-on-reset (POR) circuit keeps the I/Os in a high-impedance state during power up. External supply voltage supervisors (SVS) can be used to monitor the voltage on the 3.3-V and 1.2-V rails and drive XRS low when supplies are outside operational specifications.

5.9.2 Reset Timing

\overline{XRS} is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR). During power up, the POR circuit drives the \overline{XRS} pin low. A watchdog or NMI watchdog reset also drives the pin low. An external circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between \overline{XRS} and V_{DDIO} . A capacitor should be placed between \overline{XRS} and V_{SS} for noise filtering; the capacitance should be 100 nF or smaller. These values will allow the watchdog to properly drive the \overline{XRS} pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. [Figure 5-4](#) shows the recommended reset circuit.

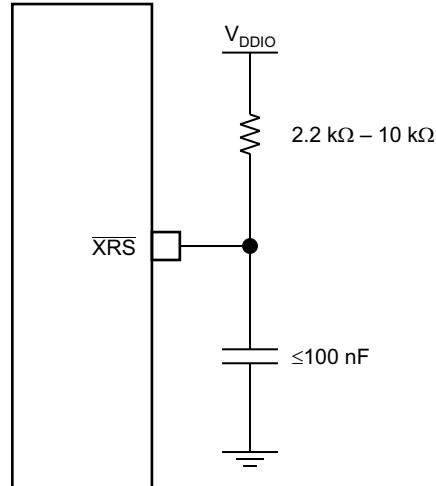


Figure 5-4. Reset Circuit

5.9.2.1 Reset Sources

The following reset sources exist on this device: \overline{XRS} , \overline{WDRS} , $\overline{NMIWDRS}$, \overline{SYSRS} , $\overline{SCCRESET}$, and $\overline{HIBRESET}$. See the Reset Signals table in the System Control chapter of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

The parameter $t_{h(\text{boot-mode})}$ must account for a reset initiated from any of these sources.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive \overline{XRS} low. Use this to disable any other devices driving the boot pins. The $\overline{SCCRESET}$ and debugger reset sources do not drive \overline{XRS} ; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP; for more details, see the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

5.9.2.2 Reset Electrical Data and Timing

Table 5-4 shows the reset (\overline{XRS}) timing requirements. Table 5-5 shows the reset (\overline{XRS}) switching characteristics. Figure 5-5 shows the power-on reset. Figure 5-6 shows the warm reset.

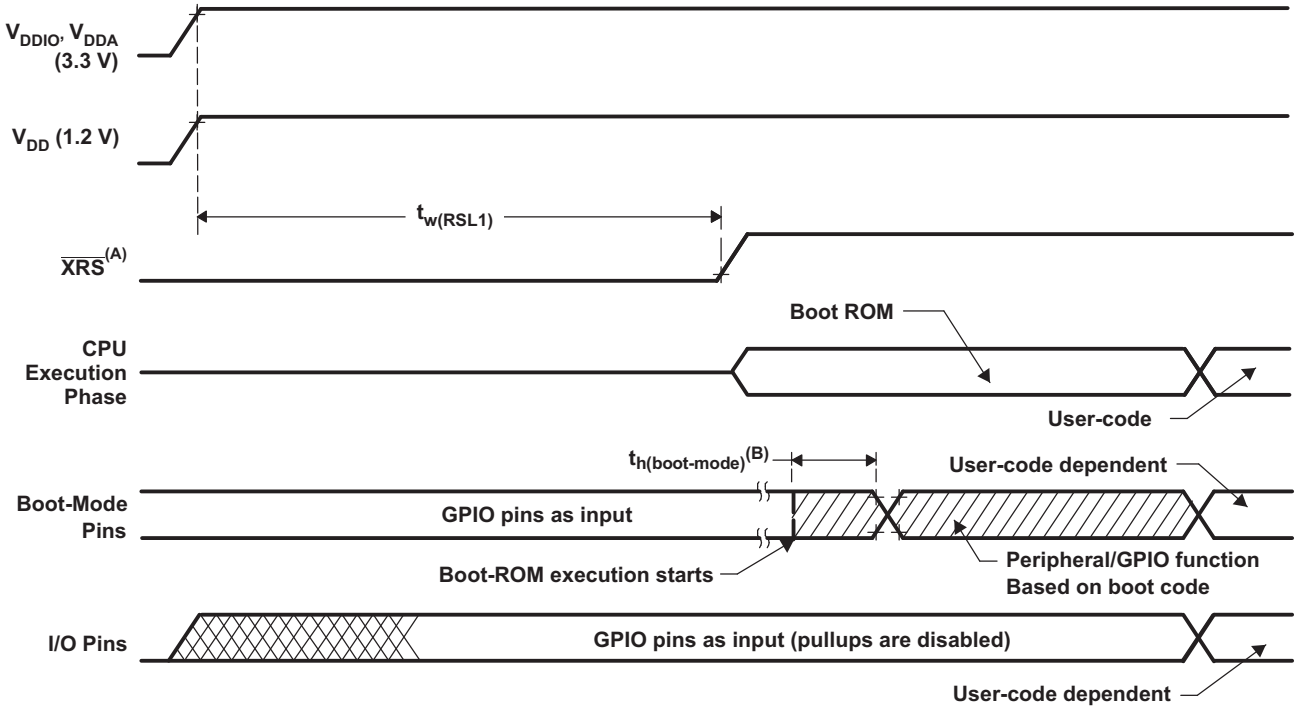
Table 5-4. Reset (\overline{XRS}) Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------|--|-----|-----|---------------|
| $t_{h(\text{boot-mode})}$ | Hold time for boot-mode pins | 1.5 | | ms |
| $t_{w(\text{RSL}2)}$ | Pulse duration, \overline{XRS} low on warm reset | 3.2 | | μs |

Table 5-5. Reset (\overline{XRS}) Switching Characteristics

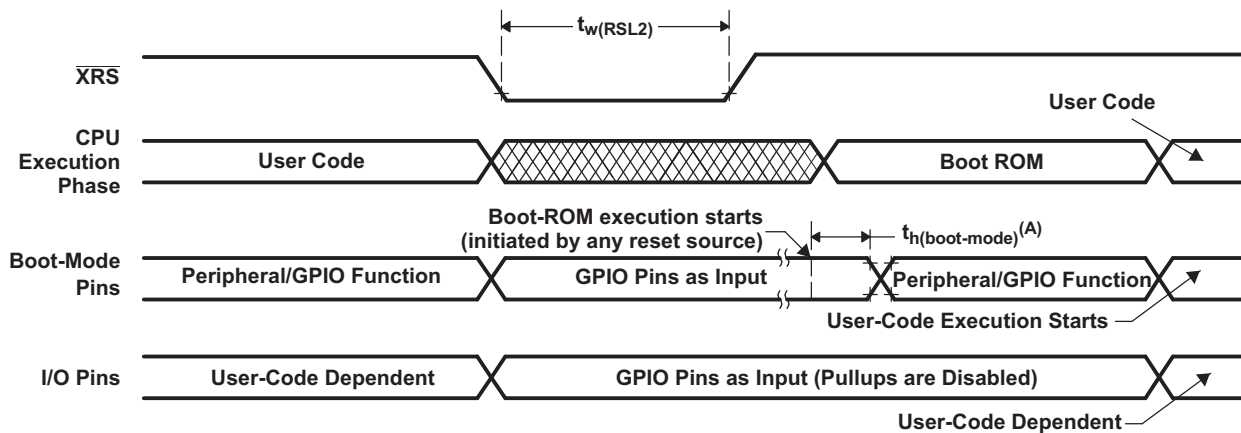
over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|----------------------|---|-----|----------------------------|-----|---------------|
| $t_{w(\text{RSL}1)}$ | Pulse duration, \overline{XRS} driven low by device after supplies are stable | | 100 | | μs |
| $t_{w(\text{WDRS})}$ | Pulse duration, reset pulse generated by watchdog | | $512t_{c(\text{OSCCCLK})}$ | | cycles |



- A. The \overline{XRS} pin can be driven externally by a supervisor or an external pullup resistor, see [Table 4-1](#).
- B. After reset from any source (see [Section 5.9.2.1](#)), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 5-5. Power-on Reset



- A. After reset from any source (see [Section 5.9.2.1](#)), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 5-6. Warm Reset

5.9.3 Clock Specifications

5.9.3.1 Clock Sources

Table 5-6 lists four possible clock sources. Figure 5-7 provides an overview of the device's clocking system.

Table 5-6. Possible Reference Clock Sources

| CLOCK SOURCE | MODULES CLOCKED | COMMENTS |
|------------------------|---|---|
| INTOSC1 | Can be used to provide clock for: <ul style="list-style-type: none"> • Watchdog block • Main PLL • CPU-Timer 2 | Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator. |
| INTOSC2 ⁽¹⁾ | Can be used to provide clock for: <ul style="list-style-type: none"> • Main PLL • Auxiliary PLL • CPU-Timer 2 | Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator. |
| XTAL | Can be used to provide clock for: <ul style="list-style-type: none"> • Main PLL • Auxiliary PLL • CPU-Timer 2 | External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin. |
| AUXCLKIN | Can be used to provide clock for: <ul style="list-style-type: none"> • Auxiliary PLL • CPU-Timer 2 | Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock. |

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

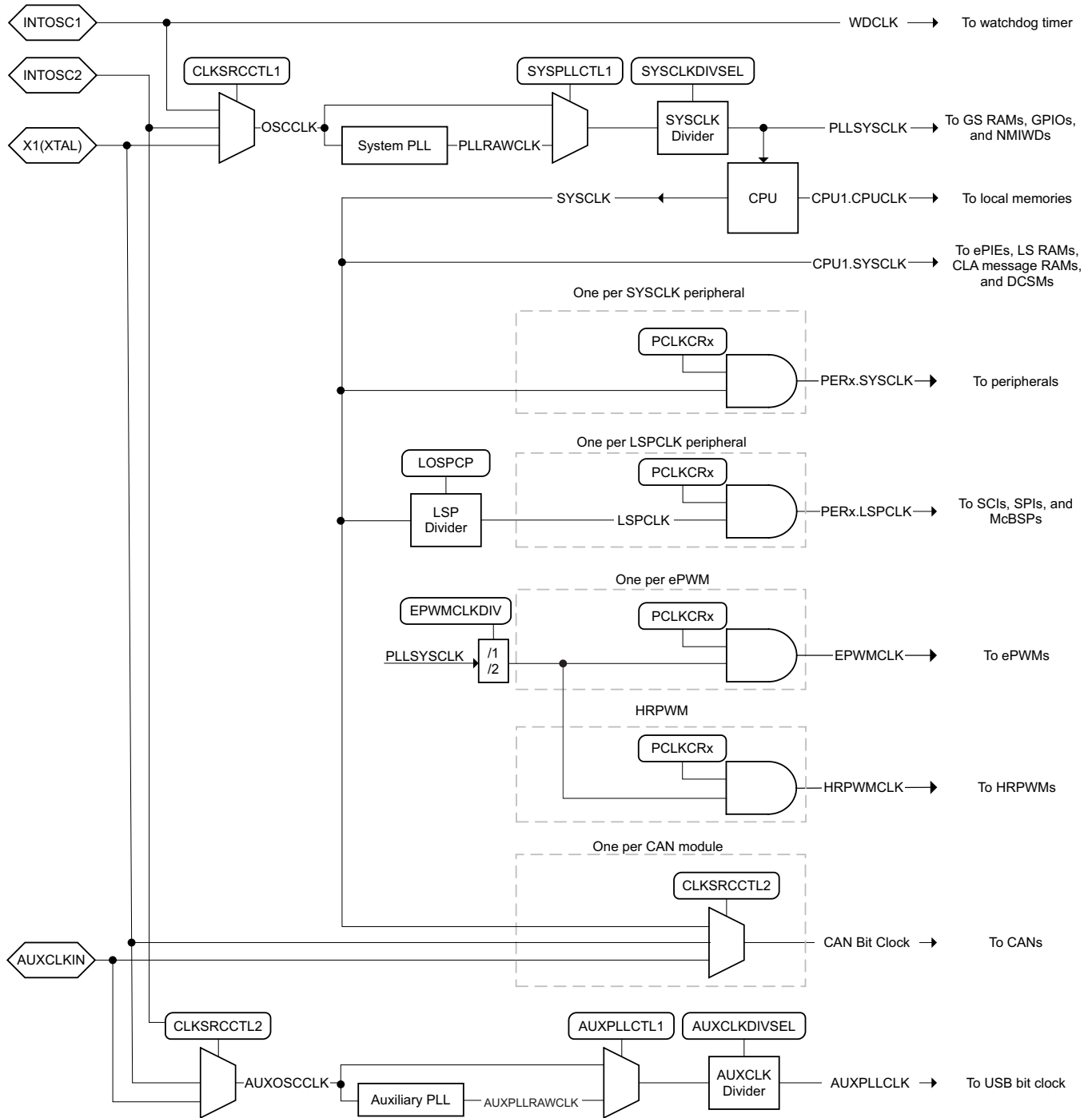


Figure 5-7. Clocking System

5.9.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

5.9.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

Table 5-7 shows the frequency requirements for the input clocks. Table 5-16 shows the crystal equivalent series resistance requirements. Table 5-8 shows the X1 input level characteristics when using an external clock source. Table 5-9 and Table 5-10 show the timing requirements for the input clocks. Table 5-11 shows the PLL lock times for the Main PLL and the USB PLL.

Table 5-7. Input Clock Frequency

| | | MIN | MAX | UNIT |
|--------------|---|-----|-----|------|
| $f_{(XTAL)}$ | Frequency, X1/X2, from external crystal or resonator | 10 | 20 | MHz |
| $f_{(X1)}$ | Frequency, X1, from external oscillator (PLL enabled) | 2 | 25 | MHz |
| | Frequency, X1, from external oscillator (PLL disabled) | 2 | 100 | MHz |
| $f_{(AUXI)}$ | Frequency, AUXCLKIN, from external oscillator | 2 | 60 | MHz |

Table 5-8. X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|-------------|--------------------------------|------------------|------------------|------|
| X1 V_{IL} | Valid low-level input voltage | -0.3 | $0.3 * V_{DDIO}$ | V |
| X1 V_{IH} | Valid high-level input voltage | $0.7 * V_{DDIO}$ | $V_{DDIO} + 0.3$ | V |

Table 5-9. X1 Timing Requirements

| | | MIN | MAX | UNIT |
|--------------|--|-----|-----|------|
| $t_{f(X1)}$ | Fall time, X1 | | 6 | ns |
| $t_{r(X1)}$ | Rise time, X1 | | 6 | ns |
| $t_{w(X1L)}$ | Pulse duration, X1 low as a percentage of $t_{c(X1)}$ | 45% | 55% | |
| $t_{w(X1H)}$ | Pulse duration, X1 high as a percentage of $t_{c(X1)}$ | 45% | 55% | |

Table 5-10. AUXCLKIN Timing Requirements

| | | MIN | MAX | UNIT |
|---------------|---|-----|-----|------|
| $t_{f(AUXI)}$ | Fall time, AUXCLKIN | | 6 | ns |
| $t_{r(AUXI)}$ | Rise time, AUXCLKIN | | 6 | ns |
| $t_{w(AUXL)}$ | Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$ | 45% | 55% | |
| $t_{w(AUXH)}$ | Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$ | 45% | 55% | |

Table 5-11. PLL Lock Times

| | | MIN | NOM | MAX | UNIT |
|-------------|---|-----|---|-----|---------|
| $t_{(PLL)}$ | Lock time, Main PLL (X1, from external oscillator) | | $50 \mu s + 2500 * t_{c(OSCCLK)}^{(1)}$ | | μs |
| $t_{(USB)}$ | Lock time, USB PLL (AUXCLKIN, from external oscillator) | | $50 \mu s + 2500 * t_{c(OSCCLK)}^{(1)}$ | | μs |

(1) The PLL lock time here defines the typical time of execution for the PLL workaround as defined in the [TMS320F2837xS Delfino™ MCUs Silicon Errata](#). Cycle count includes code execution of the PLL initialization routine, which could vary depending on compiler optimizations and flash wait states. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see `InitSysPll()` or `SysCtl_setClock()`. For the auxiliary PLL, see `InitAuxPll()` or `SysCtl_setAuxClock()`.

5.9.3.2.2 Internal Clock Frequencies

Table 5-12 provides the clock frequencies for the internal clocks.

Table 5-12. Internal Clock Frequencies

| | | MIN | NOM | MAX | UNIT |
|---------------------------|---|----------------------|-----|--------------------|------|
| f_{SYSCLK} | Frequency, device (system) clock | 2 | | 200 ⁽¹⁾ | MHz |
| $t_{\text{c(SYSCLK)}}$ | Period, device (system) clock | 5 ⁽¹⁾ | | 500 | ns |
| $f_{\text{PLLRAWCLK}}$ | Frequency, system PLL output (before SYSCLK divider) | 120 | | 400 | MHz |
| $f_{\text{AUXPLLRAWCLK}}$ | Frequency, auxiliary PLL output (before AUXCLK divider) | 120 | | 400 | MHz |
| f_{AUXPLL} | Frequency, AUXPLLCLK | 2 | 60 | 60 | MHz |
| f_{PLL} | Frequency, PLLSYSCLK | 2 | | 200 ⁽¹⁾ | MHz |
| f_{LSP} | Frequency, LSPCLK | 2 | | 200 ⁽¹⁾ | MHz |
| $t_{\text{c(LSPCLK)}}$ | Period, LSPCLK | 5 ⁽¹⁾ | | 500 | ns |
| f_{OSCCLK} | Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1) | See respective clock | | | MHz |
| f_{EPWM} | Frequency, EPWMCLK ⁽²⁾ | | | 100 | MHz |
| f_{HRPWM} | Frequency, HRPWMCLK | 60 | | 100 | MHz |

(1) Using an external clock source. If INTOSC1 or INTOSC2 is used as the clock source, then the maximum frequency is 194 MHz and the minimum period is 5.15 ns.

(2) For SYSCLK above 100 MHz, the EPWMCLK must be half of SYSCLK.

5.9.3.2.3 Output Clock Frequency and Switching Characteristics

Table 5-13 provides the frequency of the output clock. Table 5-14 shows the switching characteristics of the output clock, XCLKOUT.

Table 5-13. Output Clock Frequency

| | | MIN | MAX | UNIT |
|------------------|--------------------|-----|-----|------|
| f_{XCO} | Frequency, XCLKOUT | | 50 | MHz |

Table 5-14. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)⁽¹⁾⁽²⁾

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|----------------------|------------------------------|-------|-------|------|
| $t_{\text{f(XCO)}}$ | Fall time, XCLKOUT | | 5 | ns |
| $t_{\text{r(XCO)}}$ | Rise time, XCLKOUT | | 5 | ns |
| $t_{\text{w(XCOL)}}$ | Pulse duration, XCLKOUT low | H – 2 | H + 2 | ns |
| $t_{\text{w(XCOH)}}$ | Pulse duration, XCLKOUT high | H – 2 | H + 2 | ns |

(1) A load of 40 pF is assumed for these parameters.

(2) $H = 0.5t_{\text{c(XCO)}}$

5.9.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, multiple external clock source options are available. Figure 5-8 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 (also referred to as XTAL) and AUXCLKIN.

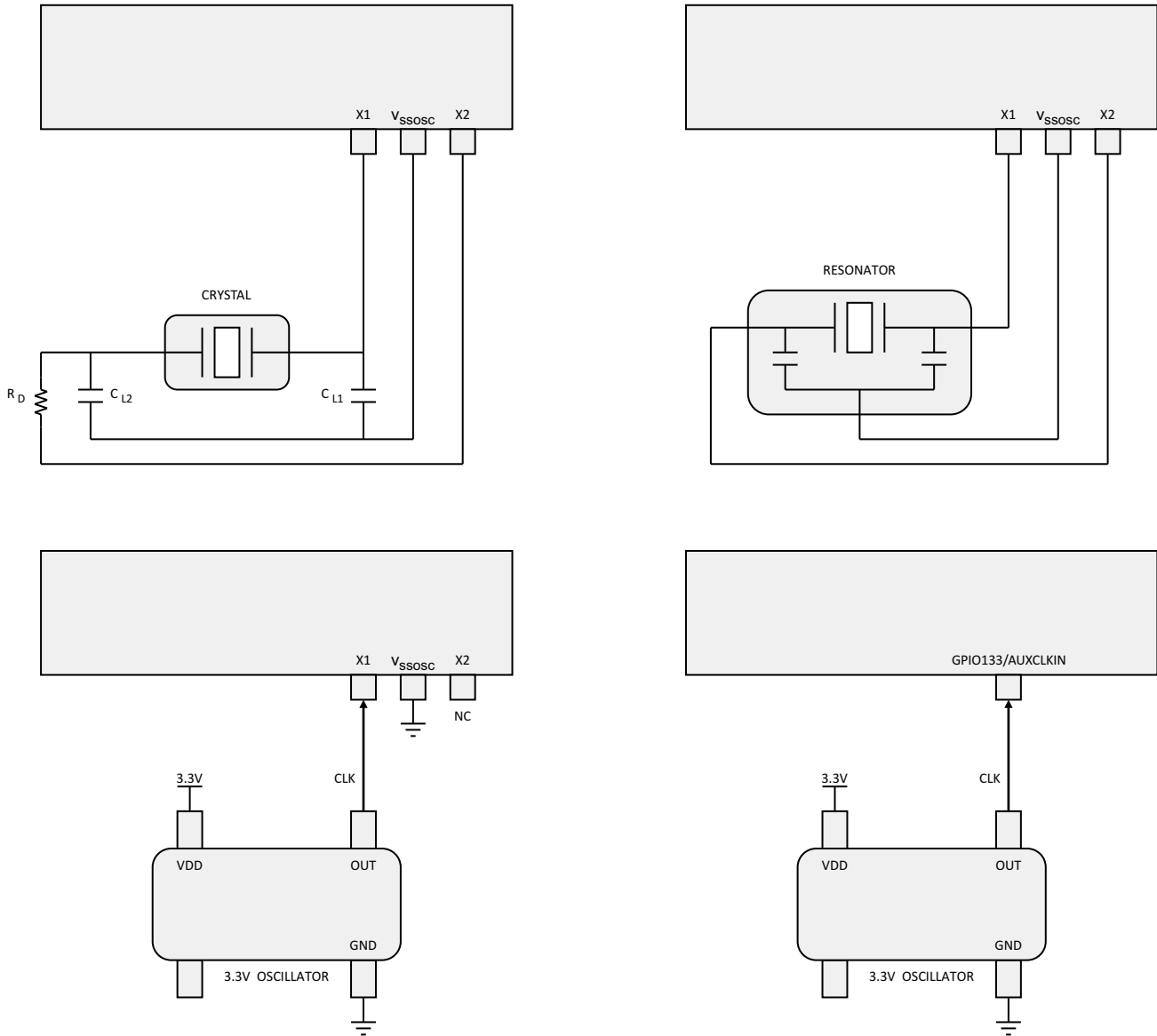


Figure 5-8. Connecting Input Clocks to a 2837xS Device

5.9.3.4 Crystal Oscillator

When using a quartz crystal, it may be necessary to include a damping resistor (R_D) in the crystal circuit to prevent over-driving the crystal (drive level can be found in the crystal data sheet). In higher-frequency applications (10 MHz or greater), R_D is generally not required. If a damping resistor is required, R_D should be as small as possible because the size of the resistance affects start-up time (smaller R_D = faster start-up time). TI recommends that the crystal manufacturer characterize the crystal with the application board. [Table 5-15](#) shows the crystal oscillator parameters. [Table 5-16](#) shows the crystal equivalent series resistance (ESR) requirements. [Table 5-17](#) shows the crystal oscillator electrical characteristics.

Table 5-15. Crystal Oscillator Parameters

| | | MIN | MAX | UNIT |
|----------|---------------------------|-----|-----|------|
| CL1, CL2 | Load capacitance | 12 | 24 | pF |
| C0 | Crystal shunt capacitance | | 7 | pF |

Table 5-16. Crystal Equivalent Series Resistance (ESR) Requirements⁽¹⁾⁽²⁾

| CRYSTAL FREQUENCY (MHz) | MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF) | MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF) |
|-------------------------|---|---|
| 10 | 55 | 110 |
| 12 | 50 | 95 |
| 14 | 50 | 90 |
| 16 | 45 | 75 |
| 18 | 45 | 65 |
| 20 | 45 | 50 |

(1) Crystal shunt capacitance (C0) should be less than or equal to 7 pF.

(2) ESR = Negative Resistance/3

Table 5-17. Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|-----|-----|-----|------|
| Start-up time ⁽¹⁾ | f = 20 MHz ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 2 | | ms |
| Crystal drive level (DL) | | | | 1 | mW |

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

5.9.3.5 Internal Oscillators

To reduce production board costs and application development time, all F2837xS devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, both oscillators are enabled at power up. INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source. INTOSC1 can also be manually configured as the system reference clock (OSCCLK). [Table 5-18](#) provides the electrical characteristics of the internal oscillators to determine if this module meets the clocking requirements of the application.

[Table 5-18](#) provides the electrical characteristics of the two internal oscillators.

NOTE

This oscillator cannot be used as the PLL source if the PLLSYSCLK is configured to frequencies above 194 MHz.

Table 5-18. Internal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|------------------------|-------|------|------|------|
| $f_{i(\text{INTOSC})}$ | Frequency, INTOSC1 and INTOSC2 | | 9.7 | 10.0 | 10.3 | MHz |
| $f_{i(\text{INTOSC-STABILITY})}$ | Frequency stability at room temperature | 30°C, Nominal V_{DD} | ±0.1% | | | |
| | Frequency stability over V_{DD} | 30°C | ±0.2% | | | |
| | Frequency stability | | -3.0% | | 3.0% | |
| $f_{i(\text{INTOSC-ST})}$ | Start-up and settling time | | | | 20 | µs |

5.9.4 Flash Parameters

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 128-bit-wide prefetch reads and a pipeline buffer. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM. This flash efficiency lets designers realize a 2x improvement in performance when migrating from the previous generation Delfino MCUs. Note that an extra wait state is automatically added when code is fetched or data is read from Bank 1 (compared to that of Bank 0), even for prefetched data.

This device also has an OTP (One-Time-Programmable) sector used for the dual code security module (DCSM), which cannot be erased after it is programmed.

Table 5-19 shows the minimum required flash wait states at different frequencies. Table 5-20 shows the flash parameters.

Table 5-19. Flash Wait States

| CPUCLK (MHz) | | MINIMUM WAIT STATES ⁽¹⁾ |
|--------------------------------|--------------------|------------------------------------|
| EXTERNAL OSCILLATOR OR CRYSTAL | INTOSC1 OR INTOSC2 | |
| 150 < CPUCLK ≤ 200 | 145 < CPUCLK ≤ 194 | 3 |
| 100 < CPUCLK ≤ 150 | 97 < CPUCLK ≤ 145 | 2 |
| 50 < CPUCLK ≤ 100 | 48 < CPUCLK ≤ 97 | 1 |
| CPUCLK ≤ 50 | CPUCLK ≤ 48 | 0 |

(1) Minimum required FRDCNTL[RWAIT].

Table 5-20. Flash Parameters

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-------|--------|
| Program Time ⁽¹⁾ | 128 data bits + 16 ECC bits | | 40 | 300 | μs |
| | 8KW sector | | 90 | 180 | ms |
| | 32KW sector | | 360 | 720 | ms |
| Erase Time ⁽²⁾ at < 25 cycles | 8KW sector | | 25 | 50 | ms |
| | 32KW sector | | 30 | 55 | |
| Erase Time ⁽²⁾ at 20k cycles | 8KW sector | | 105 | 4000 | ms |
| | 32KW sector | | 110 | 4000 | |
| N _{wec} | Write/erase cycles | | | 20000 | cycles |
| t _{retention} | Data retention duration at T _J = 85°C | 20 | | | years |

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:

- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the emulator used.

Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.

Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

NOTE

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle. For more details, see the "Flash: Minimum Programming Word Size" advisory in the [TMS320F2837xS Delfino™ MCUs Silicon Errata](#).

5.9.5 Emulation/JTAG

The JTAG port has five dedicated pins: $\overline{\text{TRST}}$, TMS, TDI, TDO, and TCK. The $\overline{\text{TRST}}$ signal should always be pulled down through a 2.2-k Ω pull-down resistor on the board. This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 k Ω to 4.7 k Ω (depending on the drive strength of the debugger ports). Typically, a 2.2-k Ω value is used.

See [Figure 5-9](#) to see how the 14-pin JTAG header connects to the MCU's JTAG port signals. [Figure 5-10](#) shows how to connect to the 20-pin header. The 20-pin JTAG header terminals EMU2, EMU3, and EMU4 are not used and should be grounded.

The PD (Power Detect) terminal of the emulator header should be connected to the board 3.3-V supply. Header GND terminals should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output terminal back to the RTCK input terminal of the header (to sense clock continuity by the emulator). Header terminal $\overline{\text{RESET}}$ is an open-drain output from the emulator header that enables board components to be reset through emulator commands (available only through the 20-pin header).

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most emulator operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22- Ω resistors should be placed in series on each JTAG signal.

For more information about hardware breakpoints and watchpoints, see [Hardware Breakpoints and Watchpoints for C28x in CCS](#).

For more information about JTAG emulation, see the [XDS Target Connection Guide](#).

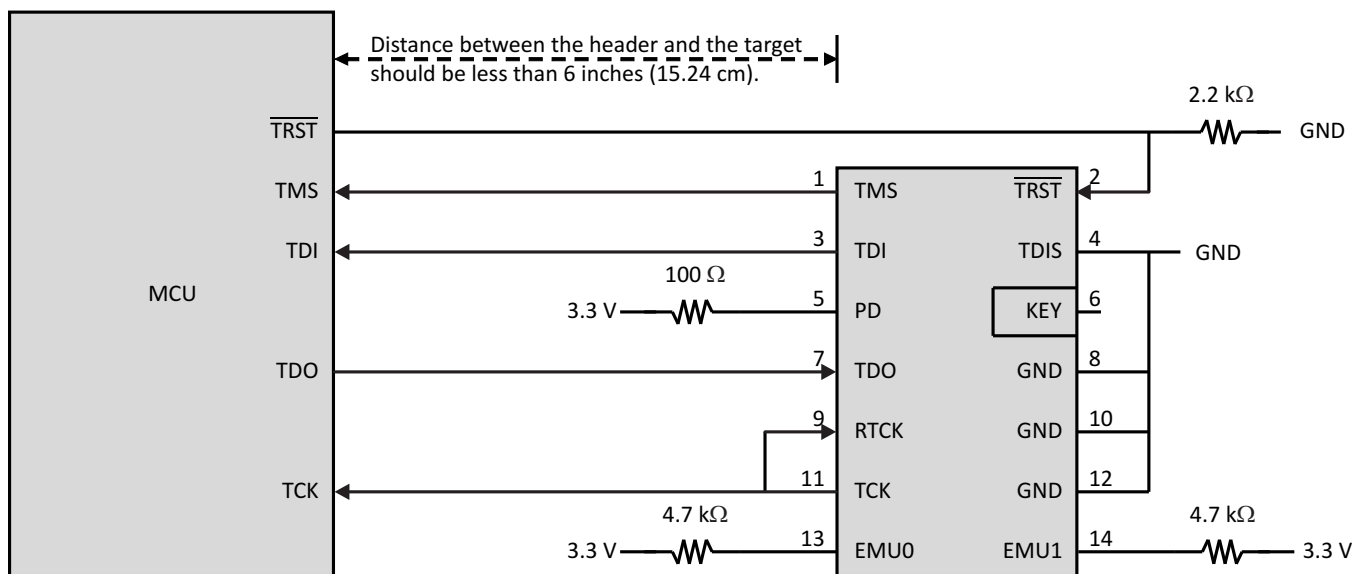


Figure 5-9. Connecting to the 14-Pin JTAG Header

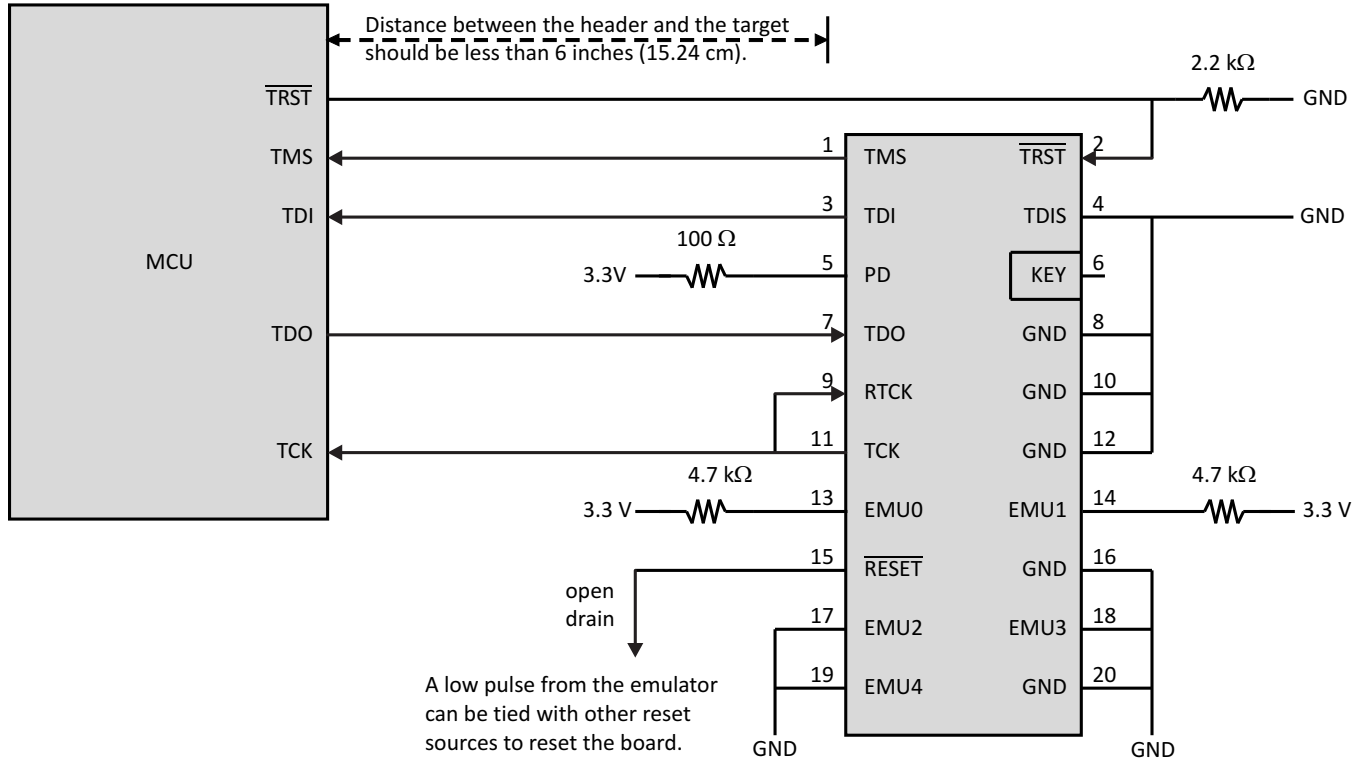


Figure 5-10. Connecting to the 20-Pin JTAG Header

5.9.5.1 JTAG Electrical Data and Timing

Table 5-21 lists the JTAG timing requirements. Table 5-22 lists the JTAG switching characteristics. Figure 5-11 shows the JTAG timing.

Table 5-21. JTAG Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|---------------------------|--|-------|-----|------|
| 1 | $t_c(\text{TCK})$ | Cycle time, TCK | 66.66 | | ns |
| 1a | $t_w(\text{TCKH})$ | Pulse duration, TCK high (40% of t_c) | 26.66 | | ns |
| 1b | $t_w(\text{TCKL})$ | Pulse duration, TCK low (40% of t_c) | 26.66 | | ns |
| 3 | $t_{su}(\text{TDI-TCKH})$ | Input setup time, TDI valid to TCK high | 13 | | ns |
| | $t_{su}(\text{TMS-TCKH})$ | Input setup time, TMS valid to TCK high | 13 | | ns |
| 4 | $t_h(\text{TCKH-TDI})$ | Input hold time, TDI valid from TCK high | 7 | | ns |
| | $t_h(\text{TCKH-TMS})$ | Input hold time, TMS valid from TCK high | 7 | | ns |

Table 5-22. JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|------------------------|-----|-----|------|
| 2 | $t_d(\text{TCKL-TDO})$ | 6 | 25 | ns |

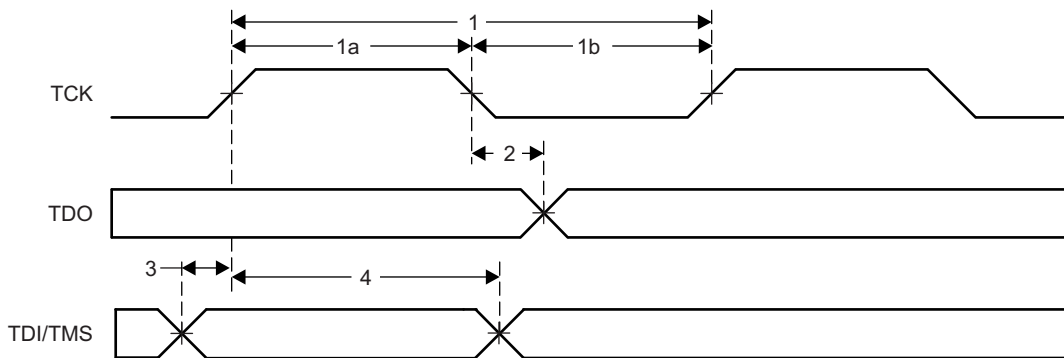


Figure 5-11. JTAG Timing

5.9.6 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADC(s), eCAP(s), ePWM(s), and external interrupts. For more details, see the X-BAR chapter in the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

5.9.6.1 GPIO - Output Timing

Table 5-23 shows the general-purpose output switching characteristics. Figure 5-12 shows the general-purpose output timing.

Table 5-23. General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | MIN | MAX | UNIT |
|--------------|---------------------------------------|-----------|-----|------------------|------|
| $t_{r(GPO)}$ | Rise time, GPIO switching low to high | All GPIOs | | 8 ⁽¹⁾ | ns |
| $t_{f(GPO)}$ | Fall time, GPIO switching high to low | All GPIOs | | 8 ⁽¹⁾ | ns |
| t_{fGPO} | Toggle frequency, GPO pins | | | 25 | MHz |

(1) Rise time and fall time vary with load. These values assume a 40-pF load.

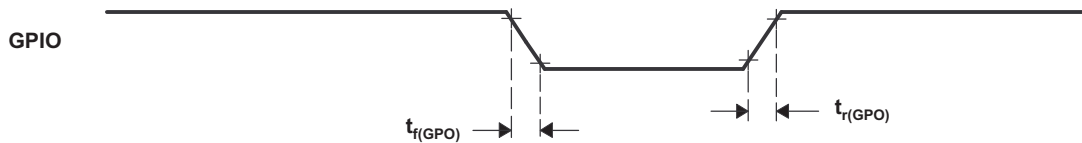


Figure 5-12. General-Purpose Output Timing

5.9.6.2 GPIO - Input Timing

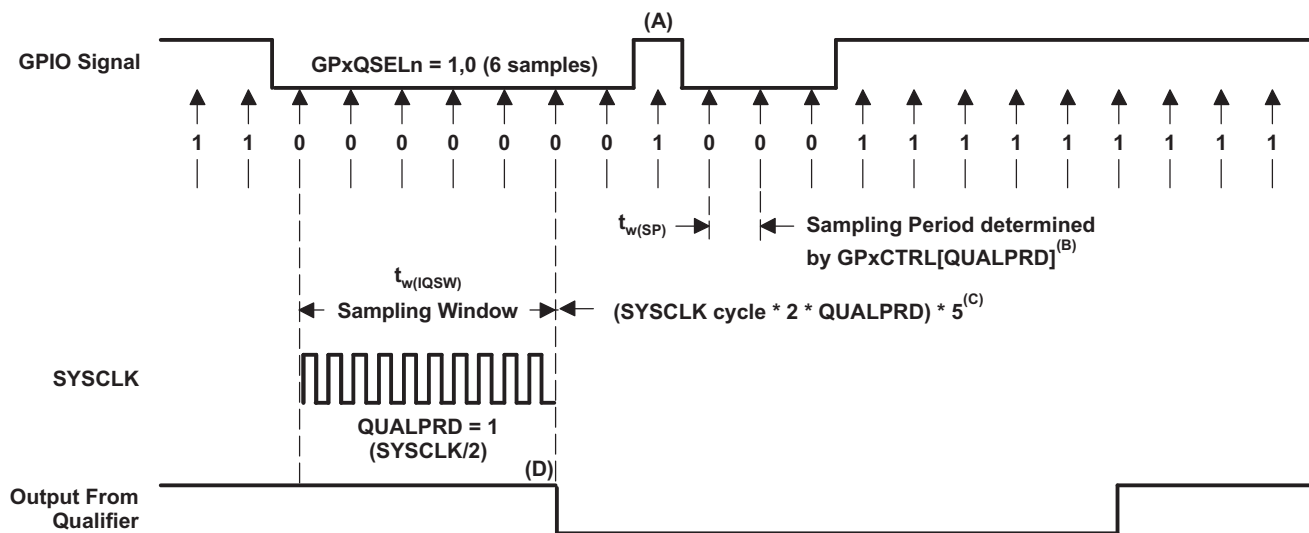
Table 5-24 shows the general-purpose input timing requirements. Figure 5-13 shows the sampling mode.

Table 5-24. General-Purpose Input Timing Requirements

| | | MIN | MAX | UNIT |
|--------------------|---------------------------------|----------------------|---|--------|
| $t_{w(SP)}$ | Sampling period | QUALPRD = 0 | $1t_{c(SYCLK)}$ | cycles |
| | | QUALPRD \neq 0 | $2t_{c(SYCLK)} * QUALPRD$ | cycles |
| $t_{w(IQSW)}$ | Input qualifier sampling window | | $t_{w(SP)} * (n^{(1)} - 1)$ | cycles |
| $t_{w(GPI)}^{(2)}$ | Pulse duration, GPIO low/high | Synchronous mode | $2t_{c(SYCLK)}$ | cycles |
| | | With input qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYCLK)}$ | cycles |

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.

(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.



- A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYCLK cycle. For any other value "n", the qualification sampling period is 2n SYCLK cycles (that is, at every 2n SYCLK cycles, the GPIO pin will be sampled).
- B. The qualification period selected through the GPxCTRL register applies to groups of 8 GPIO pins.
- C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
- D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYCLK cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYCLK-wide pulse ensures reliable recognition.

Figure 5-13. Sampling Mode

5.9.6.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

$$\text{Sampling frequency} = \text{SYSCLK}/(2 \times \text{QUALPRD}), \text{ if } \text{QUALPRD} \neq 0 \quad (1)$$

$$\text{Sampling frequency} = \text{SYSCLK}, \text{ if } \text{QUALPRD} = 0 \quad (2)$$

$$\text{Sampling period} = \text{SYSCLK cycle} \times 2 \times \text{QUALPRD}, \text{ if } \text{QUALPRD} \neq 0 \quad (3)$$

In [Equation 1](#), [Equation 2](#), and [Equation 3](#), SYSCLK cycle indicates the time period of SYSCLK.

$$\text{Sampling period} = \text{SYSCLK cycle}, \text{ if } \text{QUALPRD} = 0$$

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

$$\text{Sampling window width} = (\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 2, \text{ if } \text{QUALPRD} \neq 0$$

$$\text{Sampling window width} = (\text{SYSCLK cycle}) \times 2, \text{ if } \text{QUALPRD} = 0$$

Case 2:

Qualification using 6 samples

$$\text{Sampling window width} = (\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 5, \text{ if } \text{QUALPRD} \neq 0$$

$$\text{Sampling window width} = (\text{SYSCLK cycle}) \times 5, \text{ if } \text{QUALPRD} = 0$$

[Figure 5-14](#) shows the general-purpose input timing.

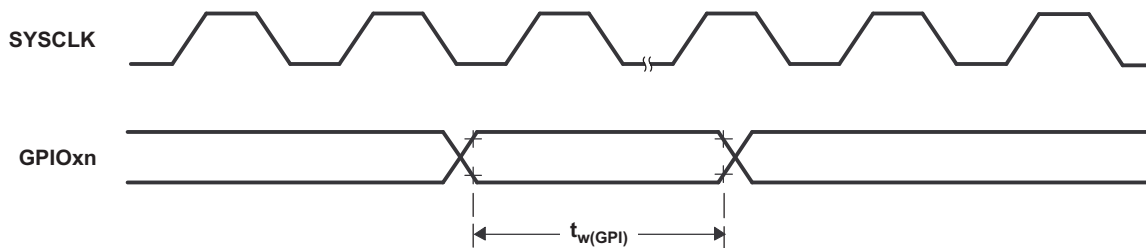


Figure 5-14. General-Purpose Input Timing

5.9.7 Interrupts

Figure 5-15 provides a high-level view of the interrupt architecture.

As shown in Figure 5-15, the devices support five external interrupts (XINT1 to XINT5) that can be mapped onto any of the GPIO pins.

In this device, 16 ePIE block interrupts are grouped into 1 CPU interrupt. In total, there are 12 CPU interrupt groups, with 16 interrupts per group.

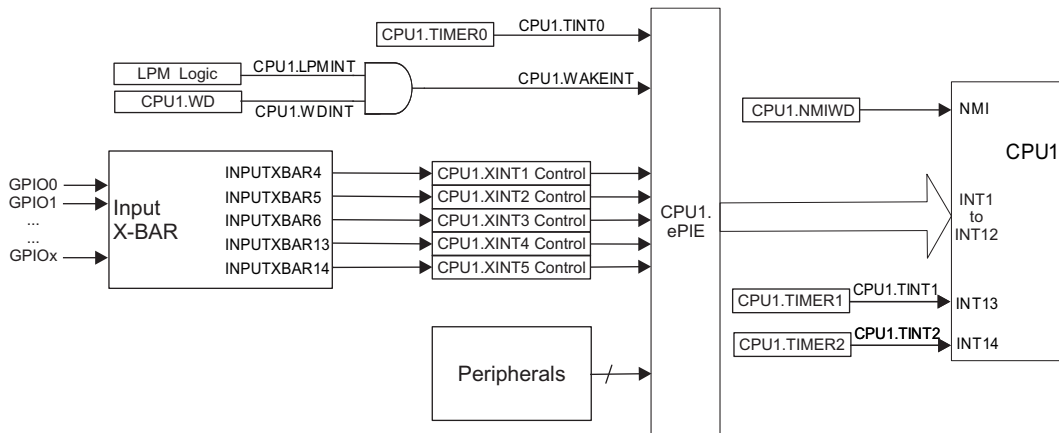


Figure 5-15. External and ePIE Interrupt Sources

5.9.7.1 External Interrupt (XINT) Electrical Data and Timing

Table 5-25 lists the external interrupt timing requirements. Table 5-26 lists the external interrupt switching characteristics. Figure 5-16 shows the external interrupt timing.

Table 5-25. External Interrupt Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------|------------------------------------|---|-----|--------|
| $t_{w(INT)}$ | Pulse duration, INT input low/high | | | |
| | Synchronous | $2t_{c(SYSCCLK)}$ | | cycles |
| | With qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCCLK)}$ | | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-24.

Table 5-26. External Interrupt Switching Characteristics⁽¹⁾

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT |
|--|----------------------------------|--|--------|
| $t_{d(INT)}$ Delay time, INT low/high to interrupt-vector fetch ⁽²⁾ | $t_{w(IQSW)} + 14t_{c(SYSCCLK)}$ | $t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCCLK)}$ | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-24.

(2) This assumes that the ISR is in a single-cycle memory.

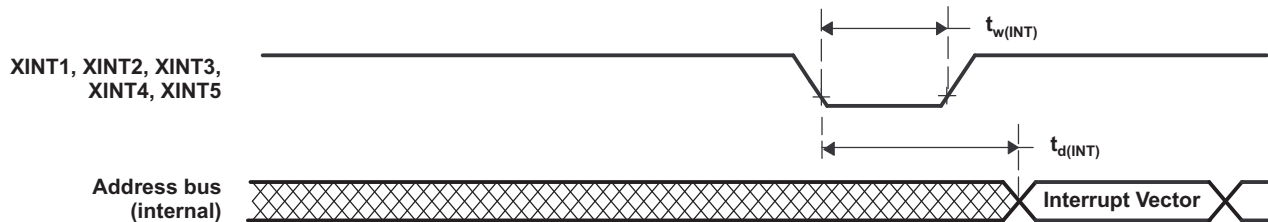


Figure 5-16. External Interrupt Timing

5.9.8 Low-Power Modes

This device has three clock-gating low-power modes and a special power-gating mode.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low Power Modes section of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

5.9.8.1 Clock-Gating Low-Power Modes

IDLE, STANDBY, and HALT modes on this device are similar to those on other C28x devices. [Table 5-27](#) describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 5-27. Effect of Clock-Gating Low-Power Modes on the Device

| MODULES/ CLOCK DOMAIN | CPU1 IDLE | CPU1 STANDBY | HALT |
|--|-----------|--------------|--|
| CPU1.CLKIN | Active | Gated | Gated |
| CPU1.SYSCLK | Active | Gated | Gated |
| CPU1.CPUCLK | Gated | Gated | Gated |
| Clock to modules Connected to PERx.SYSCLK | Active | Gated | Gated |
| CPU1.WDCLK | Active | Active | Gated if CLKSRCCTL1.WDHALTI = 0 |
| AUXPLLCLK | Active | Active | Gated |
| PLL | Powered | Powered | Software must power down PLL before entering HALT |
| INTOSC1 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| INTOSC2 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| Flash | Powered | Powered | Software-Controlled |
| X1/X2 Crystal Oscillator | Powered | Powered | Powered-Down |

5.9.8.2 Power-Gating Low-Power Modes

HIBERNATE mode is the lowest power mode on this device. It is a global low-power mode that gates the supply voltages to most of the system. HIBERNATE is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity. [Table 5-28](#) describes the effects on the system when the HIBERNATE mode is entered.

Table 5-28. Effect of Power-Gating Low-Power Mode on the Device

| MODULES/POWER DOMAINS | HIBERNATE |
|---|--|
| M0 and M1 memories | <ul style="list-style-type: none"> Remain on with memory retention if LPMCR.M0M1MODE = 0x00 Are off when LPMCR.M0M1MODE = 0x01 |
| CPU1 digital peripherals | Powered down |
| Dx, LSx, GSx memories | Power down, memory contents are lost |
| I/Os | On with output state preserved |
| Oscillators, PLL, analog peripherals, Flash | Enters Low-Power Mode |

5.9.8.3 Low-Power Mode Wakeup Timing

Table 5-29 shows the IDLE mode timing requirements, Table 5-30 shows the switching characteristics, and Figure 5-17 shows the timing diagram for IDLE mode.

Table 5-29. IDLE Mode Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------|---|-------------------------|--------------------------------|--------|
| $t_{w(WAKE)}$ | Pulse duration, external wake-up signal | Without input qualifier | $2t_{c(SYSCLK)}$ | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | |

(1) For an explanation of the input qualifier parameters, see Table 5-24.

Table 5-30. IDLE Mode Switching Characteristics⁽¹⁾

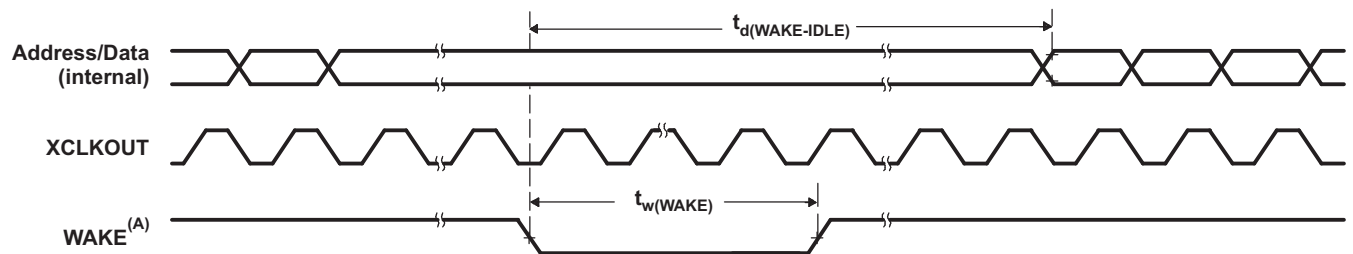
over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------------|---|-------------------------|---------------------------------|---|--------|
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume ⁽²⁾ | | | | cycles |
| | • Wakeup from Flash – Flash module in active state | Without input qualifier | | $40t_{c(SYSCLK)}$ | |
| | | With input qualifier | | $40t_{c(SYSCLK)} + t_{w(WAKE)}$ | |
| | • Wakeup from Flash – Flash module in sleep state | Without input qualifier | | $6700t_{c(SYSCLK)}^{(3)}$ | |
| | | With input qualifier | | $6700t_{c(SYSCLK)}^{(3)} + t_{w(WAKE)}$ | |
| | • Wakeup from RAM | Without input qualifier | | $25t_{c(SYSCLK)}$ | |
| With input qualifier | | | $25t_{c(SYSCLK)} + t_{w(WAKE)}$ | | |

(1) For an explanation of the input qualifier parameters, see Table 5-24.

(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

(3) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual*. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.



A. WAKE can be any enabled interrupt, \overline{WDINT} or \overline{XRS} . After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 5-17. IDLE Entry and Exit Timing Diagram

Table 5-31 shows the STANDBY mode timing requirements, Table 5-32 shows the switching characteristics, and Figure 5-18 shows the timing diagram for STANDBY mode.

Table 5-31. STANDBY Mode Timing Requirements

| | | MIN | MAX | UNIT |
|-------------------|---|---|-----------------------------------|--------|
| $t_{w(WAKE-INT)}$ | Pulse duration, external wake-up signal | QUALSTDBY = 0 $2t_{c(OSCCLK)}$ | $3t_{c(OSCCLK)}$ | cycles |
| | | QUALSTDBY > 0 $(2 + QUALSTDBY)t_{c(OSCCLK)}$ ⁽¹⁾ | $(2 + QUALSTDBY) * t_{c(OSCCLK)}$ | |

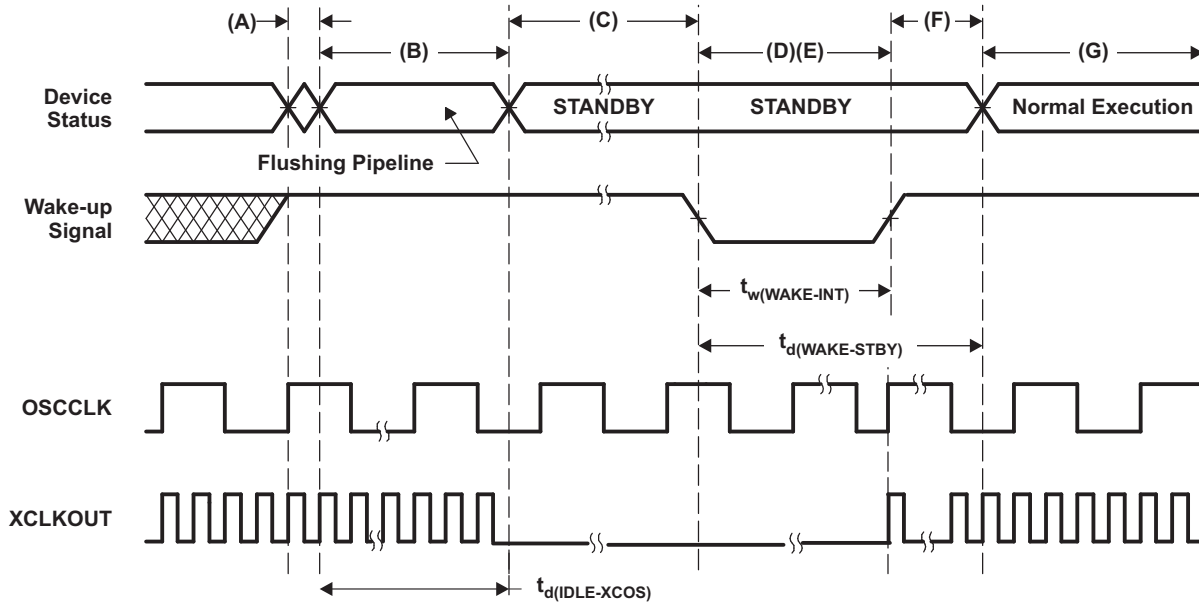
(1) QUALSTDBY is a 6-bit field in the LPMCR register.

Table 5-32. STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|-----|--|--------|
| $t_{d(IDLE-XCOS)}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(INTOSC1)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | | | cycles |
| | <ul style="list-style-type: none"> Wakeup from flash <ul style="list-style-type: none"> Flash module in active state | | $175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$ | |
| | <ul style="list-style-type: none"> Wakeup from flash <ul style="list-style-type: none"> Flash module in sleep state | | $6700t_{c(SYSCLK)}$ ⁽²⁾ + $t_{w(WAKE-INT)}$ | |
| | <ul style="list-style-type: none"> Wakeup from RAM | | $3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$ | |

- (1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
- (2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#). This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.



- A. IDLE instruction is executed to put the device into STANDBY mode.
- B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. The external wake-up signal is driven active.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.
- F. After a latency period, the STANDBY mode is exited.
- G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 5-18. STANDBY Entry and Exit Timing Diagram

Table 5-33 shows the HALT mode timing requirements, Table 5-34 shows the switching characteristics, and Figure 5-19 shows the timing diagram for HALT mode.

Table 5-33. HALT Mode Timing Requirements

| | | MIN | MAX | UNIT |
|--------------------|--|------------------------------|-----|--------|
| $t_{w(WAKE-GPIO)}$ | Pulse duration, GPIO wake-up signal ⁽¹⁾ | $t_{oscst} + 2t_{c(OSCCLK)}$ | | cycles |
| $t_{w(WAKE-XRS)}$ | Pulse duration, \overline{XRS} wake-up signal ⁽¹⁾ | $t_{oscst} + 8t_{c(OSCCLK)}$ | | cycles |

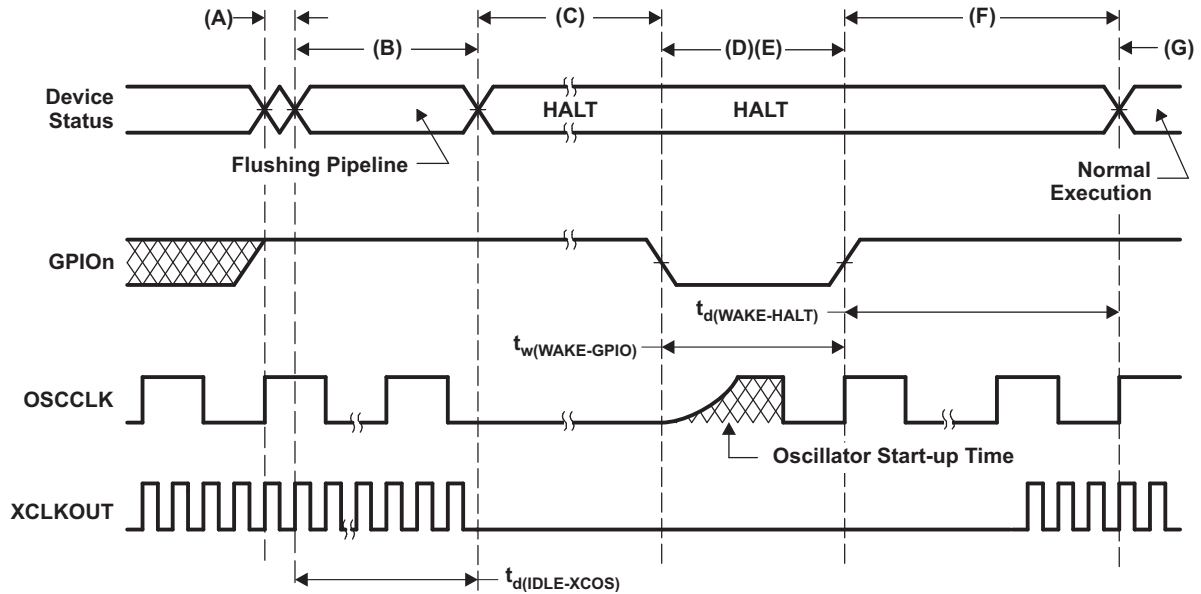
- (1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See Table 5-17 for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see Section 5.9.3.5 for t_{oscst} . Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

Table 5-34. HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|--------------------|---|----------------------------|-----|--------|
| $t_{d(IDLE-XCOS)}$ | Delay time, IDLE instruction executed to XCLKOUT stop | $16t_{c(INTOSC1)}$ | | cycles |
| $t_{d(WAKE-HALT)}$ | Delay time, external wake signal end to CPU1 program execution resume | | | cycles |
| | <ul style="list-style-type: none"> Wakeup from flash <ul style="list-style-type: none"> Flash module in active state | $75t_{c(OSCCLK)}$ | | |
| | <ul style="list-style-type: none"> Wakeup from flash <ul style="list-style-type: none"> Flash module in sleep state | $17500t_{c(OSCCLK)}^{(1)}$ | | |
| | <ul style="list-style-type: none"> Wakeup from RAM | $75t_{c(OSCCLK)}$ | | |

- (1) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#). This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.



- A. IDLE instruction is executed to put the device into HALT mode.
- B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing a 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. When the GPIO pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wakeup sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.
- F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
- G. Normal operation resumes.
- H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 5-19. HALT Entry and Exit Timing Diagram

Table 5-35 shows the HIBERNATE mode timing requirements, Table 5-36 shows the switching characteristics, and Figure 5-20 shows the timing diagram for HIBERNATE mode.

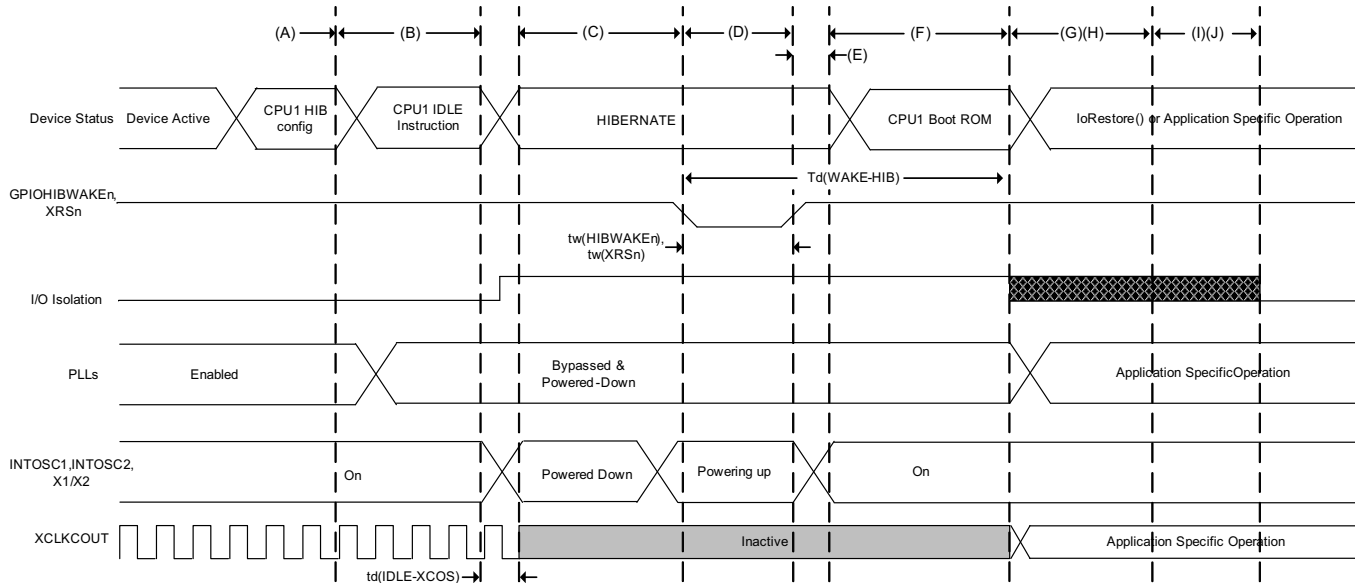
Table 5-35. HIBERNATE Mode Timing Requirements

| | | MIN | MAX | UNIT |
|------------------|---|-----|-----|---------------|
| $t_{w(HIBWAKE)}$ | Pulse duration, $\overline{HIBWAKE}$ signal | 40 | | μs |
| $t_{w(WAKEXRS)}$ | Pulse duration, \overline{XRS} wake-up signal | 40 | | μs |

Table 5-36. HIBERNATE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|--------------------|--|-----|-------------------|--------|
| $t_{d(IDLE-XCOS)}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $30t_{c(SYSCLK)}$ | cycles |
| $t_{d(WAKE-HIB)}$ | Delay time, external wake signal to IORestore function start | | 1.5 | ms |



- A. CPU1 does necessary application-specific context save to M0/M1 memories if required. This includes GPIO state if using I/O Isolation. Configures the LPMCR register of CPU1 for HIBERNATE mode. Powers down Flash Pump/Bank, USB-PHY, CMPSS, DAC, and ADC using their register configurations. The application should also power down the PLL and peripheral clocks before entering HIBERNATE.
- B. IDLE instruction is executed to put the device into HIBERNATE mode.
- C. The device is now in HIBERNATE mode. If configured, I/O isolation is turned on, M0 and M1 memories are retained. CPU1 is powered down. Digital peripherals are powered down. The oscillators, PLLs, analog peripherals, and Flash are in their software-controlled Low-Power modes. Dx, LSx, and GSx memories are also powered down, and their memory contents lost.
- D. A falling edge on the GPIOHIBWAKE pin will drive the wakeup of the devices clock sources INTOSC1, INTOSC2, and X1/X2 OSC. The wakeup source must keep the GPIOHIBWAKE pin low long enough to ensure full power-up of these clock sources.
- E. After the clock sources are powered up, the GPIOHIBWAKE pin must be driven high to trigger the wakeup sequence of the remainder of the device.
- F. The BootROM will then begin to execute. The BootROM can distinguish a HIBERNATE wakeup by reading the CPU1.REC.HIBRESETn bit. After the TI OTP trims are loaded, the BootROM code will branch to the user-defined IoRestore function if it has been configured.
- G. At this point, the device is out of HIBERNATE mode, and the application may continue.
- H. The IoRestore function is a user-defined function where the application may reconfigure GPIO states, disable I/O isolation, reconfigure the PLL, restore peripheral configurations, or branch to application code. This is up to the application requirements.
- I. If the application has not branched to application code, the BootROM will continue after completing IoRestore. It will disable I/O isolation automatically if it was not taken care of inside of IoRestore.
- J. BootROM will then boot as determined by the HIBBOOTMODE register. Refer to the ROM Code and Peripheral Booting chapter of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) for more information.

Figure 5-20. HIBERNATE Entry and Exit Timing Diagram

NOTE

1. If the IORESTOREADDR is configured as the default value, the BootROM will continue its execution to boot as determined by the HIBBOOTMODE register. Refer to the ROM Code and Peripheral Booting chapter of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) for more information.
2. The user may choose to disable I/O Isolation at any point in the IoRestore function. Regardless if the user has disabled Isolation in the IoRestore function or if IoRestore is not defined, the BootROM will automatically disable isolation before booting as determined by the HIBBOOTMODE register.

5.9.9 External Memory Interface (EMIF)

The EMIF provides a means of connecting the CPU to various external storage devices like asynchronous memories (SRAM, NOR flash) or synchronous memory (SDRAM).

5.9.9.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects (EMIF_CS[4:2]). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable time-out
- Select strobe option

5.9.9.2 Synchronous DRAM Support

The EMIF memory controller is compliant with the JESD21-C SDR SDRAMs that use a 32-bit or 16-bit data bus. The EMIF has a single SDRAM chip select (EMIF_CS[0]).

The address space of the EMIF, for the synchronous memory (SDRAM), lies beyond the 22-bit range of the program address bus and can only be accessed through the data bus, which places a restriction on the C compiler being able to work effectively on data in this space. Therefore, when using SDRAM, the user is advised to copy data (using the DMA) from external memory to RAM before working on it. See the examples in C2000Ware ([C2000Ware for C2000 MCUs](#)) and the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with 8-, 9-, 10-, and 11-column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents because the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. The EMIF module does not support mobile SDRAM devices.

On this device, the EMIF does not support burst access for SDRAM configurations. This means every access to an external SDRAM device will have CAS latency.

5.9.9.3 EMIF Electrical Data and Timing

5.9.9.3.1 Asynchronous RAM

Table 5-37 shows the EMIF asynchronous memory timing requirements. Table 5-38 shows the EMIF asynchronous memory switching characteristics. Figure 5-21 through Figure 5-24 show the EMIF asynchronous memory timing diagrams.

Table 5-37. EMIF Asynchronous Memory Timing Requirements⁽¹⁾

| NO. | | | MIN | MAX | UNIT |
|-------------------------|------------------------|--|-----------------|-----|------|
| Reads and Writes | | | | | |
| | E | EMIF clock period | $t_{c(SYSCLK)}$ | | ns |
| 2 | $t_{w(EM_WAIT)}$ | Pulse duration, EMxWAIT assertion and deassertion | 2E | | ns |
| Reads | | | | | |
| 12 | $t_{su(EMDV-EMOEH)}$ | Setup time, EMxD[y:0] valid before \overline{EMxOE} high | 15 | | ns |
| 13 | $t_{h(EMOEH-EMDIV)}$ | Hold time, EMxD[y:0] valid after \overline{EMxOE} high | 0 | | ns |
| 14 | $t_{su(EMOEL-EMWAIT)}$ | Setup Time, EMxWAIT asserted before end of Strobe Phase ⁽²⁾ | 4E+20 | | ns |
| Writes | | | | | |
| 28 | $t_{su(EMWEL-EMWAIT)}$ | Setup Time, EMxWAIT asserted before end of Strobe Phase ⁽²⁾ | 4E+20 | | ns |

(1) E = EMxCLK period in ns.

(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMxWAIT must be asserted to add extended wait states. Figure 5-22 and Figure 5-24 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-38. EMIF Asynchronous Memory Switching Characteristics⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-------------------------|-----------------------|--|--------------------------------|--------------------------------|------|
| Reads and Writes | | | | | |
| 1 | $t_{d(TURNAROUND)}$ | Turn around time | (TA)*E-3 | (TA)*E+2 | ns |
| Reads | | | | | |
| 3 | $t_{c(EMRCYCLE)}$ | EMIF read cycle time (EW = 0) | (RS+RST+RH+2)*E-3 | (RS+RST+RH+2)*E+2 | ns |
| | | EMIF read cycle time (EW = 1) | (RS+RST+RH+2+ (EWC*16))*E-3 | (RS+RST+RH+2+ (EWC*16))*E+2 | ns |
| 4 | $t_{su(EMCEL-EMOEL)}$ | Output setup time, $\overline{EMxCS}[y:2]$ low to \overline{EMxOE} low (SS = 0) | (RS)*E-3 | (RS)*E+2 | ns |
| | | Output setup time, $\overline{EMxCS}[y:2]$ low to \overline{EMxOE} low (SS = 1) | -3 | 2 | ns |
| 5 | $t_{h(EMOEH-EMCEH)}$ | Output hold time, \overline{EMxOE} high to $\overline{EMxCS}[y:2]$ high (SS = 0) | (RH)*E-3 | (RH)*E | ns |
| | | Output hold time, \overline{EMxOE} high to $\overline{EMxCS}[y:2]$ high (SS = 1) | -3 | 0 | ns |
| 6 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, EMxBA[y:0] valid to \overline{EMxOE} low | (RS)*E-3 | (RS)*E+2 | ns |
| 7 | $t_{h(EMOEH-EMBAIV)}$ | Output hold time, \overline{EMxOE} high to EMxBA[y:0] invalid | (RH)*E-3 | (RH)*E | ns |

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed through the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4-1], RS[16-1], RST[64-4], RH[8-1], WS[16-1], WST[64-1], WH[8-1], and MEWC[1-256]. See the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) for more information.

(2) E = EMxCLK period in ns.

(3) EWC = external wait cycles determined by EMxWAIT input signal. EWC supports the following range of values. EWC[256-1]. The maximum wait time before time-out is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) for more information.

Table 5-38. EMIF Asynchronous Memory Switching Characteristics⁽¹⁾⁽²⁾⁽³⁾ (continued)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---------------|------------------------|--|------------------------------|------------------------------|------|
| 8 | $t_{su}(EMAV-EMOEL)$ | Output setup time, $\overline{EMxA}[y:0]$ valid to \overline{EMxOE} low | $(RS)*E-3$ | $(RS)*E+2$ | ns |
| 9 | $t_h(EMOEH-EMAIV)$ | Output hold time, \overline{EMxOE} high to $\overline{EMxA}[y:0]$ invalid | $(RH)*E-3$ | $(RH)*E$ | ns |
| 10 | $t_w(EMOEL)$ | \overline{EMxOE} active low width (EW = 0) | $(RST)*E-1$ | $(RST)*E+1$ | ns |
| | | \overline{EMxOE} active low width (EW = 1) | $(RST+(EWC*16))*E-1$ | $(RST+(EWC*16))*E+1$ | ns |
| 11 | $t_d(EMWAITH-EMOEH)$ | Delay time from $\overline{EMxWAIT}$ deasserted to \overline{EMxOE} high | 4E+10 | 5E+15 | ns |
| 29 | $t_{su}(EMDQMV-EMOEL)$ | Output setup time, $\overline{EMxDQM}[y:0]$ valid to \overline{EMxOE} low | $(RS)*E-3$ | $(RS)*E+2$ | ns |
| 30 | $t_h(EMOEH-EMDQMIV)$ | Output hold time, \overline{EMxOE} high to $\overline{EMxDQM}[y:0]$ invalid | $(RH)*E-3$ | $(RH)*E$ | ns |
| Writes | | | | | |
| 15 | $t_c(EMWCYCLE)$ | EMIF write cycle time (EW = 0) | $(WS+WST+WH+2)*E-3$ | $(WS+WST+WH+2)*E+1$ | ns |
| | | EMIF write cycle time (EW = 1) | $(WS+WST+WH+2+(EWC*16))*E-3$ | $(WS+WST+WH+2+(EWC*16))*E+1$ | ns |
| 16 | $t_{su}(EMCEL-EMWEL)$ | Output setup time, $\overline{EMxCS}[y:2]$ low to \overline{EMxWE} low (SS = 0) | $(WS)*E-3$ | $(WS)*E+1$ | ns |
| | | Output setup time, $\overline{EMxCS}[y:2]$ low to \overline{EMxWE} low (SS = 1) | -3 | 1 | ns |
| 17 | $t_h(EMWEH-EMCEH)$ | Output hold time, \overline{EMxWE} high to $\overline{EMxCS}[y:2]$ high (SS = 0) | $(WH)*E-3$ | $(WH)*E$ | ns |
| | | Output hold time, \overline{EMxWE} high to $\overline{EMxCS}[y:2]$ high (SS = 1) | -3 | 0 | ns |
| 18 | $t_{su}(EMDQMV-EMWEL)$ | Output setup time, $\overline{EMxDQM}[y:0]$ valid to \overline{EMxWE} low | $(WS)*E-3$ | $(WS)*E+1$ | ns |
| 19 | $t_h(EMWEH-EMDQMIV)$ | Output hold time, \overline{EMxWE} high to $\overline{EMxDQM}[y:0]$ invalid | $(WH)*E-3$ | $(WH)*E$ | ns |
| 20 | $t_{su}(EMBAV-EMWEL)$ | Output setup time, $\overline{EMxBA}[y:0]$ valid to \overline{EMxWE} low | $(WS)*E-3$ | $(WS)*E+1$ | ns |
| 21 | $t_h(EMWEH-EMBAIV)$ | Output hold time, \overline{EMxWE} high to $\overline{EMxBA}[y:0]$ invalid | $(WH)*E-3$ | $(WH)*E$ | ns |
| 22 | $t_{su}(EMAV-EMWEL)$ | Output setup time, $\overline{EMxA}[y:0]$ valid to \overline{EMxWE} low | $(WS)*E-3$ | $(WS)*E+1$ | ns |
| 23 | $t_h(EMWEH-EMAIV)$ | Output hold time, \overline{EMxWE} high to $\overline{EMxA}[y:0]$ invalid | $(WH)*E-3$ | $(WH)*E$ | ns |
| 24 | $t_w(EMWEL)$ | \overline{EMxWE} active low width (EW = 0) | $(WST)*E-1$ | $(WST)*E+1$ | ns |
| | | \overline{EMxWE} active low width (EW = 1) | $(WST+(EWC*16))*E-1$ | $(WST+(EWC*16))*E+1$ | ns |
| 25 | $t_d(EMWAITH-EMWEH)$ | Delay time from $\overline{EMxWAIT}$ deasserted to \overline{EMxWE} high | 4E+10 | 5E+15 | ns |
| 26 | $t_{su}(EMDV-EMWEL)$ | Output setup time, $\overline{EMxD}[y:0]$ valid to \overline{EMxWE} low | $(WS)*E-3$ | $(WS)*E+1$ | ns |
| 27 | $t_h(EMWEH-EMDIV)$ | Output hold time, \overline{EMxWE} high to $\overline{EMxD}[y:0]$ invalid | $(WH)*E-3$ | $(WH)*E$ | ns |

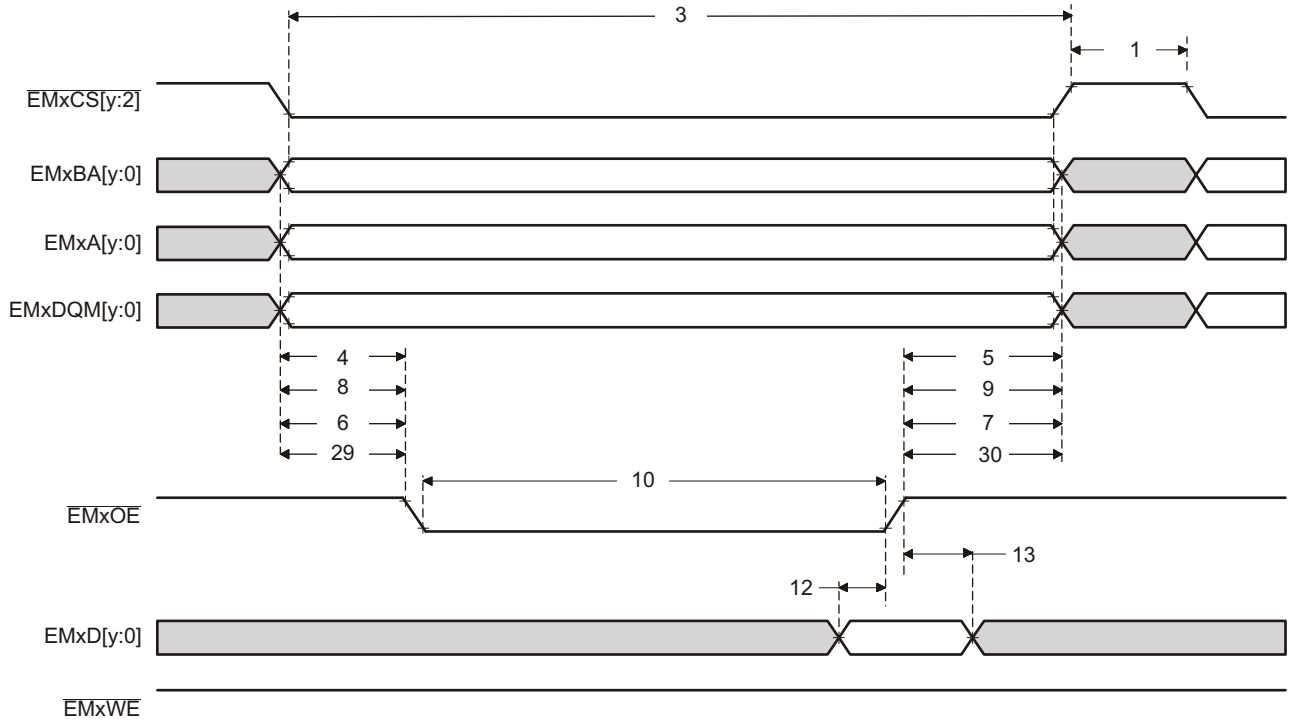


Figure 5-21. Asynchronous Memory Read Timing

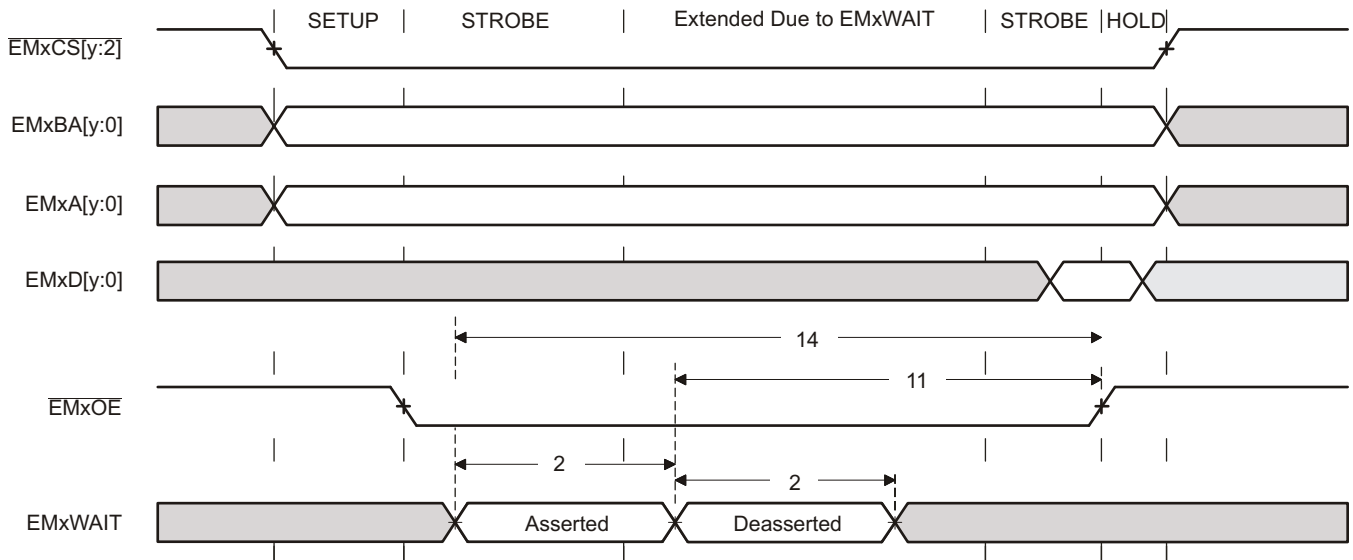


Figure 5-22. EMxWAIT Read Timing Requirements

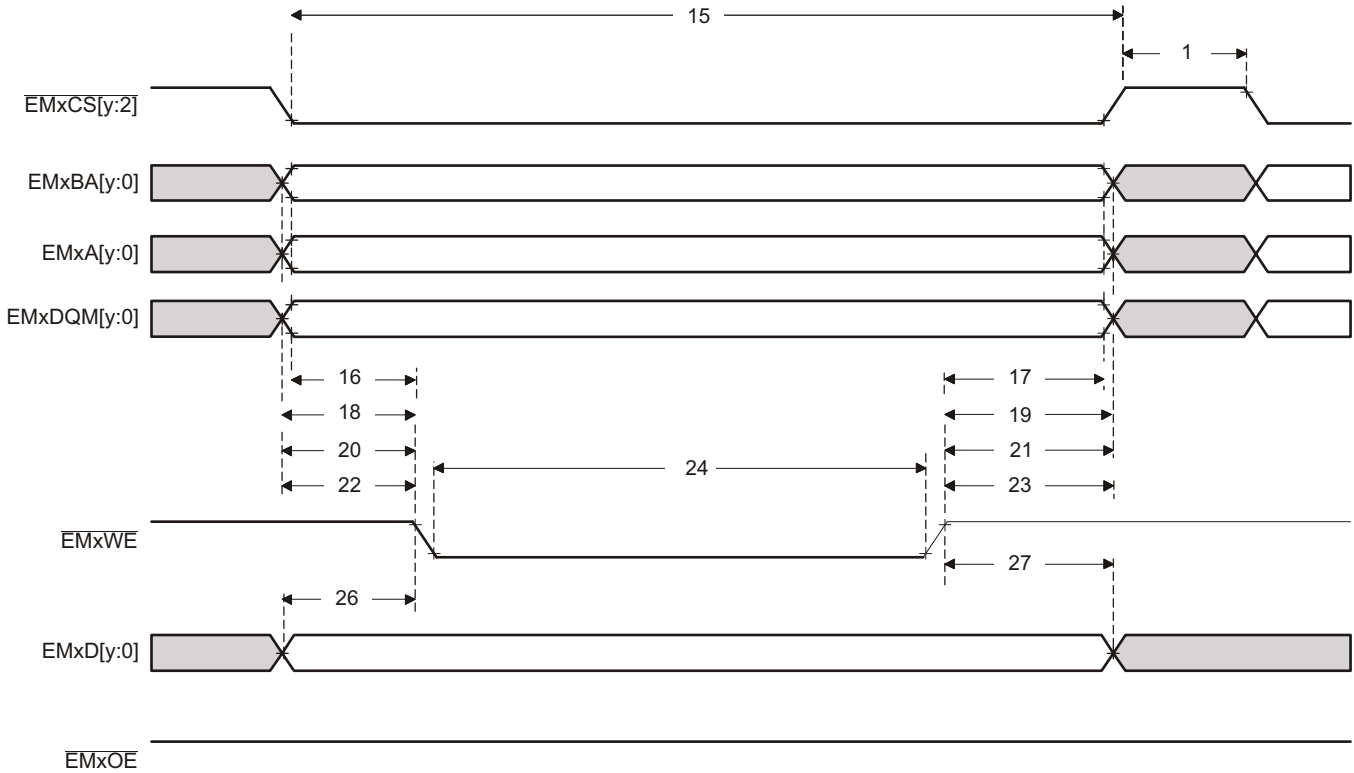


Figure 5-23. Asynchronous Memory Write Timing

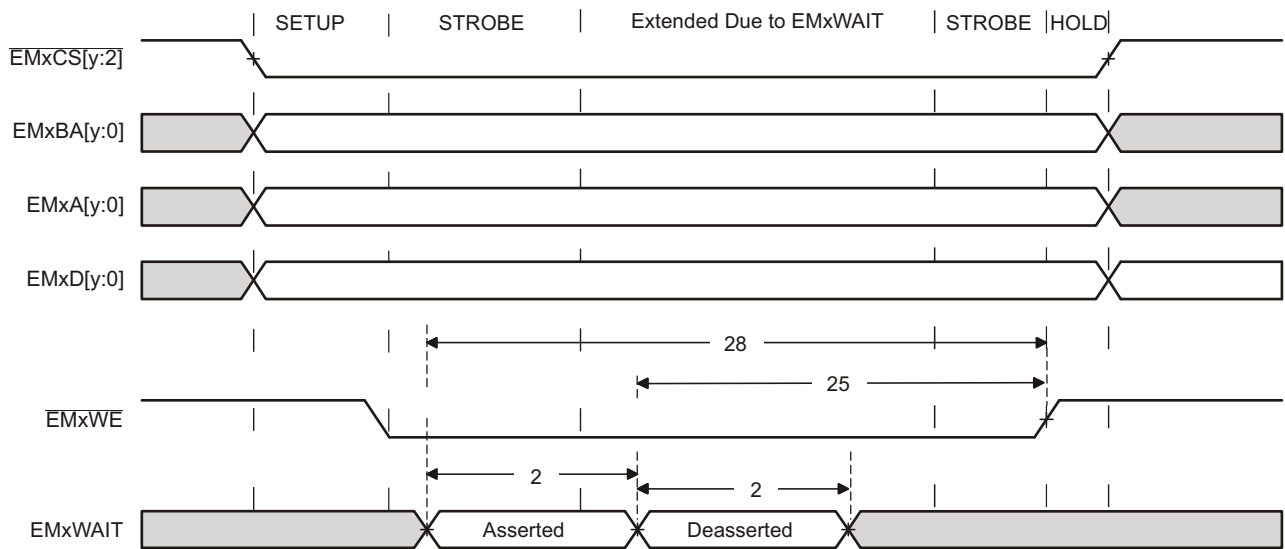


Figure 5-24. EMxWAIT Write Timing Requirements

5.9.9.3.2 Synchronous RAM

Table 5-39 shows the EMIF synchronous memory timing requirements. Table 5-40 shows the EMIF synchronous memory switching characteristics. Figure 5-25 and Figure 5-26 show the synchronous memory timing diagrams.

Table 5-39. EMIF Synchronous Memory Timing Requirements

| NO. | | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 19 | $t_{su}(EMIFDV-EM_CLKH)$ Input setup time, read data valid on EMxD[y:0] before EMxCLK rising | 2 | | ns |
| 20 | $t_h(CLKH-DIV)$ Input hold time, read data valid on EMxD[y:0] after EMxCLK rising | 1.5 | | ns |

Table 5-40. EMIF Synchronous Memory Switching Characteristics

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 1 | $t_c(CLK)$ Cycle time, EMIF clock EMxCLK | 10 | | ns |
| 2 | $t_w(CLK)$ Pulse width, EMIF clock EMxCLK high or low | 3 | | ns |
| 3 | $t_d(CLKH-CSV)$ Delay time, EMxCLK rising to $\overline{EMxCS}[y:2]$ valid | | 8 | ns |
| 4 | $t_{oh}(CLKH-CSIV)$ Output hold time, EMxCLK rising to $\overline{EMxCS}[y:2]$ invalid | 1 | | ns |
| 5 | $t_d(CLKH-DQMV)$ Delay time, EMxCLK rising to EMxDQM[y:0] valid | | 8 | ns |
| 6 | $t_{oh}(CLKH-DQMIV)$ Output hold time, EMxCLK rising to EMxDQM[y:0] invalid | 1 | | ns |
| 7 | $t_d(CLKH-AV)$ Delay time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] valid | | 8 | ns |
| 8 | $t_{oh}(CLKH-AIV)$ Output hold time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] invalid | 1 | | ns |
| 9 | $t_d(CLKH-DV)$ Delay time, EMxCLK rising to EMxD[y:0] valid | | 8 | ns |
| 10 | $t_{oh}(CLKH-DIV)$ Output hold time, EMxCLK rising to EMxD[y:0] invalid | 1 | | ns |
| 11 | $t_d(CLKH-RASV)$ Delay time, EMxCLK rising to EMxRAS valid | | 8 | ns |
| 12 | $t_{oh}(CLKH-RASIV)$ Output hold time, EMxCLK rising to EMxRAS invalid | 1 | | ns |
| 13 | $t_d(CLKH-CASV)$ Delay time, EMxCLK rising to EMxCAS valid | | 8 | ns |
| 14 | $t_{oh}(CLKH-CASIV)$ Output hold time, EMxCLK rising to EMxCAS invalid | 1 | | ns |
| 15 | $t_d(CLKH-WEV)$ Delay time, EMxCLK rising to \overline{EMxWE} valid | | 8 | ns |
| 16 | $t_{oh}(CLKH-WEIV)$ Output hold time, EMxCLK rising to \overline{EMxWE} invalid | 1 | | ns |
| 17 | $t_d(CLKH-DHZ)$ Delay time, EMxCLK rising to EMxD[y:0] tri-stated | | 8 | ns |
| 18 | $t_{oh}(CLKH-DLZ)$ Output hold time, EMxCLK rising to EMxD[y:0] driving | 1 | | ns |

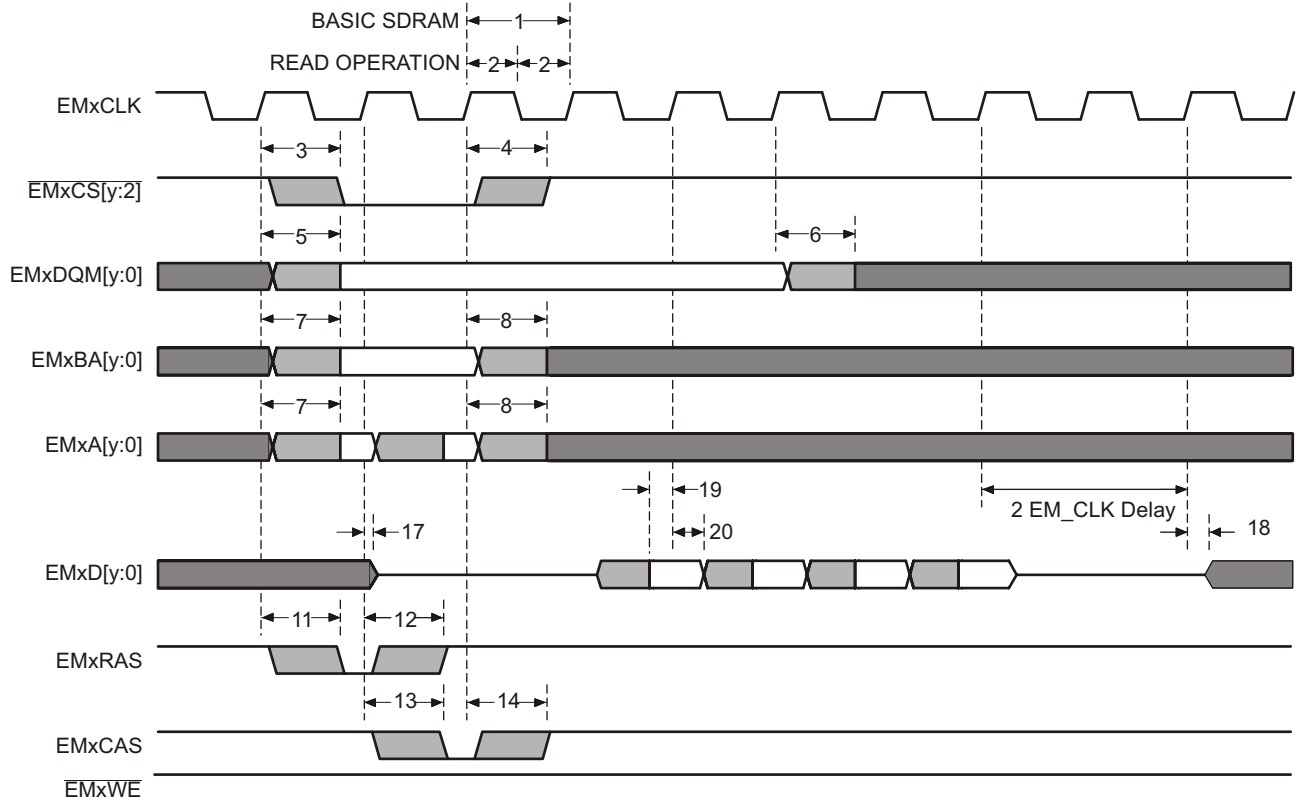


Figure 5-25. Basic SDRAM Read Operation

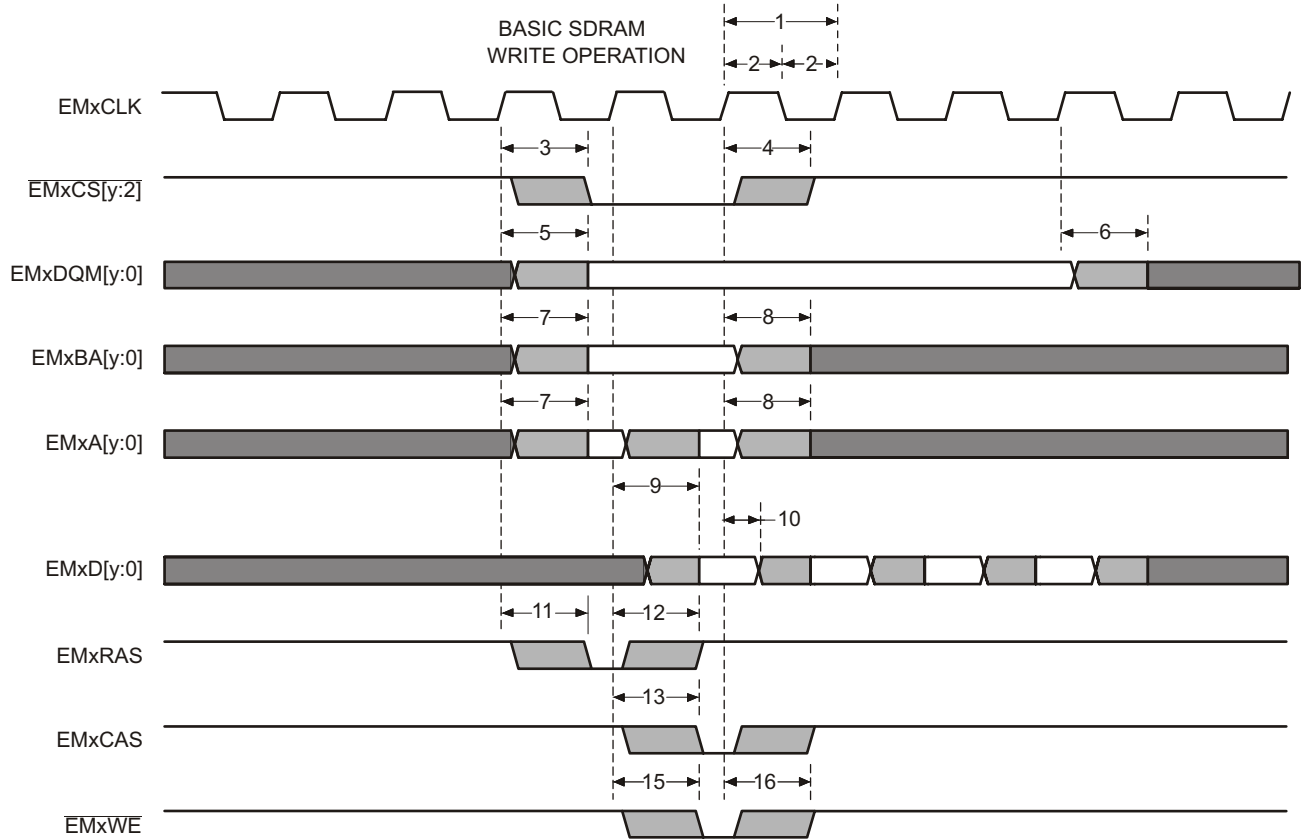


Figure 5-26. Basic SDRAM Write Operation

5.10 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the ADC, temperature sensor, buffered DAC, and CMPSS.

The analog subsystem has the following features:

- Flexible voltage references
 - The ADCs are referenced to V_{REFHIX} and V_{REFLOX} pins.
 - V_{REFHIX} pin voltage must be driven in externally.
- The buffered DACs are referenced to V_{REFHIX} and V_{REFLOX} .
 - Alternately, these DACs can be referenced to the VDAC pin and V_{SSA} .
- The comparator DACs are referenced to V_{DDA} and V_{SSA} .
 - Alternately, these DACs can be referenced to the VDAC pin and V_{SSA} .
- Flexible pin usage
 - Buffered DAC and comparator subsystem functions multiplexed with ADC inputs
- Internal connection to V_{REFLO} on all ADCs for offset self-calibration

[Figure 5-27](#) shows the Analog Subsystem Block Diagram for the 337-ball ZWT package. [Figure 5-28](#) shows the Analog Subsystem Block Diagram for the 176-pin PTP package. [Figure 5-29](#) shows the Analog Subsystem Block Diagram for the 100-pin PZP package.

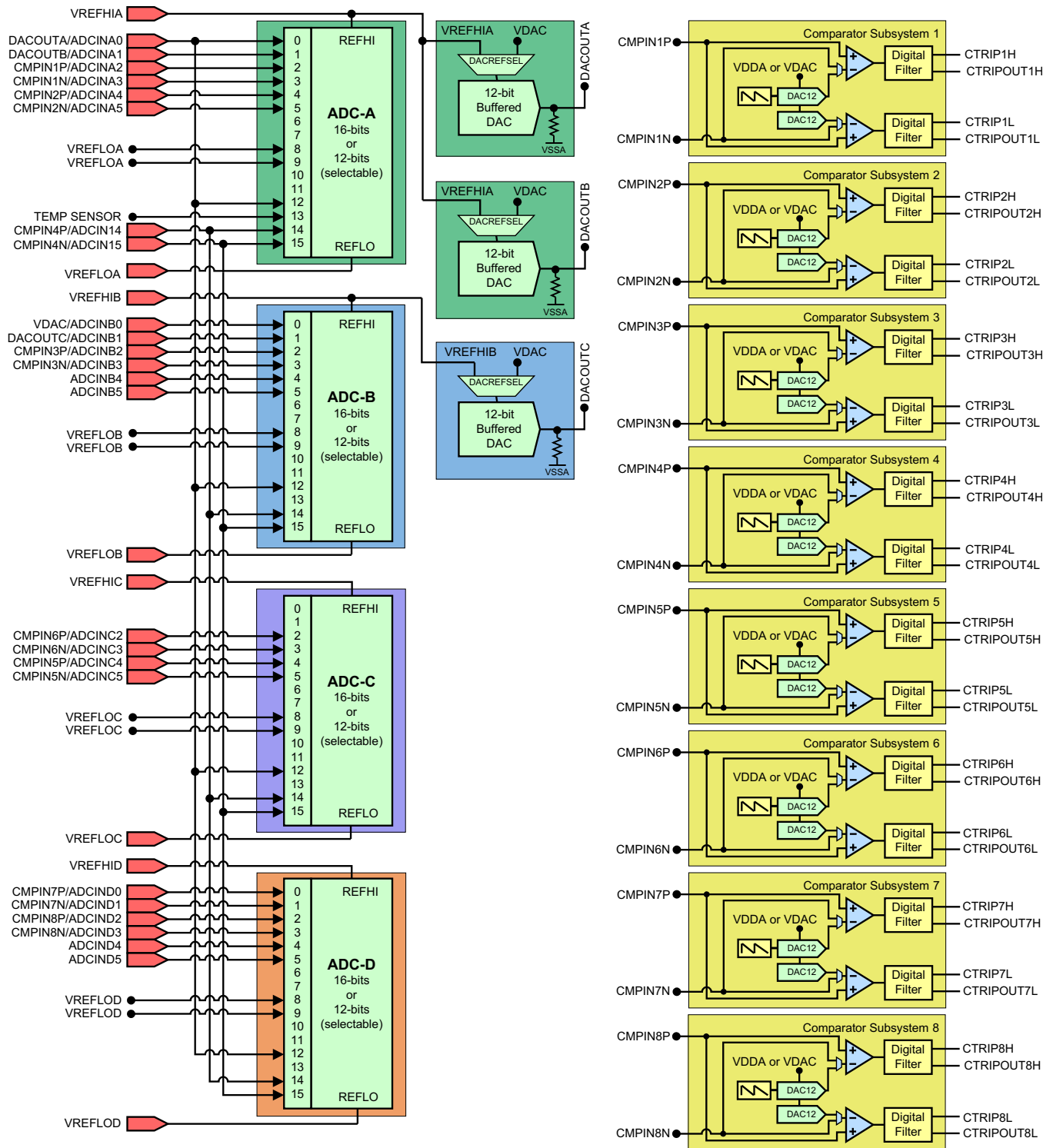


Figure 5-27. Analog Subsystem Block Diagram (337-Ball ZWT)

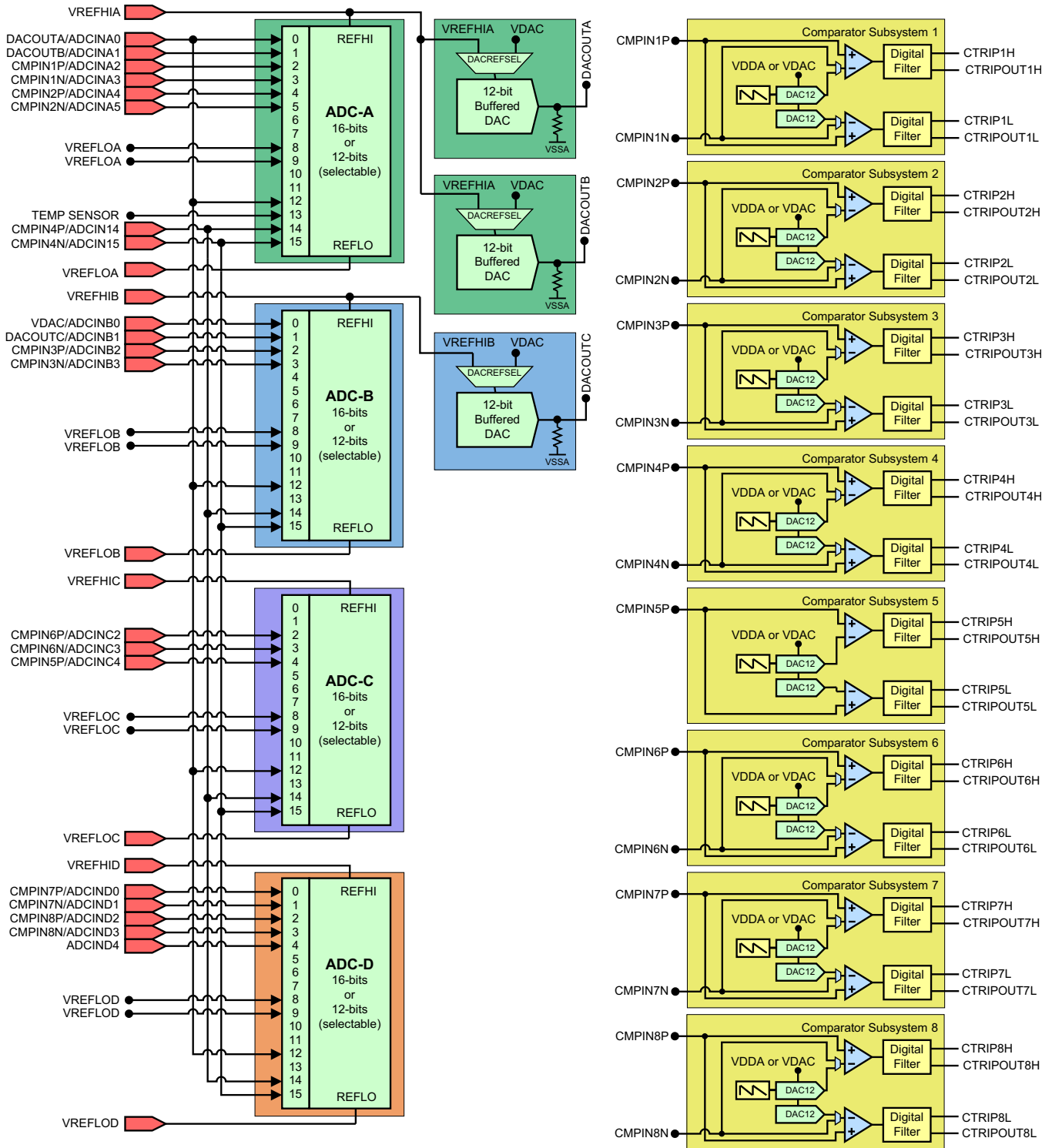


Figure 5-28. Analog Subsystem Block Diagram (176-Pin PTP)

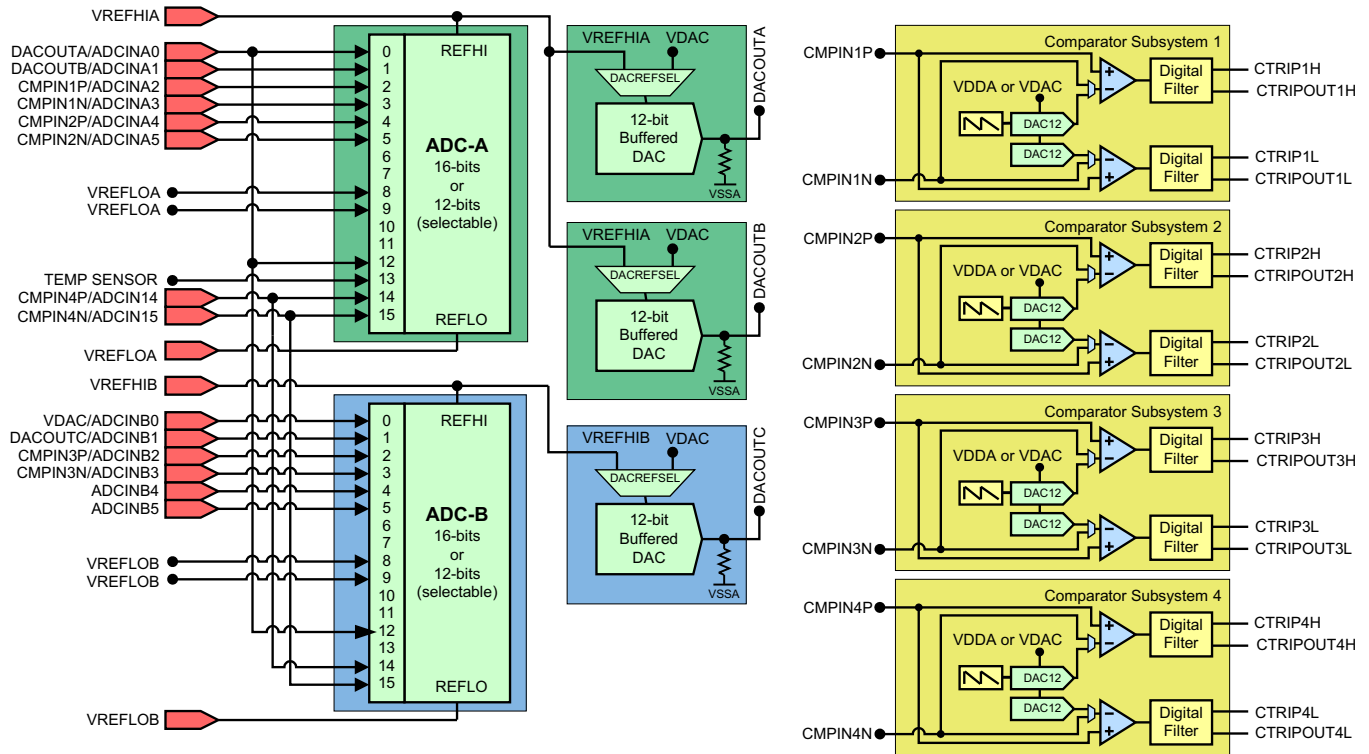


Figure 5-29. Analog Subsystem Block Diagram (100-Pin PZP)

5.10.1 Analog-to-Digital Converter (ADC)

The ADCs on this device are successive approximation (SAR) style ADCs with selectable resolution of either 16 bits or 12 bits. There are multiple ADC modules which allow simultaneous sampling. The ADC wrapper is start-of-conversion (SOC) based [see the SOC Principle of Operation section of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#)].

Each ADC has the following features:

- Selectable resolution of 16 bits or 12 bits
- Ratiometric external reference set by V_{REFHI} and V_{REFLO}
- Differential signal conversions (16-bit mode only)
- Single-ended signal conversions (12-bit mode only)
- Input multiplexer with up to 16 channels (single-ended) or 8 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
 - Software immediate start
 - All ePWMs
 - GPIO XINT2
 - CPU timers
 - ADCINT1 or 2
- Four flexible PIE interrupts
- Burst mode
- Four post-processing blocks, each with:
 - Saturating offset calibration
 - Error from setpoint calculation
 - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
 - Trigger-to-sample delay capture

Figure 5-30 shows the ADC module block diagram.

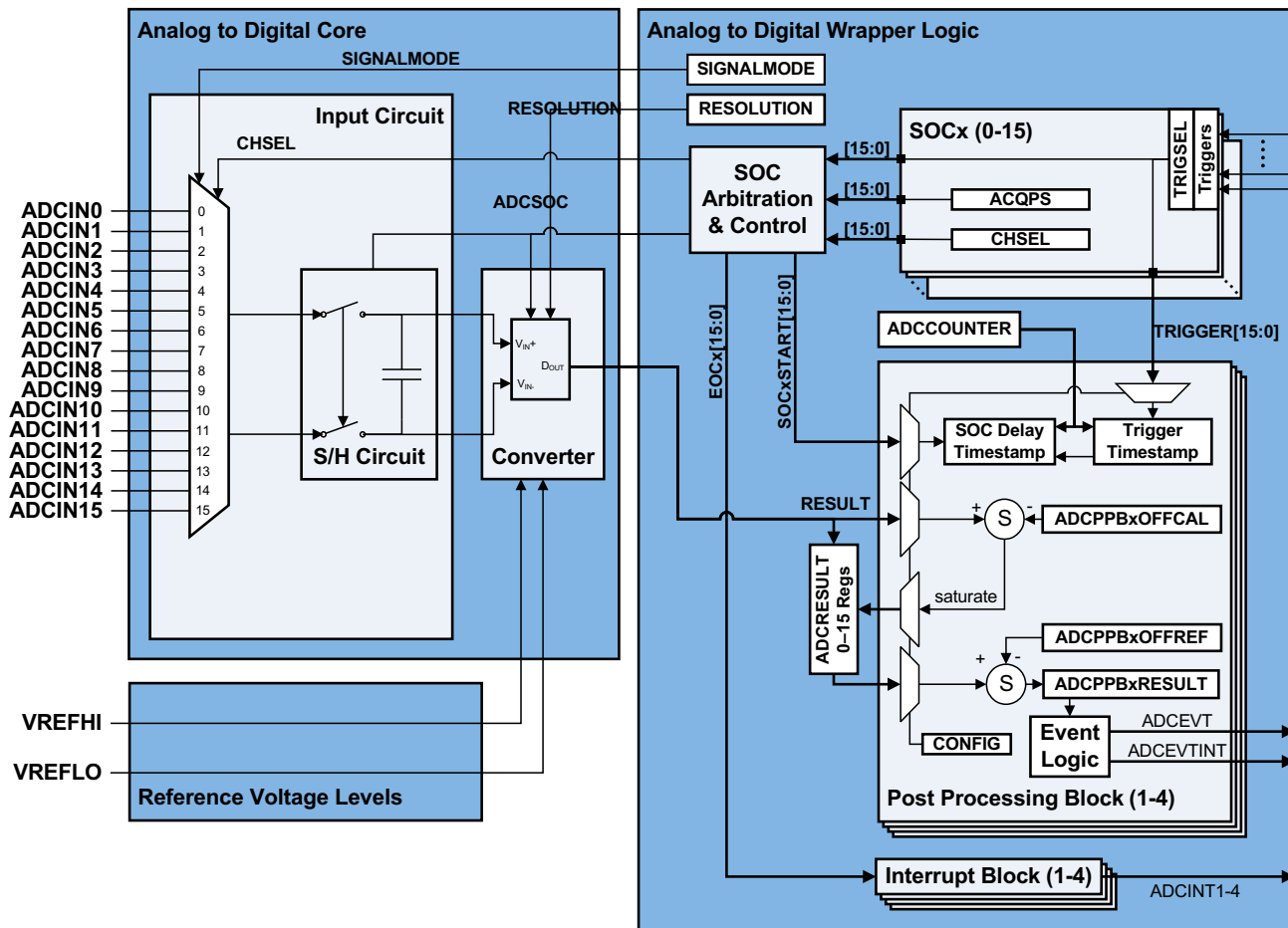


Figure 5-30. ADC Module Block Diagram

5.10.1.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCx, while others are controlled by each ADC module. Table 5-41 summarizes the basic ADC options and their level of configurability.

Table 5-41. ADC Options and Configuration Levels

| OPTIONS | CONFIGURABILITY |
|-----------------------------|--|
| Clock | By the module ⁽¹⁾ |
| Resolution | By the module ⁽¹⁾ |
| Signal mode | By the module |
| Reference voltage source | Not configurable (external reference only) |
| Trigger source | By the SOC ⁽¹⁾ |
| Converted channel | By the SOC |
| Acquisition window duration | By the SOC ⁽¹⁾ |
| EOC location | By the module |
| Burst mode | By the module ⁽¹⁾ |

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

5.10.1.1.1 Signal Mode

The ADC supports two signal modes: single-ended and differential. In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO. In differential signaling mode, the input voltage to the converter is sampled through a pair of input pins, one of which is the positive input (ADCINxP) and the other is the negative input (ADCINxN). The actual input voltage is the difference between the two (ADCINxP – ADCINxN). [Figure 5-31](#) shows the differential signaling mode. [Figure 5-32](#) shows the single-ended signaling mode.

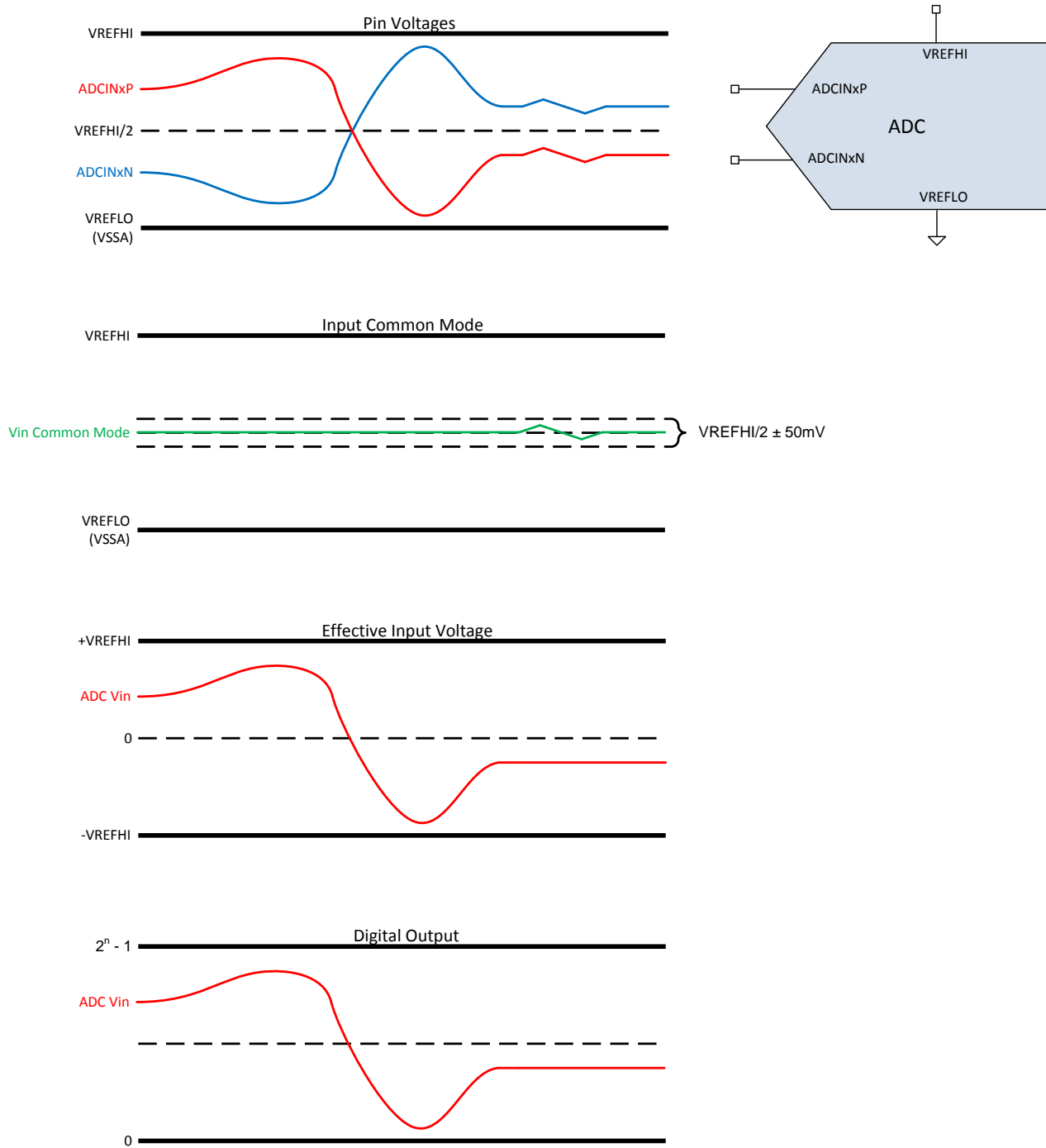


Figure 5-31. Differential Signaling Mode

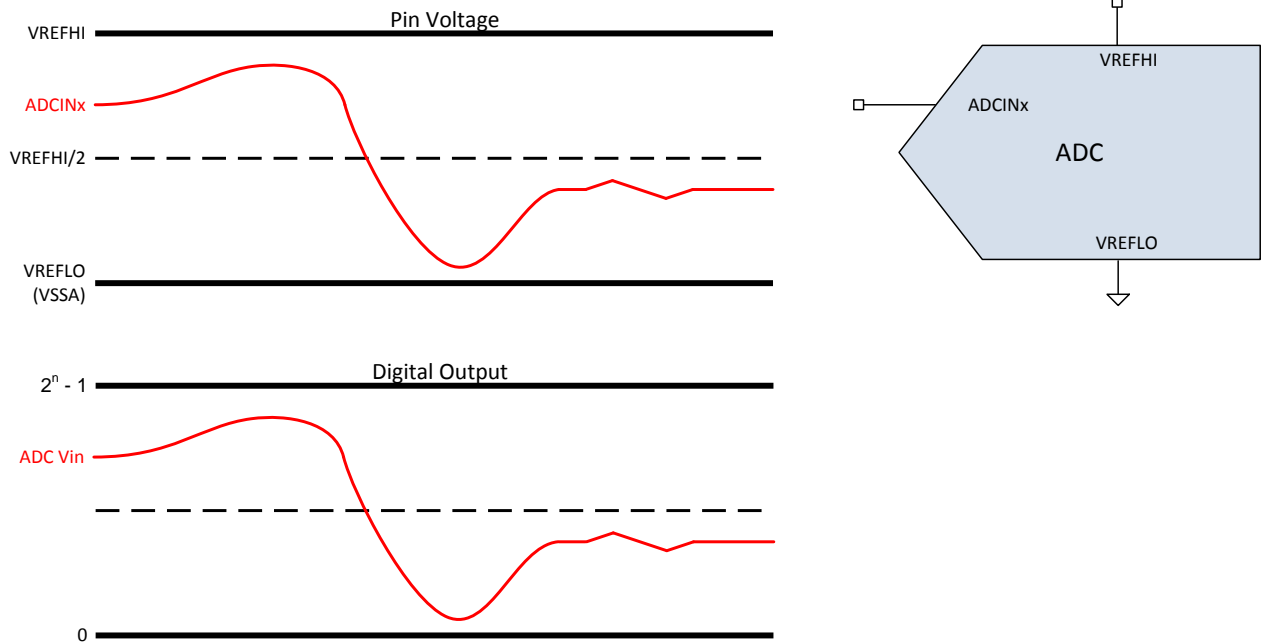


Figure 5-32. Single-ended Signaling Mode

5.10.1.2 ADC Electrical Data and Timing

Table 5-42 shows the ADC operating conditions for 16-bit differential mode. Table 5-43 shows the ADC characteristics for 16-bit differential mode. Table 5-44 shows the ADC operating conditions for 12-bit single-ended mode. Table 5-45 shows the ADC characteristics for 12-bit single-ended mode. Table 5-46 shows the ADCEXTSOC timing requirements.

Table 5-42. ADC Operating Conditions (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

| | MIN | TYP | MAX | UNIT |
|--|-------------------------|--------------------|-------------------------|------|
| ADCCLK (derived from PERx.SYSCLK) | 5 | | 50 | MHz |
| Sample window duration (set by ACQPS and PERx.SYSCLK) ⁽¹⁾ | 320 | | | ns |
| V _{REFHI} | 2.4 | 2.5 or 3.0 | V _{DDA} | V |
| V _{REFLO} | V _{SSA} | 0 | V _{SSA} | V |
| V _{REFHI} – V _{REFLO} | 2.4 | | V _{DDA} | V |
| ADC input conversion range | V _{REFLO} | | V _{REFHI} | V |
| ADC input signal common mode voltage ⁽²⁾⁽³⁾ | V _{REFCM} – 50 | V _{REFCM} | V _{REFCM} + 50 | mV |

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

(2) $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$

(3) The V_{REFCM} requirements will not be met if the negative ADC input pin is connected to V_{SSA} or V_{REFLO}.

NOTE

The ADC inputs should be kept below V_{DDA} + 0.3 V during operation. If an ADC input exceeds this level, the V_{REF} internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same V_{REF}.

Table 5-43. ADC Characteristics (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|---------------|-----|---------|
| ADC conversion cycles ⁽²⁾ | | 29.6 | | 31 | ADCCLKs |
| Power-up time (after setting ADCPWDNZ to first conversion) | | | | 500 | μs |
| Gain error | | -64 | ±9 | 64 | LSBs |
| Offset error ⁽³⁾ | | -16 | ±9 | 16 | LSBs |
| Channel-to-channel gain error | | | ±6 | | LSBs |
| Channel-to-channel offset error | | | ±3 | | LSBs |
| ADC-to-ADC gain error | Identical V _{REFHI} and V _{REFLO} for all ADCs | | ±6 | | LSBs |
| ADC-to-ADC offset error | Identical V _{REFHI} and V _{REFLO} for all ADCs | | ±3 | | LSBs |
| DNL ⁽⁴⁾ | | > -1 | ±0.5 | 1 | LSBs |
| INL | | -3 | ±1.5 | 3 | LSBs |
| SNR ⁽⁵⁾⁽⁶⁾ | V _{REFHI} = 2.5 V, f _{in} = 10 kHz | | 87.6 | | dB |
| THD ⁽⁵⁾⁽⁶⁾ | V _{REFHI} = 2.5 V, f _{in} = 10 kHz | | -93.5 | | dB |
| SFDR ⁽⁵⁾⁽⁶⁾ | V _{REFHI} = 2.5 V, f _{in} = 10 kHz | | 95.4 | | dB |
| SINAD ⁽⁵⁾⁽⁶⁾ | V _{REFHI} = 2.5 V, f _{in} = 10 kHz | | 86.6 | | dB |
| ENOB ⁽⁵⁾⁽⁶⁾ | V _{REFHI} = 2.5 V, f _{in} = 10 kHz, single ADC ⁽⁷⁾ | | 14.1 | | bits |
| | V _{REFHI} = 2.5 V, f _{in} = 10 kHz, synchronous ADCs ⁽⁸⁾ | | 14.1 | | |
| | V _{REFHI} = 2.5 V, f _{in} = 10 kHz, asynchronous ADCs ⁽⁹⁾ | | Not supported | | |
| PSRR | V _{DDA} = 3.3-V DC + 200 mV DC up to Sine at 1 kHz | | 77 | | dB |
| PSRR | V _{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz | | 74 | | dB |
| CMRR | DC to 1 MHz | | 60 | | dB |
| V _{REFHI} input current | | | 190 | | μA |
| ADC-to-ADC isolation ⁽⁶⁾⁽¹⁰⁾⁽¹¹⁾ | V _{REFHI} = 2.5 V, synchronous ADCs ⁽⁸⁾ | -2 | | 2 | LSBs |
| | V _{REFHI} = 2.5 V, asynchronous ADCs ⁽⁹⁾ | | Not supported | | |

- (1) Typical values are measured with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V.
- (2) See Section 5.10.1.2.2.
- (3) Difference from conversion result 32768 when ADCINp = ADCINn = V_{REFCM}.
- (4) No missing codes.
- (5) AC parameters will be impacted by clock source accuracy and jitter, this should be taken into account when selecting the clock source for the system. The clock source used for these parameters was a high-accuracy external clock fed through the PLL. The on-chip Internal Oscillator has higher jitter than an external crystal and these parameters will degrade if it is used as a clock source.
- (6) I/O activity is minimized on pins adjacent to ADC input and V_{REFHI} pins as part of best practices to reduce capacitive coupling and crosstalk.
- (7) One ADC operating while all other ADCs are idle.
- (8) All ADCs operating with identical ADCCLK, S+H durations, triggers, and resolution.
- (9) Any ADCs operating with heterogeneous ADCCLK, S+H durations, triggers, or resolution.
- (10) Maximum DC code deviation due to operation of multiple ADCs simultaneously.
- (11) Value based on characterization.

Table 5-44. ADC Operating Conditions (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)

| | MIN | TYP | MAX | UNIT |
|--|--------------------|------------|--------------------|------|
| ADCCLK (derived from PERx.SYSCLK) | 5 | | 50 | MHz |
| Sample window duration (set by ACQPS and PERx.SYSCLK) ⁽¹⁾ | 75 | | | ns |
| V _{REFHI} | 2.4 | 2.5 or 3.0 | V _{DDA} | V |
| V _{REFLO} | V _{SSA} | 0 | V _{SSA} | V |
| V _{REFHI} – V _{REFLO} | 2.4 | | V _{DDA} | V |
| ADC input conversion range | V _{REFLO} | | V _{REFHI} | V |

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

NOTE

The ADC inputs should be kept below $V_{DDA} + 0.3$ V during operation. If an ADC input exceeds this level, the V_{REF} internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same V_{REF} .

Table 5-45. ADC Characteristics (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|---------------|-----|---------|
| ADC conversion cycles ⁽²⁾ | | 10.1 | | 11 | ADCCLKs |
| Power-up time | | | | 500 | μs |
| Gain error | | -5 | ±3 | 5 | LSBs |
| Offset error | | -4 | ±2 | 4 | LSBs |
| Channel-to-channel gain error | | | ±4 | | LSBs |
| Channel-to-channel offset error | | | ±2 | | LSBs |
| ADC-to-ADC gain error | Identical V _{REFHI} and V _{REFLO} for all ADCs | | ±4 | | LSBs |
| ADC-to-ADC offset error | Identical V _{REFHI} and V _{REFLO} for all ADCs | | ±2 | | LSBs |
| DNL ⁽³⁾ | | > -1 | ±0.5 | 1 | LSBs |
| INL | | -2 | ±1.0 | 2 | LSBs |
| SNR ⁽⁴⁾⁽⁵⁾ | V _{REFHI} = 2.5 V, f _{in} = 100 kHz | | 68.8 | | dB |
| THD ⁽⁴⁾⁽⁵⁾ | V _{REFHI} = 2.5 V, f _{in} = 100 kHz | | -78.4 | | dB |
| SFDR ⁽⁴⁾⁽⁵⁾ | V _{REFHI} = 2.5 V, f _{in} = 100 kHz | | 79.2 | | dB |
| SINAD ⁽⁴⁾⁽⁵⁾ | V _{REFHI} = 2.5 V, f _{in} = 100 kHz | | 68.4 | | dB |
| ENOB ⁽⁴⁾⁽⁵⁾ | V _{REFHI} = 2.5 V, f _{in} = 100 kHz, single ADC ⁽⁶⁾ , all packages | | 11.1 | | bits |
| | V _{REFHI} = 2.5 V, f _{in} = 100 kHz, synchronous ADCs ⁽⁷⁾ , all packages | | 11.1 | | |
| | V _{REFHI} = 2.5 V, f _{in} = 100 kHz, asynchronous ADCs ⁽⁸⁾ , 100-pin PZP package | | Not supported | | |
| | V _{REFHI} = 2.5 V, f _{in} = 100 kHz, asynchronous ADCs ⁽⁸⁾ , 176-pin PTP package | | 9.7 | | |
| | V _{REFHI} = 2.5 V, f _{in} = 100 kHz, asynchronous ADCs ⁽⁸⁾ , 337-ball ZWT package | | 10.9 | | |
| PSRR | V _{DDA} = 3.3-V DC + 200 mV DC up to Sine at 1 kHz | | 60 | | dB |
| PSRR | V _{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz | | 57 | | dB |
| ADC-to-ADC isolation ⁽⁵⁾⁽⁹⁾⁽¹⁰⁾ | V _{REFHI} = 2.5 V, synchronous ADCs ⁽⁷⁾ , all packages | -1 | | 1 | LSBs |
| | V _{REFHI} = 2.5 V, asynchronous ADCs ⁽⁸⁾ , 100-pin PZP package | | Not supported | | |
| | V _{REFHI} = 2.5 V, asynchronous ADCs ⁽⁸⁾ , 176-pin PTP package | -9 | | 9 | |
| | V _{REFHI} = 2.5 V, asynchronous ADCs ⁽⁸⁾ , 337-ball ZWT package | -2 | | 2 | |
| V _{REFHI} input current | | | 130 | | μA |

- (1) Typical values are measured with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V.
- (2) See Section 5.10.1.2.2.
- (3) No missing codes.
- (4) AC parameters will be impacted by clock source accuracy and jitter, this should be taken into account when selecting the clock source for the system. The clock source used for these parameters was a high-accuracy external clock fed through the PLL. The on-chip Internal Oscillator has higher jitter than an external crystal and these parameters will degrade if it is used as a clock source.
- (5) I/O activity is minimized on pins adjacent to ADC input and V_{REFHI} pins as part of best practices to reduce capacitive coupling and crosstalk.
- (6) One ADC operating while all other ADCs are idle.
- (7) All ADCs operating with identical ADCCLK, S+H durations, triggers, and resolution.
- (8) Any ADCs operating with heterogeneous ADCCLK, S+H durations, triggers, or resolution.
- (9) Maximum DC code deviation due to operation of multiple ADCs simultaneously.
- (10) Value based on characterization.

Table 5-46. ADCEXTSOC Timing Requirements⁽¹⁾

| | | | MIN | MAX | UNIT |
|--------------|------------------------------------|----------------|---|-----|--------|
| $t_{w(INT)}$ | Pulse duration, INT input low/high | Synchronous | $2t_{c(SYSCCLK)}$ | | cycles |
| | | With qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCCLK)}$ | | cycles |

(1) For an explanation of the input qualifier parameters, see [Table 5-24](#).

5.10.1.2.1 ADC Input Models

NOTE

ADC channels ADCINA0, ADCINA1, and ADCINB1 have a 50-kΩ pulldown resistor to V_{SSA} .

For differential operation, the ADC input characteristics are given by [Table 5-47](#) and [Figure 5-33](#).

Table 5-47. Differential Input Model Parameters

| | DESCRIPTION | VALUE (16-BIT MODE) |
|----------|-----------------------------|--------------------------------|
| C_p | Parasitic input capacitance | See Table 5-49 |
| R_{on} | Sampling switch resistance | 700 Ω |
| C_h | Sampling capacitor | 16.5 pF |
| R_s | Nominal source impedance | 50 Ω |

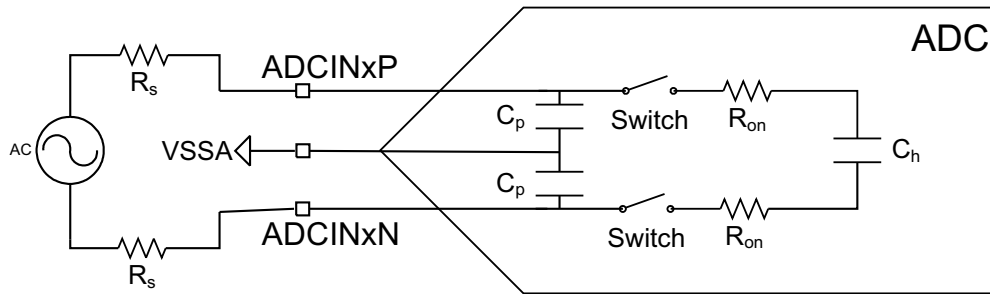


Figure 5-33. Differential Input Model

For single-ended operation, the ADC input characteristics are given by [Table 5-48](#) and [Figure 5-34](#).

Table 5-48. Single-Ended Input Model Parameters

| | DESCRIPTION | VALUE (12-BIT MODE) |
|----------|-----------------------------|--------------------------------|
| C_p | Parasitic input capacitance | See Table 5-49 |
| R_{on} | Sampling switch resistance | 425 Ω |
| C_h | Sampling capacitor | 14.5 pF |
| R_s | Nominal source impedance | 50 Ω |

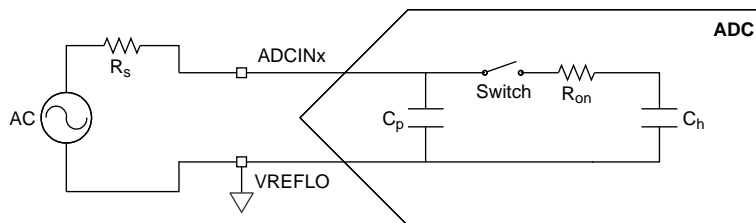


Figure 5-34. Single-Ended Input Model

Table 5-49 shows the parasitic capacitance on each channel. Also, enabling a comparator adds approximately 1.4 pF of capacitance on positive comparator inputs and 2.5 pF of capacitance on negative comparator inputs.

Table 5-49. Per-Channel Parasitic Capacitance

| ADC CHANNEL | C _p (pF) | |
|------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| ADCINA0 | 12.9 | N/A |
| ADCINA1 | 10.3 | N/A |
| ADCINA2 | 5.9 | 7.3 |
| ADCINA3 | 6.3 | 8.8 |
| ADCINA4 | 5.9 | 7.3 |
| ADCINA5 | 6.3 | 8.8 |
| ADCINB0 ⁽¹⁾ | 117.0 | N/A |
| ADCINB1 | 10.6 | N/A |
| ADCINB2 | 5.9 | 7.3 |
| ADCINB3 | 6.2 | 8.7 |
| ADCINB4 | 5.2 | N/A |
| ADCINB5 | 5.1 | N/A |
| ADCINC2 | 5.5 | 6.9 |
| ADCINC3 | 5.8 | 8.3 |
| ADCINC4 | 5.0 | 6.4 |
| ADCINC5 | 5.3 | 7.8 |
| ADCIND0 | 5.3 | 6.7 |
| ADCIND1 | 5.7 | 8.2 |
| ADCIND2 | 5.3 | 6.7 |
| ADCIND3 | 5.6 | 8.1 |
| ADCIND4 | 4.3 | N/A |
| ADCIND5 | 4.3 | N/A |
| ADCIN14 | 8.6 | 10.0 |
| ADCIN15 | 9.0 | 11.5 |

(1) The increased capacitance is due to VDAC functionality.

These input models should be used along with actual signal source impedance to determine the acquisition window duration. See the Choosing an Acquisition Window Duration section of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) for more information.

The user should analyze the ADC input setting assuming worst-case initial conditions on C_h. This will require assuming that C_h could start the S+H window completely charged to V_{REFHI} or completely discharged to V_{REFLO}. When the ADC transitions from an odd-numbered channel to an even-numbered channel, or vice-versa, the actual initial voltage on C_h will be close to being completely discharged to V_{REFLO}. For even-to-even or odd-to-odd channel transitions, the initial voltage on C_h will be close to the voltage of the previously converted channel.

5.10.1.2.2 ADC Timing Diagrams

Table 5-51 lists the ADC timings in 12-bit mode (SYSCLK cycles). Table 5-52 lists the ADC timings in 16-bit mode. Figure 5-35 and Figure 5-36 show the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 5-50 lists the descriptions of the ADC timing parameters that are in Figure 5-35 and Figure 5-36.

Table 5-50. ADC Timing Parameters

| PARAMETER | DESCRIPTION |
|-----------|--|
| t_{SH} | <p>The duration of the S+H window.</p> <p>At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by $(ACQPS + 1)$ SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} will not necessarily be the same for different SOCs.</p> <p>Note: The value on the S+H capacitor will be captured approximately 5 ns before the end of the S+H window regardless of device clock settings.</p> |
| t_{LAT} | <p>The time from the end of the S+H window until the ADC conversion results latch in the ADCRESULTx register.</p> <p>If the ADCRESULTx register is read before this time, the previous conversion results will be returned.</p> |
| t_{EOC} | <p>The time from the end of the S+H window until the next ADC conversion S+H window can begin. The subsequent sample can start before the conversion results are latched.</p> |
| t_{INT} | <p>The time from the end of the S+H window until an ADCINT flag is set (if configured).</p> <p>If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} will coincide with the conversion results being latched into the result register.</p> <p>If the INTPULSEPOS bit is 0, t_{INT} will coincide with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to ensure the read occurs after the results latch (otherwise, the previous results will be read).</p> |

Table 5-51. ADC Timings in 12-Bit Mode (SYSCLK Cycles)

| ADCCLK PRESCALE | | SYSCLK CYCLES | | | | ADCCLK CYCLES | |
|--------------------|---------------------|---------------|-----------|------------------|-----------------|---------------|--|
| ADCCTL2 [PRESCALE] | RATIO ADCCLK:SYSCLK | t_{EOC} | t_{LAT} | $t_{INT(EARLY)}$ | $t_{INT(LATE)}$ | t_{EOC} | |
| 0 | 1 | 11 | 13 | 1 | 11 | 11.0 | |
| 1 | 1.5 | Invalid | | | | | |
| 2 | 2 | 21 | 23 | 1 | 21 | 10.5 | |
| 3 | 2.5 | 26 | 28 | 1 | 26 | 10.4 | |
| 4 | 3 | 31 | 34 | 1 | 31 | 10.3 | |
| 5 | 3.5 | 36 | 39 | 1 | 36 | 10.3 | |
| 6 | 4 | 41 | 44 | 1 | 41 | 10.3 | |
| 7 | 4.5 | 46 | 49 | 1 | 46 | 10.2 | |
| 8 | 5 | 51 | 55 | 1 | 51 | 10.2 | |
| 9 | 5.5 | 56 | 60 | 1 | 56 | 10.2 | |
| 10 | 6 | 61 | 65 | 1 | 61 | 10.2 | |
| 11 | 6.5 | 66 | 70 | 1 | 66 | 10.2 | |
| 12 | 7 | 71 | 76 | 1 | 71 | 10.1 | |
| 13 | 7.5 | 76 | 81 | 1 | 76 | 10.1 | |
| 14 | 8 | 81 | 86 | 1 | 81 | 10.1 | |
| 15 | 8.5 | 86 | 91 | 1 | 86 | 10.1 | |

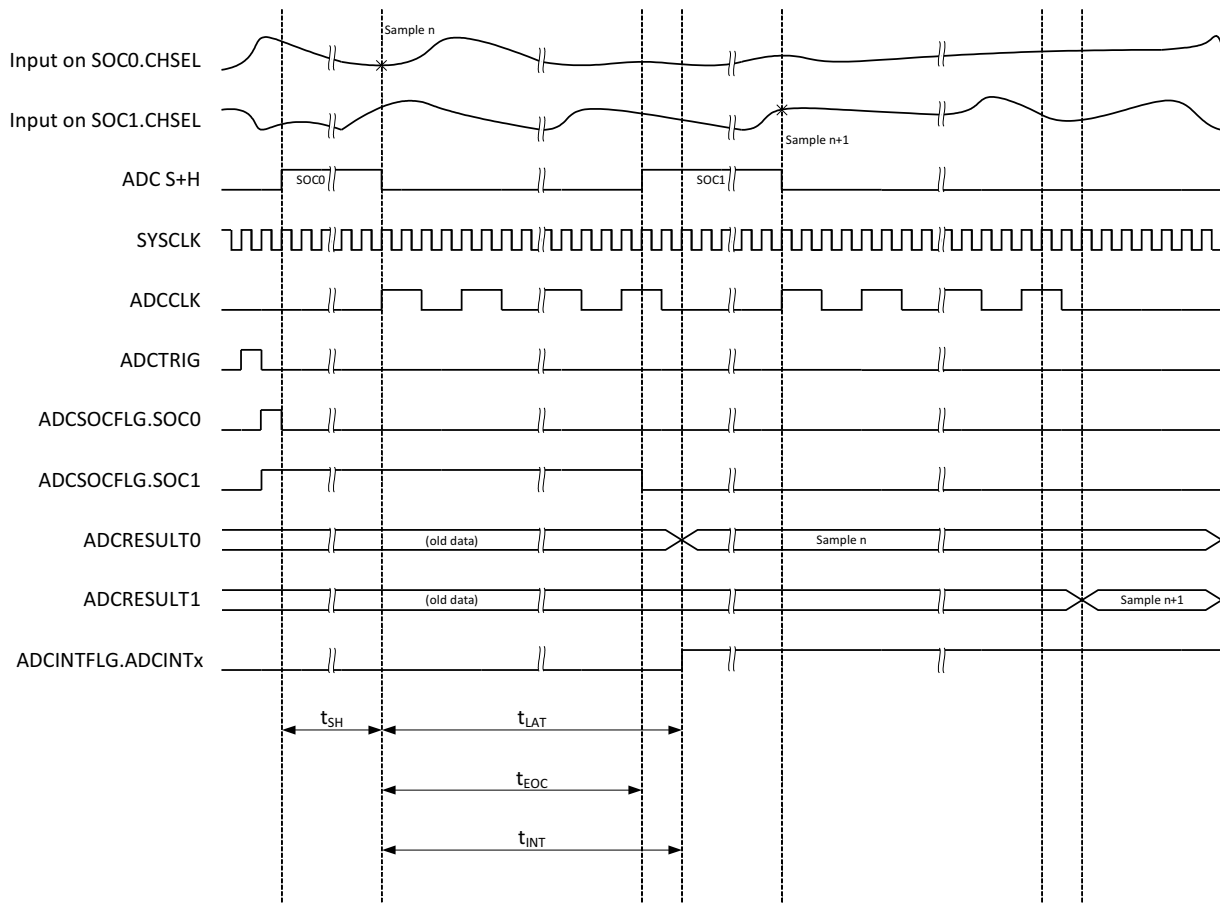


Figure 5-35. ADC Timings for 12-Bit Mode

Table 5-52. ADC Timings in 16-Bit Mode

| ADCCLK PRESCALE | | SYSCLK CYCLES | | | | ADCCLK CYCLES |
|--------------------|---------------------|---------------|-----------|------------------|-----------------|---------------|
| ADCCTL2 [PRESCALE] | RATIO ADCCLK:SYSCLK | t_{EOC} | t_{LAT} | $t_{INT(EARLY)}$ | $t_{INT(LATE)}$ | t_{EOC} |
| 0 | 1 | 31 | 32 | 1 | 31 | 31.0 |
| 1 | 1.5 | Invalid | | | | |
| 2 | 2 | 60 | 61 | 1 | 60 | 30.0 |
| 3 | 2.5 | 75 | 75 | 1 | 75 | 30.0 |
| 4 | 3 | 90 | 91 | 1 | 90 | 30.0 |
| 5 | 3.5 | 104 | 106 | 1 | 104 | 29.7 |
| 6 | 4 | 119 | 120 | 1 | 119 | 29.8 |
| 7 | 4.5 | 134 | 134 | 1 | 134 | 29.8 |
| 8 | 5 | 149 | 150 | 1 | 149 | 29.8 |
| 9 | 5.5 | 163 | 165 | 1 | 163 | 29.6 |
| 10 | 6 | 178 | 179 | 1 | 178 | 29.7 |
| 11 | 6.5 | 193 | 193 | 1 | 193 | 29.7 |
| 12 | 7 | 208 | 209 | 1 | 208 | 29.7 |
| 13 | 7.5 | 222 | 224 | 1 | 222 | 29.6 |
| 14 | 8 | 237 | 238 | 1 | 237 | 29.6 |
| 15 | 8.5 | 252 | 252 | 1 | 252 | 29.6 |

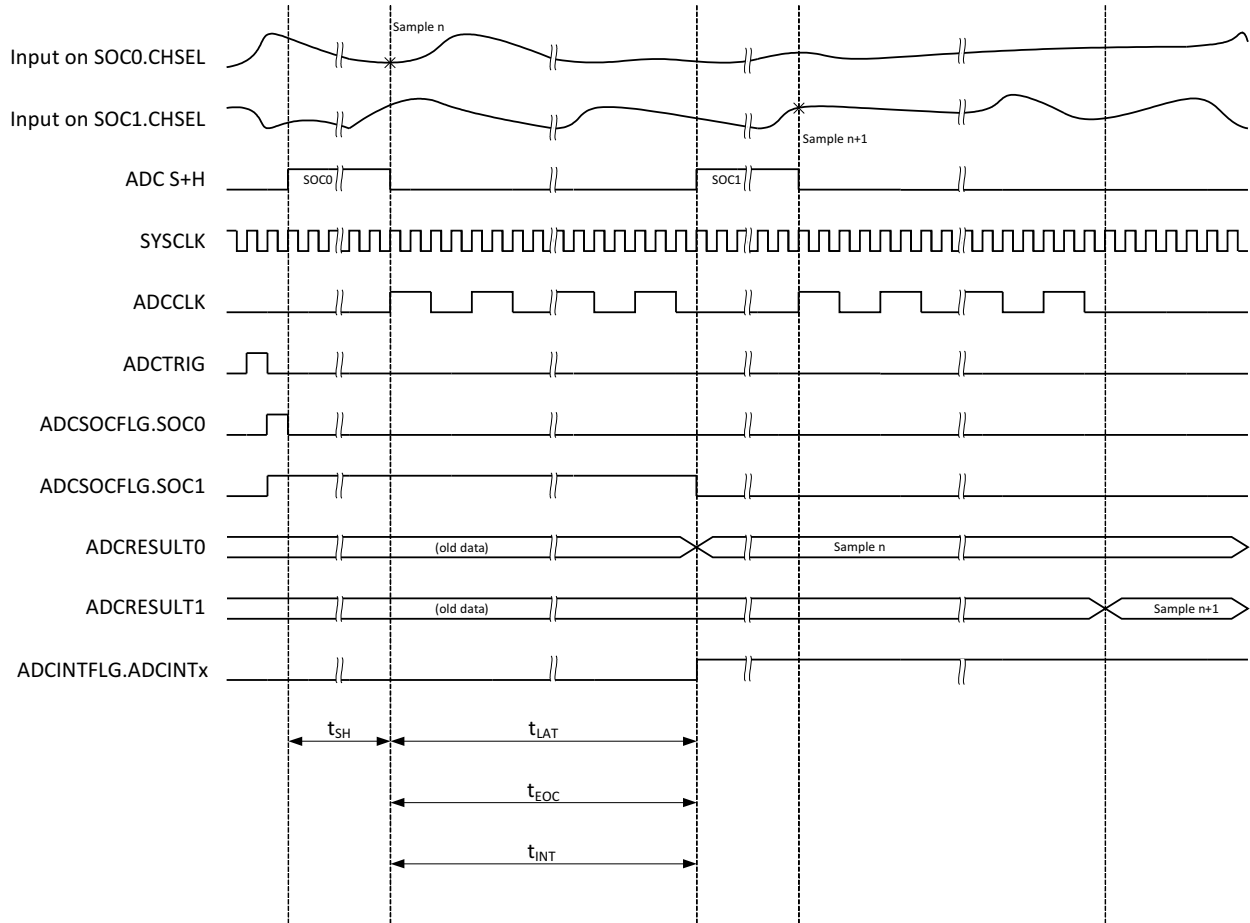


Figure 5-36. ADC Timings for 16-Bit Mode

5.10.1.3 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in [Table 5-53](#).

Table 5-53. Temperature Sensor Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|--|-----|-----|-----|------|
| Temperature accuracy | | ±15 | | °C |
| Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor) | | 500 | | µs |
| ADC acquisition time | 700 | | | ns |

5.10.2 Comparator Subsystem (CMPSS)

Each CMPSS module includes two comparators, two internal voltage reference DACs (CMPSS DACs), two digital glitch filters, and one ramp generator. There are two inputs, CMPINxP and CMPINxN. Each of these inputs will be internally connected to an ADCIN pin. The CMPINxP pin is always connected to the positive input of the CMPSS comparators. CMPINxN can be used instead of the DAC output to drive the negative comparator inputs. There are two comparators, and therefore two outputs from the CMPSS module, which are connected to the input of a digital filter module before being passed on to the Comparator TRIP crossbar and either PWM modules or directly to a GPIO pin. Figure 5-37 shows the CMPSS connectivity on the 337-ball ZWT and 176-pin PTP packages. Figure 5-38 shows CMPSS connectivity on the 100-pin PZP package.

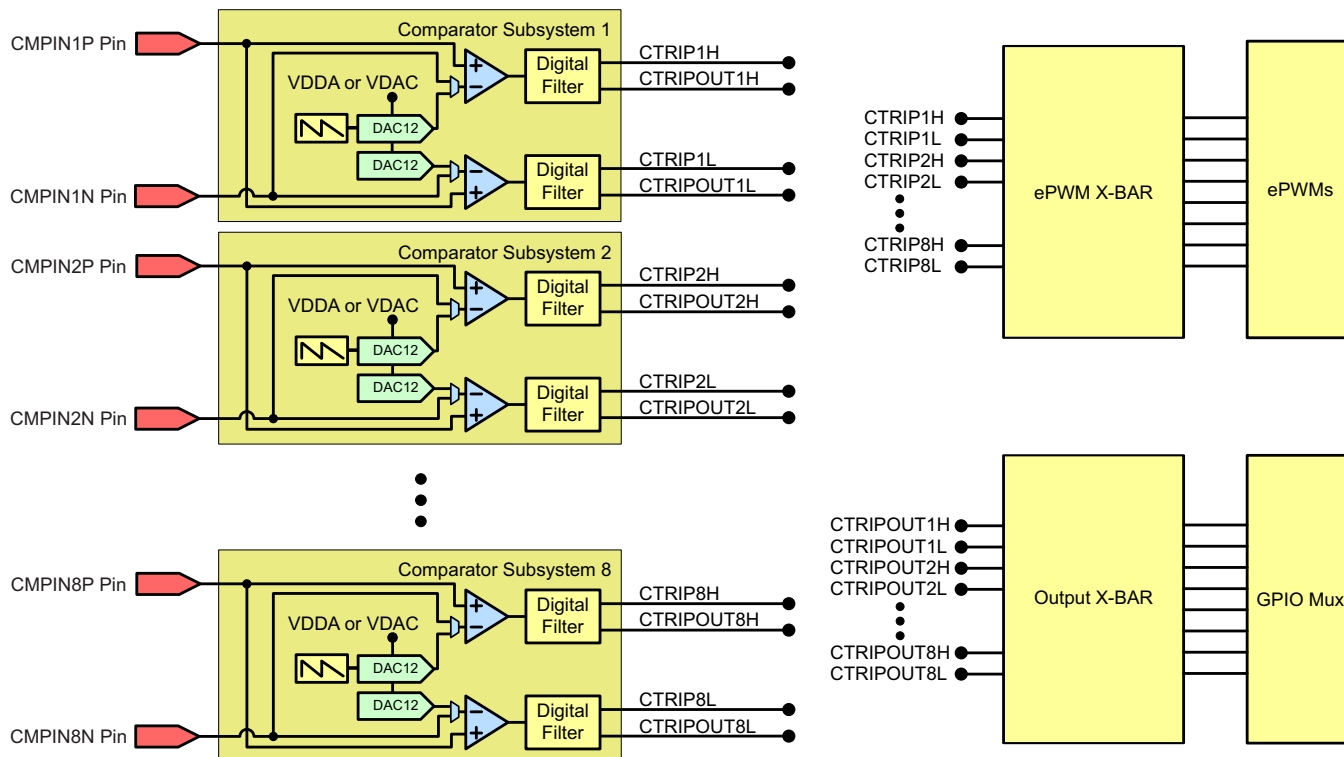


Figure 5-37. CMPSS Connectivity (337-Ball ZWT and 176-Pin PTP)

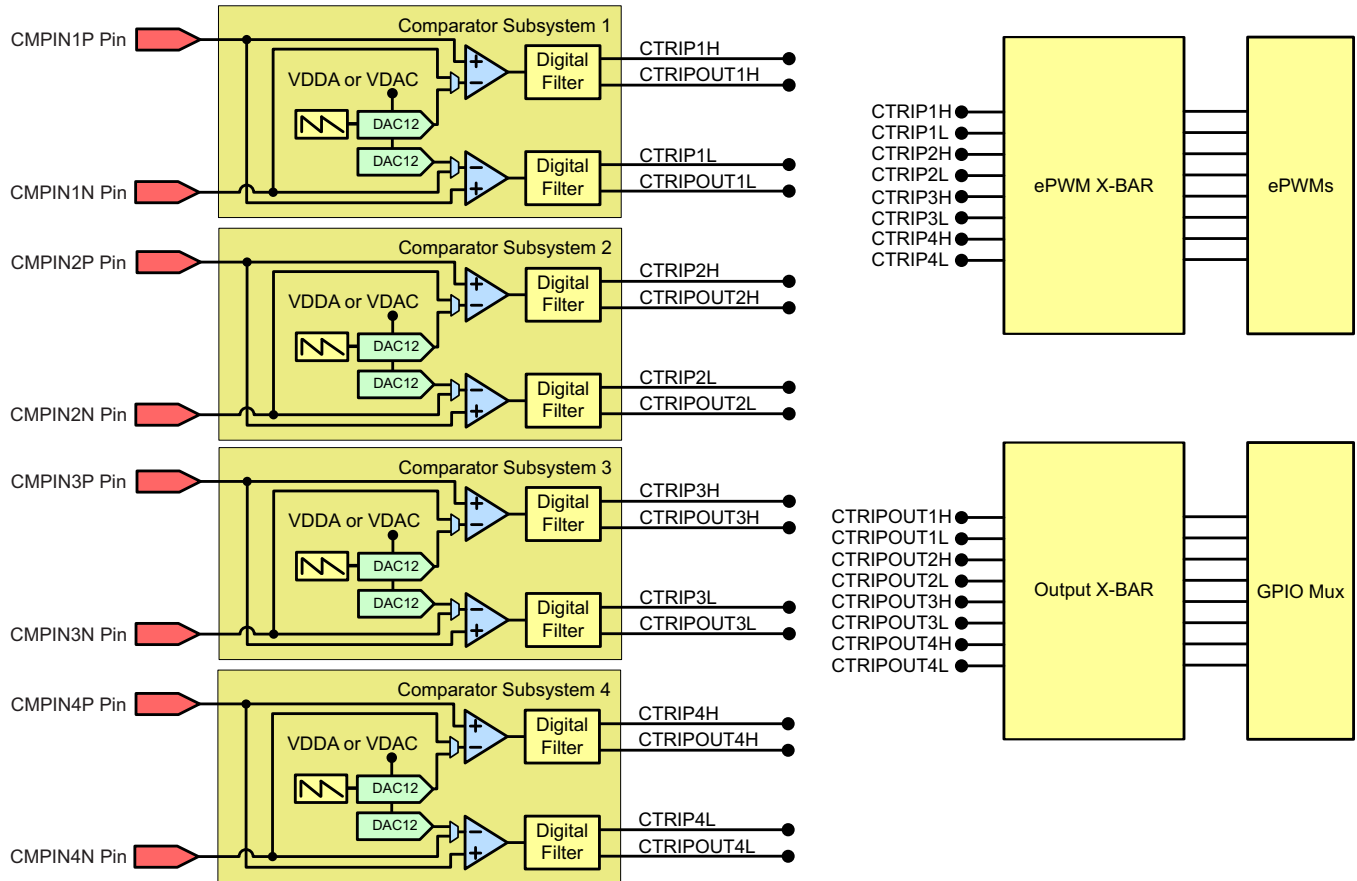


Figure 5-38. CMPSS Connectivity (100-Pin PZP)

5.10.2.1 CMPSS Electrical Data and Timing

Table 5-54 shows the comparator electrical characteristics. Figure 5-39 shows the CMPSS comparator input referred offset. Figure 5-40 shows the CMPSS comparator hysteresis.

Table 5-54. Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------|-----|-----|------------------|------------------|
| Power-up time (from COMPCTL[COMPDACE] to comparator ready) | | | | 10 | μs |
| Comparator input (CMPINxx) range | | 0 | | V _{DDA} | V |
| Input referred offset error | | -20 | | 20 | mV |
| Hysteresis ⁽¹⁾ | 1x | | 12 | | CMPSS DAC LSB |
| | 2x | | 24 | | |
| | 3x | | 36 | | |
| | 4x | | 48 | | |
| Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR) | Step response | | 21 | 60 | ns |
| | Ramp response (1.65 V/μs) | | 26 | | |
| | Ramp response (8.25 mV/μs) | | 30 | | |

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

NOTE

The CMPSS inputs must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If a CMPSS input exceeds this level, an internal blocking circuit will isolate the internal comparator from the external pin until the external pin voltage returns below V_{DDA} + 0.3 V. During this time, the internal comparator input will be floating and can decay below V_{DDA} within approximately 0.5 μs. After this time, the comparator could begin to output an incorrect result depending on the value of the other comparator input.

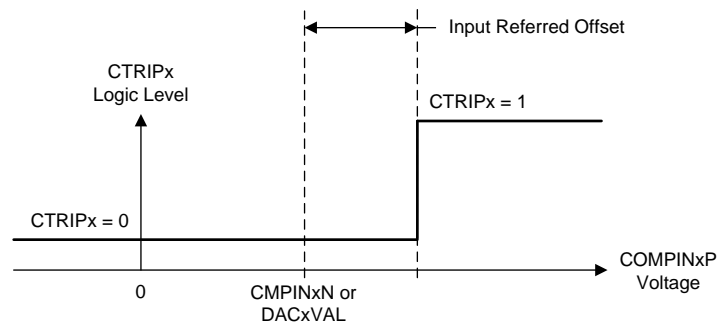


Figure 5-39. CMPSS Comparator Input Referred Offset

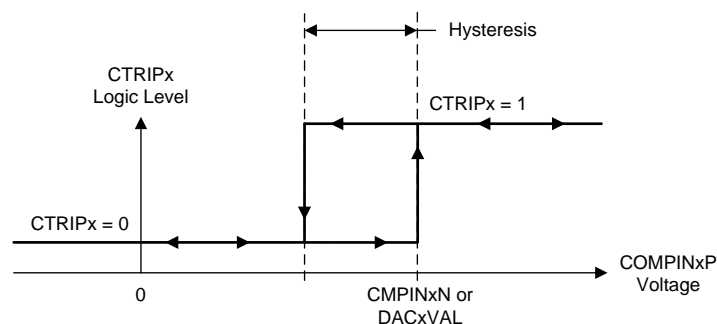


Figure 5-40. CMPSS Comparator Hysteresis

Table 5-55 shows the CMPSS DAC static electrical characteristics. Figure 5-41 shows the CMPSS DAC static offset. Figure 5-42 shows the CMPSS DAC static gain. Figure 5-43 shows the CMPSS DAC static linearity.

Table 5-55. CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-------|------------|-----------|------------|
| CMPSS DAC output range | Internal reference | 0 | | V_{DDA} | V |
| | External reference | 0 | | VDAC | |
| Static offset error ⁽¹⁾ | | -25 | | 25 | mV |
| Static gain error ⁽¹⁾ | | -2 | | 2 | % of FSR |
| Static DNL | Endpoint corrected | >-1 | | 4 | LSB |
| Static INL | Endpoint corrected | -16 | | 16 | LSB |
| Settling time | Settling to 1 LSB after full-scale output change | | | 1 | μ s |
| Resolution | | | 12 | | bits |
| CMPSS DAC output disturbance ⁽²⁾ | Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module | -100 | | 100 | LSB |
| CMPSS DAC disturbance time ⁽²⁾ | | | 200 | | ns |
| VDAC reference voltage | When VDAC is reference | 2.4 | 2.5 or 3.0 | V_{DDA} | V |
| VDAC load ⁽³⁾ | When VDAC is reference | | 6 | | k Ω |

(1) Includes comparator input referred errors.

(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.

(3) Per active CMPSS module.

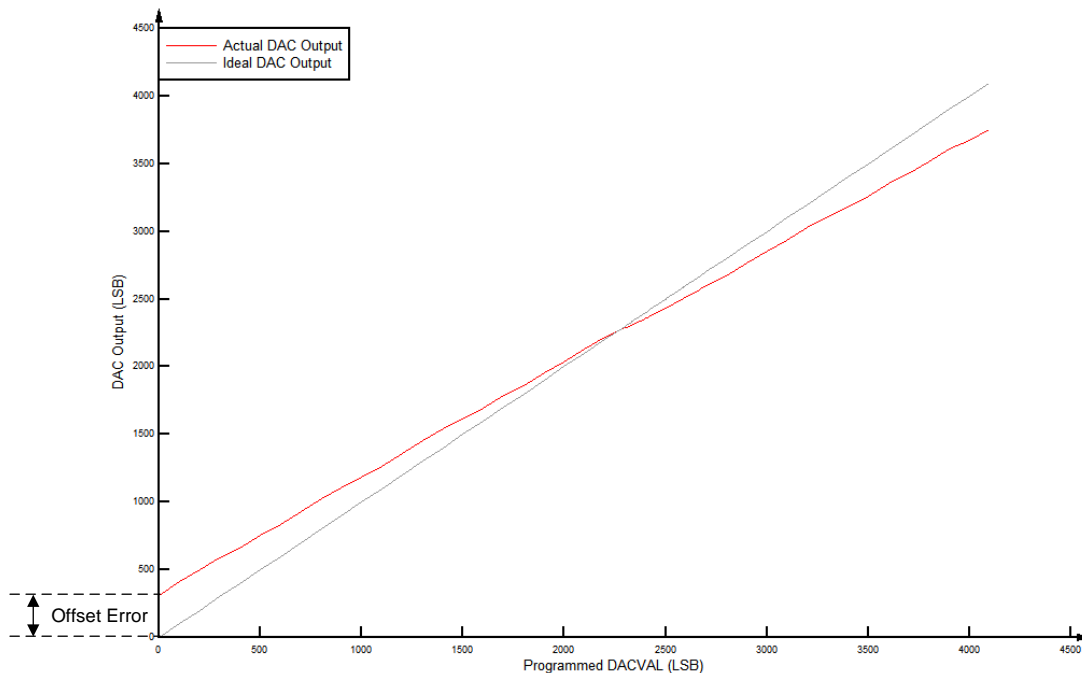


Figure 5-41. CMPSS DAC Static Offset

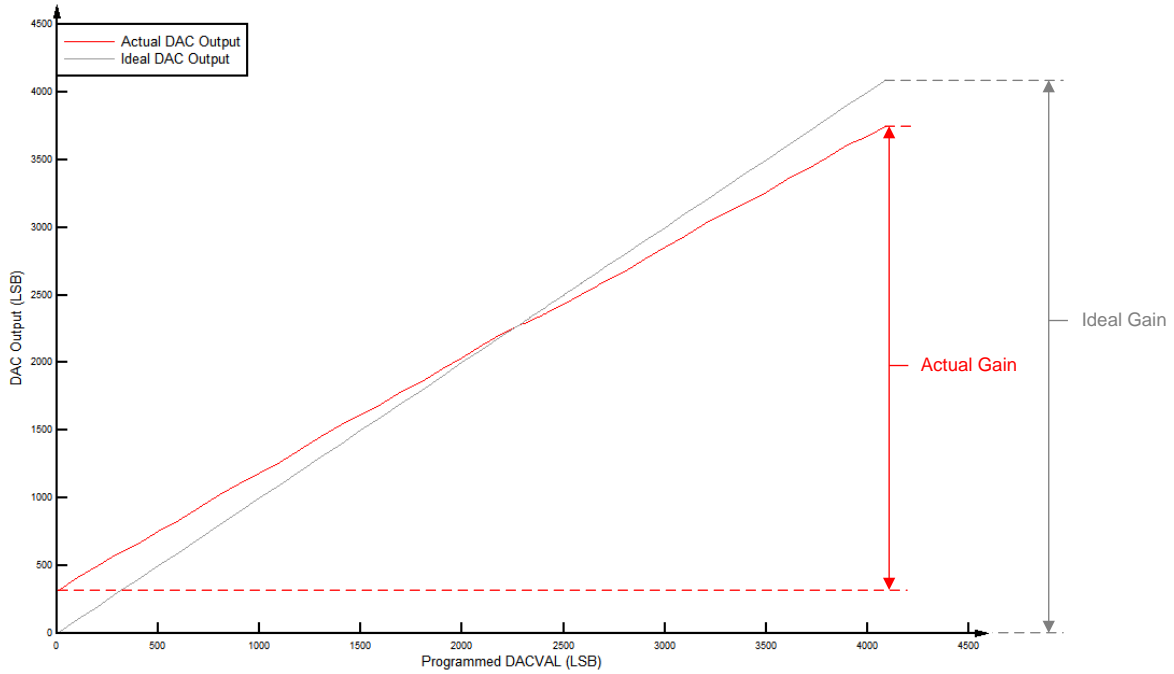


Figure 5-42. CMPSS DAC Static Gain

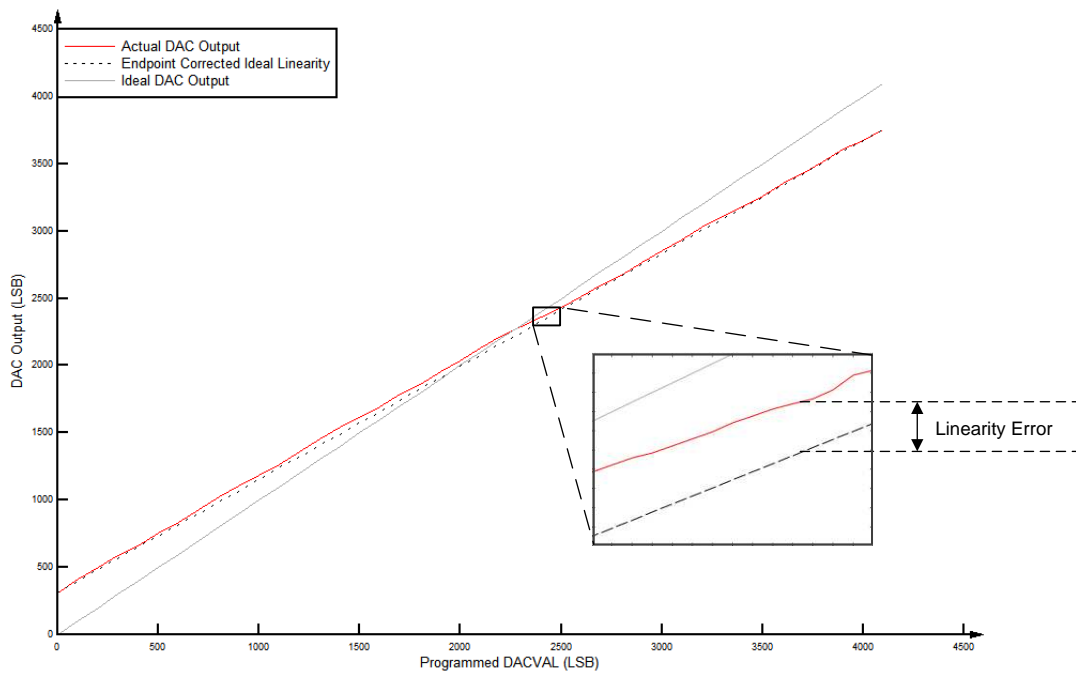


Figure 5-43. CMPSS DAC Static Linearity

5.10.3 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal reference DAC and an analog output buffer that is capable of driving an external load. An integrated pulldown resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pulldown resistor cannot be disabled and remains as a passive component on the pin, even for other shared pin mux functions. Software writes to the DAC value register can take effect immediately or can be synchronized with PWMSYNC events.

Each buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage
- Pulldown resistor on output
- Ability to synchronize with PWMSYNC

The block diagram for the buffered DAC is shown in Figure 5-44.

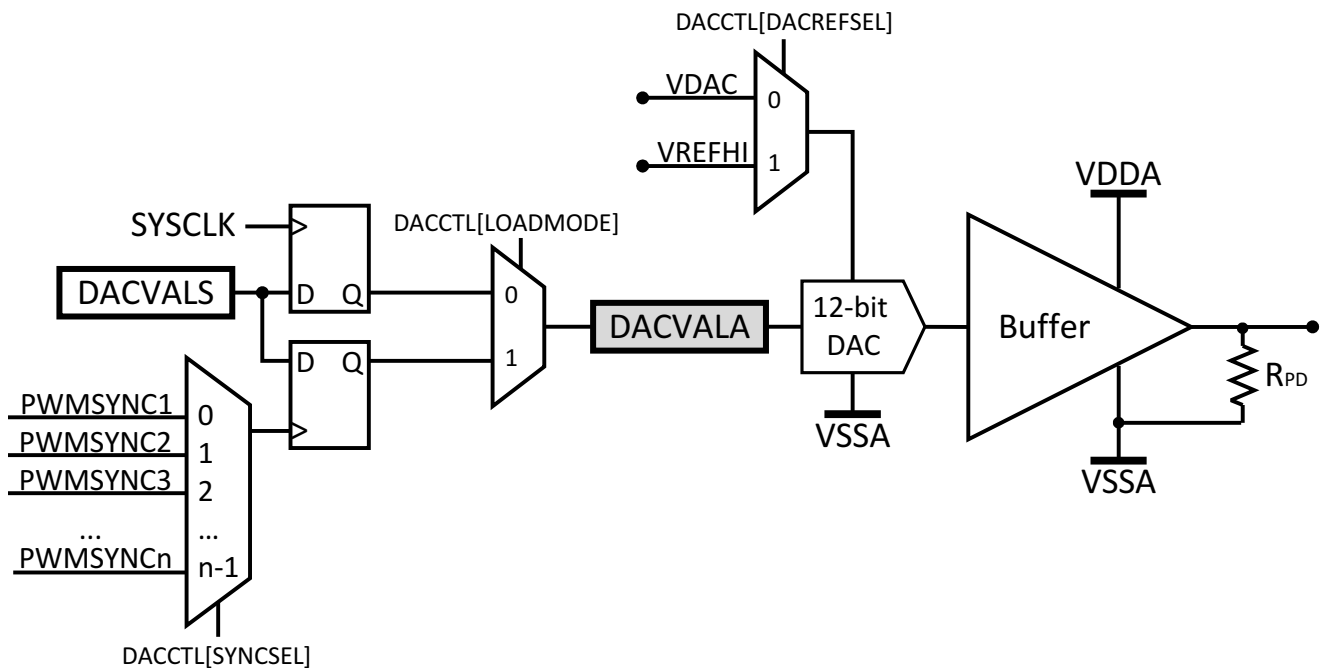


Figure 5-44. DAC Module Block Diagram

5.10.3.1 Buffered DAC Electrical Data and Timing

Table 5-56 shows the buffered DAC electrical characteristics. Figure 5-45 shows the buffered DAC offset. Figure 5-46 shows the buffered DAC gain. Figure 5-47 shows the buffered DAC linearity.

Table 5-56. Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|------------|------------------------|-----------|
| Power-up time (DACOUTEN to DAC output valid) | | | | 10 | μs |
| Trimmed offset error | Midpoint | -10 | | 10 | mV |
| Gain error ⁽²⁾ | | -2.5 | | 2.5 | % of FSR |
| DNL ⁽³⁾ | Endpoint corrected | > -1 | | 1 | LSB |
| INL | Endpoint corrected | -5 | | 5 | LSB |
| DACOUTx settling time | Settling to 2 LSBs after 0.3V-to-3V transition | | 2 | | μs |
| Resolution | | | 12 | | bits |
| Voltage output range ⁽⁴⁾ | | 0.3 | | V _{DDA} - 0.3 | V |
| Capacitive load | Output drive capability | | | 100 | pF |
| Resistive load | Output drive capability | 5 | | | kΩ |
| R _{PD} | | | 50 | | kΩ |
| Reference voltage ⁽⁵⁾ | VDAC or V _{REFHI} | 2.4 | 2.5 or 3.0 | V _{DDA} | V |
| Reference load ⁽⁶⁾ | VDAC or V _{REFHI} | | 170 | | kΩ |
| Output noise | Integrated noise from 100 Hz to 100 kHz | | 500 | | μVrms |
| | Noise density at 10 kHz | | 711 | | nVrms/√Hz |
| Glitch energy | | | 1.5 | | V-ns |
| PSRR ⁽⁷⁾ | DC up to 1 kHz | | 70 | | dB |
| | 100 kHz | | 30 | | |
| SNR | 1020 Hz | | 67 | | dB |
| THD | 1020 Hz | | -63 | | dB |
| SFDR | 1020 Hz, including harmonics and spurs | | 66 | | dBc |
| | 1020 Hz, including only spurs | | 104 | | |

- (1) Typical values are measured with V_{REFHI} = 3.3 V and V_{REFLO} = 0 V unless otherwise noted. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V.
- (2) Gain error is calculated for linear output range.
- (3) The DAC output is monotonic.
- (4) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
- (5) For best PSRR performance, VDAC or V_{REFHI} should be less than V_{DDA}.
- (6) Per active Buffered DAC module.
- (7) V_{REFHI} = 3.2 V, V_{DDA} = 3.3 V DC + 100 mV Sine.

NOTE

The VDAC pin must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If the VDAC pin exceeds this level, a blocking circuit may activate, and the internal value of VDAC may float to 0 V internally, giving improper DAC output.

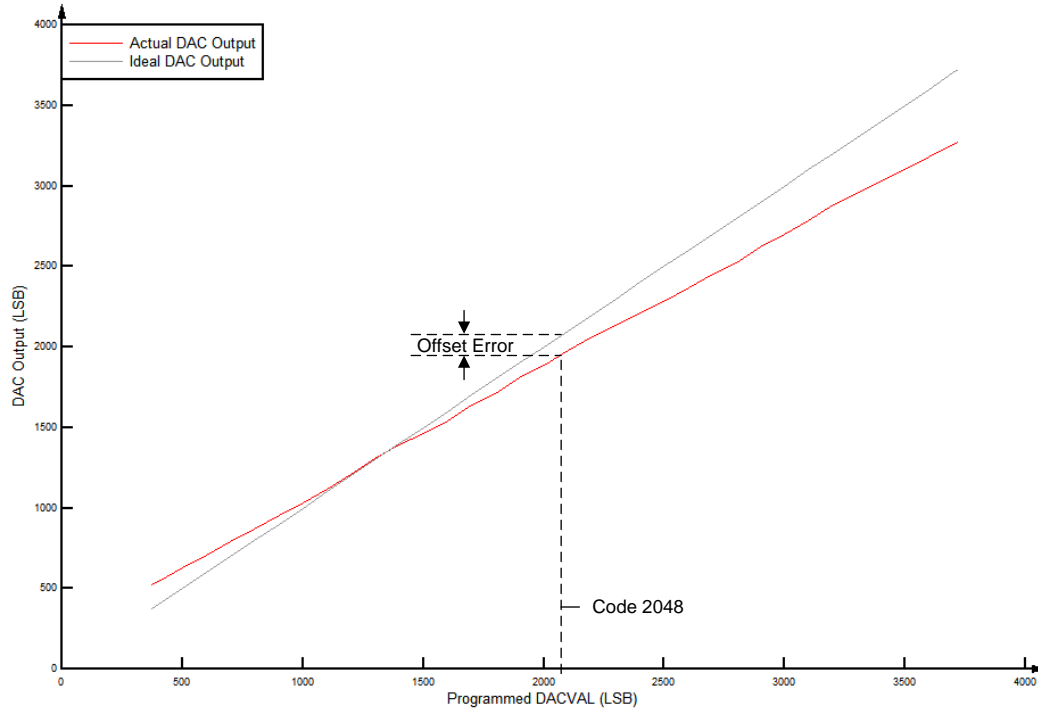


Figure 5-45. Buffered DAC Offset

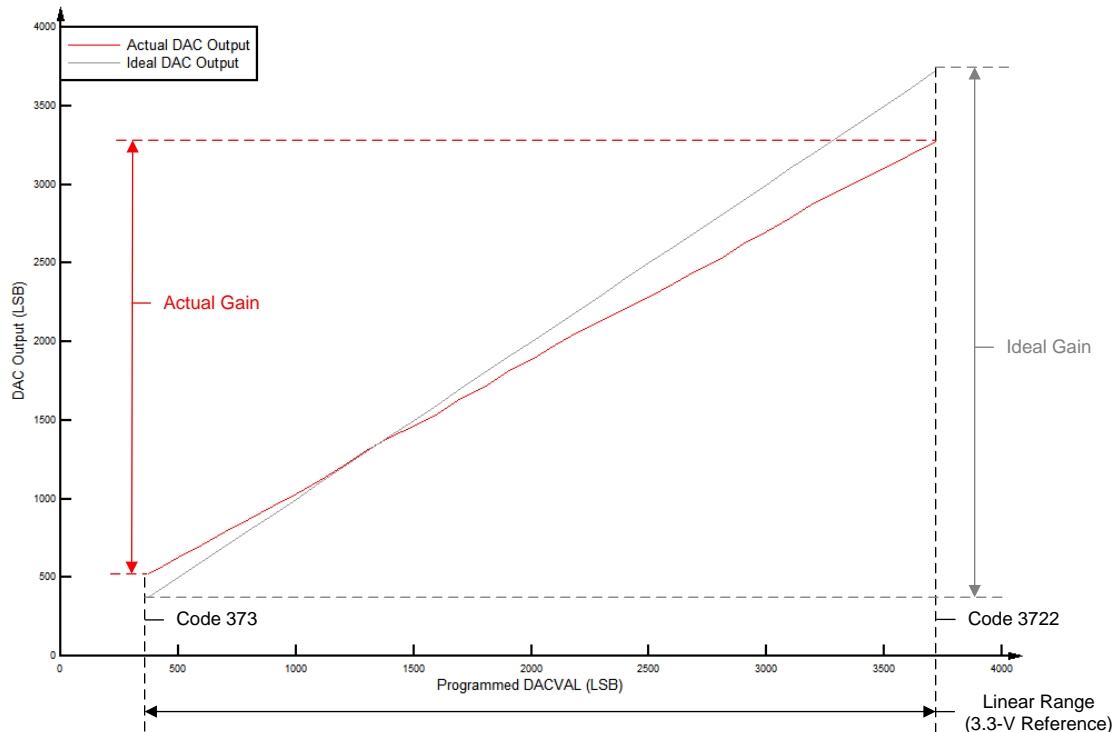


Figure 5-46. Buffered DAC Gain

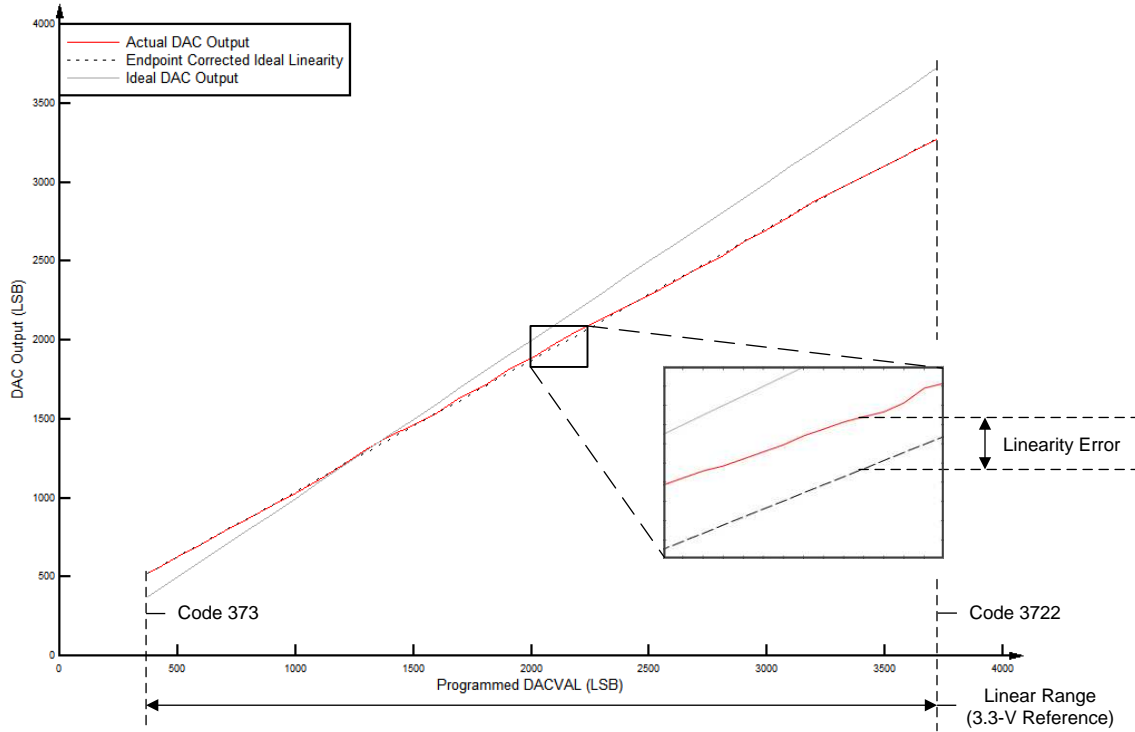


Figure 5-47. Buffered DAC Linearity

5.11 Control Peripherals

NOTE

For the actual number of each peripheral on a specific device, see [Table 3-1](#).

5.11.1 Enhanced Capture (eCAP)

The eCAP module can be used in systems where accurate timing of external events is important.

Applications for eCAP include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

- 4-event time-stamp registers (each 32 bits)
- Edge-polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event timestamps
- Continuous mode capture of timestamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All of the above resources dedicated to a single input pin
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).

The eCAP inputs connect to any GPIO input through the Input X-BAR. The APWM outputs connect to GPIO pins through the Output X-BAR to OUTPUTx positions in the GPIO mux. See [Section 4.4.2](#) and [Section 4.4.3](#).

[Figure 5-48](#) shows the block diagram of an eCAP module.

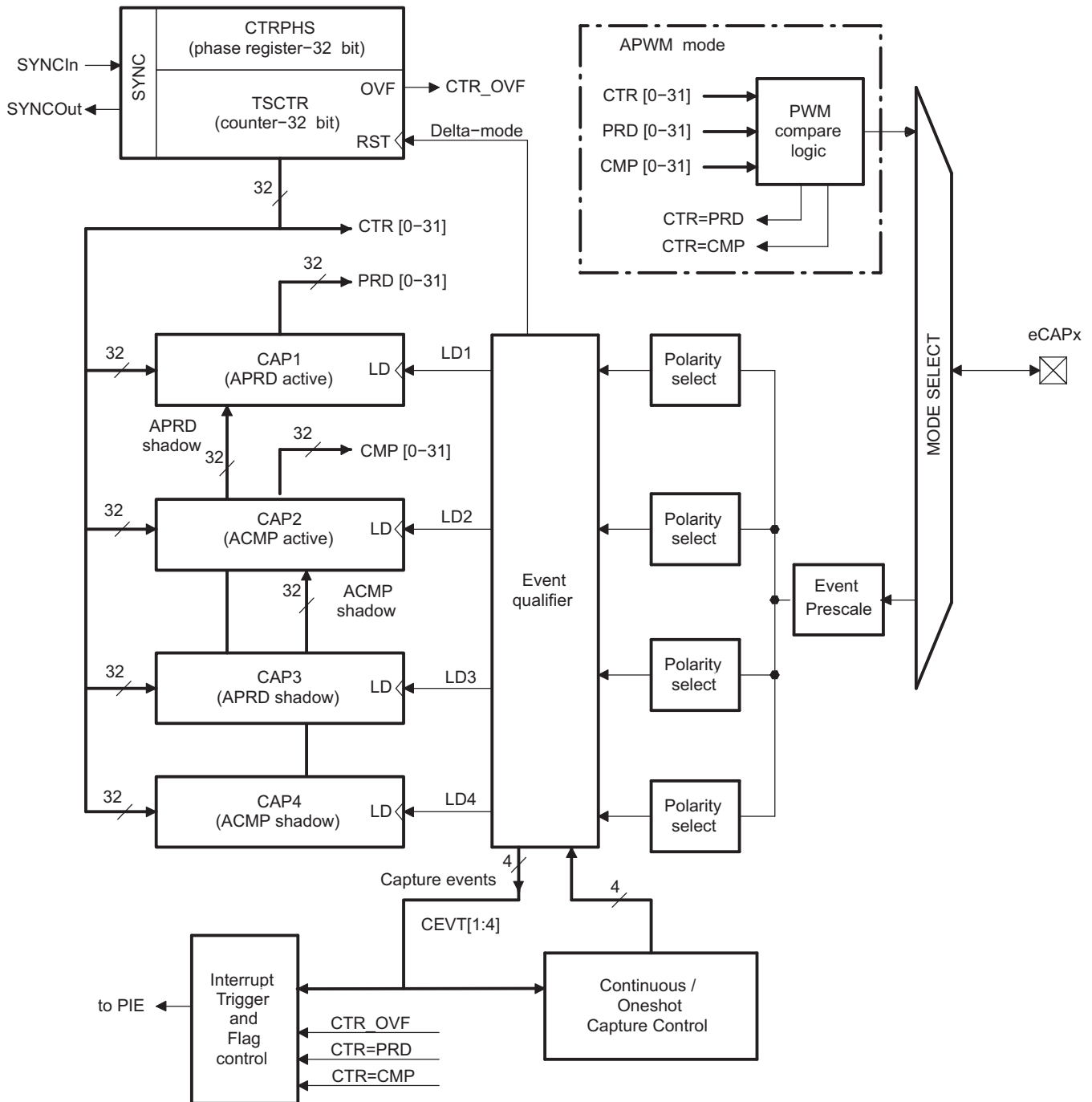


Figure 5-48. eCAP Block Diagram

The eCAP module is clocked by PERx.SYSCLK.

The clock enable bits (ECAP1–ECAP6) in the PCLKCR3 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

5.11.1.1 eCAP Electrical Data and Timing

[Table 5-57](#) shows the eCAP timing requirement and [Table 5-58](#) shows the eCAP switching characteristics.

Table 5-57. eCAP Timing Requirement⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------|---------------------------|--------------------------------|-----|--------|
| $t_{w(CAP)}$ | Capture input pulse width | | | |
| | Asynchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | With input qualifier | $1t_{c(SYSCLK)} + t_{w(IQSW)}$ | | cycles |

(1) For an explanation of the input qualifier parameters, see [Table 5-24](#).

Table 5-58. eCAP Switching Characteristics

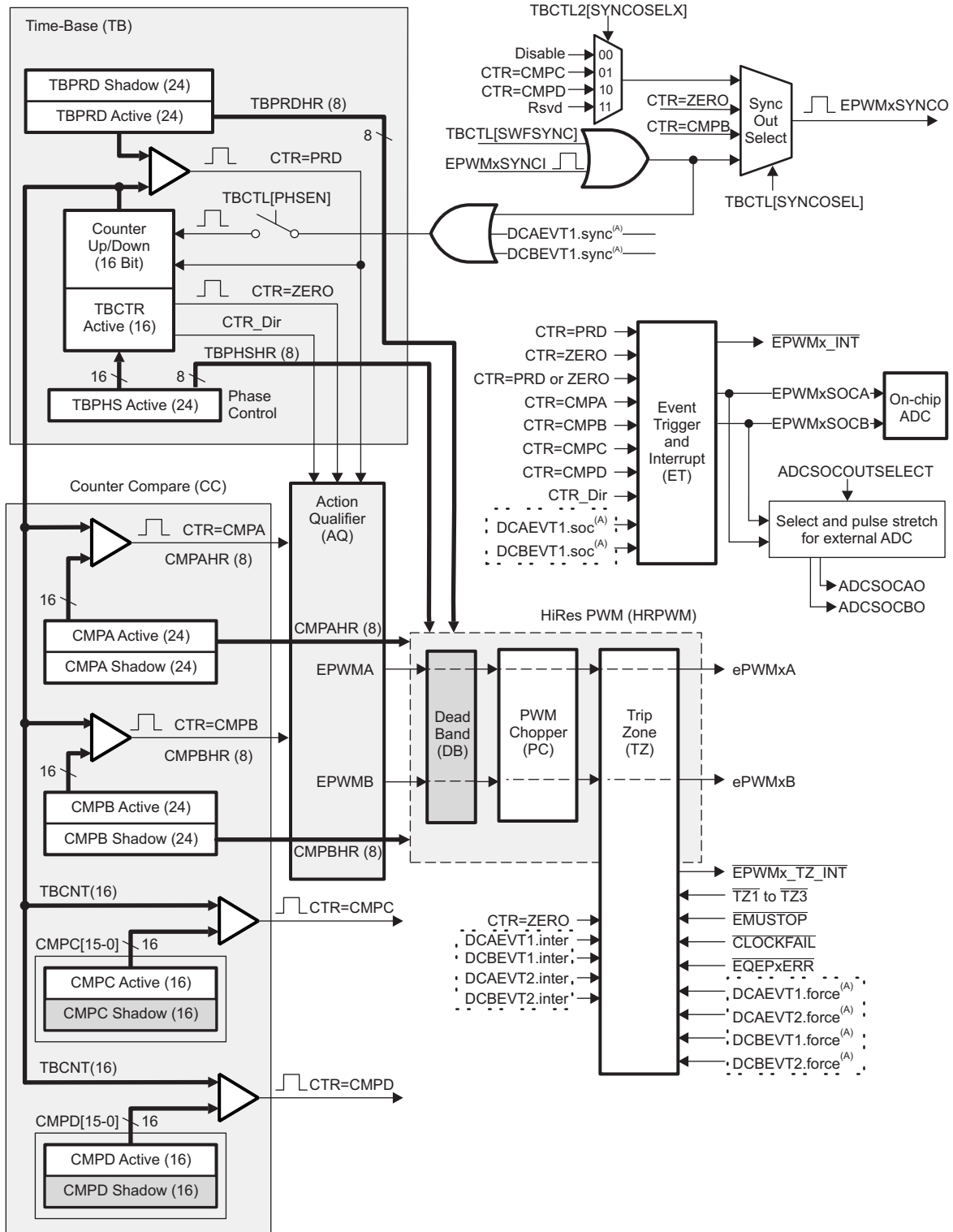
over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---------------|---------------------------------------|-----|-----|------|
| $t_{w(APWM)}$ | Pulse duration, APWMx output high/low | 20 | | ns |

5.11.2 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

[Figure 5-49](#) shows the signal interconnections with the ePWM. [Figure 5-50](#) shows the ePWM trip input connectivity.



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A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 5-49. ePWM Submodules and Critical Internal Signal Interconnects

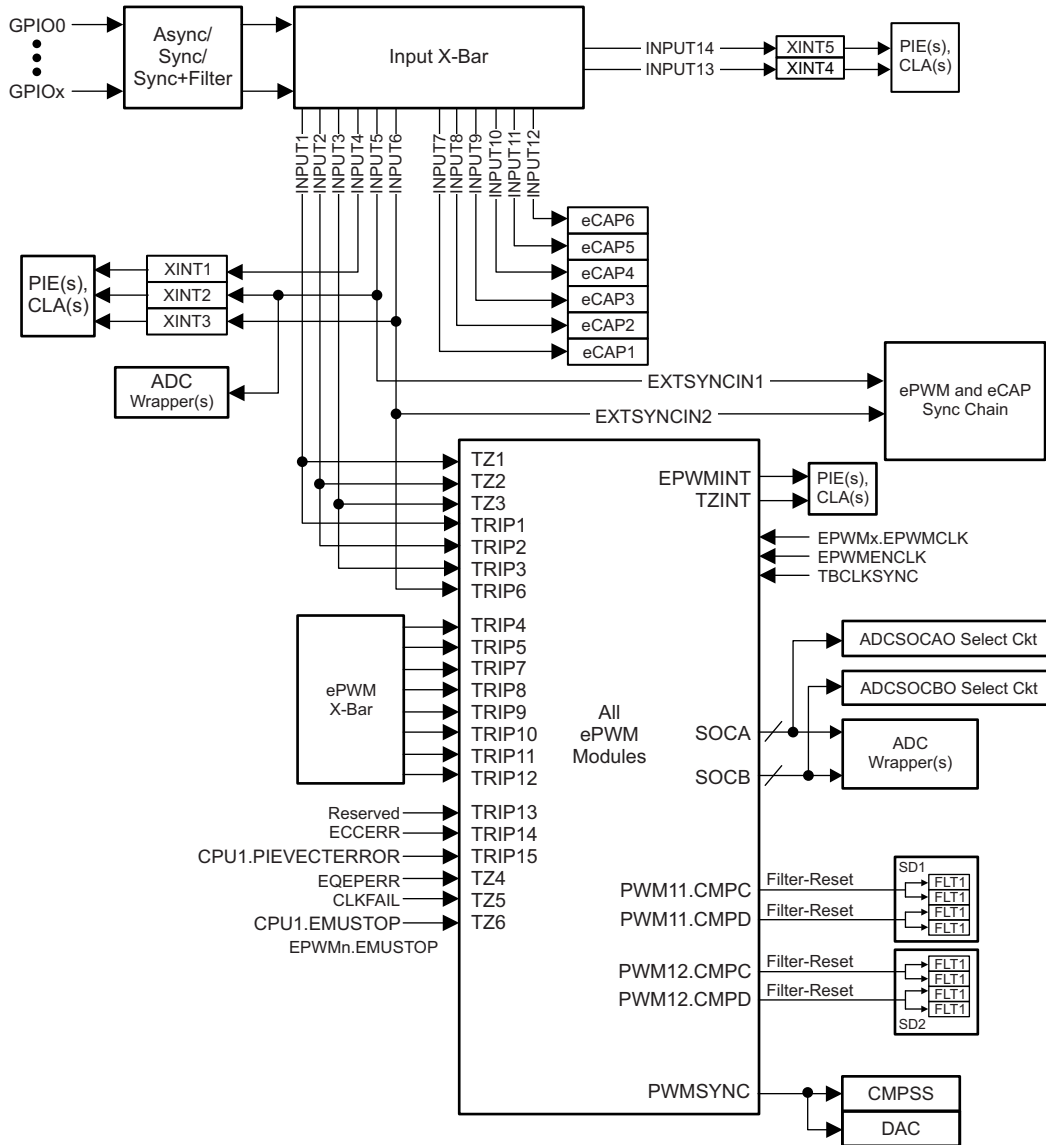


Figure 5-50. ePWM Trip Input Connectivity

5.11.2.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization chain allows synchronization between multiple modules for the system. Figure 5-51 shows the synchronization chain architecture.

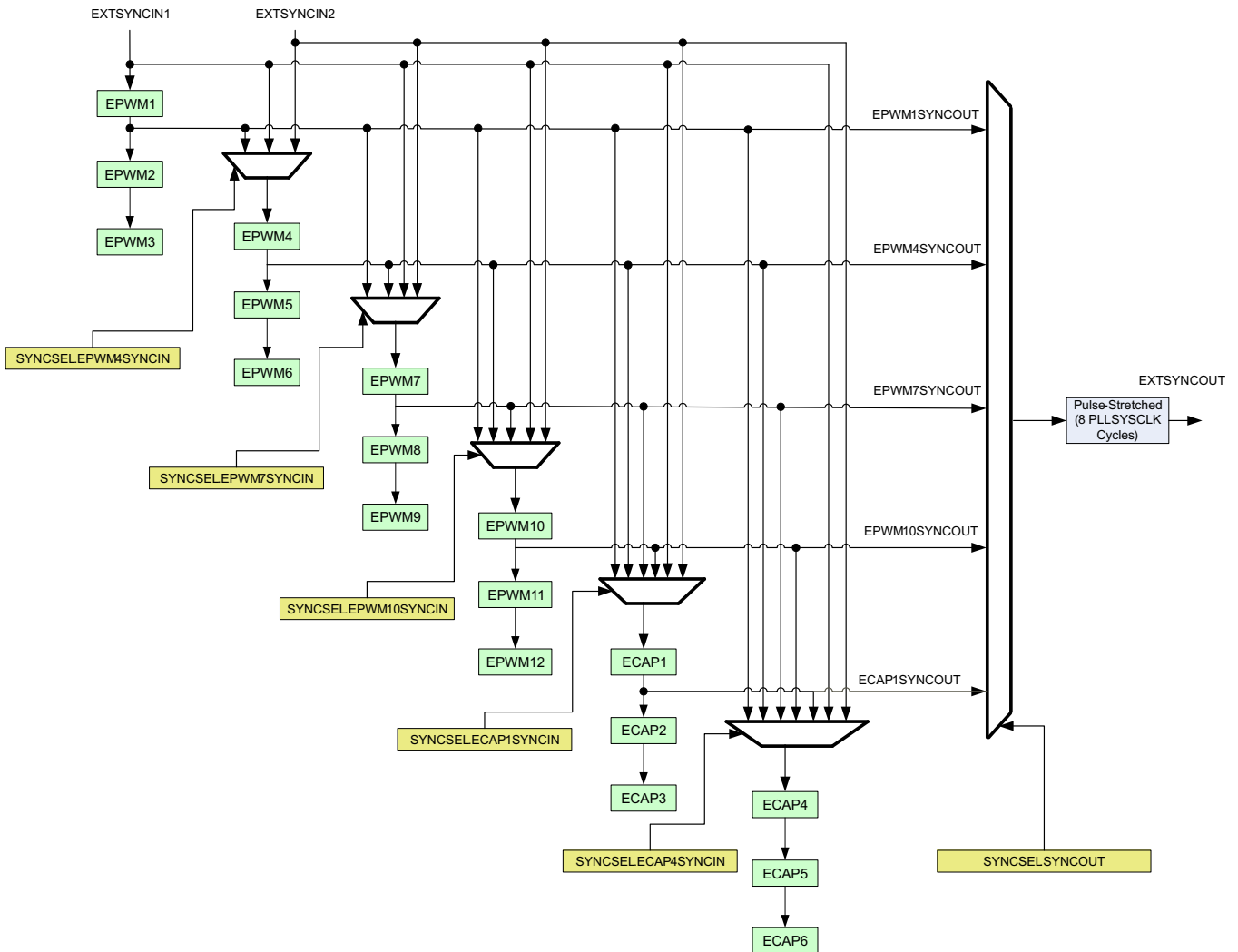


Figure 5-51. Synchronization Chain Architecture

5.11.2.2 ePWM Electrical Data and Timing

Table 5-59 shows the PWM timing requirements and Table 5-60 shows the PWM switching characteristics.

Table 5-59. ePWM Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|------------------------|----------------------|---------------------------------|--------|
| $t_{w(SYNCIN)}$ | Sync input pulse width | Asynchronous | $2t_{c(EPWMCLK)}$ | cycles |
| | | Synchronous | $2t_{c(EPWMCLK)}$ | cycles |
| | | With input qualifier | $1t_{c(EPWMCLK)} + t_{w(IQSW)}$ | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-24.

Table 5-60. ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------|--|------------------|-----|--------|
| $t_{w(PWM)}$ | Pulse duration, PWMx output high/low | 20 | | ns |
| $t_{w(SYNCOU)}$ | Sync output pulse width | $8t_{c(SYSCLK)}$ | | cycles |
| $t_{d(TZ-PWM)}$ | Delay time, trip input active to PWM forced high | | 25 | ns |
| | Delay time, trip input active to PWM forced low | | | |
| | Delay time, trip input active to PWM Hi-Z | | | |

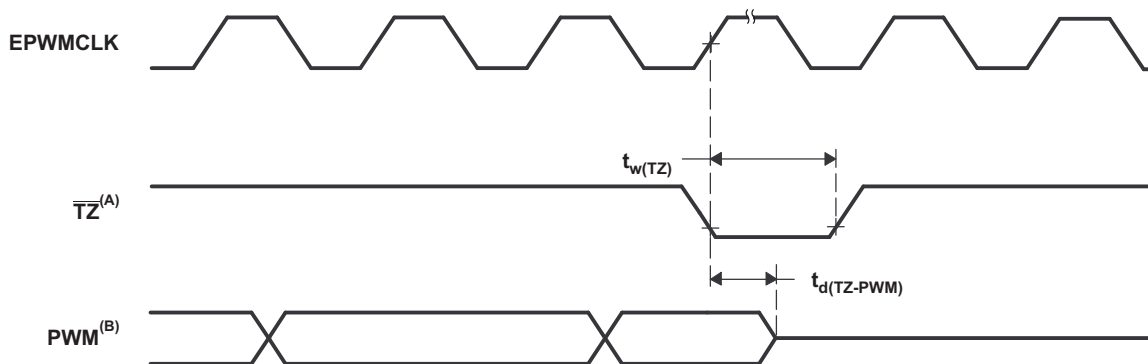
5.11.2.2.1 Trip-Zone Input Timing

Table 5-61 shows the trip-zone input timing requirements. Figure 5-52 shows the PWM Hi-Z characteristics.

Table 5-61. Trip-Zone Input Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|-------------|--|----------------------|---------------------------------|--------|
| $t_{w(TZ)}$ | Pulse duration, \overline{TZx} input low | Asynchronous | $1t_{c(EPWMCLK)}$ | cycles |
| | | Synchronous | $2t_{c(EPWMCLK)}$ | cycles |
| | | With input qualifier | $1t_{c(EPWMCLK)} + t_{w(IQSW)}$ | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-24.



- A. \overline{TZ} : $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12
- B. PWM refers to all the PWM pins in the device. The state of the PWM pins after \overline{TZ} is taken high depends on the PWM recovery software.

Figure 5-52. PWM Hi-Z Characteristics

5.11.2.3 External ADC Start-of-Conversion Electrical Data and Timing

Table 5-62 shows the external ADC start-of-conversion switching characteristics. Figure 5-53 shows the ADCSOCAO or ADCSOCBO timing.

Table 5-62. External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT |
|--|-------------------|-----|--------|
| $t_{w(ADCSOCL)}$ Pulse duration, $\overline{ADCSOCxO}$ low | $32t_{c(SYSCLK)}$ | | cycles |

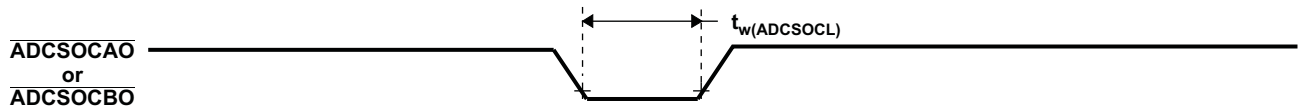


Figure 5-53. ADCSOCAO or ADCSOCBO Timing

5.11.3 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position-control systems.

Each eQEP peripheral comprises five major functional blocks:

- Quadrature Capture Unit (QCAP)
- Position Counter/Control Unit (PCCU)
- Quadrature Decoder Unit (QDU)
- Unit Time Base for speed and frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)

The eQEP peripherals are clocked by PERx.SYSCLK. [Figure 5-54](#) shows the eQEP block diagram.

5.11.3.1 eQEP Electrical Data and Timing

Table 5-63 lists the eQEP timing requirement and Table 5-64 lists the eQEP switching characteristics.

Table 5-63. eQEP Timing Requirements⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------------|---------------------------|--|--|-----|--------|
| t _{w(QEPP)} | QEP input period | Asynchronous ⁽²⁾ /Synchronous | 2t _{c(SYSCLK)} | | cycles |
| | | With input qualifier | 2[1t _{c(SYSCLK)} + t _{w(IQSW)}] | | cycles |
| t _{w(INDEXH)} | QEP Index Input High time | Asynchronous ⁽²⁾ /Synchronous | 2t _{c(SYSCLK)} | | cycles |
| | | With input qualifier | 2t _{c(SYSCLK)} + t _{w(IQSW)} | | cycles |
| t _{w(INDEXL)} | QEP Index Input Low time | Asynchronous ⁽²⁾ /Synchronous | 2t _{c(SYSCLK)} | | cycles |
| | | With input qualifier | 2t _{c(SYSCLK)} + t _{w(IQSW)} | | cycles |
| t _{w(STROBH)} | QEP Strobe High time | Asynchronous ⁽²⁾ /Synchronous | 2t _{c(SYSCLK)} | | cycles |
| | | With input qualifier | 2t _{c(SYSCLK)} + t _{w(IQSW)} | | cycles |
| t _{w(STROBL)} | QEP Strobe Input Low time | Asynchronous ⁽²⁾ /Synchronous | 2t _{c(SYSCLK)} | | cycles |
| | | With input qualifier | 2t _{c(SYSCLK)} + t _{w(IQSW)} | | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-24.

(2) See the [TMS320F2837xS Delfino™ MCUs Silicon Errata](#) for limitations in the asynchronous mode.

Table 5-64. eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|----------------------------|--|-----|-------------------------|--------|
| t _{d(CNTR)xin} | Delay time, external clock to counter increment | | 4t _{c(SYSCLK)} | cycles |
| t _{d(PCS-OUT)QEP} | Delay time, QEP input edge to position compare sync output | | 6t _{c(SYSCLK)} | cycles |

5.11.4 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

NOTE

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

5.11.4.1 HRPWM Electrical Data and Timing

Table 5-65 lists the high-resolution PWM switching characteristics.

Table 5-65. High-Resolution PWM Characteristics

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|------|
| Micro Edge Positioning (MEP) step size ⁽¹⁾ | | 150 | 310 | ps |

- (1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD} . MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage. Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

5.11.5 *Sigma-Delta Filter Module (SDFM)*

The SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent sigma-delta ($\Sigma\Delta$) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for overcurrent and undercurrent monitoring. [Figure 5-55](#) shows a block diagram of the SDFMs.

SDFM features include:

- Eight external pins per SDFM module:
 - Four sigma-delta data input pins per SDFM module (SDx_Dy, where x = 1 to 2 and y = 1 to 4)
 - Four sigma-delta clock input pins per SDFM module (SDx_Cy, where x = 1 to 2 and y = 1 to 4)
- Four different configurable modulator clock modes:
 - Modulator clock rate equals modulator data rate
 - Modulator clock rate running at half the modulator data rate
 - Modulator data is Manchester encoded. Modulator clock not required.
 - Modulator clock rate is double that of modulator data rate
- Four independent configurable comparator units:
 - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
 - Ability to detect over-value and under-value conditions
 - Comparator Over-Sampling Ratio (COSR) value for comparator programmable from 1 to 32
- Four independent configurable data filter units:
 - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
 - Data filter Over-Sampling Ratio (DOSR) value for data filter unit programmable from 1 to 256
 - Ability to enable or disable individual filter module
 - Ability to synchronize all four independent filters of a SDFM module using the Master Filter Enable (MFE) bit or the PWM signals.
- Filter data can be 16-bit or 32-bit representation
- PWMs can be used to generate modulator clock for sigma-delta modulators

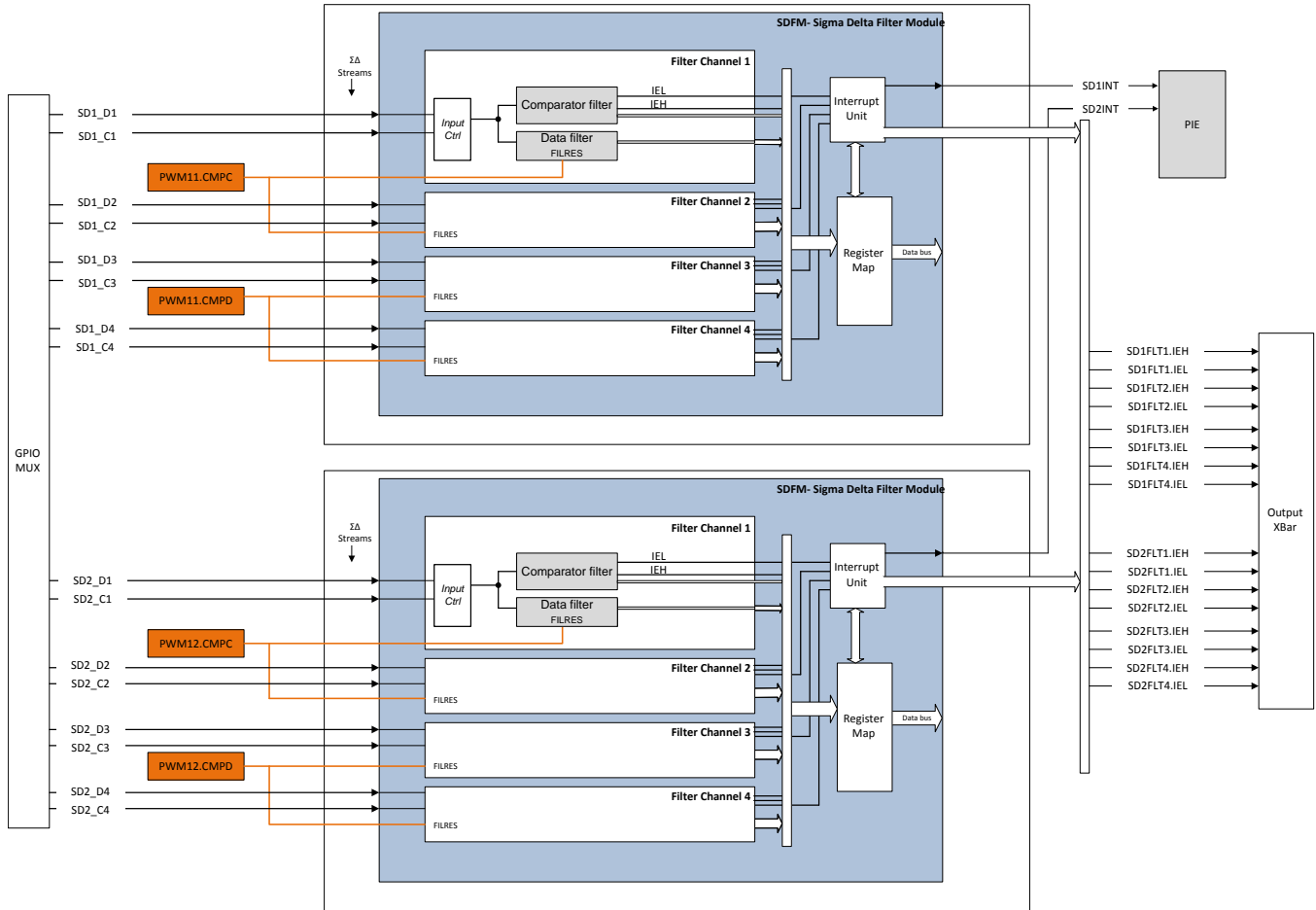


Figure 5-55. SDFM Block Diagram

5.11.5.1 SDFM Electrical Data and Timing (Using ASYNC)

SDFM operation with asynchronous GPIO is defined by setting GPyQSELn = 0b11. [Table 5-66](#) lists the SDFM timing requirements when using the asynchronous GPIO (ASYNC) option. [Figure 5-56](#) through [Figure 5-59](#) show the SDFM timing diagrams.

Table 5-66. SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option

| | | MIN | MAX | UNIT |
|-----------------------|--|---------------------|----------------------|------|
| Mode 0 | | | | |
| $t_{c(SDC)M0}$ | Cycle time, SDx_Cy | 40 | 256 * SYSCLK period | ns |
| $t_{w(SDCH)M0}$ | Pulse duration, SDx_Cy high | 10 | $t_{c(SDC)M0} - 10$ | ns |
| $t_{su(SDDV-SDCH)M0}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 5 | | ns |
| $t_{h(SDCH-SDD)M0}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 5 | | ns |
| Mode 1 | | | | |
| $t_{c(SDC)M1}$ | Cycle time, SDx_Cy | 80 | 256 * SYSCLK period | ns |
| $t_{w(SDCH)M1}$ | Pulse duration, SDx_Cy high | 10 | $t_{c(SDC)M1} - 10$ | ns |
| $t_{su(SDDV-SDCL)M1}$ | Setup time, SDx_Dy valid before SDx_Cy goes low | 5 | | ns |
| $t_{su(SDDV-SDCH)M1}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 5 | | ns |
| $t_{h(SDCL-SDD)M1}$ | Hold time, SDx_Dy wait after SDx_Cy goes low | 5 | | ns |
| $t_{h(SDCH-SDD)M1}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 5 | | ns |
| Mode 2 | | | | |
| $t_{c(SDD)M2}$ | Cycle time, SDx_Dy | 8 * $t_{c(SYSCLK)}$ | 20 * $t_{c(SYSCLK)}$ | ns |
| $t_{w(SDDH)M2}$ | Pulse duration, SDx_Dy high | 10 | | ns |
| Mode 3 | | | | |
| $t_{c(SDC)M3}$ | Cycle time, SDx_Cy | 40 | 256 * SYSCLK period | ns |
| $t_{w(SDCH)M3}$ | Pulse duration, SDx_Cy high | 10 | $t_{c(SDC)M3} - 5$ | ns |
| $t_{su(SDDV-SDCH)M3}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 5 | | ns |
| $t_{h(SDCH-SDD)M3}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 5 | | ns |

WARNING

The SDFM clock inputs (SDx_Cy pins) directly clock the SDFM module when there is no GPIO input synchronization. Any glitches or ringing noise on these inputs can corrupt the SDFM module operation. Special precautions should be taken on these signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination for ringing due to any impedance mismatch of the clock driver and spacing of traces from other noisy signals are recommended.

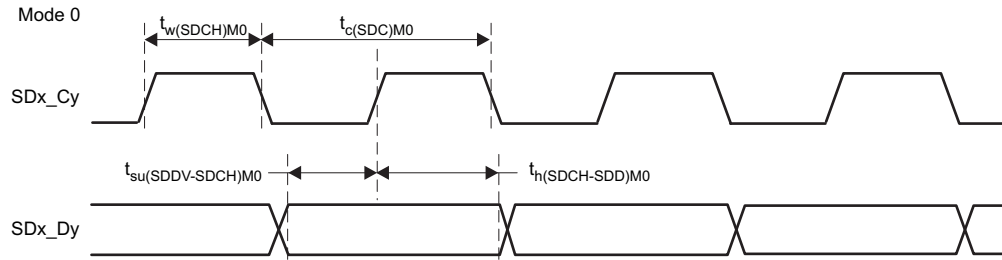


Figure 5-56. SDFM Timing Diagram – Mode 0

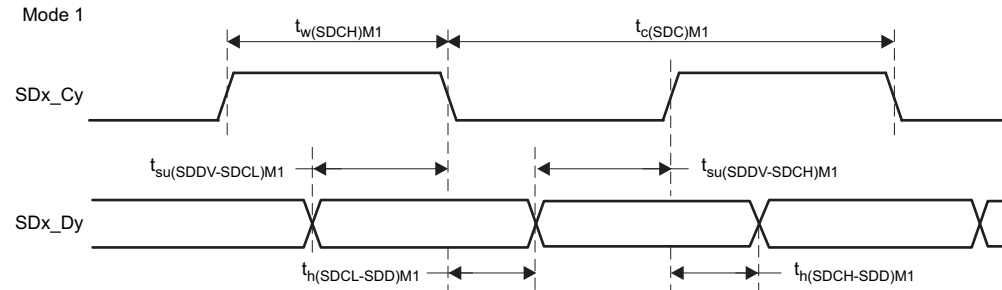


Figure 5-57. SDFM Timing Diagram – Mode 1

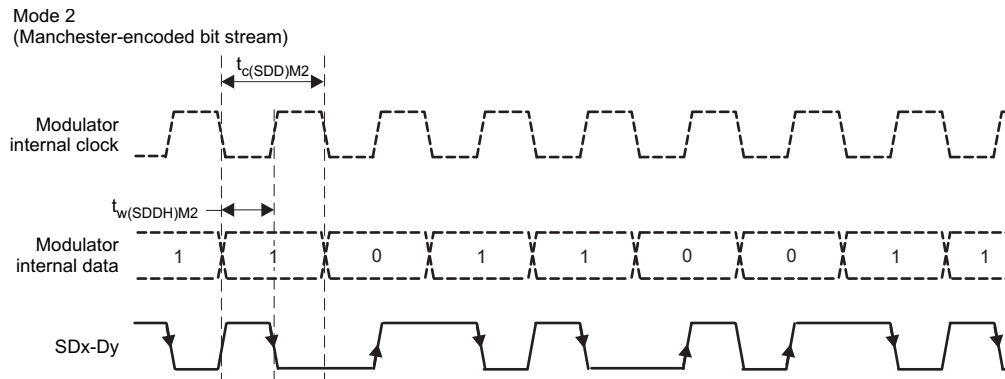


Figure 5-58. SDFM Timing Diagram – Mode 2

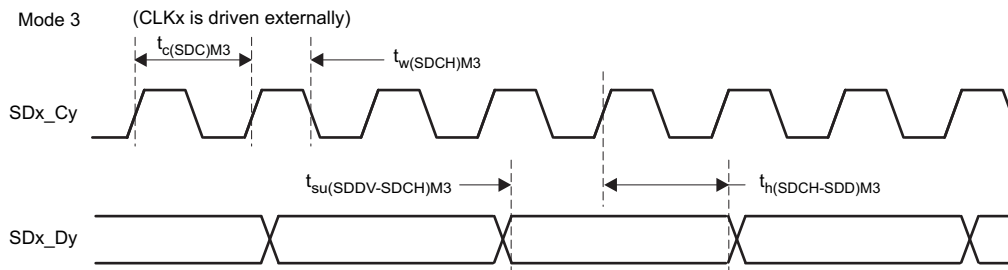


Figure 5-59. SDFM Timing Diagram – Mode 3

5.11.5.2 SDFM Electrical Data and Timing (Using 3-Sample GPIO Input Qualification)

SDFM operation with qualified GPIO (3-sample window) is defined by setting GPyQSELn = 0b01. When using this qualified GPIO (3-sample window) mode, the timing requirement for the $t_{w(GPI)}$ pulse duration of $2t_{c(SYSCLK)}$ must be met. It is important for both SD-Cx and SD-Dx pairs to be configured with the same GPIO qualification option. Table 5-67 lists the SDFM timing requirements when using the GPIO input qualification (3-sample window) option. Figure 5-56 through Figure 5-59 show the SDFM timing diagrams.

Table 5-67. SDFM Timing Requirements When Using GPIO Input Qualification (3-Sample Window⁽¹⁾) Option

| | | MIN | MAX | UNIT |
|-----------------------|--|--------------------|---------------------|------|
| Mode 0 | | | | |
| $t_{c(SDC)}M0$ | Cycle time, SDx_Cy | 10 * SYSCLK period | 256 * SYSCLK period | ns |
| $t_{w(SDCHL)}M0$ | Pulse duration, SDx_Cy high/low | 4 * SYSCLK period | 6 * SYSCLK period | ns |
| $t_{w(SDDHL)}M0$ | Pulse duration, SDx_Dy high/low | 4 * SYSCLK period | | ns |
| $t_{su(SDDV-SDCH)}M0$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 2 * SYSCLK period | | ns |
| $t_h(SDCH-SDD)}M0$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 2 * SYSCLK period | | ns |
| Mode 1 | | | | |
| $t_{c(SDC)}M1$ | Cycle time, SDx_Cy | 20 * SYSCLK period | 256 * SYSCLK period | ns |
| $t_{w(SDCH)}M1$ | Pulse duration, SDx_Cy high | 4 * SYSCLK period | 6 * SYSCLK period | ns |
| $t_{w(SDDHL)}M1$ | Pulse duration, SDx_Dy high/low | 4 * SYSCLK period | | ns |
| $t_{su(SDDV-SDCL)}M1$ | Setup time, SDx_Dy valid before SDx_Cy goes low | 2 * SYSCLK period | | ns |
| $t_{su(SDDV-SDCH)}M1$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 2 * SYSCLK period | | ns |
| $t_h(SDCL-SDD)}M1$ | Hold time, SDx_Dy wait after SDx_Cy goes low | 2 * SYSCLK period | | ns |
| $t_h(SDCH-SDD)}M1$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 2 * SYSCLK period | | ns |
| Mode 2 | | | | |
| $t_{c(SDD)}M2$ | Cycle time, SDx_Dy | Option unavailable | | |
| $t_{w(SDDH)}M2$ | Pulse duration, SDx_Dy high | | | |
| Mode 3 | | | | |
| $t_{c(SDC)}M3$ | Cycle time, SDx_Cy | 10 * SYSCLK period | 256 * SYSCLK period | ns |
| $t_{w(SDCHL)}M3$ | Pulse duration, SDx_Cy high | 4 * SYSCLK period | 6 * SYSCLK period | ns |
| $t_{w(SDDHL)}M3$ | Pulse duration, SDx_Dy high/low | 4 * SYSCLK period | | ns |
| $t_{su(SDDV-SDCH)}M3$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 2 * SYSCLK period | | ns |
| $t_h(SDCH-SDD)}M3$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 2 * SYSCLK period | | ns |

(1) SDFM timing requirements apply only when the GPIO input qualification type is the 3-sample window (GPyQSELx = 1; QUALPRD = 0) option. It is important that both the SD-Cx and SD-Dx pairs be configured with the 3-sample window option.

NOTE

The SDFM Qualified GPIO (3-sample) mode provides protection against SDFM module corruption due to occasional random noise glitches on the SDx_Cy pin that may result in a false comparator trip and filter output.

The SDFM Qualified GPIO (3-sample) mode does not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

5.12 Communications Peripherals

NOTE

For the actual number of each peripheral on a specific device, see [Table 3-1](#).

5.12.1 Controller Area Network (CAN)

The CAN module performs CAN protocol communication according to ISO 11898-1 (identical to Bosch® CAN protocol specification 2.0 A, B). The bit rate can be programmed to values up to 1 Mbps. A CAN transceiver chip is required for the connection to the physical layer (CAN bus).

For communication on a CAN network, individual message objects can be configured. The message objects and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the message handler. These functions are: acceptance filtering; the transfer of messages between the CAN Core and the Message RAM; and the handling of transmission requests.

The register set of the CAN may be accessed directly by the CPU through the module interface. These registers are used to control and configure the CAN core and the message handler, and to access the message RAM.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (“message objects” are also referred to as “mailboxes” in this document; the two terms are used interchangeably), each with the following properties:
 - Configurable as receive or transmit
 - Configurable with standard (11-bit) or extended (29-bit) identifier
 - Supports programmable identifier receive mask
 - Supports data and remote frames
 - Holds 0 to 8 bytes of data
 - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus-on, after bus-off state by a programmable 32-bit timer
- Message-RAM parity-check mechanism
- Two interrupt lines

NOTE

For a CAN bit clock of 200 MHz, the smallest bit rate possible is 7.8125 kbps.

NOTE

Depending on the timing settings used, the accuracy of the on-chip zero-pin oscillator (specified in the data manual) may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 5-60 shows the CAN block diagram.

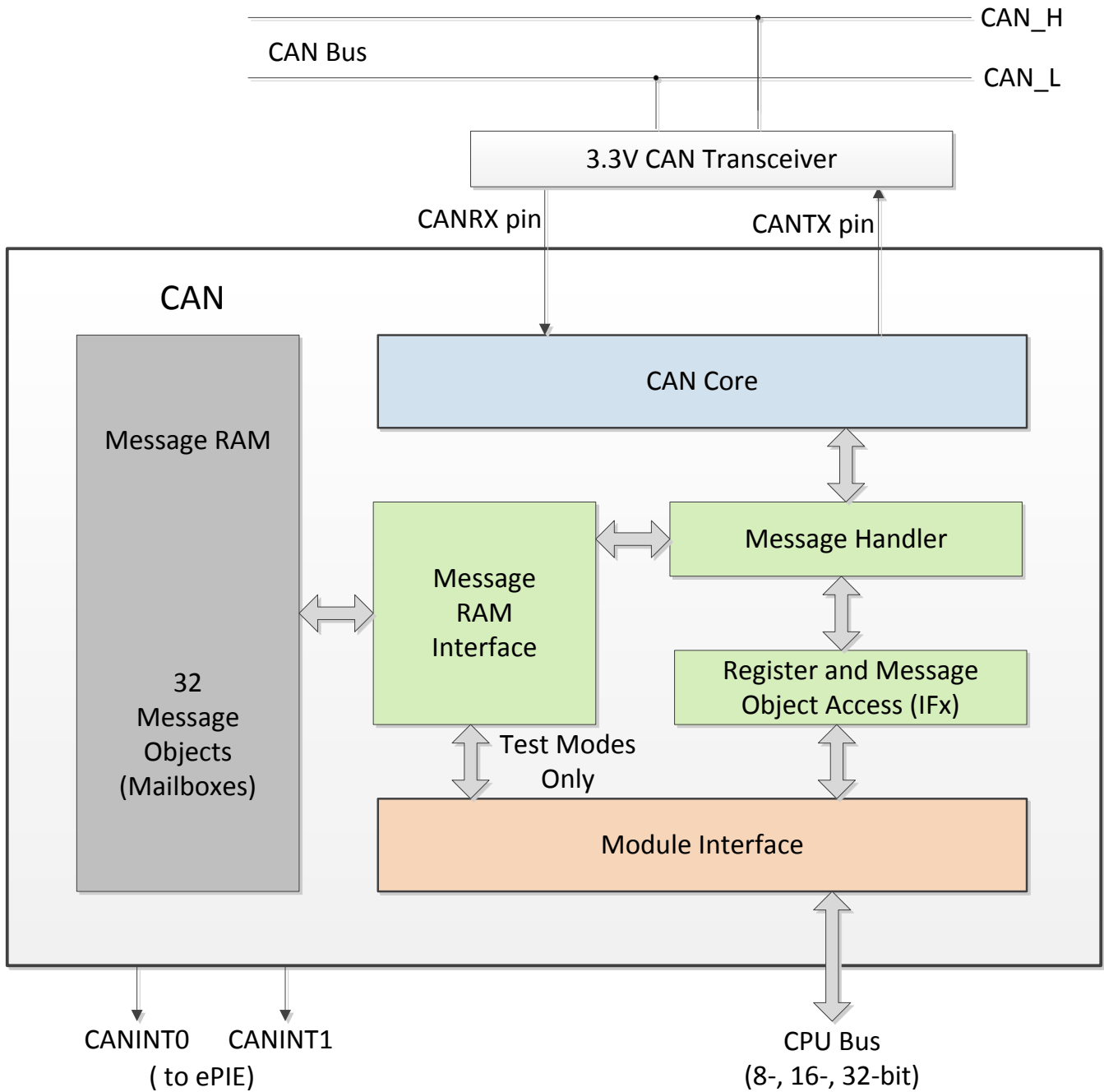


Figure 5-60. CAN Block Diagram

5.12.2 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the Philips Semiconductors I²C-bus specification (version 2.1):
 - Support for 1-bit to 8-bit format transfers
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple master-transmitters and slave-receivers
 - Support for multiple slave-transmitters and master-receivers
 - Combined master transmit/receive and receive/transmit mode
 - Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
 - Transmit-data ready
 - Receive-data ready
 - Register-access ready
 - No-acknowledgment received
 - Arbitration lost
 - Stop condition detected
 - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

Figure 5-61 shows how the I2C peripheral module interfaces within the device.

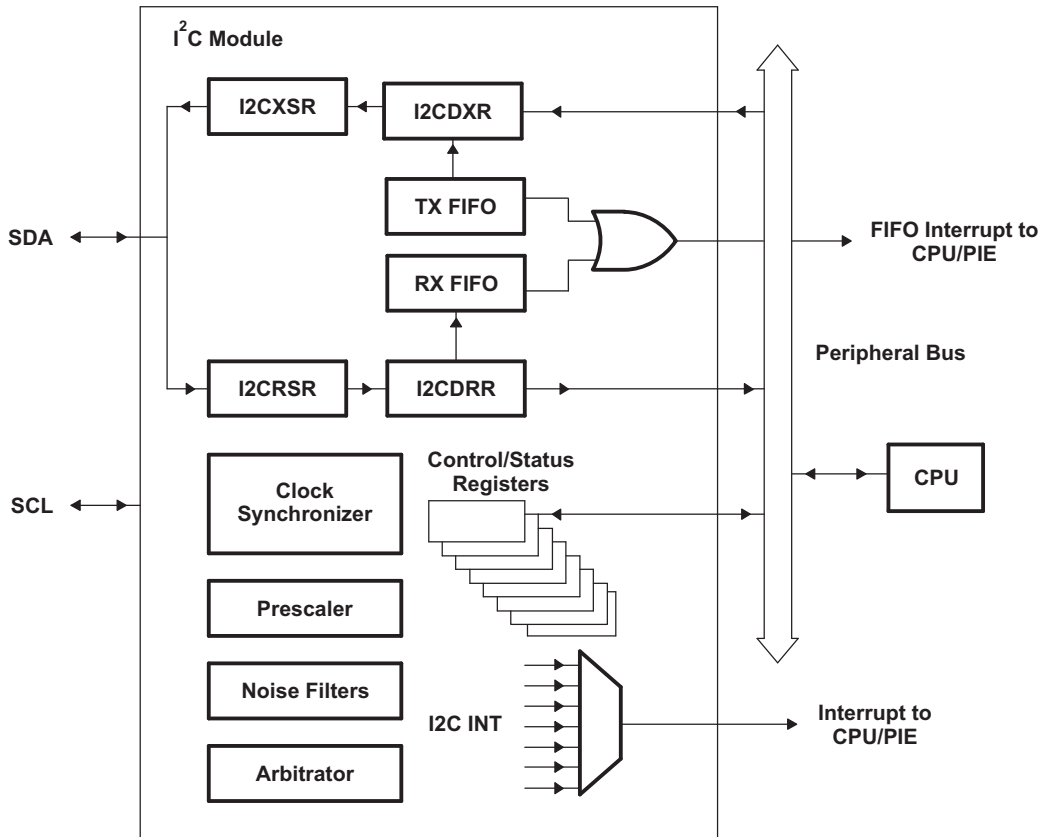


Figure 5-61. I2C Peripheral Module Interfaces

5.12.2.1 I2C Electrical Data and Timing

Table 5-68 shows the I2C timing requirements. Table 5-69 shows the I2C switching characteristics.

Table 5-68. I2C Timing Requirements

| | | MIN | MAX | UNIT |
|------------------------|--|-----------------|-----|---------|
| $t_{h(SDA-SCL)START}$ | Hold time, START condition, SCL fall delay after SDA fall | 0.6 | | μs |
| $t_{su(SCL-SDA)START}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 0.6 | | μs |
| $t_h(SCL-DAT)$ | Hold time, data after SCL fall | 0 | | μs |
| $t_{su}(DAT-SCL)$ | Setup time, data before SCL rise | 100 | | ns |
| $t_r(SDA)$ | Rise time, SDA | Input tolerance | 300 | ns |
| $t_r(SCL)$ | Rise time, SCL | Input tolerance | 300 | ns |
| $t_f(SDA)$ | Fall time, SDA | Input tolerance | 300 | ns |
| $t_f(SCL)$ | Fall time, SCL | Input tolerance | 300 | ns |
| $t_{su}(SCL-SDA)STOP$ | Setup time, STOP condition, SCL rise before SDA rise delay | 0.6 | | μs |

Table 5-69. I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------|--|-----------------------------------|------------------|---------|
| f_{SCL} | SCL clock frequency | 0 | 400 | kHz |
| $t_w(SCLL)$ | Pulse duration, SCL clock low | 1.3 | | μs |
| $t_w(SCLH)$ | Pulse duration, SCL clock high | 0.6 | | μs |
| $t_w(SP)$ | Pulse duration of spikes that will be suppressed by the input filter | 0 | 50 | ns |
| t_{BUF} | Bus free time between STOP and START conditions | 1.3 | | μs |
| $t_v(SCL-DAT)$ | Valid time, data after SCL fall | | 0.9 | μs |
| $t_v(SCL-ACK)$ | Valid time, Acknowledge after SCL fall | | 0.9 | μs |
| V_{IL} | Valid low-level input voltage | -0.3 | $0.3 * V_{DDIO}$ | V |
| V_{IH} | Valid high-level input voltage | $0.7 * V_{DDIO}$ | $V_{DDIO} + 0.3$ | V |
| V_{OL} | Low-level output voltage | Sinking 3 mA | 0.4 | V |
| I_i | Input current on pins | $0.1 V_{bus} < V_i < 0.9 V_{bus}$ | 10 | μA |

NOTE

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured from 7 MHz to 12 MHz.

5.12.3 Multichannel Buffered Serial Port (McBSP)

The McBSP module has the following features:

- Compatible with McBSP in TMS320C28x and TMS320F28x DSP devices
- Full-duplex communication
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- 8-bit data transfer mode can be configured to transmit with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Supports AC97, I2S, and SPI protocols
- McBSP clock rate,

$$\text{CLKG} = \frac{\text{CLKSRG}}{(1 + \text{CLKGDV})}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR.

Figure 5-62 shows the block diagram of the McBSP module.

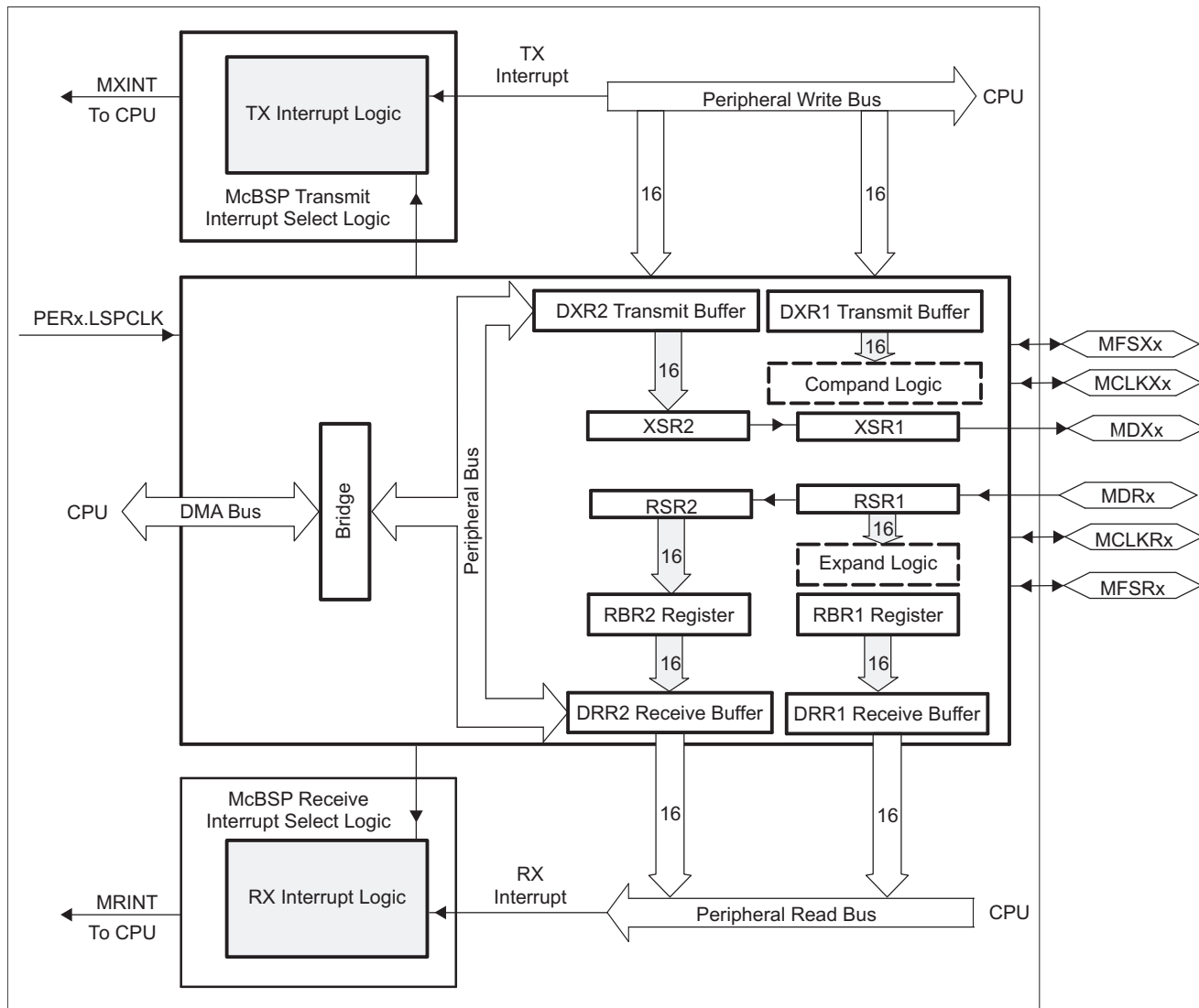


Figure 5-62. McBSP Block Diagram

5.12.3.1 McBSP Electrical Data and Timing

5.12.3.1.1 McBSP Transmit and Receive Timing

Table 5-70 shows the McBSP timing requirements. Table 5-71 shows the McBSP switching characteristics. Figure 5-63 and Figure 5-64 show the McBSP timing diagrams.

Table 5-70. McBSP Timing Requirements^{(1) (2)}

| NO. | | | MIN | MAX | UNIT |
|-----|--|---|------------|-------|------|
| | McBSP module clock (CLKG, CLKX, CLKR) range | | 1 | | kHz |
| | | | | 25 | MHz |
| | McBSP module cycle time (CLKG, CLKX, CLKR) range | | 40 | | ns |
| | | | | 1 | ms |
| M11 | $t_{c(CLKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P | ns |
| M12 | $t_{w(CLKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P – 7 | ns |
| M13 | $t_{r(CLKRX)}$ | Rise time, CLKR/X | CLKR/X ext | 7 | ns |
| M14 | $t_{f(CLKRX)}$ | Fall time, CLKR/X | CLKR/X ext | 7 | ns |
| M15 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 18 | ns |
| | | | CLKR ext | 2 | |
| M16 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 0 | ns |
| | | | CLKR ext | 6 | |
| M17 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 18 | ns |
| | | | CLKR ext | 5 | |
| M18 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 0 | ns |
| | | | CLKR ext | 3 | |
| M19 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 18 | ns |
| | | | CLKX ext | 2 | |
| M20 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | 0 | ns |
| | | | CLKX ext | 6 | |

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

(2) $2P = 1/CLKG$ in ns. CLKG is the output of sample rate generator mux. $CLKG = CLKSRG / (1 + CLKGDV)$. CLKSRG can be LSPCLK, CLKX, CLKR as source. $CLKSRG \leq (SYSCLK/2)$.

Table 5-71. McBSP Switching Characteristics^{(1) (2)}

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | | MIN | MAX | UNIT | |
|-----------|----------------------|---|------------|---------------|---------------|------|--|
| M1 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P | | ns | |
| M2 | $t_{w(CKRXH)}$ | Pulse duration, CLKR/X high | CLKR/X int | $D - 5^{(3)}$ | $D + 5^{(3)}$ | ns | |
| M3 | $t_{w(CKRXL)}$ | Pulse duration, CLKR/X low | CLKR/X int | $C - 5^{(3)}$ | $C + 5^{(3)}$ | ns | |
| M4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | 0 | 4 | ns | |
| | | | CLKR ext | 3 | 27 | | |
| M5 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | 0 | 4 | ns | |
| | | | CLKX ext | 3 | 27 | | |
| M6 | $t_{dis(CKXH-DXHZ)}$ | Disable time, CLKX high to DX high impedance following last data bit | CLKX int | 8 | | ns | |
| | | | CLKX ext | 14 | | | |
| M7 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted. | CLKX int | 9 | | ns | |
| | | | CLKX ext | 28 | | | |
| | | Delay time, CLKX high to DX valid Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes | DXENA = 0 | CLKX int | 8 | | |
| | | | | CLKX ext | 14 | | |
| DXENA = 1 | CLKX int | P + 8 | | | | | |
| | CLKX ext | P + 14 | | | | | |
| M8 | $t_{en(CKXH-DX)}$ | Enable time, CLKX high to DX driven Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes | DXENA = 0 | CLKX int | 0 | ns | |
| | | | | CLKX ext | 6 | | |
| | | DXENA = 1 | CLKX int | P | | | |
| | | | CLKX ext | P + 6 | | | |
| M9 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode. | DXENA = 0 | FSX int | 8 | ns | |
| | | | | FSX ext | 14 | | |
| | | DXENA = 1 | FSX int | P + 8 | | | |
| | | | FSX ext | P + 14 | | | |
| M10 | $t_{en(FXH-DX)}$ | Enable time, FSX high to DX driven Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode | DXENA = 0 | FSX int | 0 | ns | |
| | | | | FSX ext | 6 | | |
| | | DXENA = 1 | FSX int | P | | | |
| | | | FSX ext | P + 6 | | | |

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

(2) $2P = 1/CLKG$ in ns.

(3) C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

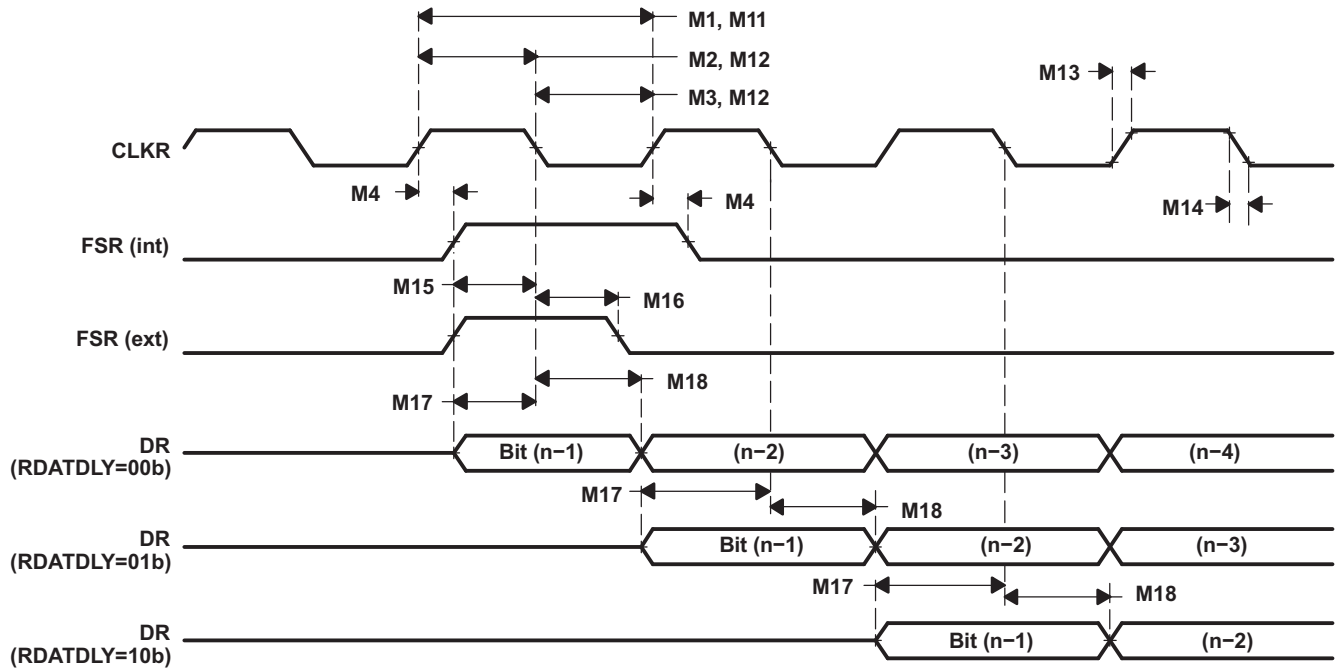


Figure 5-63. McBSP Receive Timing

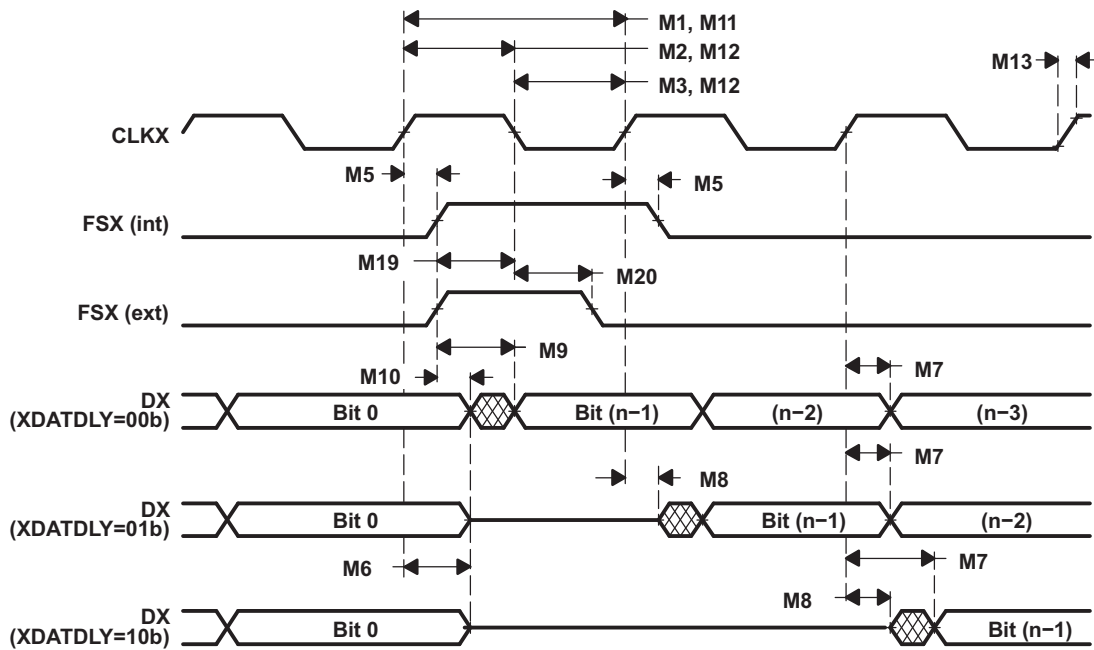


Figure 5-64. McBSP Transmit Timing

5.12.3.1.2 McBSP as SPI Master or Slave Timing

For CLKSTP = 10b and CLKXP = 0, Table 5-72 shows the timing requirements, Table 5-73 shows the switching characteristics, and Figure 5-65 shows the timing diagram.

Table 5-72. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)⁽¹⁾

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|-----------------------------|--------------------------------------|-------------------|-----|---------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M30 | t _{su} (DRV-CKXL) | Setup time, DR valid before CLKX low | 30 | | 8P – 10 | | ns |
| M31 | t _h (CKXL-DRV) | Hold time, DR valid after CLKX low | 1 | | 8P – 10 | | ns |
| M32 | t _{su} (BFXL-CKXH) | Setup time, FSX low before CLKX high | | | 8P + 10 | | ns |
| M33 | t _c (CKX) | Cycle time, CLKX | 2P ⁽²⁾ | | 16P | | ns |

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.

(2) 2P = 1/CLKG

Table 5-73. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)

| NO. | PARAMETER | MASTER | | SLAVE | | UNIT |
|-----|-----------------------------|-------------------|-----|--------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| M24 | t _h (CKXL-FXL) | 2P ⁽¹⁾ | | | | ns |
| M25 | t _d (FXL-CKXH) | P | | | | ns |
| M28 | t _{dis} (FXH-DXHZ) | 6 | | 6P + 6 | | ns |
| M29 | t _d (FXL-DXV) | 6 | | 4P + 6 | | ns |

(1) 2P = 1/CLKG

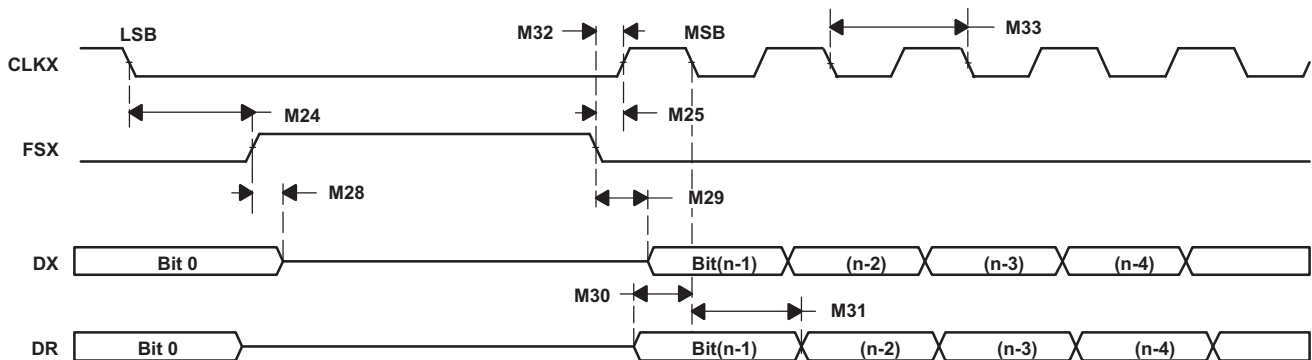


Figure 5-65. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

For CLKSTP = 11b and CLKXP = 0, Table 5-74 shows the timing requirements, Table 5-75 shows the switching characteristics, and Figure 5-66 shows the timing diagram.

Table 5-74. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)⁽¹⁾

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|--------------------|---------------------------------------|-------------------|-----|----------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M39 | $t_{su(DRV-CKXH)}$ | Setup time, DR valid before CLKX high | 30 | | 8P – 10 | | ns |
| M40 | $t_h(CKXH-DRV)$ | Hold time, DR valid after CLKX high | 1 | | 8P – 10 | | ns |
| M41 | $t_{su(FXL-CKXH)}$ | Setup time, FSX low before CLKX high | | | 16P + 10 | | ns |
| M42 | $t_c(CKX)$ | Cycle time, CLKX | 2P ⁽²⁾ | | 16P | | ns |

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.

(2) 2P = 1/CLKG

Table 5-75. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)

| NO. | PARAMETER | MASTER | | SLAVE | | UNIT |
|-----|---------------------|-------------------|-----|--------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| M34 | $t_h(CKXL-FXL)$ | P | | | | ns |
| M35 | $t_d(FXL-CKXH)$ | 2P ⁽¹⁾ | | | | ns |
| M37 | $t_{dis}(CKXL-DXH)$ | P + 6 | | 7P + 6 | | ns |
| M38 | $t_d(FXL-DXV)$ | 6 | | 4P + 6 | | ns |

(1) 2P = 1/CLKG

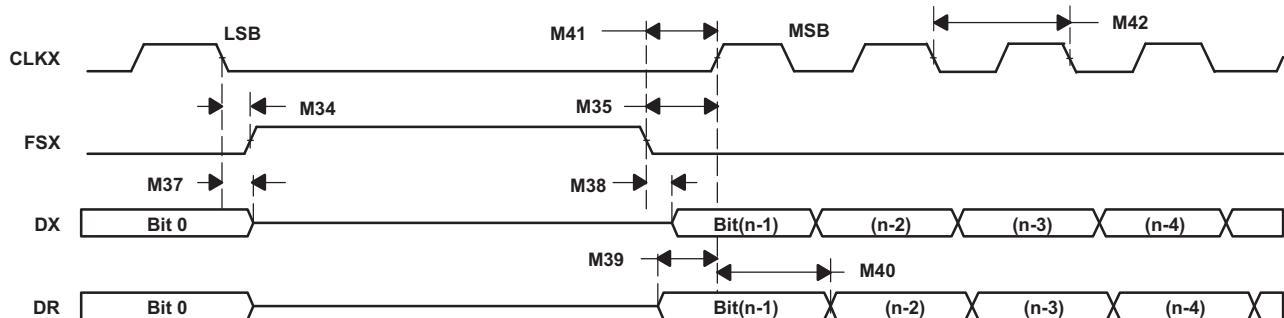


Figure 5-66. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

For CLKSTP = 10b and CLKXP = 1, Table 5-76 shows the timing requirements, Table 5-77 shows the switching characteristics, and Figure 5-67 shows the timing diagram.

Table 5-76. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)⁽¹⁾

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|--------------------|---------------------------------------|-------------------|-----|---------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M49 | $t_{su}(DRV-CKXH)$ | Setup time, DR valid before CLKX high | 30 | | 8P – 10 | | ns |
| M50 | $t_h(CKXH-DRV)$ | Hold time, DR valid after CLKX high | 1 | | 8P – 10 | | ns |
| M51 | $t_{su}(FXL-CKXL)$ | Setup time, FSX low before CLKX low | | | 8P + 10 | | ns |
| M52 | $t_c(CKX)$ | Cycle time, CLKX | 2P ⁽²⁾ | | 16P | | ns |

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.

(2) 2P = 1/CLKG

Table 5-77. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)

| NO. | PARAMETER | MASTER | | SLAVE | | UNIT |
|-----|---------------------|-------------------|-----|--------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| M43 | $t_h(CKXH-FXL)$ | 2P ⁽¹⁾ | | | | ns |
| M44 | $t_d(FXL-CKXL)$ | P | | | | ns |
| M47 | $t_{dis}(FXH-DXHZ)$ | 6 | | 6P + 6 | | ns |
| M48 | $t_d(FXL-DXV)$ | 6 | | 4P + 6 | | ns |

(1) 2P = 1/CLKG

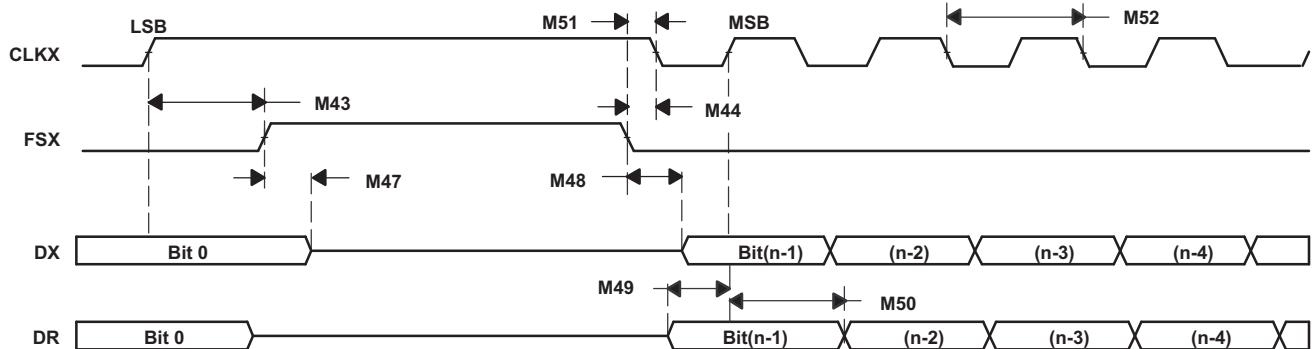


Figure 5-67. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

For CLKSTP = 11b and CLKXP = 1, Table 5-78 shows the timing requirements, Table 5-79 shows the switching characteristics, and Figure 5-68 shows the timing diagram.

Table 5-78. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)⁽¹⁾

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|--------------------|--------------------------------------|-------------------|-----|----------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M58 | $t_{su(DRV-CKXL)}$ | Setup time, DR valid before CLKX low | 30 | | 8P – 10 | | ns |
| M59 | $t_h(CKXL-DRV)$ | Hold time, DR valid after CLKX low | 1 | | 8P – 10 | | ns |
| M60 | $t_{su(FXL-CKXL)}$ | Setup time, FSX low before CLKX low | | | 16P + 10 | | ns |
| M61 | $t_c(CKX)$ | Cycle time, CLKX | 2P ⁽²⁾ | | 16P | | ns |

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.

(2) 2P = 1/CLKG

Table 5-79. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)⁽¹⁾

| NO. | PARAMETER | MASTER ⁽²⁾ | | SLAVE | | UNIT | |
|-----|----------------------|--|-------------------|-------|--------|---------|----|
| | | MIN | MAX | MIN | MAX | | |
| M53 | $t_h(CKXH-FXL)$ | Hold time, FSX low after CLKX high | P | | | ns | |
| M54 | $t_d(FXL-CKXL)$ | Delay time, FSX low to CLKX low | 2P ⁽¹⁾ | | | ns | |
| M55 | $t_d(CLKXH-DXV)$ | Delay time, CLKX high to DX valid | -2 | 0 | 3P + 6 | 5P + 20 | ns |
| M56 | $t_{dis}(CKXH-DXHZ)$ | Disable time, DX high impedance following last data bit from CLKX high | P + 6 | | 7P + 6 | | ns |
| M57 | $t_d(FXL-DXV)$ | Delay time, FSX low to DX valid | 6 | | 4P + 6 | | ns |

(1) 2P = 1/CLKG

(2) C = CLKX low pulse width = P

D = CLKX high pulse width = P

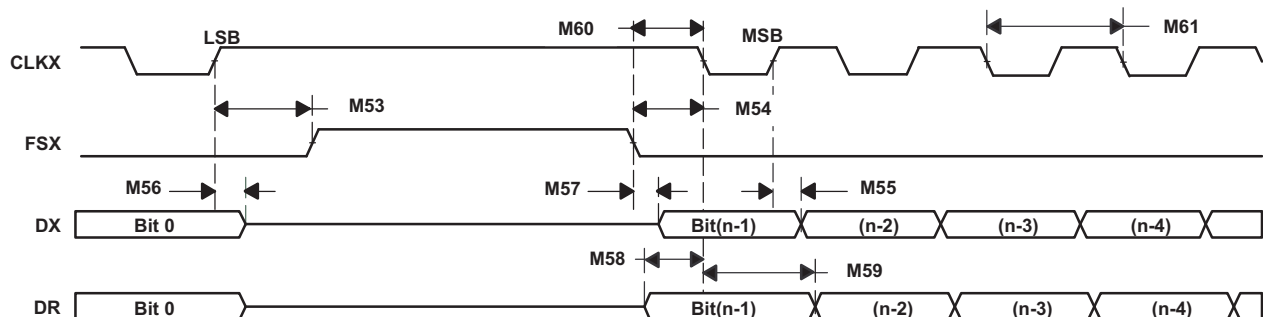


Figure 5-68. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.12.4 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register. [Figure 5-69](#) shows the SCI block diagram.

Features of the SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
 - NOTE:** Both pins can be used as GPIO if not used for SCI.
 - Baud rate programmable to 64K different rates
- Data-word format
 - One start bit
 - Data-word length programmable from 1 to 8 bits
 - Optional even/odd/no parity bit
 - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wakeup multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
 - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
 - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

NOTE

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

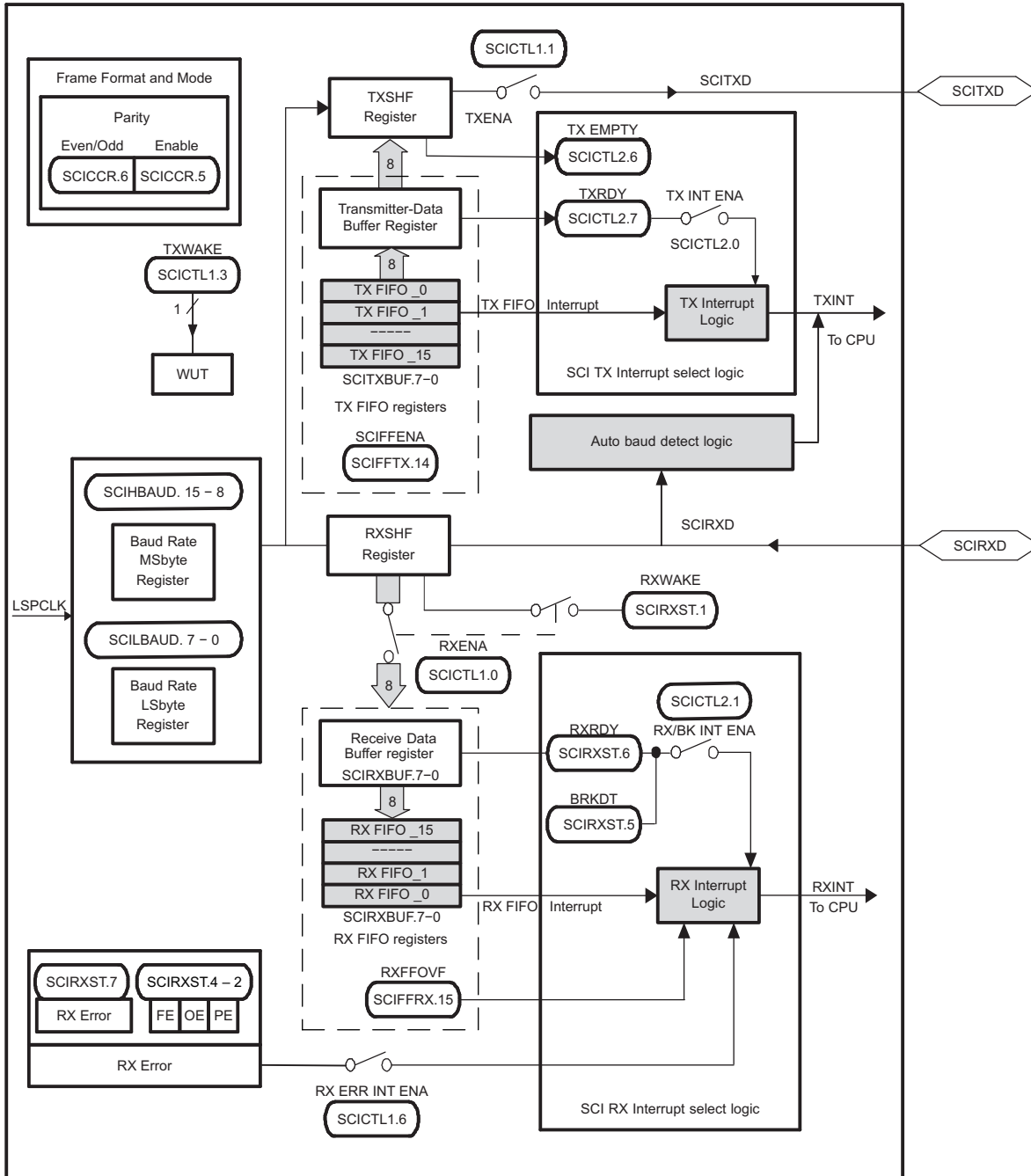


Figure 5-69. SCI Block Diagram

The major elements used in full-duplex operation include:

- A transmitter (TX) and its major registers:
 - SCITXBUF register – Transmitter Data Buffer register. Contains data (loaded by the CPU) to be transmitted
 - TXSHF register – Transmitter Shift register. Accepts data from the SCITXBUF register and shifts data onto the SCITXD pin, 1 bit at a time
- A receiver (RX) and its major registers:
 - RXSHF register – Receiver Shift register. Shifts data in from the SCIRXD pin, 1 bit at a time
 - SCIRXBUF register – Receiver Data Buffer register. Contains data to be read by the CPU. Data from a remote processor is loaded into the RXSHF register and then into the SCIRXBUF and SCIRXEMU registers
- A programmable baud generator
- Data-memory-mapped control and status registers enable the CPU to access the I2C module registers and FIFOs.

The SCI receiver and transmitter operate independently.

5.12.5 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI. The port supports 16-level receive and transmit FIFOs for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive-and-transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- 16-level transmit and receive FIFO
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules
- DMA support
- High-speed mode for up to 50-MHz full-duplex communication

The SPI operates in master or slave mode. The master initiates data transfer by sending the SPICLK signal. For both the slave and the master, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. If the CLOCK PHASE bit (SPICTL.3) is high, data is transmitted and received a half-cycle before the SPICLK transition. As a result, both controllers send and receive data simultaneously. The application software determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Master sends data; slave sends dummy data
- Master sends data; slave sends data
- Master sends dummy data; slave sends data

The master can initiate a data transfer at any time because it controls the SPICLK signal. The software, however, determines how the master detects when the slave is ready to broadcast data.

Figure 5-70 shows the SPI CPU Interface.

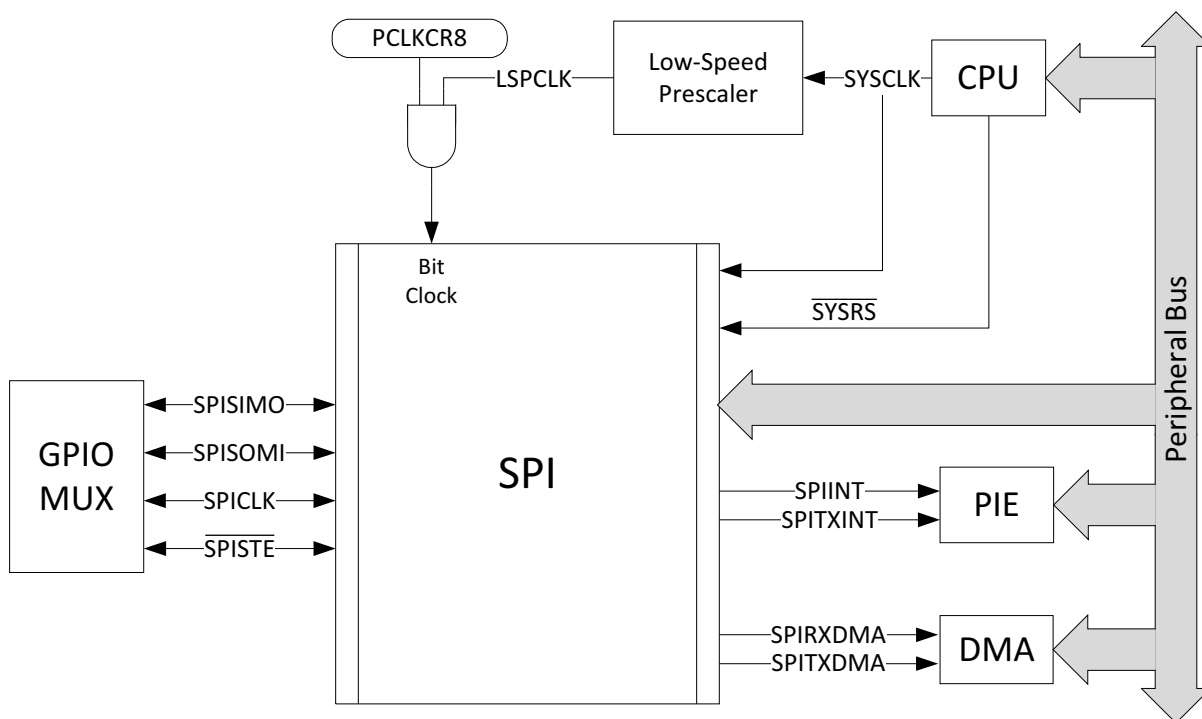


Figure 5-70. SPI CPU Interface

5.12.5.1 SPI Electrical Data and Timing

The following sections contain the SPI External Timings in Non-High-Speed Mode:

[Section 5.12.5.1.1](#) Non-High-Speed Master Mode Timings

[Section 5.12.5.1.2](#) Non-High-Speed Slave Mode Timings

The following sections contain the SPI External Timings in High-Speed Mode:

[Section 5.12.5.1.3](#) High-Speed Master Mode Timings

[Section 5.12.5.1.4](#) High-Speed Slave Mode Timings

NOTE

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

To use the SPI in High-Speed mode, the application must use the high-speed enabled GPIOs (see [Section 4.4.5](#)).

5.12.5.1.1 Non-High-Speed Master Mode Timings

Table 5-80 lists the SPI master mode switching characteristics where the clock phase = 0. Figure 5-71 shows the SPI master mode external timing where the clock phase = 0.

Table 5-81 lists the SPI master mode switching characteristics where the clock phase = 1. Figure 5-72 shows the SPI master mode external timing where the clock phase = 1.

Table 5-82 lists the SPI master mode timing requirements.

Table 5-80. SPI Master Mode Switching Characteristics (Clock Phase = 0)

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | (BRR + 1) CONDITION ⁽¹⁾ | MIN | MAX | UNIT |
|-----|--|---------------------------------------|---|---|------|
| 1 | $t_{c(SPC)M}$ Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$ | |
| 3 | $t_{w(SPC2)M}$ Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | |
| 4 | $t_{d(SIMO)M}$ Delay time, SPICLK to SPISIMO valid | Even, Odd | | 3 | ns |
| 5 | $t_{v(SIMO)M}$ Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 23 | $t_{d(SPC)M}$ Delay time, \overline{SPISTE} active to SPICLK | Even | $t_{c(SPC)M} - 3$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 24 | $t_{d(STE)M}$ Delay time, SPICLK to \overline{SPISTE} inactive | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

Table 5-81. SPI Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

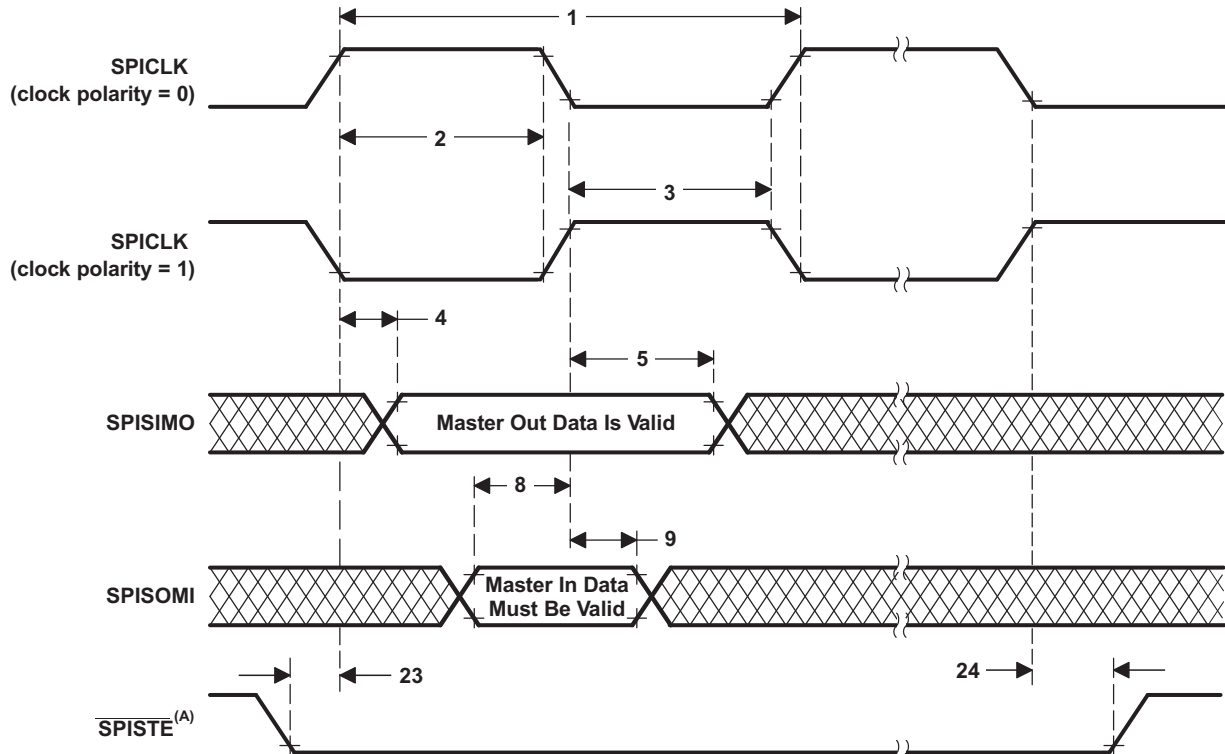
| NO. | PARAMETER | (BRR + 1) CONDITION ⁽¹⁾ | MIN | MAX | UNIT |
|-----|--|------------------------------------|---|---|------|
| 1 | $t_{c(SPC)M}$ Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | |
| 3 | $t_{w(SPC2)M}$ Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$ | |
| 4 | $t_{d(SIMO)M}$ Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$ | | |
| 5 | $t_{v(SIMO)M}$ Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 23 | $t_{d(SPC)M}$ Delay time, \overline{SPISTE} active to SPICLK | Even, Odd | $t_{c(SPC)M} - 3$ | | ns |
| 24 | $t_{d(STE)M}$ Delay time, SPICLK to \overline{SPISTE} inactive | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

Table 5-82. SPI Master Mode Timing Requirements

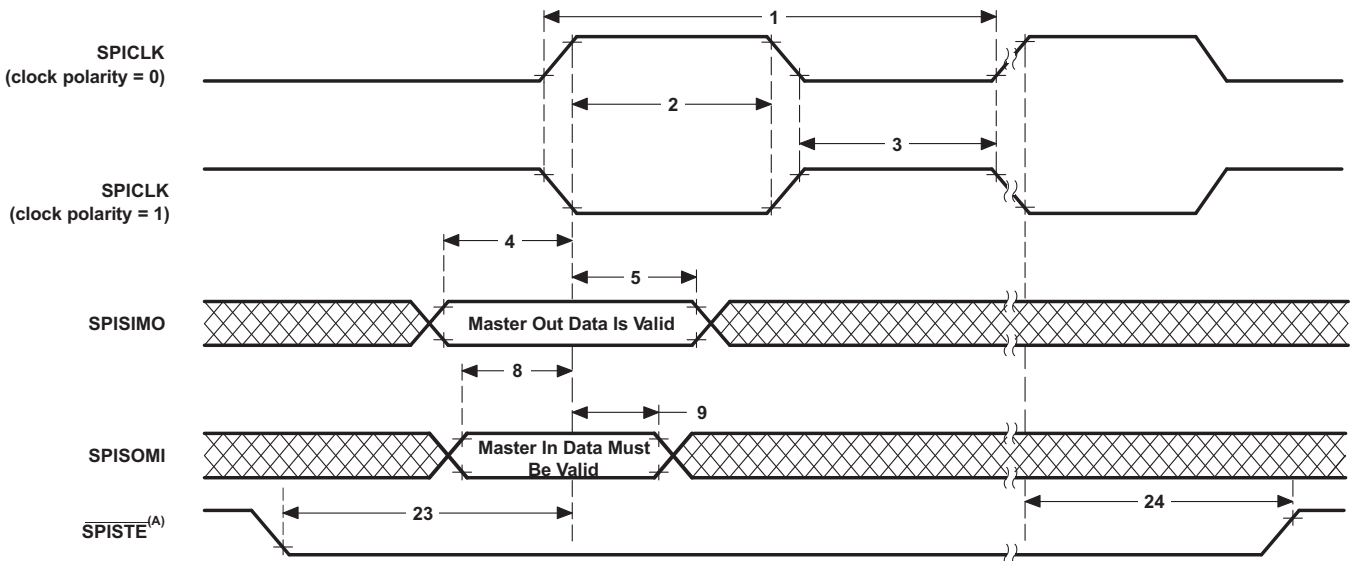
| NO. | PARAMETER | (BRR + 1) CONDITION ⁽¹⁾ | MIN | MAX | UNIT |
|-----|---|------------------------------------|-----|-----|------|
| 8 | $t_{su(SOMI)M}$ Setup time, SPISOMI valid before SPICLK | Even, Odd | 20 | | ns |
| 9 | $t_h(SOMI)M$ Hold time, SPISOMI valid after SPICLK | Even, Odd | 0 | | ns |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.



- A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 5-71. SPI Master Mode External Timing (Clock Phase = 0)



- A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 5-72. SPI Master Mode External Timing (Clock Phase = 1)

5.12.5.1.2 Non-High-Speed Slave Mode Timings

Table 5-83 lists the SPI slave mode switching characteristics. Table 5-84 lists the SPI slave mode timing requirements.

Figure 5-73 shows the SPI slave mode external timing where the clock phase = 0. Figure 5-74 shows the SPI slave mode external timing where the clock phase = 1.

Table 5-83. SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 15 | $t_{d(SOMI)S}$ Delay time, SPICLK to SPISOMI valid | | 20 | ns |
| 16 | $t_{v(SOMI)S}$ Valid time, SPISOMI valid after SPICLK | 0 | | ns |

Table 5-84. SPI Slave Mode Timing Requirements

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|----------------------|-----|------|
| 12 | $t_{c(SPC)S}$ Cycle time, SPICLK | $4t_{c(SYSCLK)}$ | | ns |
| 13 | $t_{w(SPC1)S}$ Pulse duration, SPICLK, first pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 14 | $t_{w(SPC2)S}$ Pulse duration, SPICLK, second pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 19 | $t_{su(SIMO)S}$ Setup time, SPISIMO valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 20 | $t_{h(SIMO)S}$ Hold time, SPISIMO valid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 25 | $t_{su(STE)S}$ Setup time, \overline{SPISTE} active before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 26 | $t_{h(STE)S}$ Hold time, \overline{SPISTE} inactive after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |

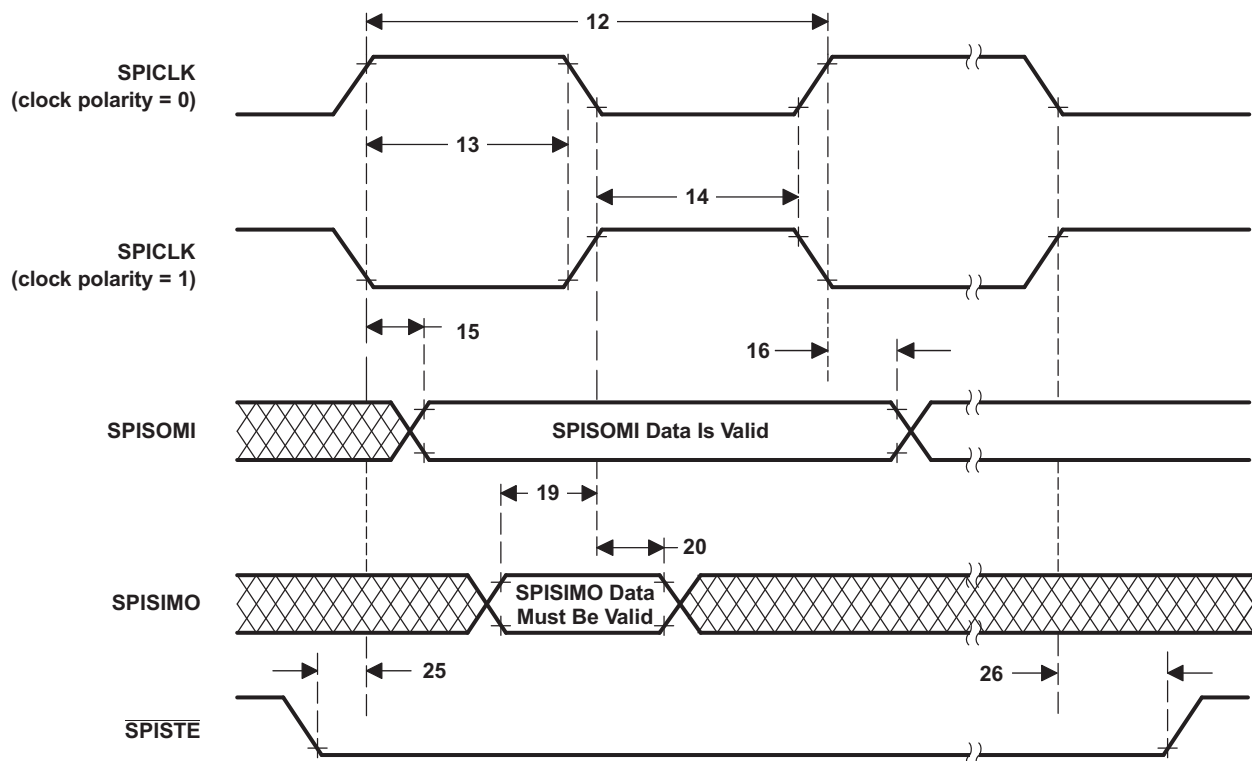


Figure 5-73. SPI Slave Mode External Timing (Clock Phase = 0)

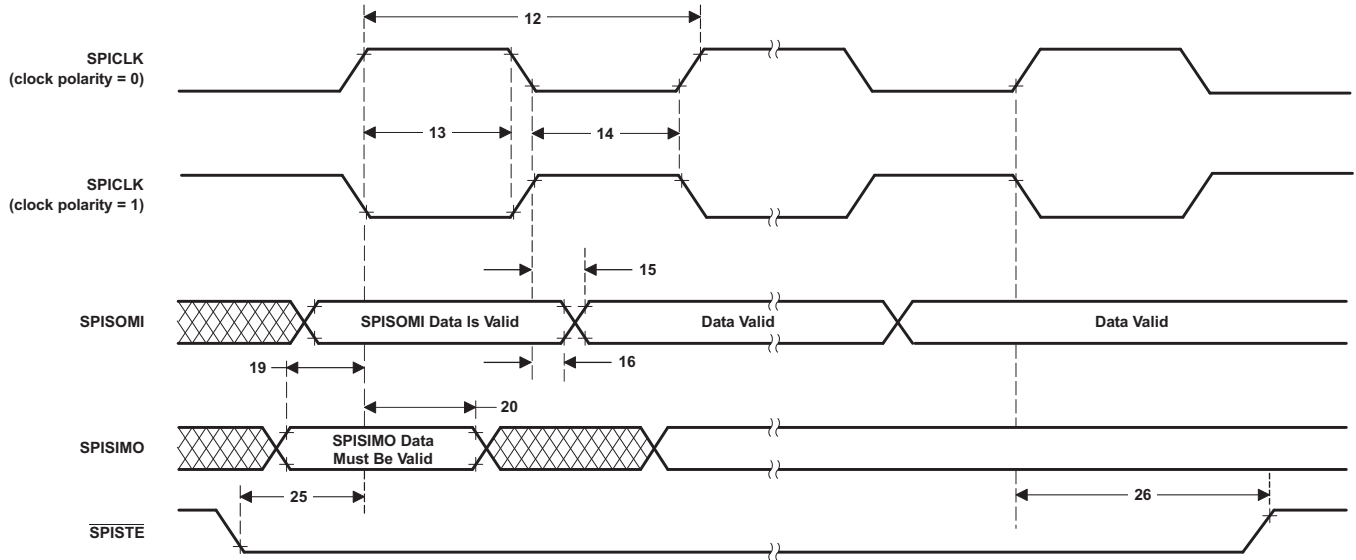


Figure 5-74. SPI Slave Mode External Timing (Clock Phase = 1)

5.12.5.1.3 High-Speed Master Mode Timings

Table 5-85 lists the SPI high-speed master mode switching characteristics where the clock phase = 0. Figure 5-75 shows the high-speed SPI master mode external timing where the clock phase = 0.

Table 5-86 lists the SPI high-speed master mode switching characteristics where the clock phase = 1. Figure 5-76 shows the high-speed SPI master mode external timing where the clock phase = 1.

Table 5-87 lists the SPI high-speed master mode timing requirements.

Table 5-85. SPI High-Speed Master Mode Switching Characteristics (Clock Phase = 0)

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | (BRR + 1) CONDITION ⁽¹⁾ | MIN | MAX | UNIT |
|-----|--|------------------------------------|---|---|------|
| 1 | $t_{c(SPC)M}$ Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 4 | $t_{d(SIMO)M}$ Delay time, SPICLK to SPISIMO valid | Even, Odd | | 1 | ns |
| 5 | $t_{v(SIMO)M}$ Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 1$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |
| 23 | $t_{d(SPC)M}$ Delay time, \overline{SPISTE} active to SPICLK | Even | $t_{c(SPC)M} - 1$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |
| 24 | $t_{d(STE)M}$ Delay time, SPICLK to \overline{SPISTE} inactive | Even | $0.5t_{c(SPC)M} - 1$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

Table 5-86. SPI High-Speed Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

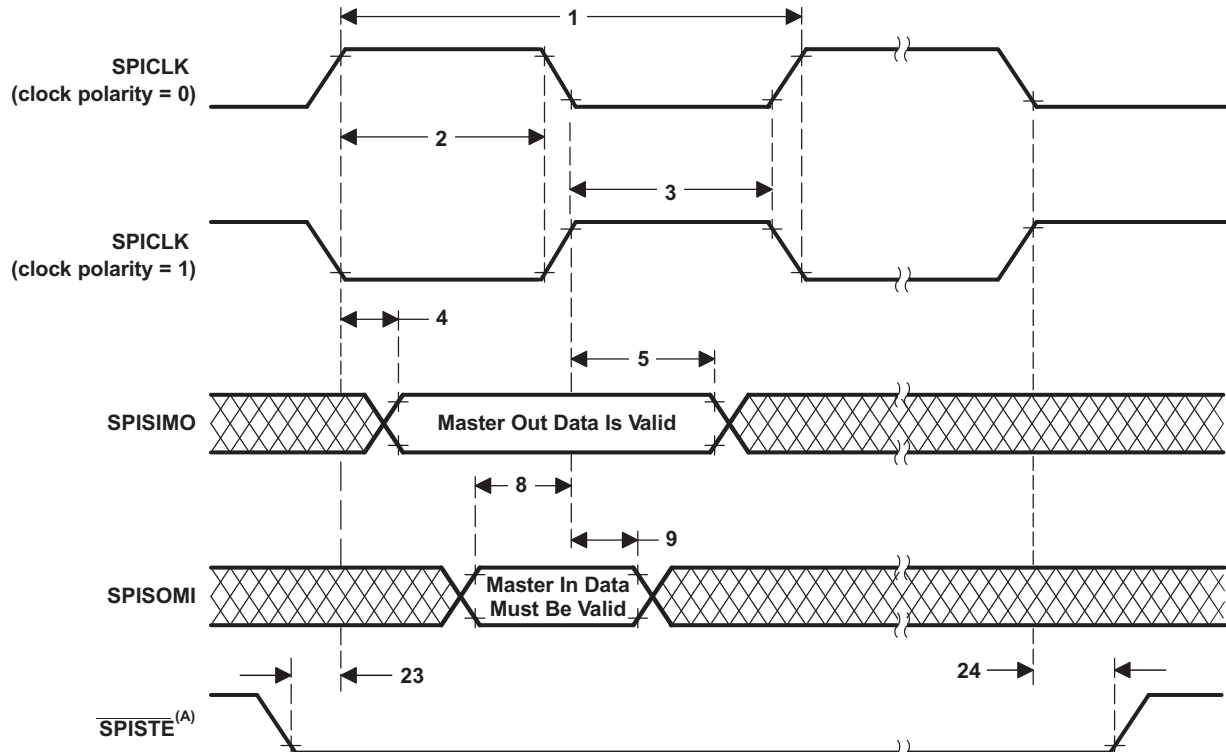
| NO. | PARAMETER | (BRR + 1) CONDITION ⁽¹⁾ | MIN | MAX | UNIT |
|-----|--|---------------------------------------|---|---|------|
| 1 | $t_{c(SPC)M}$ Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 4 | $t_{d(SIMO)M}$ Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 1$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | | |
| 5 | $t_{v(SIMO)M}$ Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 1$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |
| 23 | $t_{d(SPC)M}$ Delay time, \overline{SPISTE} active to SPICLK | Even, Odd | $t_{c(SPC)M} - 1$ | | ns |
| 24 | $t_{d(STE)M}$ Delay time, SPICLK to \overline{SPISTE} inactive | Even | $0.5t_{c(SPC)M} - 1$ | | ns |
| | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

Table 5-87. SPI High-Speed Master Mode Timing Requirements

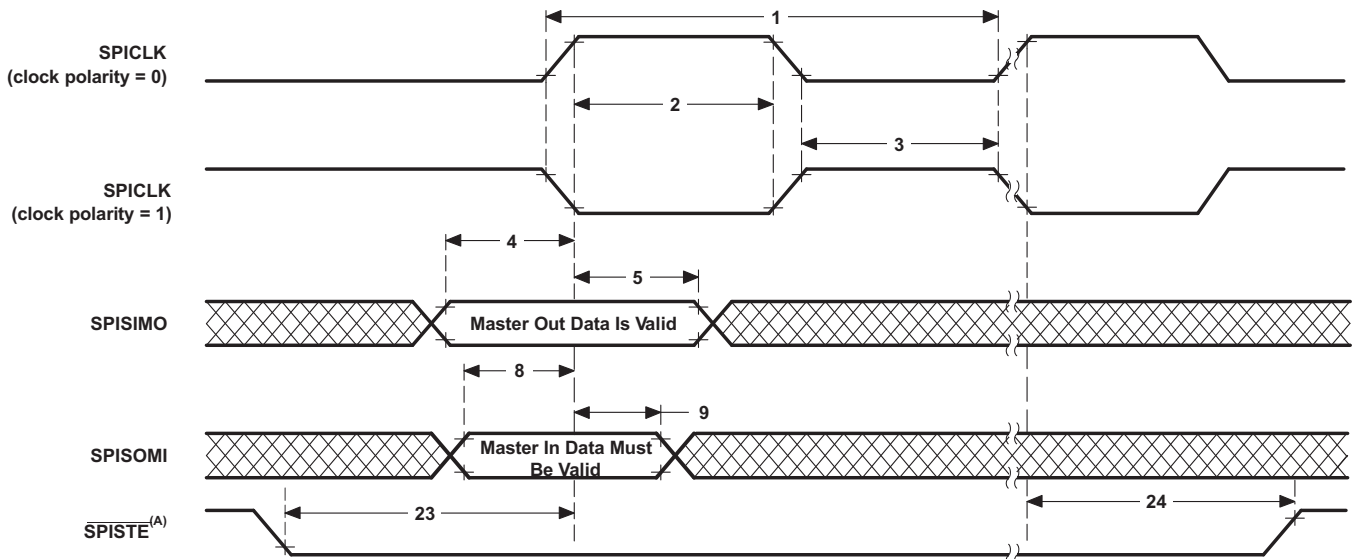
| NO. | PARAMETER | (BRR + 1) CONDITION ⁽¹⁾ | MIN | MAX | UNIT |
|-----|---|---------------------------------------|-----|-----|------|
| 8 | $t_{su(SOMI)M}$ Setup time, SPISOMI valid before SPICLK | Even, Odd | 1 | | ns |
| 9 | $t_{h(SOMI)M}$ Hold time, SPISOMI valid after SPICLK | Even, Odd | 5 | | ns |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.



- A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 5-75. High-Speed SPI Master Mode External Timing (Clock Phase = 0)



- A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 5-76. High-Speed SPI Master Mode External Timing (Clock Phase = 1)

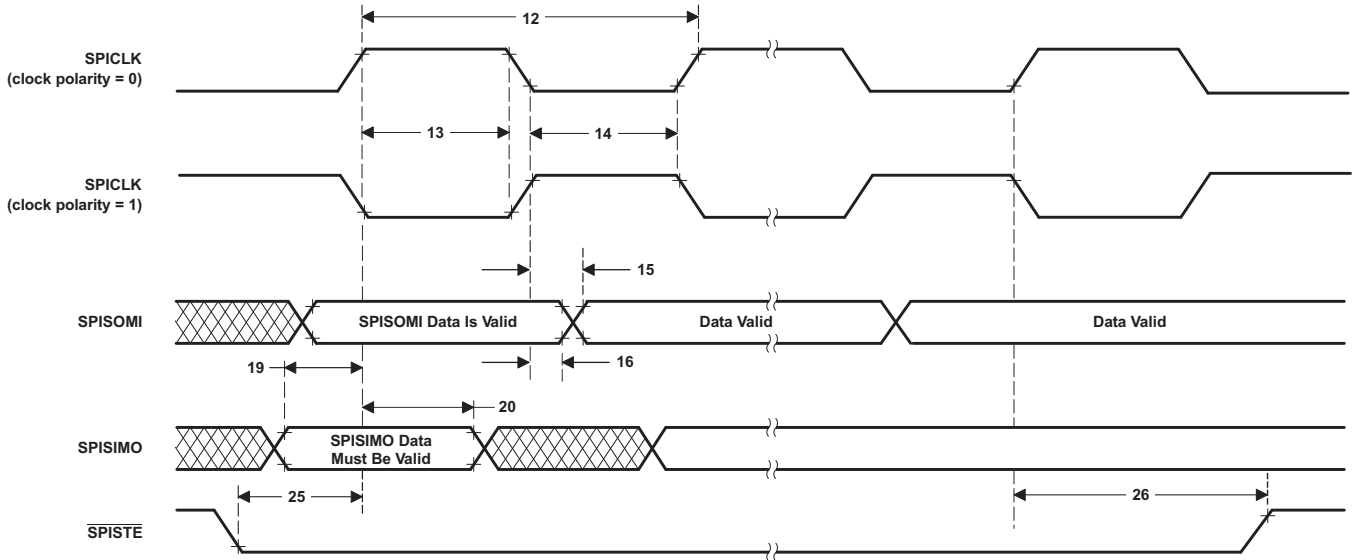


Figure 5-78. High-Speed SPI Slave Mode External Timing (Clock Phase = 1)

5.12.6 Universal Serial Bus (USB) Controller

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed and low-speed operation
- Integrated PHY
- Three transfer types: control, interrupt, and bulk
- 32 endpoints
 - One dedicated control IN endpoint and one dedicated control OUT endpoint
 - 15 configurable IN endpoints and 15 configurable OUT endpoints
- 4KB of dedicated endpoint memory

Figure 5-79 shows the USB block diagram.

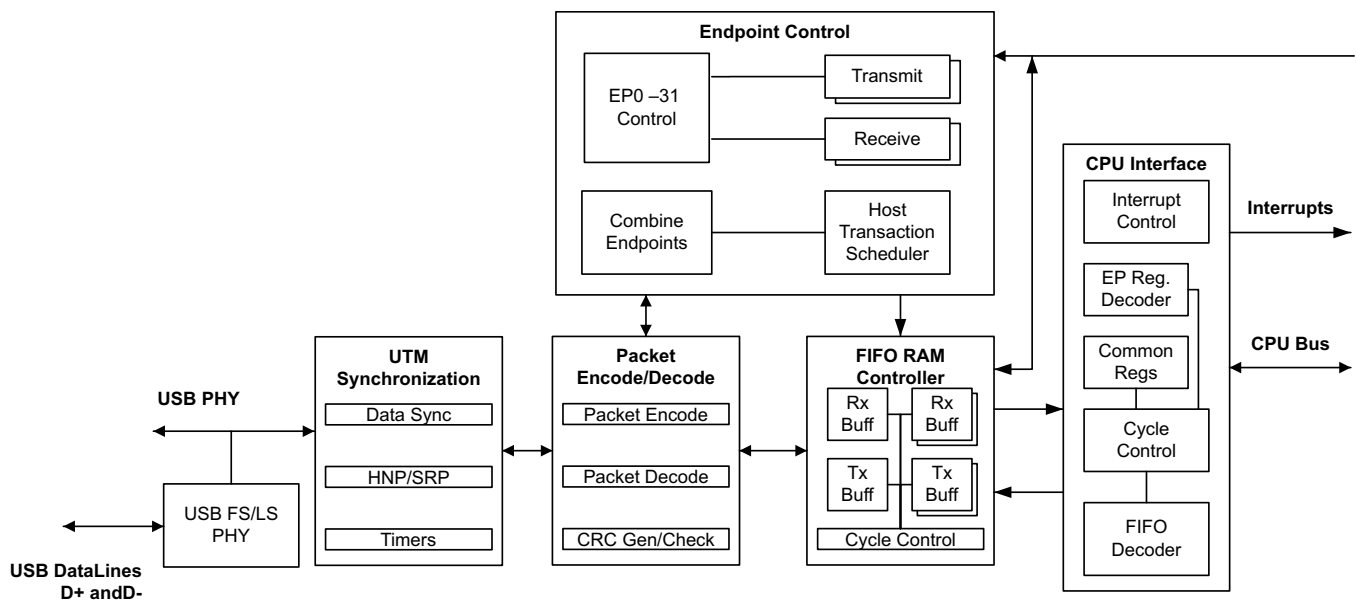


Figure 5-79. USB Block Diagram

NOTE

The accuracy of the on-chip zero-pin oscillator (Table 5-18, Internal Oscillator Electrical Characteristics) will not meet the accuracy requirements of the USB protocol. An external clock source must be used for applications using USB. For applications using the USB boot mode, see Section 6.9 (Boot ROM and Peripheral Booting) for clock frequency requirements.

5.12.6.1 USB Electrical Data and Timing

Table 5-90 shows the USB input ports DP and DM timing requirements. Table 5-91 shows the USB output ports DP and DM switching characteristics.

Table 5-90. USB Input Ports DP and DM Timing Requirements

| | | MIN | MAX | UNIT |
|-----------------|--------------------------------------|-----|-----|------|
| V(CM) | Differential input common mode range | 0.8 | 2.5 | V |
| Z(IN) | Input impedance | 300 | | kΩ |
| VCRS | Crossover voltage | 1.3 | 2.0 | V |
| V _{IL} | Static SE input logic-low level | 0.8 | | V |
| V _{IH} | Static SE input logic-high level | | 2.0 | V |
| VDI | Differential input voltage | | 0.2 | V |

Table 5-91. USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|--|-----|-----|------|
| V _{OH} | D+, D– single-ended USB 2.0 load conditions | 2.8 | 3.6 | V |
| V _{OL} | D+, D– single-ended USB 2.0 load conditions | 0 | 0.3 | V |
| Z(DRV) | D+, D– impedance | 28 | 44 | Ω |
| t _r | Rise time Full speed, differential, C _L = 50 pF, 10%/90%, R _{pu} on D+ | 4 | 20 | ns |
| t _f | Fall time Full speed, differential, C _L = 50 pF, 10%/90%, R _{pu} on D+ | 4 | 20 | ns |

The uPP interface supports the following:

- Mainstream high-speed data converters with parallel conversion interface.
- Mainstream high-speed streaming interface with frame START indication.
- Mainstream high-speed streaming interface with data ENABLE indication.
- Mainstream high-speed streaming interface with synchronization WAIT signal.
- SDR (single-data-rate) or DDR (double-data-rate, interleaved) interface.
- Multiplexing of interleaved data in SDR transmit case.
- Demultiplexing and multiplexing of interleaved data in DDR case.
- I/O interface clock frequency up to 50 MHz for SDR, and 25 MHz for DDR.
- Single-channel 8-bit input receive or output transmit mode.
- Max throughput is 50MB/s for pure read or pure write.
- Available as a DSP to FPGA general-purpose streaming interface.

Figure 5-81 shows the uPP functional block diagram.

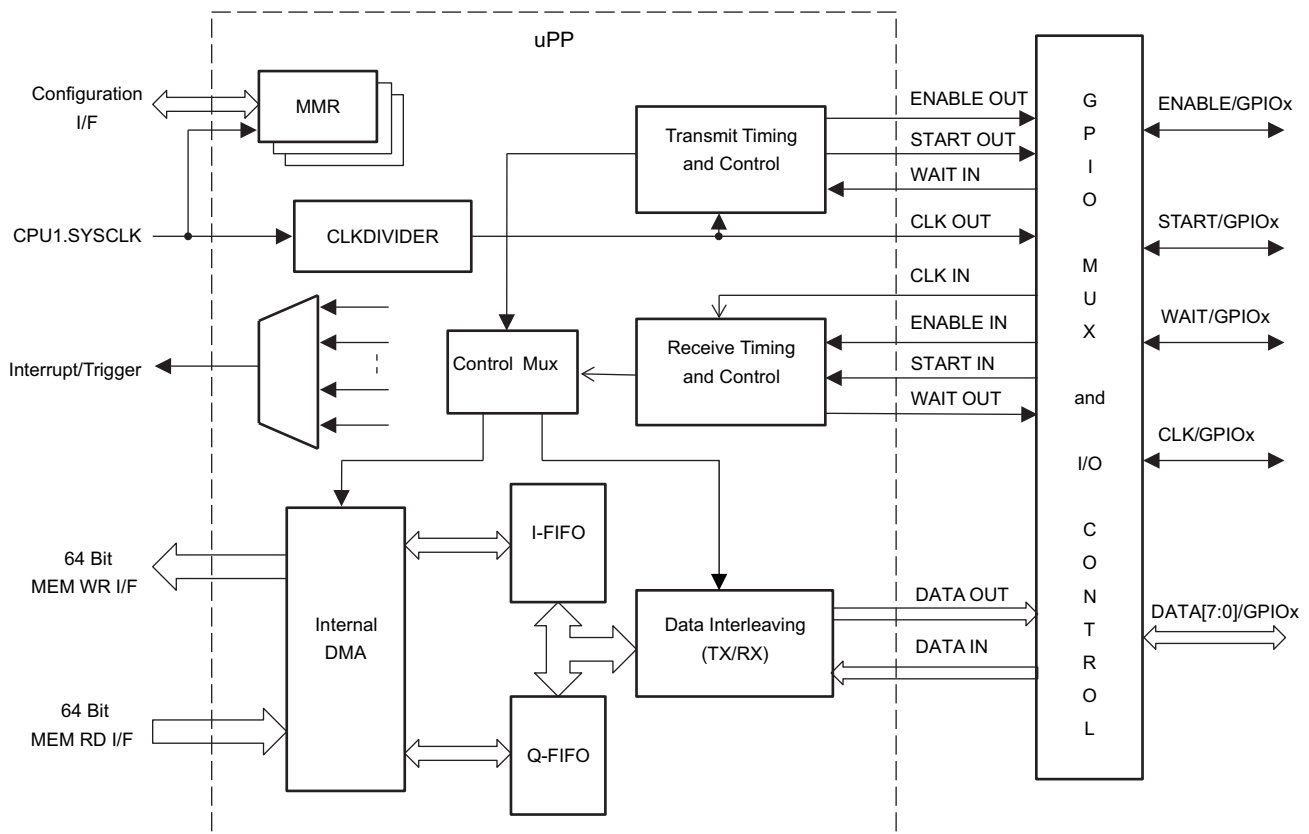


Figure 5-81. uPP Functional Block Diagram

5.12.7.1 uPP Electrical Data and Timing

Table 5-92 shows the uPP timing requirements. Table 5-93 shows the uPP switching characteristics. Figure 5-82 through Figure 5-85 show the uPP timing diagrams.

Table 5-92. uPP Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|--------------------|--|----------|-----|------|
| 1 | $t_{c(CLK)}$ | Cycle time, CLK | SDR mode | 20 | ns |
| | | | DDR mode | 40 | |
| 2 | $t_{w(CLKH)}$ | Pulse width, CLK high | SDR mode | 8 | ns |
| | | | DDR mode | 18 | |
| 3 | $t_{w(CLKL)}$ | Pulse width, CLK low | SDR mode | 8 | ns |
| | | | DDR mode | 18 | |
| 4 | $t_{su(STV-CLKH)}$ | Setup time, START valid before CLK high | 4 | | ns |
| 5 | $t_{h(CLKH-STV)}$ | Hold time, START valid after CLK high | 0.8 | | ns |
| 6 | $t_{su(ENV-CLKH)}$ | Setup time, ENABLE valid before CLK high | 4 | | ns |
| 7 | $t_{h(CLKH-ENV)}$ | Hold time, ENABLE valid after CLK high | 0.8 | | ns |
| 8 | $t_{su(DV-CLKH)}$ | Setup time, DATA valid before CLK high | 4 | | ns |
| 9 | $t_{h(CLKH-DV)}$ | Hold time, DATA valid after CLK high | 0.8 | | ns |
| 10 | $t_{su(DV-CLKL)}$ | Setup time, DATA valid before CLK low | 4 | | ns |
| 11 | $t_{h(CLKL-DV)}$ | Hold time, DATA valid after CLK low | 0.8 | | ns |
| 19 | $t_{su(WTV-CLKH)}$ | Setup time, WAIT valid before CLK high | SDR mode | 20 | ns |
| 20 | $t_{h(CLKH-WTV)}$ | Hold time, WAIT valid after CLK high | SDR mode | 0 | ns |
| 21 | $t_{su(WTV-CLKL)}$ | Setup time, WAIT valid before CLK low | DDR mode | 20 | ns |
| 22 | $t_{h(CLKL-WTV)}$ | Hold time, WAIT valid after CLK low | DDR mode | 0 | ns |

Table 5-93. uPP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|-------------------|---|----------|-----|------|
| 12 | $t_{c(CLK)}$ | Cycle time, CLK | SDR mode | 20 | ns |
| | | | DDR mode | 40 | |
| 13 | $t_{w(CLKH)}$ | Pulse width, CLK high | SDR mode | 8 | ns |
| | | | DDR mode | 18 | |
| 14 | $t_{w(CLKL)}$ | Pulse width, CLK low | SDR mode | 8 | ns |
| | | | DDR mode | 18 | |
| 15 | $t_{d(CLKH-STV)}$ | Delay time, START valid after CLK high | 3 | 12 | ns |
| 16 | $t_{d(CLKH-ENV)}$ | Delay time, ENABLE valid after CLK high | 3 | 12 | ns |
| 17 | $t_{d(CLKH-DV)}$ | Delay time, DATA valid after CLK high | 3 | 12 | ns |
| 18 | $t_{d(CLKL-DV)}$ | Delay time, DATA valid after CLK low | 3 | 12 | ns |

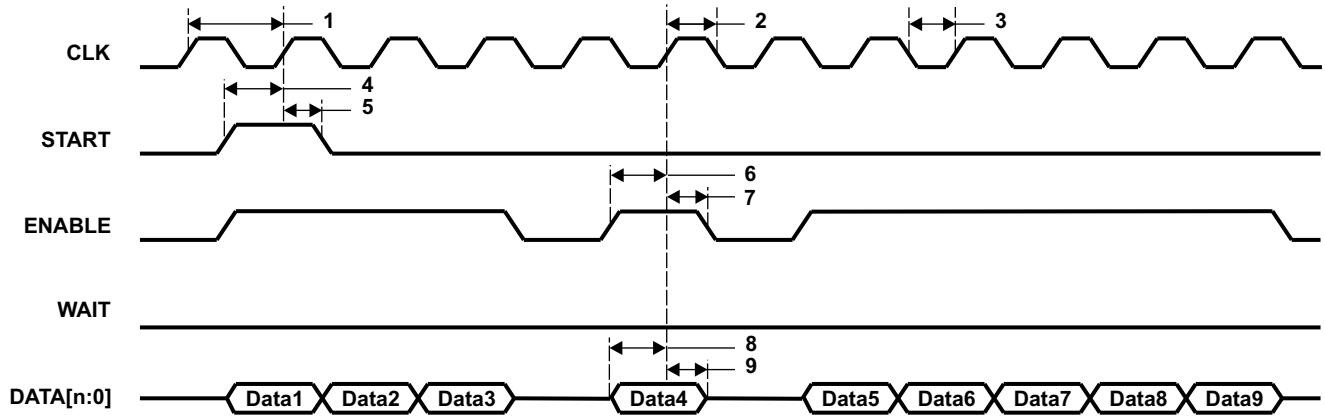


Figure 5-82. uPP Single Data Rate (SDR) Receive Timing

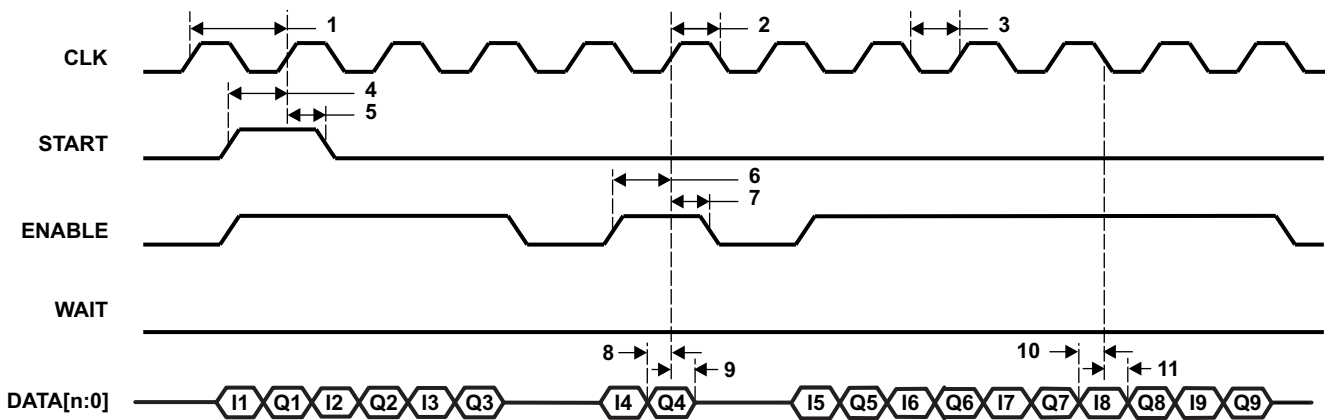


Figure 5-83. uPP Double Data Rate (DDR) Receive Timing

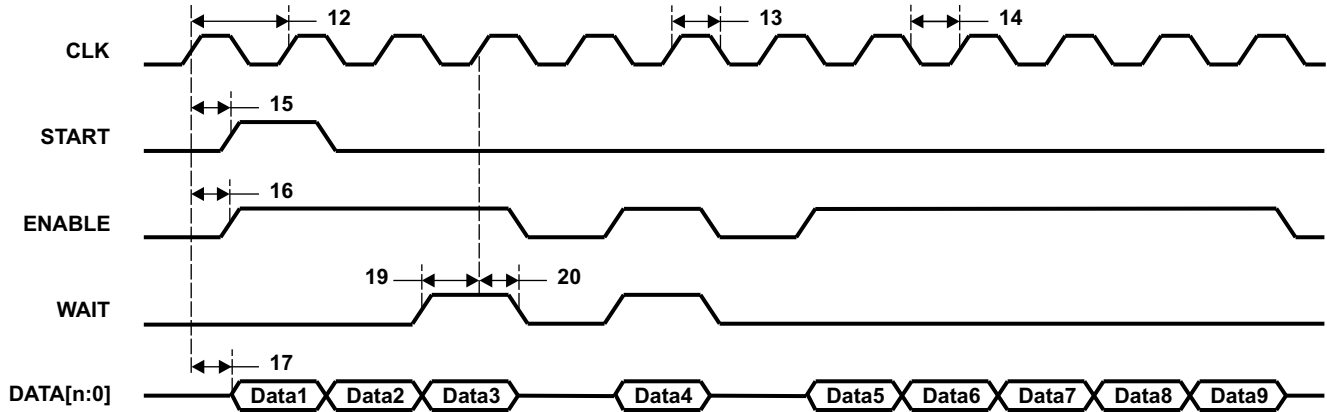


Figure 5-84. uPP Single Data Rate (SDR) Transmit Timing

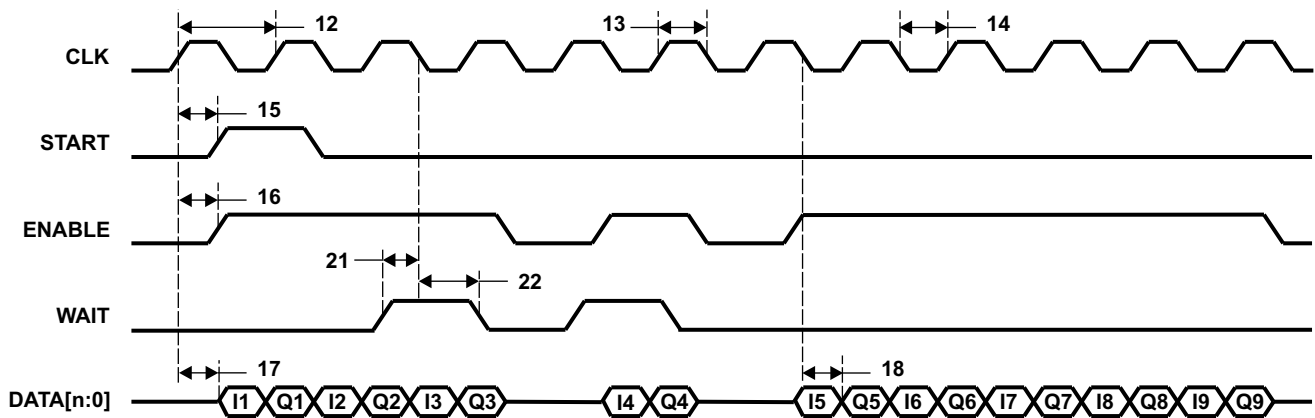


Figure 5-85. uPP Double Data Rate (DDR) Transmit Timing

6 Detailed Description

6.1 Overview

The Delfino TMS320F2837xS is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as [industrial motor drives](#); [solar inverters and digital power](#); [electrical vehicles and transportation](#); and [sensing and signal processing](#). Complete development packages for digital power and industrial drives are available as part of the [powerSUITE](#) and [DesignDRIVE](#) initiatives.

The real-time control subsystem is based on TI's 32-bit C28x floating-point CPU, which provides 200 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations; and the VCU accelerator, which reduces the time for complex math operations common in encoded applications.

The F2837xS microcontroller family features a CLA real-time control coprocessor. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics.

The TMS320F2837xS supports up to 1MB (512KW) of onboard flash memory with error correction code (ECC) and up to 164KB (82KW) of SRAM. Two 128-bit secure zones are also available on the CPU for code protection.

Performance analog and control peripherals are also integrated on the F2837xS MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. The new sigma-delta filter module (SDFM) works in conjunction with the sigma-delta modulator to enable isolated current shunt measurements. The Comparator Subsystem (CMPSS) with windowed comparators allows for protection of power stages when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

Peripherals such as EMIFs, CAN modules (ISO 11898-1/CAN 2.0B-compliant), and a new uPP interface extend the connectivity of the F2837xS. The uPP interface is a new feature of the C2000 MCUs and supports high-speed parallel connection to FPGAs or other processors with similar uPP interfaces. Lastly, a USB 2.0 port with MAC and PHY lets users easily add universal serial bus (USB) connectivity to their application.

6.2 Functional Block Diagram

[Figure 6-1](#) shows the CPU system and associated peripherals.

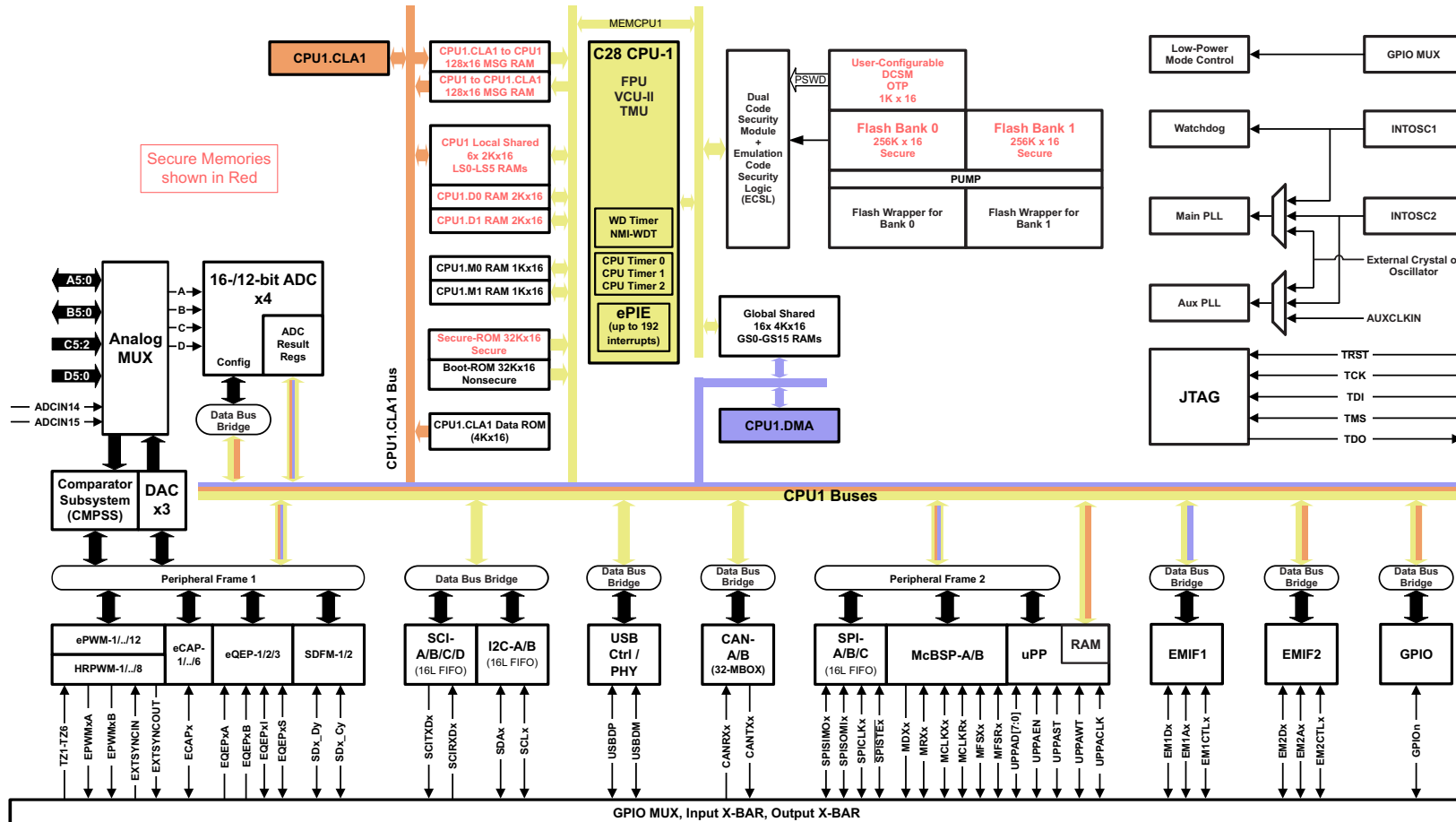


Figure 6-1. Functional Block Diagram

6.3 Memory

6.3.1 C28x Memory Map

The C28x memory map is described in [Table 6-1](#). Memories accessible by the CLA or DMA (direct memory access) are noted as well.

Table 6-1. C28x Memory Map

| MEMORY | SIZE | START ADDRESS | END ADDRESS | CLA ACCESS | DMA ACCESS |
|-------------------------|-----------|---------------|-------------|------------|------------|
| M0 RAM | 1K x 16 | 0x0000 0000 | 0x0000 03FF | | |
| M1 RAM | 1K x 16 | 0x0000 0400 | 0x0000 07FF | | |
| PieVectTable | 512 x 16 | 0x0000 0D00 | 0x0000 0EFF | | |
| CLA to CPU MSGRAM | 128 x 16 | 0x0000 1480 | 0x0000 14FF | Yes | |
| CPU to CLA MSGRAM | 128 x 16 | 0x0000 1500 | 0x0000 157F | Yes | |
| UPP TX MSG RAM | 512 x 16 | 0x0000 6C00 | 0x0000 6DFF | Yes | |
| UPP RX MSG RAM | 512 x 16 | 0x0000 6E00 | 0x0000 6FFF | Yes | |
| LS0 RAM | 2K x 16 | 0x0000 8000 | 0x0000 87FF | Yes | |
| LS1 RAM | 2K x 16 | 0x0000 8800 | 0x0000 8FFF | Yes | |
| LS2 RAM | 2K x 16 | 0x0000 9000 | 0x0000 97FF | Yes | |
| LS3 RAM | 2K x 16 | 0x0000 9800 | 0x0000 9FFF | Yes | |
| LS4 RAM | 2K x 16 | 0x0000 A000 | 0x0000 A7FF | Yes | |
| LS5 RAM | 2K x 16 | 0x0000 A800 | 0x0000 AFFF | Yes | |
| D0 RAM | 2K x 16 | 0x0000 B000 | 0x0000 B7FF | | |
| D1 RAM | 2K x 16 | 0x0000 B800 | 0x0000 BFFF | | |
| GS0 RAM | 4K x 16 | 0x0000 C000 | 0x0000 CFFF | | Yes |
| GS1 RAM | 4K x 16 | 0x0000 D000 | 0x0000 DFFF | | Yes |
| GS2 RAM | 4K x 16 | 0x0000 E000 | 0x0000 EFFF | | Yes |
| GS3 RAM | 4K x 16 | 0x0000 F000 | 0x0000 FFFF | | Yes |
| GS4 RAM | 4K x 16 | 0x0001 0000 | 0x0001 0FFF | | Yes |
| GS5 RAM | 4K x 16 | 0x0001 1000 | 0x0001 1FFF | | Yes |
| GS6 RAM | 4K x 16 | 0x0001 2000 | 0x0001 2FFF | | Yes |
| GS7 RAM | 4K x 16 | 0x0001 3000 | 0x0001 3FFF | | Yes |
| GS8 RAM | 4K x 16 | 0x0001 4000 | 0x0001 4FFF | | Yes |
| GS9 RAM | 4K x 16 | 0x0001 5000 | 0x0001 5FFF | | Yes |
| GS10 RAM | 4K x 16 | 0x0001 6000 | 0x0001 6FFF | | Yes |
| GS11 RAM | 4K x 16 | 0x0001 7000 | 0x0001 7FFF | | Yes |
| GS12 RAM ⁽¹⁾ | 4K x 16 | 0x0001 8000 | 0x0001 8FFF | | Yes |
| GS13 RAM ⁽¹⁾ | 4K x 16 | 0x0001 9000 | 0x0001 9FFF | | Yes |
| GS14 RAM ⁽¹⁾ | 4K x 16 | 0x0001 A000 | 0x0001 AFFF | | Yes |
| GS15 RAM ⁽¹⁾ | 4K x 16 | 0x0001 B000 | 0x0001 BFFF | | Yes |
| CAN A Message RAM | 2K x 16 | 0x0004 9000 | 0x0004 97FF | | |
| CAN B Message RAM | 2K x 16 | 0x0004 B000 | 0x0004 B7FF | | |
| Flash Bank 0 | 256K x 16 | 0x0008 0000 | 0x000B FFFF | | |
| Flash Bank 1 | 256K x 16 | 0x000C 0000 | 0x000F FFFF | | |
| Secure ROM | 32K x 16 | 0x003F 0000 | 0x003F 7FFF | | |
| Boot ROM | 32K x 16 | 0x003F 8000 | 0x003F FFBF | | |
| Vectors | 64 x 16 | 0x003F FFC0 | 0x003F FFFF | | |

(1) Available only on F28379S, F28378S, F28377S, and F28375S.

6.3.2 Flash Memory Map

The F28379S, F28378S, F28377S, and F28375S devices have two flash banks [512KB (256KW) each] for a total of 1MB (512KW). Only one bank can be programmed or erased at a time. The Flash API can be executed from RAM, or since there are two Flash banks for one CPU, the Flash API code can be executed from one bank to erase/program the other bank. Note that an extra wait state is automatically added when code is fetched or data is read from Bank 1 (compared to that of Bank 0), even for prefetched data. See [Section 5.9.4](#) for details on flash wait states. [Table 6-2](#) shows the addresses of flash sectors.

Table 6-2. Addresses of Flash Sectors on F28379S, F28378S, F28377S, and F28375S

| SECTOR | SIZE | START ADDRESS | END ADDRESS |
|-----------------------------------|----------|---------------|-------------|
| OTP Sectors | | | |
| TI OTP Bank 0 | 1K x 16 | 0x0007 0000 | 0x0007 03FF |
| User configurable DCSM OTP Bank 0 | 1K x 16 | 0x0007 8000 | 0x0007 83FF |
| Reserved ⁽¹⁾ | 1K x 16 | 0x0007 0800 | 0x0007 0BFF |
| Reserved | 1K x 16 | 0x0007 8800 | 0x0007 8BFF |
| Bank 0 Sectors | | | |
| Sector A | 8K x 16 | 0x0008 0000 | 0x0008 1FFF |
| Sector B | 8K x 16 | 0x0008 2000 | 0x0008 3FFF |
| Sector C | 8K x 16 | 0x0008 4000 | 0x0008 5FFF |
| Sector D | 8K x 16 | 0x0008 6000 | 0x0008 7FFF |
| Sector E | 32K x 16 | 0x0008 8000 | 0x0008 FFFF |
| Sector F | 32K x 16 | 0x0009 0000 | 0x0009 7FFF |
| Sector G | 32K x 16 | 0x0009 8000 | 0x0009 FFFF |
| Sector H | 32K x 16 | 0x000A 0000 | 0x000A 7FFF |
| Sector I | 32K x 16 | 0x000A 8000 | 0x000A FFFF |
| Sector J | 32K x 16 | 0x000B 0000 | 0x000B 7FFF |
| Sector K | 8K x 16 | 0x000B 8000 | 0x000B 9FFF |
| Sector L | 8K x 16 | 0x000B A000 | 0x000B BFFF |
| Sector M | 8K x 16 | 0x000B C000 | 0x000B DFFF |
| Sector N | 8K x 16 | 0x000B E000 | 0x000B FFFF |
| Bank 1 Sectors | | | |
| Sector O | 8K x 16 | 0x000C 0000 | 0x000C 1FFF |
| Sector P | 8K x 16 | 0x000C 2000 | 0x000C 3FFF |
| Sector Q | 8K x 16 | 0x000C 4000 | 0x000C 5FFF |
| Sector R | 8K x 16 | 0x000C 6000 | 0x000C 7FFF |
| Sector S | 32K x 16 | 0x000C 8000 | 0x000C FFFF |
| Sector T | 32K x 16 | 0x000D 0000 | 0x000D 7FFF |
| Sector U | 32K x 16 | 0x000D 8000 | 0x000D FFFF |
| Sector V | 32K x 16 | 0x000E 0000 | 0x000E 7FFF |
| Sector W | 32K x 16 | 0x000E 8000 | 0x000E FFFF |
| Sector X | 32K x 16 | 0x000F 0000 | 0x000F 7FFF |
| Sector Y | 8K x 16 | 0x000F 8000 | 0x000F 9FFF |
| Sector Z | 8K x 16 | 0x000F A000 | 0x000F BFFF |
| Sector AA | 8K x 16 | 0x000F C000 | 0x000F DFFF |
| Sector AB | 8K x 16 | 0x000F E000 | 0x000F FFFF |

(1) Any kind of access to this region may result in a spurious ECC error event.

Table 6-2. Addresses of Flash Sectors on F28379S, F28378S, F28377S, and F28375S (continued)

| SECTOR | SIZE | START ADDRESS | END ADDRESS |
|---------------------------------------|----------|---------------|-------------|
| Flash ECC Locations | | | |
| TI OTP ECC Bank 0 | 128 × 16 | 0x0107 0000 | 0x0107 007F |
| Reserved | 128 × 16 | 0x0107 0200 | 0x0107 027F |
| User-configurable DCSM OTP ECC Bank 0 | 128 × 16 | 0x0107 1000 | 0x0107 107F |
| Reserved | 128 × 16 | 0x0107 1200 | 0x0107 127F |
| Flash ECC Bank 0 | 32K × 16 | 0x0108 0000 | 0x0108 7FFF |
| Flash ECC Bank 1 | 32K × 16 | 0x0108 8000 | 0x0108 FFFF |

The F28376S and F28374S devices have one flash bank of 512KB (256KW) and the code to program the flash should be executed out of RAM. See [Section 5.9.4](#) for details on flash wait states. [Table 6-3](#) shows the addresses of flash sectors.

Table 6-3. Addresses of Flash Sectors on F28376S and F28374S

| SECTOR | SIZE | START ADDRESS | END ADDRESS |
|---------------------------------------|----------|---------------|-------------|
| OTP Sectors | | | |
| TI OTP Bank 0 | 1K × 16 | 0x0007 0000 | 0x0007 03FF |
| User configurable DCSM OTP Bank 0 | 1K × 16 | 0x0007 8000 | 0x0007 83FF |
| Bank 0 Sectors | | | |
| Sector A | 8K × 16 | 0x0008 0000 | 0x0008 1FFF |
| Sector B | 8K × 16 | 0x0008 2000 | 0x0008 3FFF |
| Sector C | 8K × 16 | 0x0008 4000 | 0x0008 5FFF |
| Sector D | 8K × 16 | 0x0008 6000 | 0x0008 7FFF |
| Sector E | 32K × 16 | 0x0008 8000 | 0x0008 FFFF |
| Sector F | 32K × 16 | 0x0009 0000 | 0x0009 7FFF |
| Sector G | 32K × 16 | 0x0009 8000 | 0x0009 FFFF |
| Sector H | 32K × 16 | 0x000A 0000 | 0x000A 7FFF |
| Sector I | 32K × 16 | 0x000A 8000 | 0x000A FFFF |
| Sector J | 32K × 16 | 0x000B 0000 | 0x000B 7FFF |
| Sector K | 8K × 16 | 0x000B 8000 | 0x000B 9FFF |
| Sector L | 8K × 16 | 0x000B A000 | 0x000B BFFF |
| Sector M | 8K × 16 | 0x000B C000 | 0x000B DFFF |
| Sector N | 8K × 16 | 0x000B E000 | 0x000B FFFF |
| Flash ECC Locations | | | |
| TI OTP ECC Bank 0 | 128 × 16 | 0x0107 0000 | 0x0107 007F |
| User-configurable DCSM OTP ECC Bank 0 | 128 × 16 | 0x0107 1000 | 0x0107 107F |
| Flash ECC Bank 0 | 32K × 16 | 0x0108 0000 | 0x0108 7FFF |

6.3.3 EMIF Chip Select Memory Map

The EMIF memory map is shown in [Table 6-4](#).

Table 6-4. EMIF Chip Select Memory Map

| EMIF CHIP SELECT | SIZE ⁽¹⁾ | START ADDRESS | END ADDRESS | CLA ACCESS | DMA ACCESS |
|--|---------------------|---------------|-------------|-----------------|------------|
| EMIF1_CS0n - Data | 256M × 16 | 0x8000 0000 | 0x8FFF FFFF | | Yes |
| EMIF1_CS2n - Program + Data ⁽²⁾ | 2M × 16 | 0x0010 0000 | 0x002F FFFF | | Yes |
| EMIF1_CS3n - Program + Data | 512K × 16 | 0x0030 0000 | 0x0037 FFFF | | Yes |
| EMIF1_CS4n - Program + Data | 393K × 16 | 0x0038 0000 | 0x003D FFFF | | Yes |
| EMIF2_CS0n - Data | 3M × 16 | 0x9000 0000 | 0x91FF FFFF | | |
| EMIF2_CS2n - Program + Data | 4K × 16 | 0x0000 2000 | 0x0000 2FFF | Yes (Data only) | |

- (1) Available memory size listed in this table is the maximum possible size assuming 32-bit memory. This may not apply to other memory sizes because of pin mux setting. See [Section 4.4.1](#) to find the available address lines for your use case.
- (2) The 2M × 16 size is for a 32-bit interface with the assumption that 16-bit accesses are not performed; hence, byte enables are not used (tied to active value on board). If byte enables are used, then the maximum size is smaller because byte enables are muxed with address pins (see [Section 4.4.1](#)). If 16-bit memory is used, then the maximum size is 1M × 16.

6.3.4 Peripheral Registers Memory Map

The peripheral registers memory map can be found in [Table 6-5](#). Registers in the peripheral frames share a secondary master (CLA or DMA) selection with all other registers within the same peripheral frame. See the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) for details on the CPU subsystem and secondary master selection.

Table 6-5. Peripheral Registers Memory Map

| REGISTERS | STRUCTURE NAME | START ADDRESS | END ADDRESS | PROTECTED ⁽¹⁾ | CLA ACCESS | DMA ACCESS |
|---------------------------|------------------|---------------|-------------|--------------------------|-------------------------------|------------|
| AdcaResultRegs | ADC_RESULT_REGS | 0x0000 0B00 | 0x0000 0B1F | | Yes | Yes |
| AdcbResultRegs | ADC_RESULT_REGS | 0x0000 0B20 | 0x0000 0B3F | | Yes | Yes |
| AdccResultRegs | ADC_RESULT_REGS | 0x0000 0B40 | 0x0000 0B5F | | Yes | Yes |
| AdcdResultRegs | ADC_RESULT_REGS | 0x0000 0B60 | 0x0000 0B7F | | Yes | Yes |
| CpuTimer0Regs | CPUTIMER_REGS | 0x0000 0C00 | 0x0000 0C07 | | | |
| CpuTimer1Regs | CPUTIMER_REGS | 0x0000 0C08 | 0x0000 0C0F | | | |
| CpuTimer2Regs | CPUTIMER_REGS | 0x0000 0C10 | 0x0000 0C17 | | | |
| PieCtrlRegs | PIE_CTRL_REGS | 0x0000 0CE0 | 0x0000 0CFF | | | |
| Cla1SoftIntRegs | CLA_SOFTINT_REGS | 0x0000 0CE0 | 0x0000 0CFF | | Yes – CLA only, no CPU access | |
| DmaRegs | DMA_REGS | 0x0000 1000 | 0x0000 11FF | | | |
| Cla1Regs | CLA_REGS | 0x0000 1400 | 0x0000 147F | | | |
| Peripheral Frame 1 | | | | | | |
| EPwm1Regs | EPWM_REGS | 0x0000 4000 | 0x0000 40FF | Yes | Yes | Yes |
| EPwm2Regs | EPWM_REGS | 0x0000 4100 | 0x0000 41FF | Yes | Yes | Yes |
| EPwm3Regs | EPWM_REGS | 0x0000 4200 | 0x0000 42FF | Yes | Yes | Yes |
| EPwm4Regs | EPWM_REGS | 0x0000 4300 | 0x0000 43FF | Yes | Yes | Yes |
| EPwm5Regs | EPWM_REGS | 0x0000 4400 | 0x0000 44FF | Yes | Yes | Yes |
| EPwm6Regs | EPWM_REGS | 0x0000 4500 | 0x0000 45FF | Yes | Yes | Yes |
| EPwm7Regs | EPWM_REGS | 0x0000 4600 | 0x0000 46FF | Yes | Yes | Yes |
| EPwm8Regs | EPWM_REGS | 0x0000 4700 | 0x0000 47FF | Yes | Yes | Yes |
| EPwm9Regs | EPWM_REGS | 0x0000 4800 | 0x0000 48FF | Yes | Yes | Yes |
| EPwm10Regs | EPWM_REGS | 0x0000 4900 | 0x0000 49FF | Yes | Yes | Yes |
| EPwm11Regs | EPWM_REGS | 0x0000 4A00 | 0x0000 4AFF | Yes | Yes | Yes |
| EPwm12Regs | EPWM_REGS | 0x0000 4B00 | 0x0000 4BFF | Yes | Yes | Yes |
| ECap1Regs | ECAP_REGS | 0x0000 5000 | 0x0000 501F | Yes | Yes | Yes |

Table 6-5. Peripheral Registers Memory Map (continued)

| REGISTERS | STRUCTURE NAME | START ADDRESS | END ADDRESS | PROTECTED ⁽¹⁾ | CLA ACCESS | DMA ACCESS |
|---------------------------|----------------------|---------------|-------------|--------------------------|------------|------------|
| ECap2Regs | ECAP_REGS | 0x0000 5020 | 0x0000 503F | Yes | Yes | Yes |
| ECap3Regs | ECAP_REGS | 0x0000 5040 | 0x0000 505F | Yes | Yes | Yes |
| ECap4Regs | ECAP_REGS | 0x0000 5060 | 0x0000 507F | Yes | Yes | Yes |
| ECap5Regs | ECAP_REGS | 0x0000 5080 | 0x0000 509F | Yes | Yes | Yes |
| ECap6Regs | ECAP_REGS | 0x0000 50A0 | 0x0000 50BF | Yes | Yes | Yes |
| EQep1Regs | EQEP_REGS | 0x0000 5100 | 0x0000 513F | Yes | Yes | Yes |
| EQep2Regs | EQEP_REGS | 0x0000 5140 | 0x0000 517F | Yes | Yes | Yes |
| EQep3Regs | EQEP_REGS | 0x0000 5180 | 0x0000 51BF | Yes | Yes | Yes |
| DacaRegs | DAC_REGS | 0x0000 5C00 | 0x0000 5C0F | Yes | Yes | Yes |
| DacbRegs | DAC_REGS | 0x0000 5C10 | 0x0000 5C1F | Yes | Yes | Yes |
| DaccRegs | DAC_REGS | 0x0000 5C20 | 0x0000 5C2F | Yes | Yes | Yes |
| Cmpss1Regs | CMPSS_REGS | 0x0000 5C80 | 0x0000 5C9F | Yes | Yes | Yes |
| Cmpss2Regs | CMPSS_REGS | 0x0000 5CA0 | 0x0000 5CBF | Yes | Yes | Yes |
| Cmpss3Regs | CMPSS_REGS | 0x0000 5CC0 | 0x0000 5CDF | Yes | Yes | Yes |
| Cmpss4Regs | CMPSS_REGS | 0x0000 5CE0 | 0x0000 5CFF | Yes | Yes | Yes |
| Cmpss5Regs | CMPSS_REGS | 0x0000 5D00 | 0x0000 5D1F | Yes | Yes | Yes |
| Cmpss6Regs | CMPSS_REGS | 0x0000 5D20 | 0x0000 5D3F | Yes | Yes | Yes |
| Cmpss7Regs | CMPSS_REGS | 0x0000 5D40 | 0x0000 5D5F | Yes | Yes | Yes |
| Cmpss8Regs | CMPSS_REGS | 0x0000 5D60 | 0x0000 5D7F | Yes | Yes | Yes |
| Sdfm1Regs | SDFM_REGS | 0x0000 5E00 | 0x0000 5E7F | Yes | Yes | Yes |
| Sdfm2Regs | SDFM_REGS | 0x0000 5E80 | 0x0000 5EFF | Yes | Yes | Yes |
| Peripheral Frame 2 | | | | | | |
| McbspaRegs | MCBSP_REGS | 0x0000 6000 | 0x0000 603F | Yes | Yes | Yes |
| McbspbRegs | MCBSP_REGS | 0x0000 6040 | 0x0000 607F | Yes | Yes | Yes |
| SpiaRegs | SPI_REGS | 0x0000 6100 | 0x0000 610F | Yes | Yes | Yes |
| SpibRegs | SPI_REGS | 0x0000 6110 | 0x0000 611F | Yes | Yes | Yes |
| SpicRegs | SPI_REGS | 0x0000 6120 | 0x0000 612F | Yes | Yes | Yes |
| UppRegs | UPP_REGS | 0x0000 6200 | 0x0000 62FF | Yes | Yes | Yes |
| Peripheral Frame 3 | | | | | | |
| WdRegs | WD_REGS | 0x0000 7000 | 0x0000 703F | Yes | | |
| NmiIntruptRegs | NMI_INTRUPT_REGS | 0x0000 7060 | 0x0000 706F | Yes | | |
| XintRegs | XINT_REGS | 0x0000 7070 | 0x0000 707F | Yes | | |
| SciaRegs | SCI_REGS | 0x0000 7200 | 0x0000 720F | Yes | | |
| ScibRegs | SCI_REGS | 0x0000 7210 | 0x0000 721F | Yes | | |
| ScicRegs | SCI_REGS | 0x0000 7220 | 0x0000 722F | Yes | | |
| ScidRegs | SCI_REGS | 0x0000 7230 | 0x0000 723F | Yes | | |
| I2caRegs | I2C_REGS | 0x0000 7300 | 0x0000 733F | Yes | | |
| I2cbRegs | I2C_REGS | 0x0000 7340 | 0x0000 737F | Yes | | |
| AdcaRegs | ADC_REGS | 0x0000 7400 | 0x0000 747F | Yes | Yes | |
| AdcbRegs | ADC_REGS | 0x0000 7480 | 0x0000 74FF | Yes | Yes | |
| AdccRegs | ADC_REGS | 0x0000 7500 | 0x0000 757F | Yes | Yes | |
| AdcdRegs | ADC_REGS | 0x0000 7580 | 0x0000 75FF | Yes | Yes | |
| InputXbarRegs | INPUT_XBAR_REGS | 0x0000 7900 | 0x0000 791F | Yes | | |
| XbarRegs | XBAR_REGS | 0x0000 7920 | 0x0000 793F | Yes | | |
| TrigRegs | TRIG_REGS | 0x0000 7940 | 0x0000 794F | Yes | | |
| DmaClaSrcSelRegs | DMA_CLA_SRC_SEL_REGS | 0x0000 7980 | 0x0000 798F | Yes | | |
| EPwmXbarRegs | EPWM_XBAR_REGS | 0x0000 7A00 | 0x0000 7A3F | Yes | | |
| OutputXbarRegs | OUTPUT_XBAR_REGS | 0x0000 7A80 | 0x0000 7ABF | Yes | | |
| GpioCtrlRegs | GPIO_CTRL_REGS | 0x0000 7C00 | 0x0000 7D7F | Yes | | |
| GpioDataRegs | GPIO_DATA_REGS | 0x0000 7F00 | 0x0000 7F2F | Yes | Yes | |
| UsbaRegs | USB_REGS | 0x0004 0000 | 0x0004 0FFF | Yes | | |

Table 6-5. Peripheral Registers Memory Map (continued)

| REGISTERS | STRUCTURE NAME | START ADDRESS | END ADDRESS | PROTECTED ⁽¹⁾ | CLA ACCESS | DMA ACCESS |
|------------------------|---------------------------|---------------|-------------|--------------------------|------------|------------|
| Emif1Regs | EMIF_REGS | 0x0004 7000 | 0x0004 77FF | Yes | | |
| Emif2Regs | EMIF_REGS | 0x0004 7800 | 0x0004 7FFF | Yes | | |
| CanaRegs | CAN_REGS | 0x0004 8000 | 0x0004 87FF | Yes | | |
| CanbRegs | CAN_REGS | 0x0004 A000 | 0x0004 A7FF | Yes | | |
| FlashPumpSemaphoreRegs | FLASH_PUMP_SEMAPHORE_REGS | 0x0005 0024 | 0x0005 0025 | Yes | | |
| DevCfgRegs | DEV_CFG_REGS | 0x0005 D000 | 0x0005 D17F | Yes | | |
| AnalogSubsysRegs | ANALOG_SUBSYS_REGS | 0x0005 D180 | 0x0005 D1FF | Yes | | |
| ClkCfgRegs | CLK_CFG_REGS | 0x0005 D200 | 0x0005 D2FF | Yes | | |
| CpuSysRegs | CPU_SYS_REGS | 0x0005 D300 | 0x0005 D3FF | Yes | | |
| RomPrefetchRegs | ROM_PREFETCH_REGS | 0x0005 E608 | 0x0005 E60B | Yes | | |
| DcsmZ1Regs | DCSM_Z1_REGS | 0x0005 F000 | 0x0005 F02F | Yes | | |
| DcsmZ2Regs | DCSM_Z2_REGS | 0x0005 F040 | 0x0005 F05F | Yes | | |
| DcsmCommonRegs | DCSM_COMMON_REGS | 0x0005 F070 | 0x0005 F07F | Yes | | |
| MemCfgRegs | MEM_CFG_REGS | 0x0005 F400 | 0x0005 F47F | Yes | | |
| Emif1ConfigRegs | EMIF1_CONFIG_REGS | 0x0005 F480 | 0x0005 F49F | Yes | | |
| Emif2ConfigRegs | EMIF2_CONFIG_REGS | 0x0005 F4A0 | 0x0005 F4BF | Yes | | |
| AccessProtectionRegs | ACCESS_PROTECTION_REGS | 0x0005 F4C0 | 0x0005 F4FF | Yes | | |
| MemoryErrorRegs | MEMORY_ERROR_REGS | 0x0005 F500 | 0x0005 F53F | Yes | | |
| RomWaitStateRegs | ROM_WAIT_STATE_REGS | 0x0005 F540 | 0x0005 F541 | Yes | | |
| Flash0CtrlRegs | FLASH_CTRL_REGS | 0x0005 F800 | 0x0005 FAFF | Yes | | |
| Flash0EccRegs | FLASH_ECC_REGS | 0x0005 FB00 | 0x0005 FB3F | Yes | | |
| Flash1CtrlRegs | FLASH_CTRL_REGS | 0x0005 FC00 | 0x0005 FEFF | Yes | | |
| Flash1EccRegs | FLASH_ECC_REGS | 0x0005 FF00 | 0x0005 FF3F | Yes | | |

(1) The CPU (not applicable for CLA or DMA) contains a write followed by read protection mode to ensure that any read operation that follows a write operation within a protected address range is executed as written by delaying the read operation until the write is initiated.

6.3.5 Memory Types

Table 6-6 provides more information about each memory type.

Table 6-6. Memory Types

| MEMORY TYPE | ECC-CAPABLE | PARITY | SECURITY | HIBERNATE RETENTION | ACCESS PROTECTION |
|----------------------------|-------------|--------|----------|---------------------|-------------------|
| M0, M1 | Yes | – | – | Yes | – |
| D0, D1 | Yes | – | Yes | – | Yes |
| LSx | – | Yes | Yes | – | Yes |
| GSx | – | Yes | – | – | Yes |
| CPU/CLA MSGRAM | – | Yes | Yes | – | Yes |
| Boot ROM | – | – | – | N/A | – |
| Secure ROM | – | – | Yes | N/A | – |
| Flash | Yes | – | Yes | N/A | N/A |
| User-configurable DCSM OTP | Yes | – | Yes | N/A | N/A |

6.3.5.1 Dedicated RAM (Mx and Dx RAM)

The CPU subsystem has four dedicated ECC-capable RAM blocks: M0, M1, D0, and D1. M0/M1 memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them). D0/D1 memories are secure blocks and also have the access-protection feature (CPU write/CPU fetch protection).

6.3.5.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have parity. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately.

Table 6-7 shows the master access for the LSx RAM.

**Table 6-7. Master Access for LSx RAM
(With Assumption That all Other Access Protections are Disabled)**

| MSEL_LSx | CLAPGM_LSx | CPU ALLOWED ACCESS | CLA ALLOWED ACCESS | COMMENT |
|----------|------------|-----------------------------------|-------------------------|--|
| 00 | X | All | – | LSx memory is configured as CPU dedicated RAM. |
| 01 | 0 | All | Data Read Data Write | LSx memory is shared between CPU and CLA1. |
| 01 | 1 | Emulation Read Emulation Write | Fetch Only | LSx memory is CLA1 program memory. |

6.3.5.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Both the CPU and DMA have full read and write access to these memories.

All GSx RAM blocks have parity.

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

6.3.5.4 CLA Message RAM (CLA MSGRAM)

These RAM blocks can be used to share data between the CPU and CLA. The CLA has read and write access to the "CLA to CPU MSGRAM." The CPU has read and write access to the "CPU to CLA MSGRAM." The CPU and CLA both have read access to both MSGRAMs.

This RAM has parity.

6.4 Identification

Table 6-8 shows the Device Identification Registers.

Table 6-8. Device Identification Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION |
|--------------------------------|-------------|------------|--|
| PARTIDH | 0x0005 D00A | 2 | Device part identification number ⁽¹⁾ |
| | | | TMS320F28379S 0x**F9 0400 |
| | | | TMS320F28378S 0x**FA 0400 |
| | | | TMS320F28377S 0x**FF 0400 |
| | | | TMS320F28376S 0x**FE 0400 |
| | | | TMS320F28375S 0x**FD 0400 |
| TMS320F28374S 0x**FC 0400 | | | |
| REVID | 0x0005 D00C | 2 | Silicon revision number |
| | | | Revision B 0x0000 0002 |
| | | | Revision C 0x0000 0003 |
| UID_UNIQUE | 0x0007 03CC | 2 | Unique identification number. This number is different on each individual device with the same PARTIDH. This can be used as a serial number in the application. This number is present only on TMS Revision C devices. |
| JTAG ID | N/A | N/A | JTAG Device ID 0x0B99 C02F |

(1) PARTIDH may have one of two values for each part number, with the eight most significant bits identified with '**' above being 0x00 or 0x02.

6.5 Bus Architecture – Peripheral Connectivity

Table 6-9 shows a broad view of the peripheral and configuration register accessibility from each bus master. Peripherals within peripheral frames 1 or 2 will all be mapped to the respective secondary master as a group (if SPI is assigned to CPU1.DMA, then McBSP is also assigned to CPU1.DMA).

Table 6-9. Bus Master Peripheral Access

| PERIPHERALS (BY BUS ACCESS TYPE) | CPU1.DMA | CPU1.CLA1 | CPU1 |
|---|----------|-----------|------|
| Peripheral Frame 1: <ul style="list-style-type: none"> • ePWM/HRPWM • SDFM • eCAP⁽¹⁾ • eQEP⁽¹⁾ • CMPSS⁽¹⁾ • DAC⁽¹⁾ | Y | Y | Y |
| Peripheral Frame 2: <ul style="list-style-type: none"> • SPI • McBSP • uPP⁽¹⁾ | Y | Y | Y |
| SCI | | | Y |
| I2C | | | Y |
| CAN | | | Y |
| ADC Configuration | | Y | Y |
| EMIF1 | Y | | Y |
| EMIF2 | | Y | Y |
| USB | | | Y |
| Device Capability, Peripheral Reset, Peripheral CPU Select | | | Y |
| GPIO Pin Mapping and Configuration | | | Y |
| Analog System Control | | | Y |
| uPP Message RAMs | | Y | Y |
| Reset Configuration | | | Y |
| Clock and PLL Configuration | | | Y |
| System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating) | | | Y |
| Flash Configuration | | | Y |
| CPU Timers | | | Y |
| DMA and CLA Trigger Source Select | | | Y |
| GPIO Data ⁽²⁾ | | Y | Y |
| ADC Results | Y | Y | Y |

(1) These modules are on a Peripheral Frame with DMA access; however, they cannot trigger a DMA transfer.

(2) The GPIO Data Registers are unique for each CPU1 and CPU1.CLAx. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO. See the General-Purpose Input/Output (GPIO) chapter of the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) for more details.

6.6 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the [TMS320C28x CPU and Instruction Set Reference Guide](#).

6.6.1 Floating-Point Unit

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the repeat block register, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

6.6.2 Trigonometric Math Unit

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in [Table 6-10](#).

Table 6-10. TMU Supported Instructions

| INSTRUCTIONS | C EQUIVALENT OPERATION | PIPELINE CYCLES |
|-------------------------|--|-----------------|
| MPY2PIF32 RaH,RbH | $a = b * 2\pi$ | 2/3 |
| DIV2PIF32 RaH,RbH | $a = b / 2\pi$ | 2/3 |
| DIVF32 RaH,RbH,RcH | $a = b/c$ | 5 |
| SQRTF32 RaH,RbH | $a = \text{sqrt}(b)$ | 5 |
| SINPUF32 RaH,RbH | $a = \sin(b*2\pi)$ | 4 |
| COSPUF32 RaH,RbH | $a = \cos(b*2\pi)$ | 4 |
| ATANPUF32 RaH,RbH | $a = \text{atan}(b)/2\pi$ | 4 |
| QUADF32 RaH,RbH,RcH,RdH | Operation to assist in calculating ATANPU2 | 5 |

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. A detailed explanation of the workings of the FPU can be found in the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

6.6.3 Viterbi, Complex Math, and CRC Unit II

The VCU-II is the second-generation Viterbi, Complex Math, and CRC extension to the C28x CPU. The VCU-II extends the capabilities of the C28x CPU by adding registers and instructions to accelerate the performance of Fast Fourier Transforms (FFTs) and communications-based algorithms. The C28x+VCU-II supports the following algorithm types:

- **Viterbi Decoding**

Viterbi decoding is commonly used in baseband communications applications. The Viterbi decode algorithm consists of three main parts: branch metric calculations, compare-select (Viterbi butterfly), and a traceback operation. [Table 6-11](#) shows a summary of the VCU performance for each of these operations.

Table 6-11. Viterbi Decode Performance

| VITERBI OPERATION | VCU CYCLES |
|---|------------------|
| Branch Metric Calculation (code rate = 1/2) | 1 |
| Branch Metric Calculation (code rate = 1/3) | 2p |
| Viterbi Butterfly (add-compare-select) | 2 ⁽¹⁾ |
| Traceback per Stage | 3 ⁽²⁾ |

(1) C28x CPU takes 15 cycles per butterfly.

(2) C28x CPU takes 22 cycles per stage.

- **Cyclic Redundancy Check**

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCU can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCU can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

- **Complex Math**

Complex math is used in many applications, a few of which are:

- Fast Fourier Transform

The complex FFT is used in spread spectrum communications, as well as in many signal processing algorithms.

- Complex filters

Complex filters improve data reliability, transmission distance, and power efficiency. The C28x+VCU can perform a complex I and Q multiply with coefficients (four multiplies) in a single cycle. In addition, the C28x+VCU can read/write the real and imaginary parts of 16-bit complex data to memory in a single cycle.

[Table 6-12](#) shows a summary of the VCU operations enabled by the VCU.

Table 6-12. Complex Math Performance

| COMPLEX MATH OPERATION | VCU CYCLES | NOTES |
|-------------------------------|------------|---|
| Add or Subtract | 1 | 32 +/- 32 = 32-bit (Useful for filters) |
| Add or Subtract | 1 | 16 +/- 32 = 15-bit (Useful for FFT) |
| Multiply | 2p | 16 x 16 = 32-bit |
| Multiply and Accumulate (MAC) | 2p | 32 + 32 = 32-bit, 16 x 16 = 32-bit |
| RPT MAC | 2p+N | Repeat MAC. Single cycle after the first operation. |

For more information, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

6.7 Control Law Accelerator

The CLA is an independent single-precision (32-bit) FPU processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes, the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM, eCAP, eQEP, Comparator and DAC registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

Figure 6-2 shows the CLA block diagram.

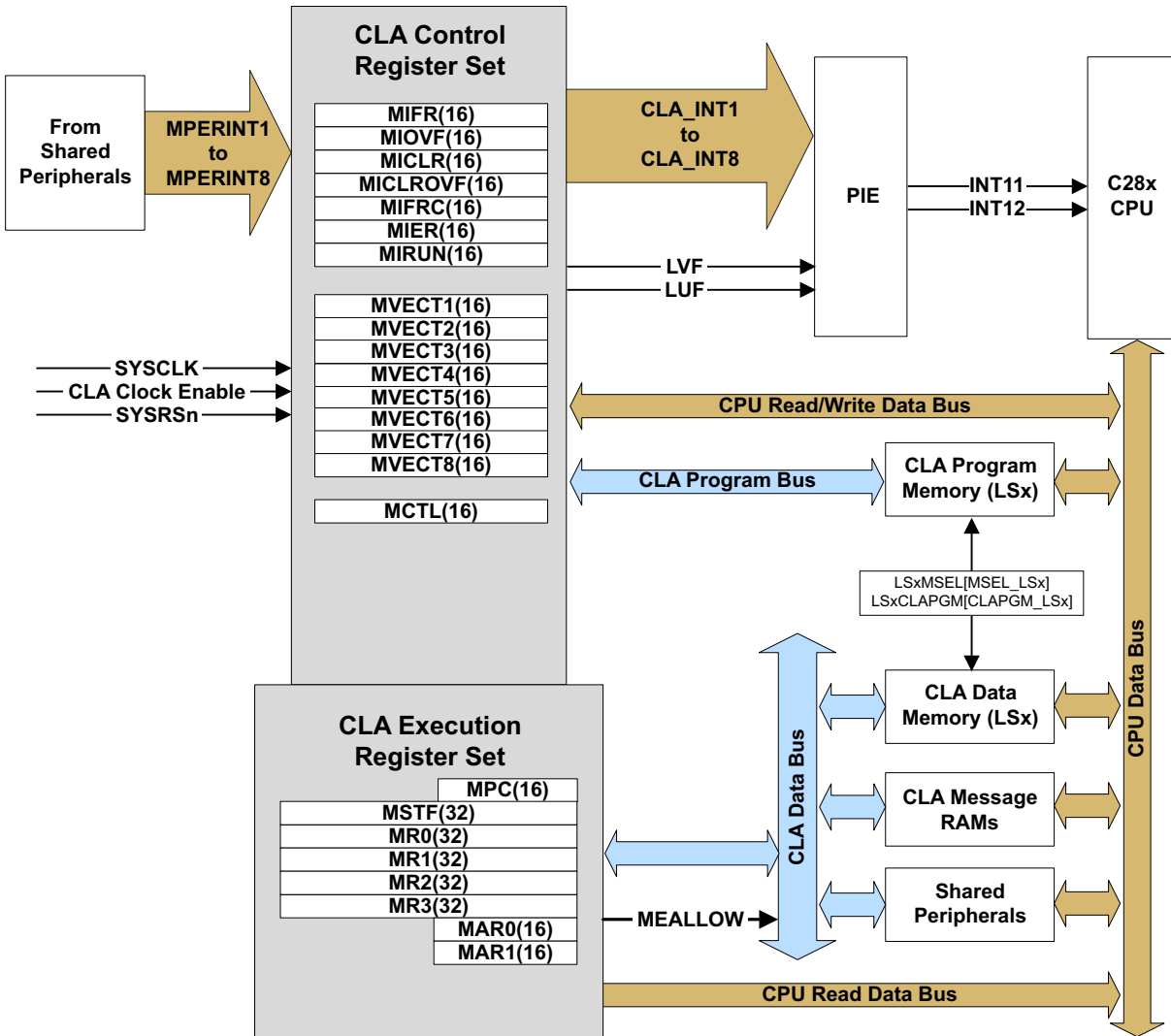


Figure 6-2. CLA Block Diagram

6.8 Direct Memory Access

The CPU has its own 6-channel DMA module. The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the interrupt trigger source, there is no mechanism within the module itself to start memory transfers periodically. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
 - ADC interrupts and EVT signals
 - Multichannel buffered serial port transmit and receive
 - External interrupts
 - CPU timers
 - EPWMxSOC signals
 - SPIx transmit and receive
 - SDFM
 - Software trigger
- Data sources and destinations:
 - GSx RAM
 - ADC result registers
 - ePWMx
 - SPI
 - McBSP
 - EMIF
- Word Size: 16-bit or 32-bit (SPI and McBSP limited to 16-bit)
- Throughput: four cycles/word (without arbitration)

Figure 6-3 shows a device-level block diagram of the DMA.

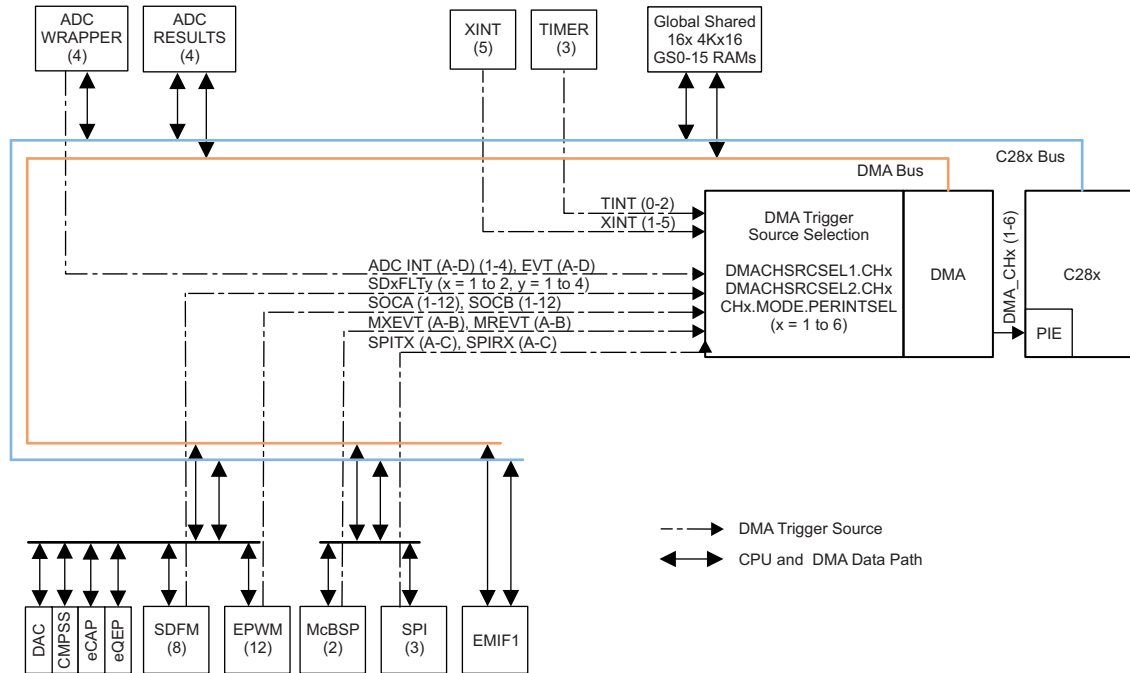


Figure 6-3. DMA Block Diagram

6.9 Boot ROM and Peripheral Booting

The device boot ROM contains bootloading software. The device boot ROM is executed each time the device comes out of reset. Users can configure the device to boot to flash (using GET mode) or choose to boot the device through one of the bootable peripherals by configuring the boot mode GPIO pins.

Table 6-13 shows the possible boot modes supported on the device. The default boot mode pins are GPIO72 (boot mode pin 1) and GPIO 84 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user-configurable Dual Code Security Module (DCSM) OTP locations. This is recommended only for cases in which the factory default boot mode pins do not fit into the customer design. More details on the locations to be programmed is available in the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

Table 6-13. Device Boot Mode

| MODE NO. | CPU1 BOOT MODE | $\overline{\text{TRST}}$ | GPIO72 (BOOT MODE PIN 1) | GPIO84 (BOOT MODE PIN 0) |
|----------|------------------------------------|--------------------------|-----------------------------------|-----------------------------------|
| 0 | Parallel I/O | 0 | 0 | 0 |
| 1 | SCI Mode | 0 | 0 | 1 |
| 2 | Wait Boot Mode | 0 | 1 | 0 |
| 3 | Get Mode | 0 | 1 | 1 |
| 4-7 | EMU Boot Mode (Emulator Connected) | 1 | X | X |

NOTE

The default behavior of Get mode is boot-to-flash. On unprogrammed devices, using Get mode will result in repeated watchdog resets, which may prevent proper JTAG connection and device initialization. Use Wait mode or another boot mode for unprogrammed devices.

CAUTION

Some reset sources are internally driven by the device. The user must ensure the pins used for boot mode are not actively driven by other devices in the system for these cases. The boot configuration has a provision for changing the boot pins in OTP. For more details, see the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

6.9.1 EMU Boot or Emulation Boot

The CPU enters this boot when it detects that $\overline{\text{TRST}}$ is HIGH (in other words, when an emulator/debugger is connected). In this mode, the user can program the EMUBOOTCTRL register (at location 0xD00) to instruct the device on how to boot. If the contents of the EMUBOOTCTRL locations are invalid, then the device would default into WAIT Boot mode. The emulation boot allows users to verify the device boot before programming the boot mode into OTP.

6.9.2 WAIT Boot Mode

The device in this boot mode loops in the boot ROM. This mode is useful if users want to connect a debugger on a secure device or if users do not want the device to execute an application in flash yet.

6.9.3 Get Mode

The default behavior of Get mode is boot-to-flash. This behavior can be changed by programming the Zx-OTPBOOTCTRL locations in user configurable DCSM OTP. The user configurable DCSM OTP on this device is divided in to two secure zones: Z1 and Z2. The Get mode function in boot ROM first checks if a valid OTPBOOTCTRL value is programmed in Z1. If the answer is yes, then the device boots as per the Z1-OTPBOOTCTRL location. The Z2-OTPBOOTCTRL location is read and decodes only if Z1-OTPBOOTCTRL is invalid or not programmed. If either Zx-OTPBOOTCTRL location is not programmed, then the device defaults to factory default operation, which is to use factory default boot mode pins to boot to flash if the boot mode pins are set to GET MODE. Users can choose the device through which to boot—SPI, I2C, CAN, and USB—by programming proper values into the user configurable DCSM OTP. More details on this can be found in the [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#).

6.9.4 Peripheral Pins Used by Bootloaders

Table 6-14 shows the GPIO pins used by each peripheral bootloader. This device supports two sets of GPIOs for each mode, as shown in Table 6-14.

Table 6-14. GPIO Pins Used by Each Peripheral Bootloader

| BOOTLOADER | GPIO PINS | NOTES |
|---------------|---|---|
| SCI-Boot0 | SCITXDA: GPIO84 SCIRXDA: GPIO85 | SCIA Boot I/O option 1 (default SCI option when chosen through Boot Mode GPIOs) |
| SCI-Boot1 | SCITXDA: GPIO28 SCIRXDA: GPIO29 | SCIA Boot option 2 – with alternate I/Os. |
| Parallel Boot | D0 – GPIO65 D1 – GPIO64 D2 – GPIO58 D3 – GPIO59 D4 – GPIO60 D5 – GPIO61 D6 – GPIO62 D7 – GPIO63 HOST_CTRL – GPIO70 DSP_CTRL – GPIO69 | |
| CAN-Boot0 | CANRXA: GPIO70 CANTXA: GPIO71 | CAN-A Boot – I/O option 1 |
| CAN-Boot1 | CANRXA: GPIO62 CANTXA: GPIO63 | CAN-A Boot – I/O option 2 |
| I2C-Boot0 | SDAA: GPIO91 SCLA: GPIO92 | I2CA Boot – I/O option 1 |
| I2C-Boot1 | SDAA: GPIO32 SCLA: GPIO33 | I2CA Boot – I/O option 2 |
| SPI-Boot0 | SPISIMOA - GPIO58 SPISOMIA - GPIO59 SPICLKA - GPIO60 SPISTEA - GPIO61 | SPIA Boot – I/O option 1 |
| SPI-Boot1 | SPISIMOA – GPIO16 SPISOMIA – GPIO17 SPICLKA – GPIO18 SPISTEA – GPIO19 | SPIA Boot – I/O option 2 |
| USB Boot | USB0DM - GPIO42 USB0DP - GPIO43 | The USB Bootloader will switch the clock source to the external crystal oscillator (X1 and X2 pins). A 20-MHz crystal should be present on the board if this boot mode is selected. |

6.10 Dual Code Security Module

The dual code security module (DCSM) prevents access to on-chip secure memories. The term “secure” means access to secure memories and resources is blocked. The term “unsecure” means access is allowed; for example, through a debugging tool such as Code Composer Studio™ (CSS).

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (CLA, LSx RAM, and flash sectors).

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP.

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

6.11 Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presetable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)
- AUXPLLCLK

6.12 Nonmaskable Interrupt With Watchdog Timer (NMIWD)

The NMIWD module is used to handle system-level errors. The conditions monitored are:

- Missing system clock due to oscillator failure
- Uncorrectable ECC error on CPU access to flash memory
- Uncorrectable ECC error on CPU, CLA, or DMA access to RAM

If the CPU does not respond to the latched error condition, then the NMI watchdog will trigger a reset after a programmable time interval. The default time is 65536 SYSCLK cycles.

6.13 Watchdog

The watchdog module is the same as the one on previous TMS320C2000 devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 6-4 shows the various functional blocks within the watchdog module.

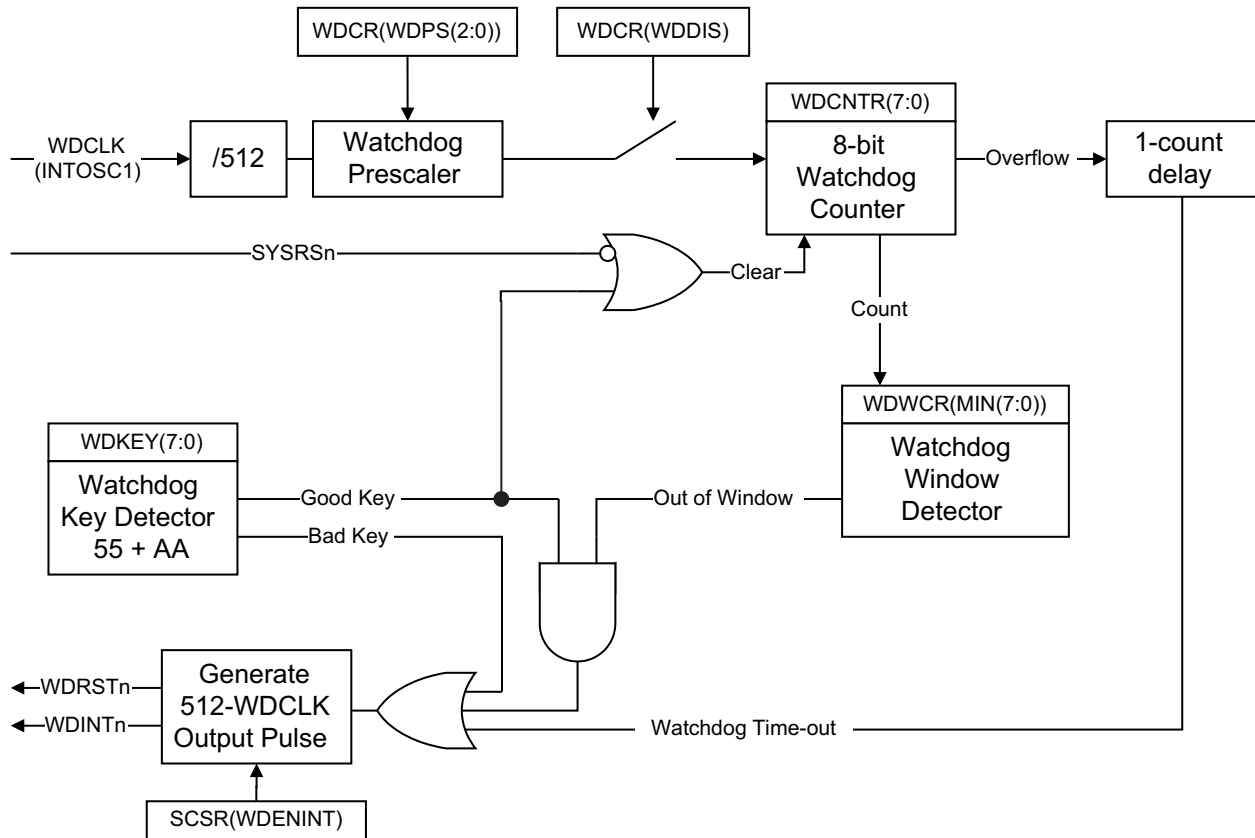


Figure 6-4. Windowed Watchdog

6.14 Configurable Logic Block (CLB)

TI uses the CLB to offer additional interfacing and control features for select C2000 devices. Functions that would otherwise be accomplished using external logic devices are now provided by on-chip TI solutions. For example, absolute encoder master protocol interfaces such as EnDat and BiSS are now provided as [Position Manager](#) solutions. Configuration files, application programmer's interface (API), and use examples for such solutions are provided with the [C2000Ware](#) software package. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality. In some cases, external communications transceivers may need to be added. See [Table 3-1](#) for the devices that support the CLB feature.

7 Applications, Implementation, and Layout

NOTE

Information in the following sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 TI Design or Reference Design

TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at [TIDesigns](#).

[Industrial Servo Drive and AC Inverter Drive Reference Design](#)

The DesignDRIVE Development Kit is a reference design for a complete industrial drive directly connecting to a three-phase ACI or PMSM motor. Many drive topologies can be created from the combined control, power, and communications technologies included on this single platform. This platform includes multiple position sensor interfaces, diverse current sensing techniques, hot-side partitioning options, and expansion for safety and industrial Ethernet.

[Differential Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors](#)

This design provides a 4-channel signal conditioning solution for differential ADCs integrated into a microcontroller measuring motor current using fluxgate sensors. Also provided is an alternative measurement circuit with external differential SAR ADCs as well as circuits for high-speed overcurrent and earth fault detection. Proper differential signal conditioning improves noise immunity on critical current measurements in motor drives. This reference design can help increase the effective resolution of the analog-to-digital conversion, improving motor drive efficiency.

8 Device and Documentation Support

8.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F28379S**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

- TMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- TMS** Fully qualified production device

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing
- TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

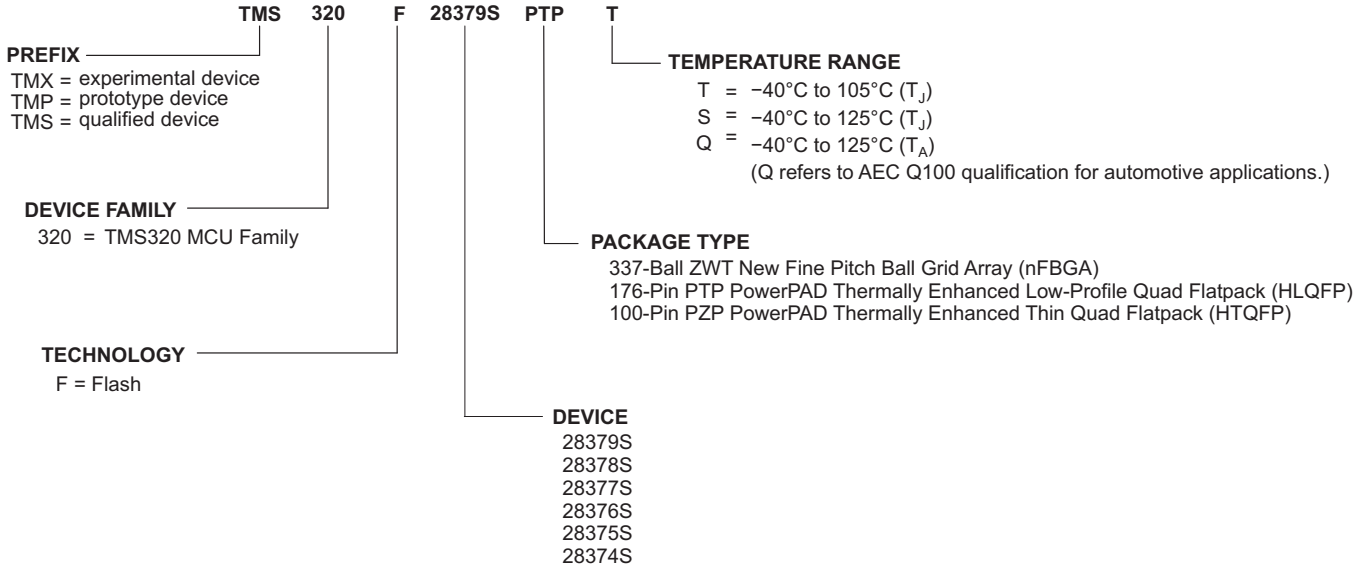
TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PTP) and temperature range (for example, T). [Figure 8-1](#) provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [TMS320F2837xS Delfino™ MCUs Silicon Errata](#).



8.2 Markings

Figure 8-2 provides an example of the 2837xS device markings and defines each of the markings. The device revision can be determined by the symbols marked on the top of the package as shown in Figure 8-2. Some prototype devices may have markings different from those illustrated.

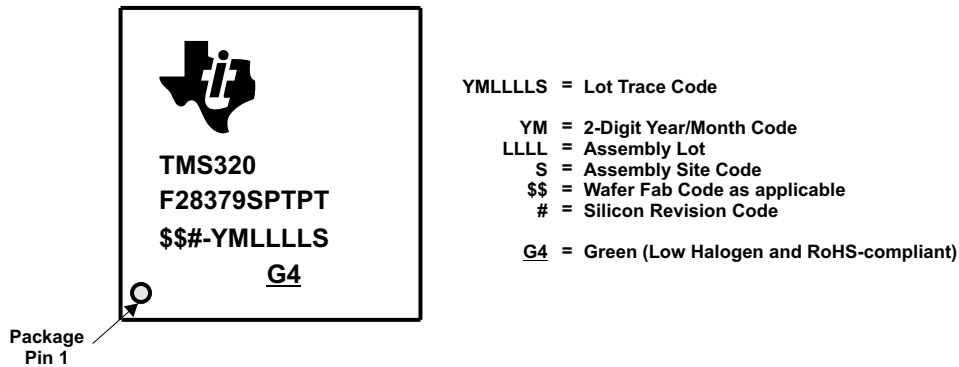


Table 8-1. Determining Silicon Revision From Lot Trace Code

| SILICON REVISION CODE | SILICON REVISION | REVID ⁽¹⁾ Address: 0x5D00C | COMMENTS |
|-----------------------|------------------|--|--|
| B | B | 0x0002 | This silicon revision is available as TMX. |
| C | C | 0x0003 | This silicon revision is available as TMS. |

(1) Silicon Revision ID

8.3 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below. To view all available tools and software for C2000™ real-time control MCUs, visit the [C2000 MCU Tools and Software](#) page.

Development Tools

[F28379D controlCARD for C2000 Real time control development kits](#)

The Delfino F28379D controlCARD from Texas Instruments is Position Manager-ready and an ideal product for initial software development and short run builds for system prototypes, test stands, and many other projects that require easy access to high-performance controllers. All C2000 controlCARDS are complete board-level modules that utilize a HSEC180 or DIMM100 form factor to provide a low-profile single-board controller solution. The host system needs to provide only a single 5V power rail to the controlCARD for it to be fully functional.

[F28379D Delfino Experimenter Kit](#)

C2000™ MCU Experimenter Kits provide a robust hardware prototyping platform for real-time, closed loop control development with Texas Instruments C2000 32-bit microcontroller family. This platform is a great tool to customize and prove-out solutions for many common power electronics applications, including motor control, digital power supplies, solar inverters, digital LED lighting, precision sensing, and more.

Software Tools

[C2000Ware for C2000 MCUs](#)

C2000Ware for C2000 microcontrollers is a cohesive set of development software and documentation designed to minimize software development time. From device-specific drivers and libraries to device peripheral examples, C2000Ware provides a solid foundation to begin development and evaluation. C2000Ware is now the recommended content delivery tool versus controlSUITE™.

[Code Composer Studio™ \(CCS\) Integrated Development Environment \(IDE\) for C2000 Microcontrollers](#)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

[Pin Mux Tool](#)

The Pin Mux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs.

[F021 Flash Application Programming Interface \(API\)](#)

The F021 Flash Application Programming Interface (API) provides a software library of functions to program, erase, and verify F021 on-chip Flash memory.

[UniFlash Standalone Flash Tool](#)

UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

Models

Various models are available for download from the product Tools & Software pages. These include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Models section of the Tools & Software page for each device, which can be found in [Table 8-2](#).

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the [Support and training for C2000™ real-time control MCUs](#) site.

Specific F2837xD/F2837xS/F2807x hands-on training resources can be found at the following sites:

- [C2000 Multi-Day Workshop](#)
- [C2000 One-Day Workshop](#)

8.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

Errata

[TMS320F2837xS Delfino™ MCUs Silicon Errata](#) describes known advisories on silicon and provides workarounds.

Technical Reference Manual

[TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 2837xS microcontrollers.

CPU User's Guides

[TMS320C28x CPU and Instruction Set Reference Guide](#) describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

[TMS320C28x Extended Instruction Sets Technical Reference Manual](#) describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

[C2000 Real-Time Control Peripherals Reference Guide](#) describes the peripheral reference guides of the 28x DSPs.

Tools Guides

[TMS320C28x Assembly Language Tools v18.9.0.STS User's Guide](#) describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

[TMS320C28x Optimizing C/C++ Compiler v18.9.0.STS User's Guide](#) describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

[Semiconductor Packing Methodology](#) describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

[Calculating Useful Lifetimes of Embedded Processors](#) provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

[An Introduction to IBIS \(I/O Buffer Information Specification\) Modeling](#) discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures and future trends.

[Serial Flash Programming of C2000™ Microcontrollers](#) discusses using a flash kernel and ROM loaders for serial programming a device.

8.5 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 8-2. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TMS320F28379S | Click here | Click here | Click here | Click here | Click here |
| TMS320F28378S | Click here | Click here | Click here | Click here | Click here |
| TMS320F28377S | Click here | Click here | Click here | Click here | Click here |
| TMS320F28376S | Click here | Click here | Click here | Click here | Click here |
| TMS320F28375S | Click here | Click here | Click here | Click here | Click here |
| TMS320F28374S | Click here | Click here | Click here | Click here | Click here |

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 Trademarks

PowerPAD, Delfino, C2000, Code Composer Studio, TMS320, controlSUITE, E2E are trademarks of Texas Instruments.

Bosch is a registered trademark of Robert Bosch GmbH Corporation.

All other trademarks are the property of their respective owners.

8.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.9 Glossary

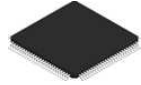
TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

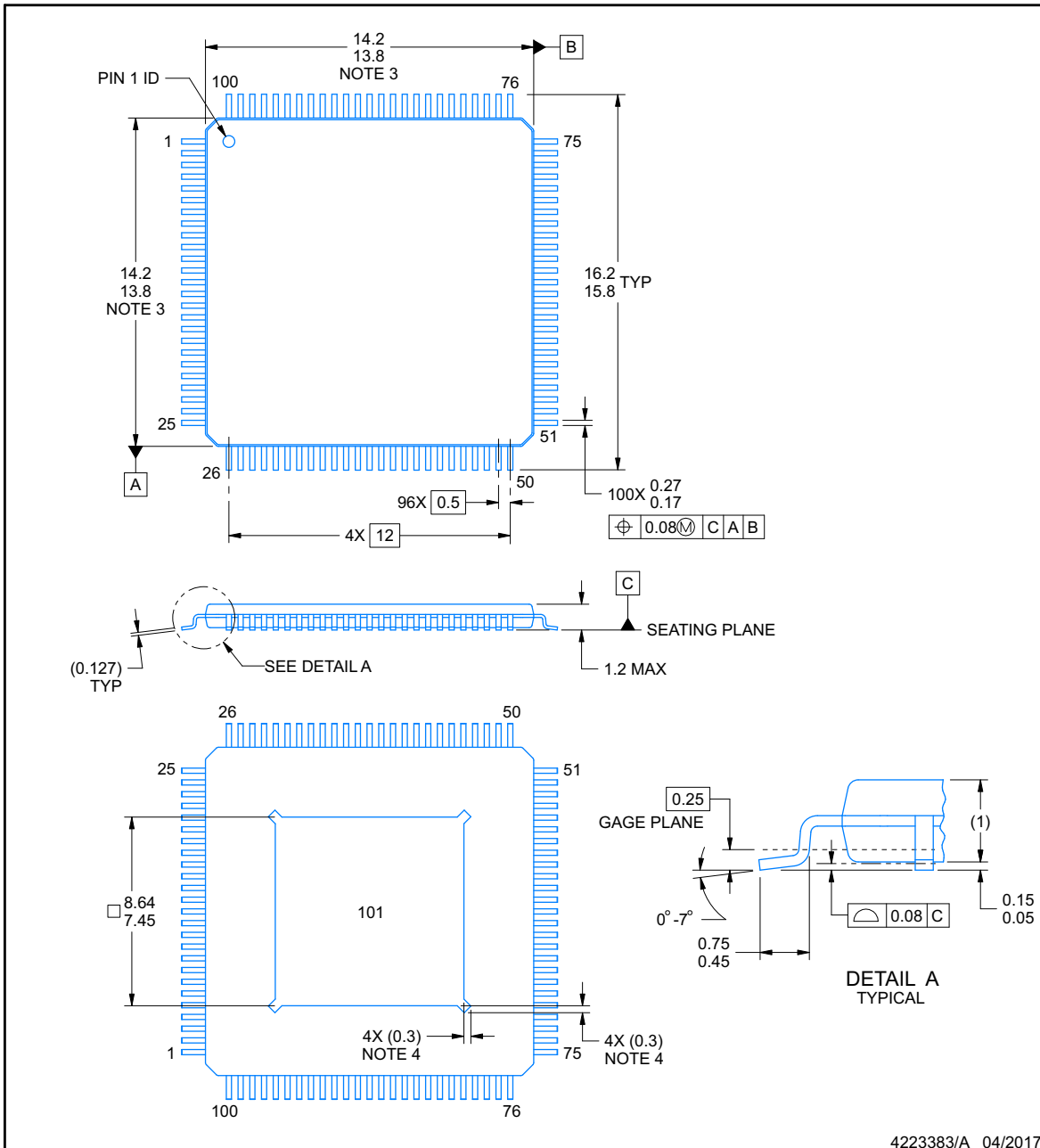
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PZP0100N



PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



4223383/A 04/2017

PowerPAD is a trademark of Texas Instruments.

NOTES:

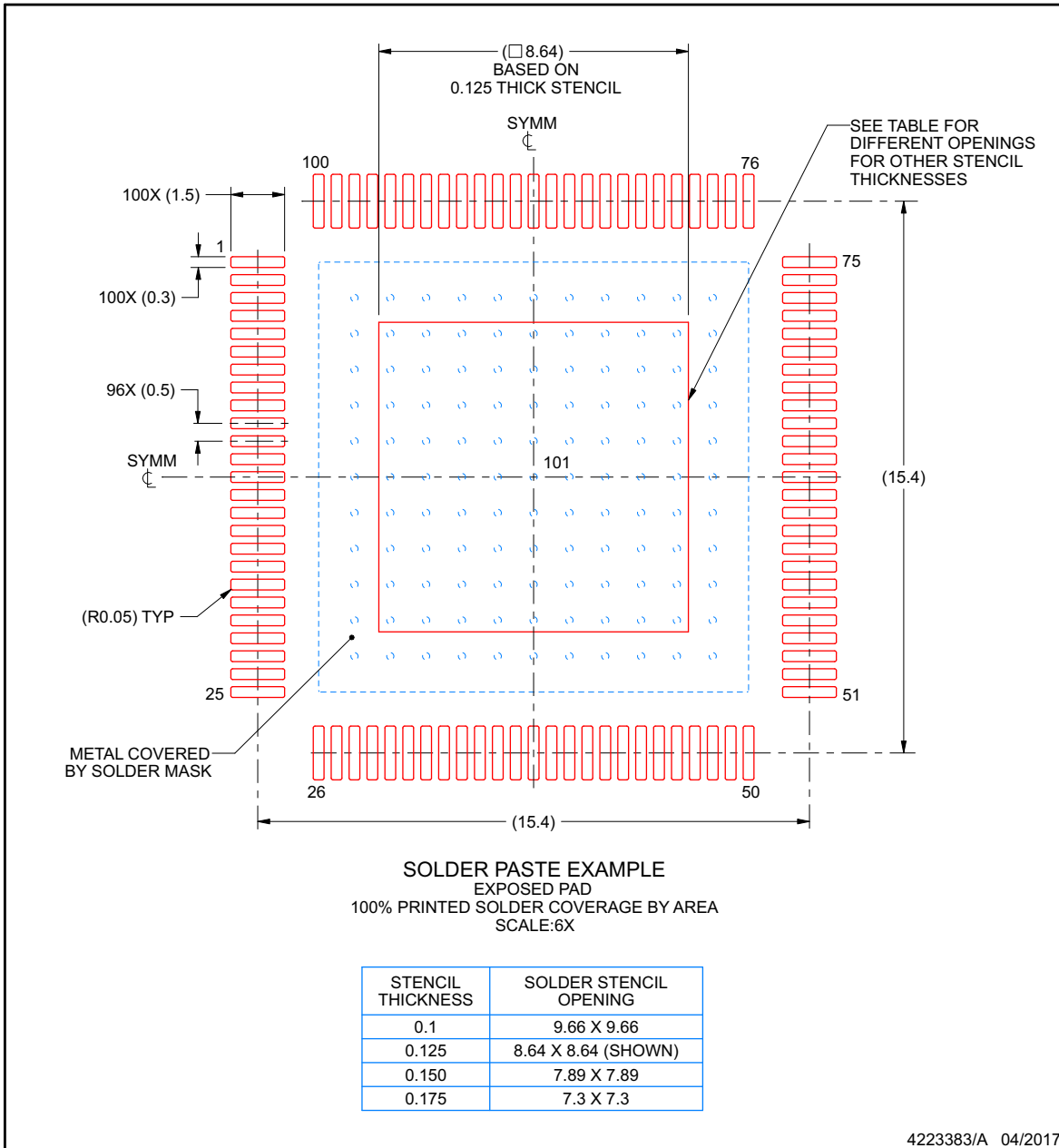
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

EXAMPLE STENCIL DESIGN

PZP0100N

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

www.ti.com

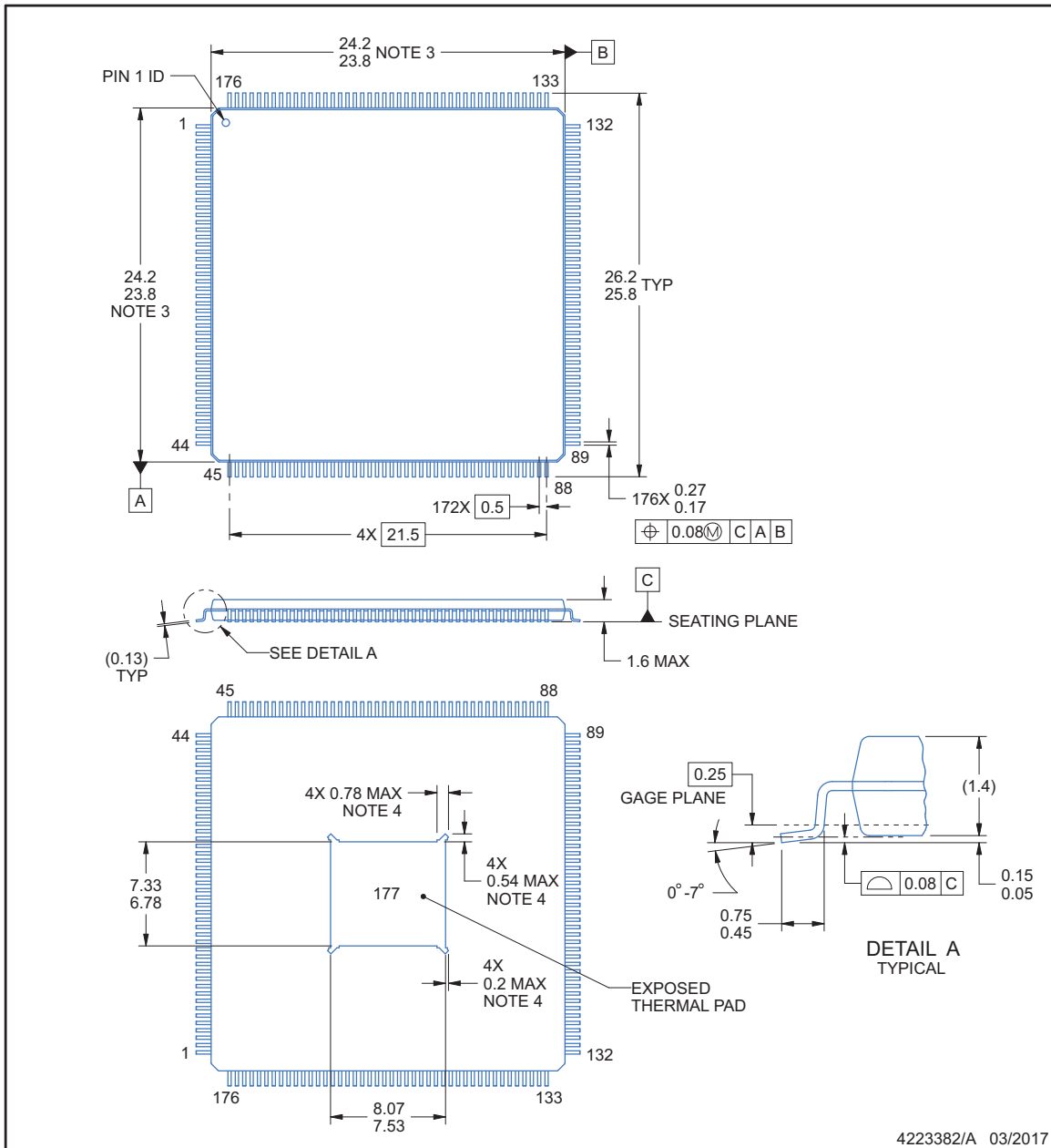


PACKAGE OUTLINE

PTP0176F

PowerPAD™ HLQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4223382/A 03/2017

PowerPAD is a trademark of Texas Instruments.

NOTES:

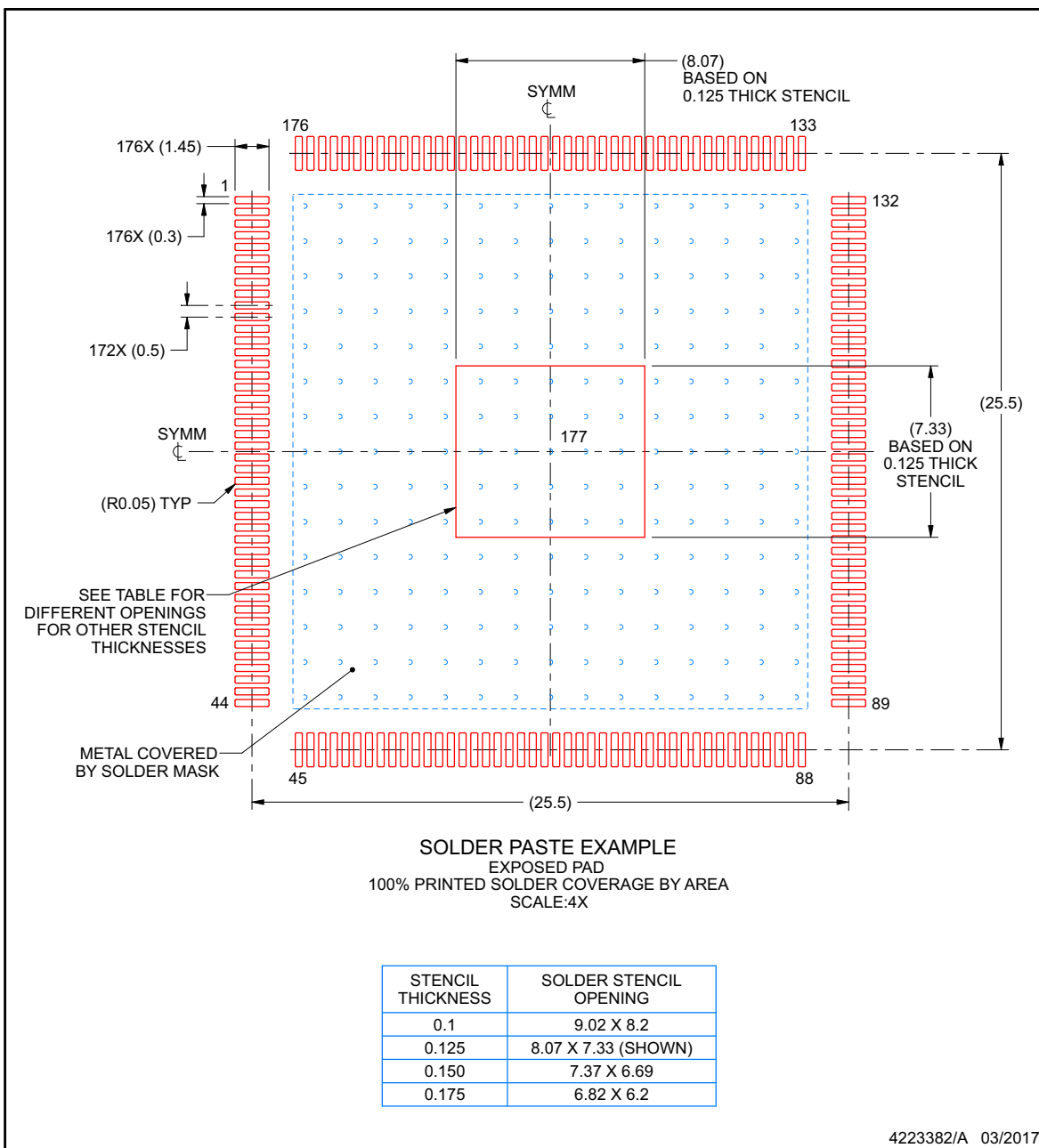
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

EXAMPLE STENCIL DESIGN

PTP0176F

PowerPAD™ HLQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TMS320F28374SPTPS | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28374SPTPS | Samples |
| TMS320F28374SPTPT | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28374SPTPT | Samples |
| TMS320F28374SPZPS | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28374SPZPS | Samples |
| TMS320F28374SPZPT | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28374SPZPT | Samples |
| TMS320F28374SZWTS | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28374SZWTS | Samples |
| TMS320F28374SZWTT | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28374SZWTT | Samples |
| TMS320F28374SZWTR | ACTIVE | NFBGA | ZWT | 337 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28374SZWTR | Samples |
| TMS320F28375SPTPS | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28375SPTPS | Samples |
| TMS320F28375SPTPT | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28375SPTPT | Samples |
| TMS320F28375SPZPQ | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS320 F28375SPZPQ | Samples |
| TMS320F28375SPZPQR | ACTIVE | HTQFP | PZP | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS320 F28375SPZPQR | Samples |
| TMS320F28375SPZPS | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28375SPZPS | Samples |
| TMS320F28375SPZPT | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28375SPZPT | Samples |
| TMS320F28375SZWTS | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28375SZWTS | Samples |
| TMS320F28375SZWTT | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28375SZWTT | Samples |
| TMS320F28376SPTPS | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28376SPTPS | Samples |
| TMS320F28376SPTPT | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28376SPTPT | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TMS320F28376SPZPS | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28376SPZPS | Samples |
| TMS320F28376SPZPT | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28376SPZPT | Samples |
| TMS320F28376SZWTS | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28376SZWTS | Samples |
| TMS320F28376SZWTT | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28376SZWTT | Samples |
| TMS320F28377SPTPQ | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS320 F28377SPTPQ | Samples |
| TMS320F28377SPTPS | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28377SPTPS | Samples |
| TMS320F28377SPTPT | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28377SPTPT | Samples |
| TMS320F28377SPZPQ | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS320 F28377SPZPQ | Samples |
| TMS320F28377SPZPS | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28377SPZPS | Samples |
| TMS320F28377SPZPT | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28377SPZPT | Samples |
| TMS320F28377SZWTQ | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 125 | TMS320 F28377SZWTQ | Samples |
| TMS320F28377SZWTS | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28377SZWTS | Samples |
| TMS320F28377SZWTT | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28377SZWTT | Samples |
| TMS320F28378SPTPS | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS320 F28378SPTPS | Samples |
| TMS320F28378SPZPS | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS320 F28378SPZPS | Samples |
| TMS320F28379SPTPS | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28379SPTPS | Samples |
| TMS320F28379SPTPT | ACTIVE | HLQFP | PTP | 176 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28379SPTPT | Samples |
| TMS320F28379SPZPS | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28379SPZPS | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TMS320F28379SPZPT | ACTIVE | HTQFP | PZP | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28379SPZPT | Samples |
| TMS320F28379SZWTS | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 0 | TMS320 F28379SZWTS | Samples |
| TMS320F28379SZWTT | ACTIVE | NFBGA | ZWT | 337 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 F28379SZWTT | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

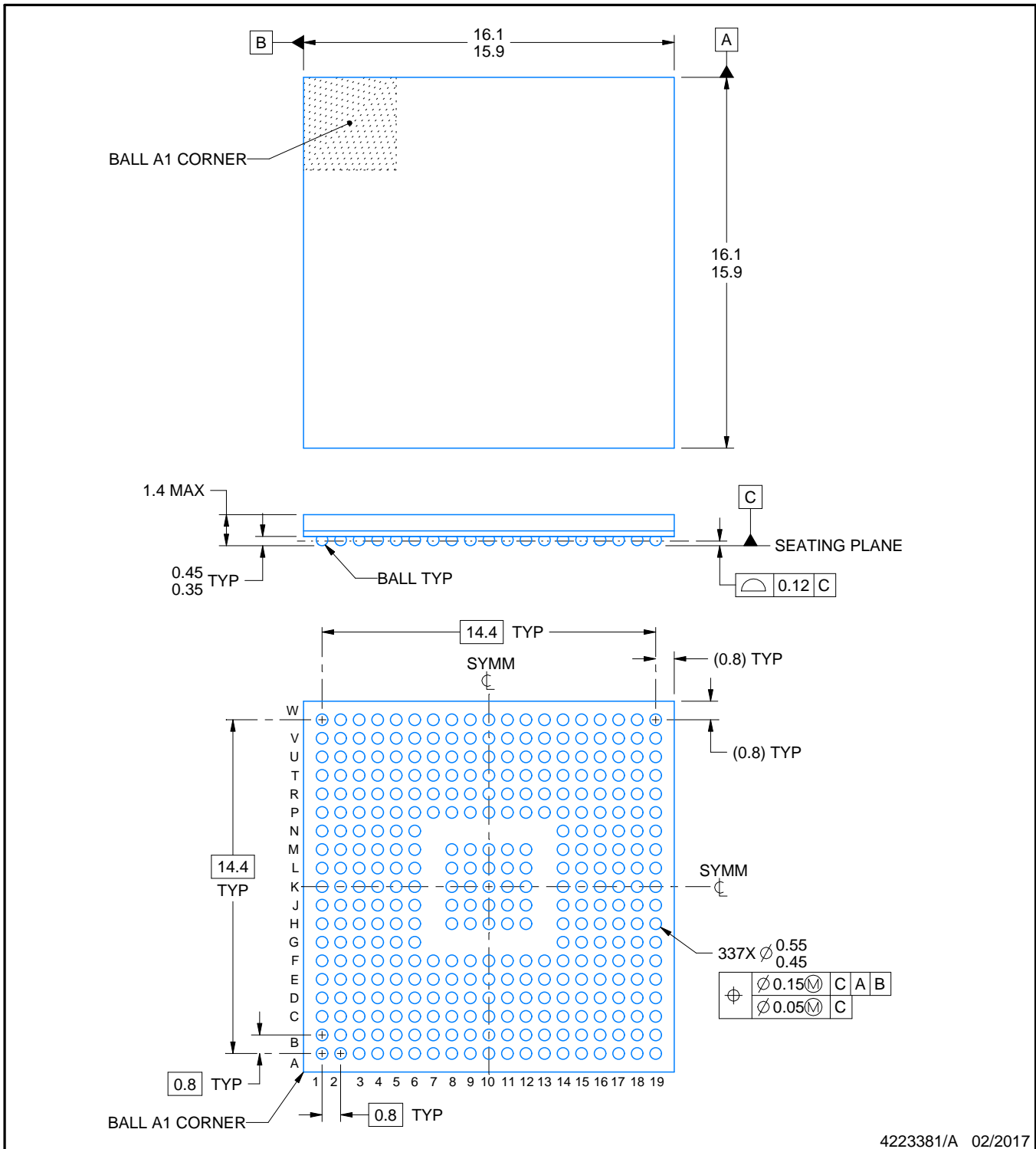
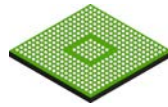
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

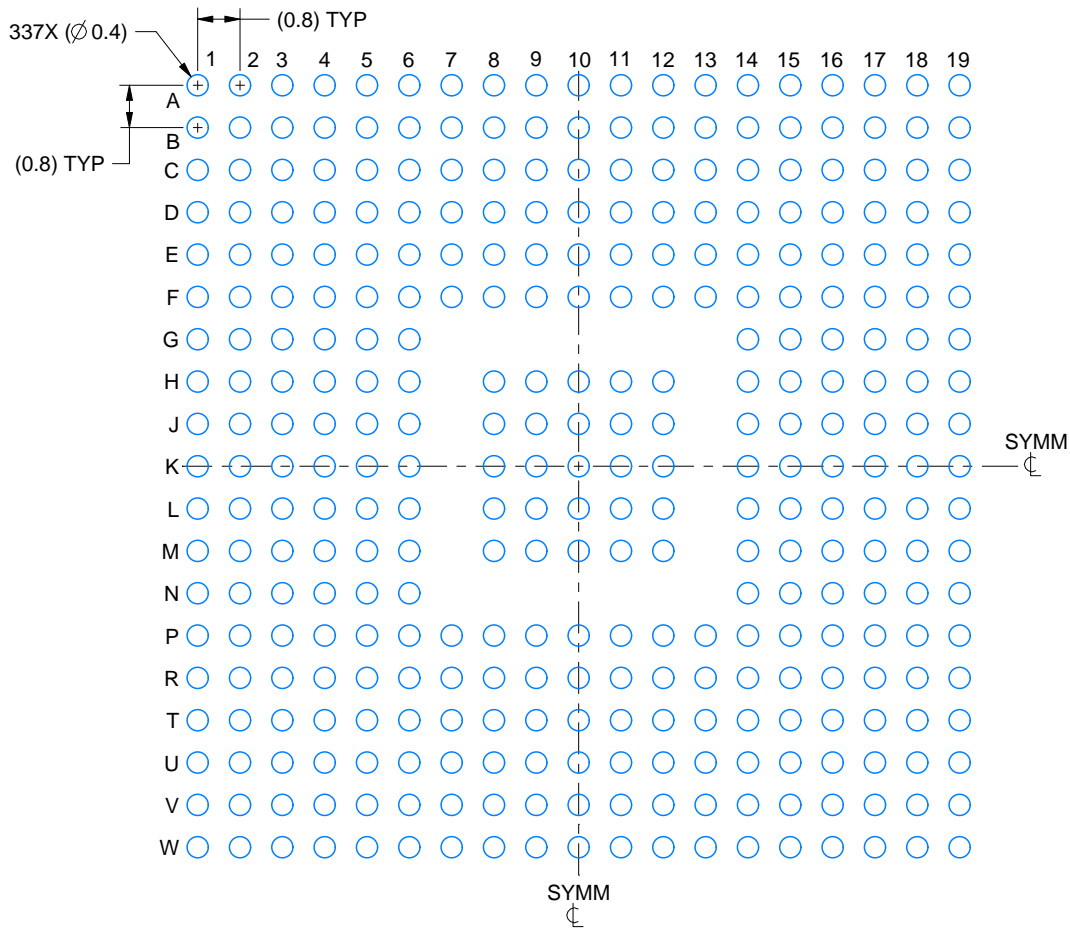
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

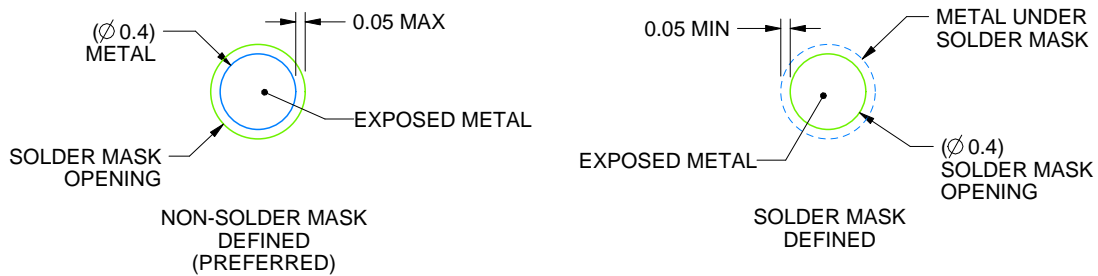
ZWT0337A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:7X



SOLDER MASK DETAILS
NOT TO SCALE

4223381/A 02/2017

NOTES: (continued)

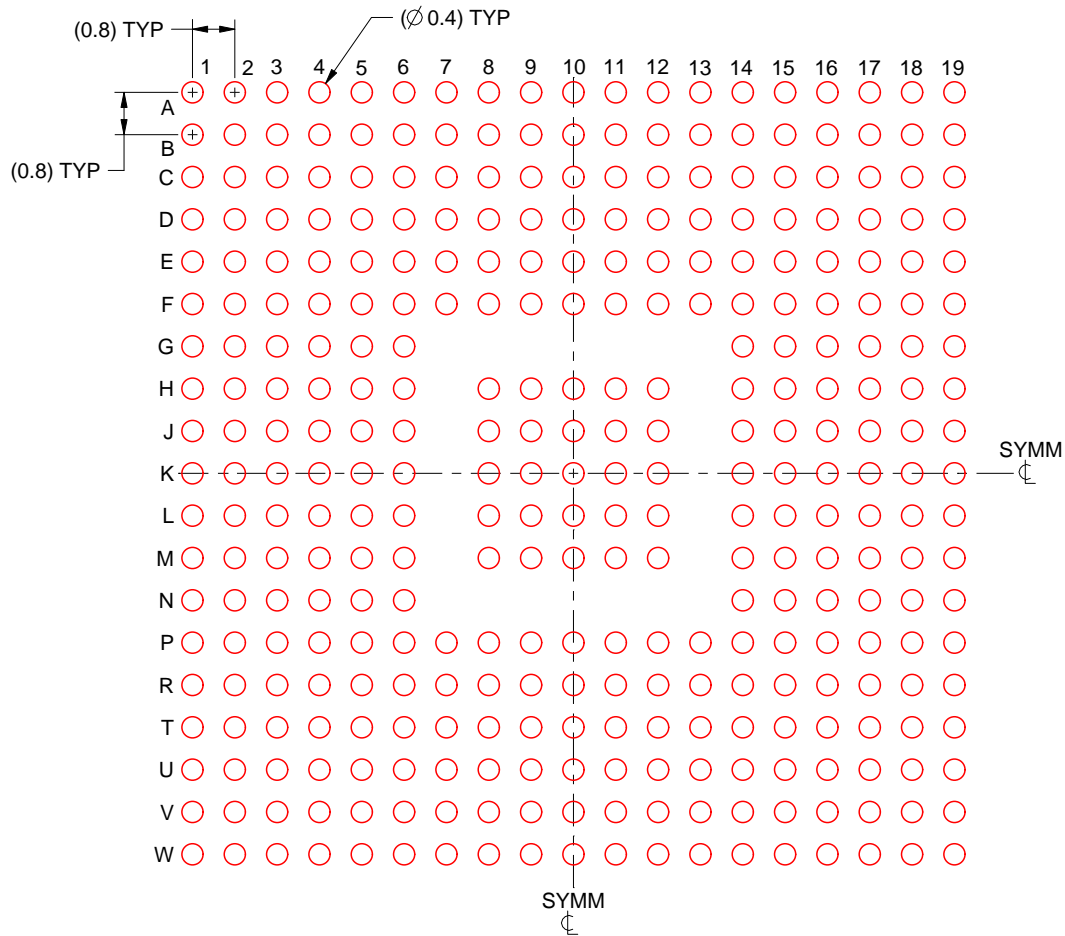
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZWT0337A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:7X

4223381/A 02/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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