



**THE DATASHEET OF  
S558-5999-W2-F**

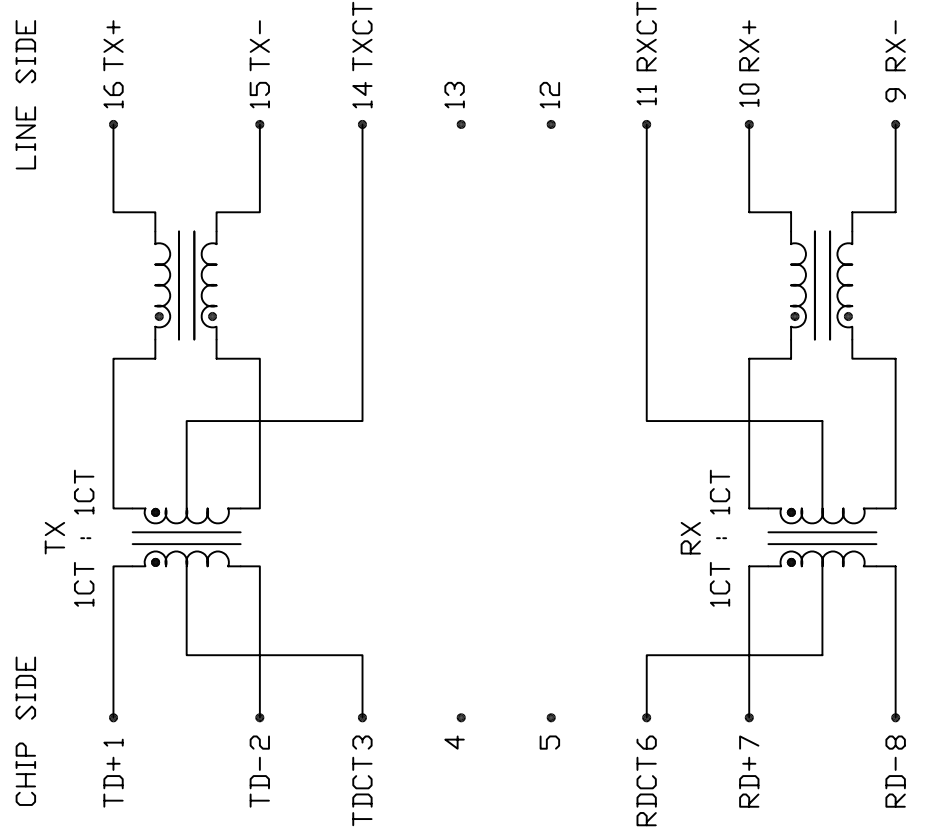


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ELECTRICAL CHARACTERISTICS

URNS RATIO  
 Tx (1-3-2) : (16-14-15)  
 Rx (7-6-8) : (10-11-9)

SCHEMATIC



POLARITY

DCL

1-2 = 7-8

LEAKAGE INDUCTANCE,  $L_e$   
 CHIP SIDE WITH LINE SIDE SHORT

INTERWINDING CAPACITANCE,  $C_w/w$   
 CHIP SIDE TO LINE SIDE

DC RESISTANCE  
 (1-2) = (7-8)

INSERTION LOSS  
 @100kHz TO 80MHz

RETURN LOSS (UNDER 100Ω ±15% ENVIRONMENT)  
 @0.5 TO 30 MHz  
 @30 TO 60 MHz  
 @60 TO 80 MHz

COMMON TO COMMON MODE ATTENUATION  
 @0.1 TO 80 MHz  
 @80 TO 125 MHz  
 @125 TO 250 MHz

CROSSTALK

@0.1 TO 80 MHz  
 @80 TO 125 MHz  
 @125 TO 250 MHz

COMMON TO DIFFERENTIAL MODE ATTENUATION  
 @0.1 TO 80 MHz  
 @80 TO 125 MHz  
 @125 TO 250 MHz

HIPOT

OPERATING TEMPERATURE -40°C TO +85°C

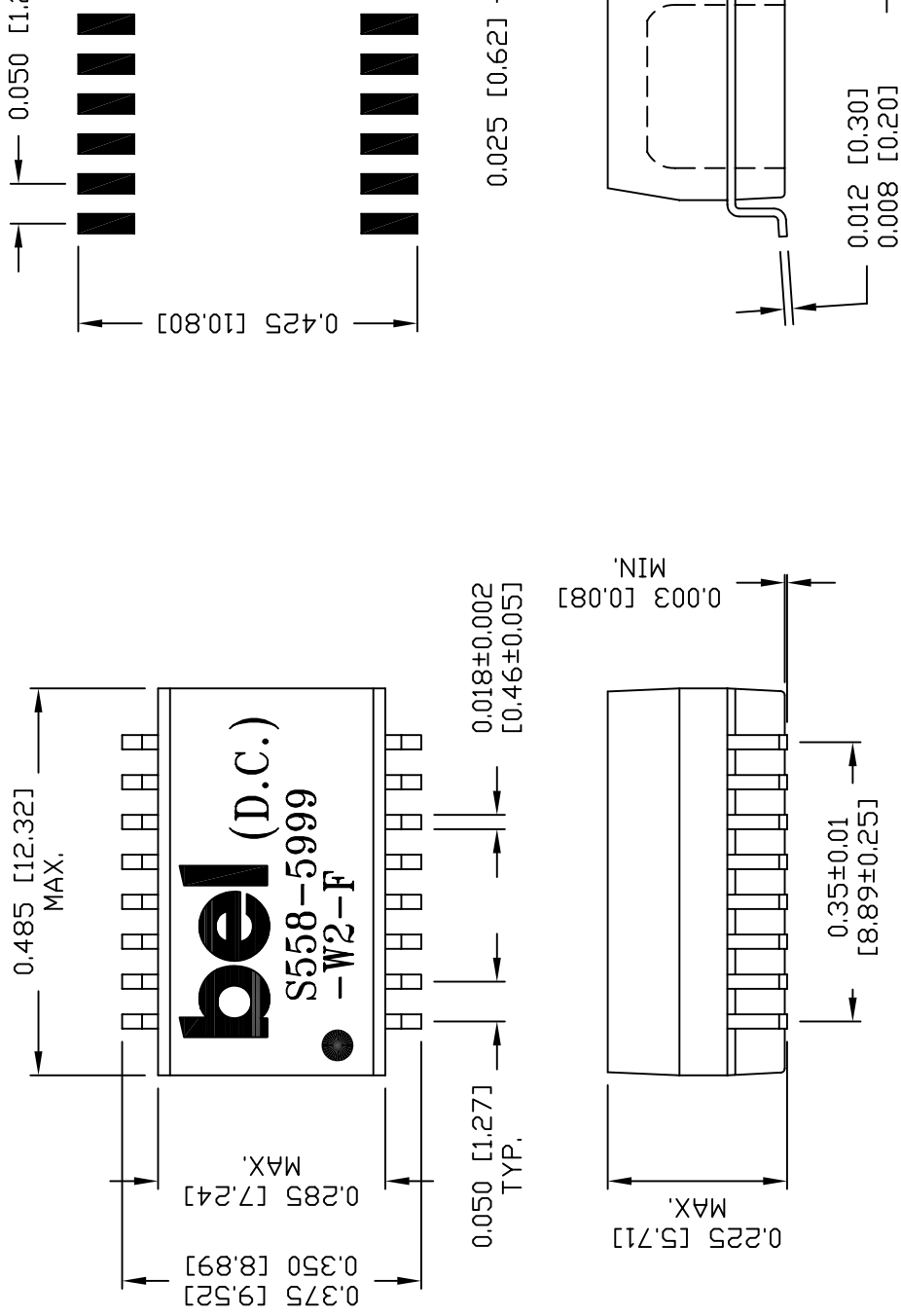
<b>ORIGINATED BY</b> Alice Pang		<b>DATE</b> 2015-01-26		<b>TITLE</b> 10/100BASE-T MODULE S558-5999-W2-F		<b>PART NO. / DRAWING NO.</b> X5585999W2-F		<b>STANDARD DIM. [ ]</b>	
<b>DRAWN BY</b> ZC Guo		<b>DATE</b> 2015-01-26				<b>FILE NAME</b> X5585999W2FC.DWG		<b>TOL. IN INCH</b>	
								.X	
								.XX	
								.XXX	

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SUGGESTED PCB PAI



NOTES:

1. STANDARD MARKING REFER TO DOC. HAND-WORK-04.
2. PACKAGE CODE: "QBS001".



ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM. [ ]
Lawrence Tsang	2015-01-26	MECHANICAL DRAWING	X5585999W2-F	TOL. IN INCH
DRAWN BY	DATE	S558-5999-W2-F	FILE NAME	.X
ZC Guo	2015-01-26		X5585999W2FC.DWG	.XX ±0.01
				.XXX ±0.005
				SCAL
				UNIT

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