THE DATASHEET OF

AD9681BBCZ-125

www.win-source.net 0086-755-83957316

Octal, 14-Bit, 125 MSPS, Serial LVDS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9681**

FEATURES

- Low power
  - 8 ADC channels integrated into 1 package
  - 110 mW per channel at 125 MSPS with scalable power options
- SNR: 74 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)
- DNL: ±0.8 LSB (typical); INL: ±1.2 LSB (typical)
- Crosstalk, worst adjacent channel, 70 MHz, −1 dBFS: −83 dB typical
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 650 MHz full power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation
- Serial port control
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Programmable clock and data alignment
  - Power-down and standby modes

APPLICATIONS

- Medical imaging
- Communications receivers
- Multichannel data acquisition

GENERAL DESCRIPTION

The AD9681 is an octal, 14-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The device operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and an LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The AD9681 automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. Data clock outputs (DCO±1, DCO±2) for capturing data on the output and frame clock outputs (FCO±1, FCO±2) for signaling a new output byte are provided. Individual channel power-down is supported, and the device typically consumes less than 2 mW when all channels are disabled.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

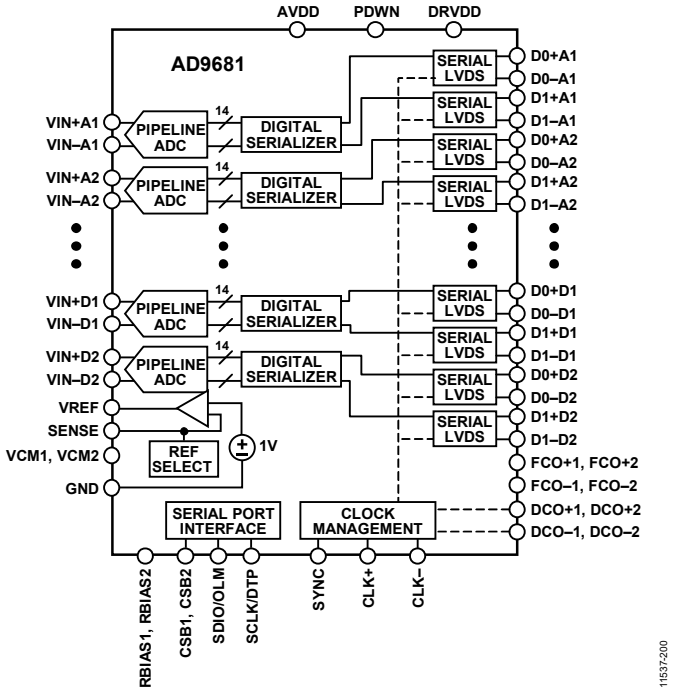

Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9681 is available in an RoHS-compliant, 144-ball CSP-BGA. It is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight ADCs are contained in a small, 10 mm × 10 mm package.
2. Low Power. The device dissipates 110 mW per channel at 125 MSPS with scalable power options.
3. Ease of Use. Data clock outputs (DCO±1, DCO±2) operate at frequencies of up to 500 MHz and support double data rate (DDR) operation.
4. User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. D
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REVISION HISTORY

3/2020—Rev. C to Rev. D

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10/2015—Rev. B to Rev. C

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2/2015—Rev. A to Rev. B

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12/2013—Rev. 0 to Rev. A

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11/2013—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

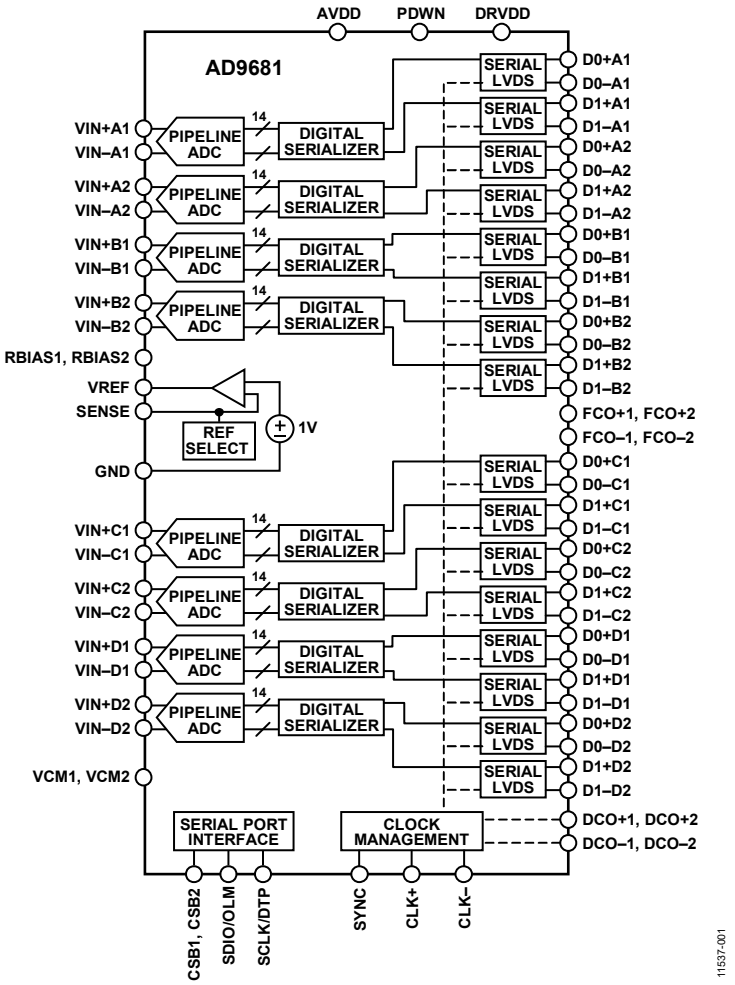

Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.23	+0.21	+0.62	% FSR
Offset Matching	Full	0	0.24	0.7	% FSR
Gain Error	Full	−8.0	−3.1	+1.7	% FSR
Gain Matching	Full	0	1.8	6.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.92	±0.8	+1.75	LSB
Integral Nonlinearity (INL)	Full	−4.0	±1.2	+4.0	LSB
TEMPERATURE DRIFT					
Offset Error	Full		−4		ppm/°C
Gain Error	Full		38		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.98	1.0	1.02	V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	25°C		3		mV
Input Resistance	Full		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		0.99		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full	0.5	0.9	1.3	V
Differential Input Resistance	Full		5.2		kΩ
Differential Input Capacitance	Full		3.5		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}	Full		368	423	mA
I_{DRVDD} (ANSI-644 Mode)	Full		120	126	mA
I_{DRVDD} (Reduced Range Mode)	25°C		90		mA
TOTAL POWER CONSUMPTION					
Total Power Dissipation (Eight Channels, Including Output Drivers ANSI-644 Mode)	Full		879	988	mW
Total Power Dissipation (Eight Channels, Including Output Drivers Reduced Range Mode)	25°C		825		mW
Power-Down Dissipation	25°C		2		mW
Standby Dissipation[2]	25°C		485		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for information about how these tests were completed.
[2] Controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		74.8		dBFS
f_{IN} = 19.7 MHz	25°C		74.7		dBFS
f_{IN} = 69.5 MHz	Full	72.6	73.9		dBFS
f_{IN} = 139.5 MHz	25°C		71.5		dBFS
f_{IN} = 201 MHz	25°C		69.6		dBFS
f_{IN} = 301 MHz	25°C		66.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		74.7		dBFS
f_{IN} = 19.7 MHz	25°C		74.7		dBFS
f_{IN} = 69.5 MHz	Full	72.3	73.8		dBFS
f_{IN} = 139.5 MHz	25°C		71.4		dBFS
f_{IN} = 201 MHz	25°C		69.3		dBFS
f_{IN} = 301 MHz	25°C		65.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.1		Bits
f_{IN} = 19.7 MHz	25°C		12.1		Bits
f_{IN} = 69.5 MHz	Full	11.7	12.0		Bits
f_{IN} = 139.5 MHz	25°C		11.6		Bits
f_{IN} = 201 MHz	25°C		11.2		Bits
f_{IN} = 301 MHz	25°C		10.6		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		94		dBc
f_{IN} = 19.7 MHz	25°C		94		dBc
f_{IN} = 69.5 MHz	Full	81	90		dBc
f_{IN} = 139.5 MHz	25°C		87		dBc
f_{IN} = 201 MHz	25°C		83		dBc
f_{IN} = 301 MHz	25°C		73		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−94		dBc
f_{IN} = 19.7 MHz	25°C		−94		dBc
f_{IN} = 69.5 MHz	Full		−90	−81	dBc
f_{IN} = 139.5 MHz	25°C		−87		dBc
f_{IN} = 201 MHz	25°C		−83		dBc
f_{IN} = 301 MHz	25°C		−73		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−98		dBc
f_{IN} = 19.7 MHz	25°C		−94		dBc
f_{IN} = 69.5 MHz	Full		−96	−84	dBc
f_{IN} = 139.5 MHz	25°C		−90		dBc
f_{IN} = 201 MHz	25°C		−85		dBc
f_{IN} = 301 MHz	25°C		−75		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 70 MHz, f_{IN2} = 72.5 MHz	25°C		94		dBc
CROSSTALK, WORST ADJACENT CHANNEL[2]	25°C		−83		dB
Crosstalk, Worst Adjacent Channel Overrange Condition[3]	25°C		−79		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz, with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is defined as 3 dB above input full scale.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUTS (CSB1, CSB2)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D0±xx, D1±xx), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	290	345	400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0±xx, D1±xx), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	160	200	230	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO/OLM pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1, 2]	Symbol	Temp	Min	Typ	Max	Unit
CLOCK[3]						
Input Clock Rate		Full	10		1000	MHz
Conversion Rate[4]		Full	10		125	MSPS
Clock Pulse Width High	t_{EH}	Full		4.00		ns
Clock Pulse Width Low	t_{EL}	Full		4.00		ns
OUTPUT PARAMETERS[3]						
Propagation Delay	t_{PD}	Full	1.5	2.3	3.1	ns
Rise Time (20% to 80%)	t_R	Full		300		ps
Fall Time (20% to 80%)	t_F	Full		300		ps
FCO±1, FCO±2 Propagation Delay	t_{FCO}	Full	1.5	2.3	3.1	ns
DCO±1, DCO±2 Propagation Delay[5]	t_{CPD}	Full		t_{FCO} + (t_{SAMPLE}/16)		ns
DCO±1, DCO±2 to Data Delay[5]	t_{DATA}	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
DCO±1, DCO±2 to FCO±1, FCO±2 Delay[5]	t_{FRAME}	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
Lane Delay	t_{LD}			90		ps
Data to Data Skew	$t_{DATA-MAX} - t_{DATA-MIN}$	Full		±50	±200	ps
Wake-Up Time (Standby)		25°C		250		ns
Wake-Up Time (Power-Down)[6]		25°C		375		µs
Pipeline Latency		Full		16		Clock cycles
APERTURE						
Aperture Delay	t_A	25°C		1		ns
Aperture Uncertainty (Jitter)	t_J	25°C		135		fs rms
Out-of-Range Recovery Time		25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Adjustable using the SPI. The conversion rate is the clock rate after the divider.
[4] The maximum conversion rate is based on two-lane output mode. See the Digital Outputs and Timing section for the maximum conversion rate in one-lane output mode.
[5] t_{SAMPLE}/16 is based on the number of bits in two LVDS data lanes. $t_{SAMPLE} = 1/f_{SAMPLE}$.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	1.2	ns min
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	−0.2	ns min
SPI TIMING REQUIREMENTS	See Figure 53		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB1/CSB2 and SCLK	2	ns min
t_H	Hold time between CSB1/CSB2 and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 53)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 53)	10	ns min

Timing Diagrams

Refer to the Memory Map Register Descriptions section and Table 21 for SPI register setting of output modes.

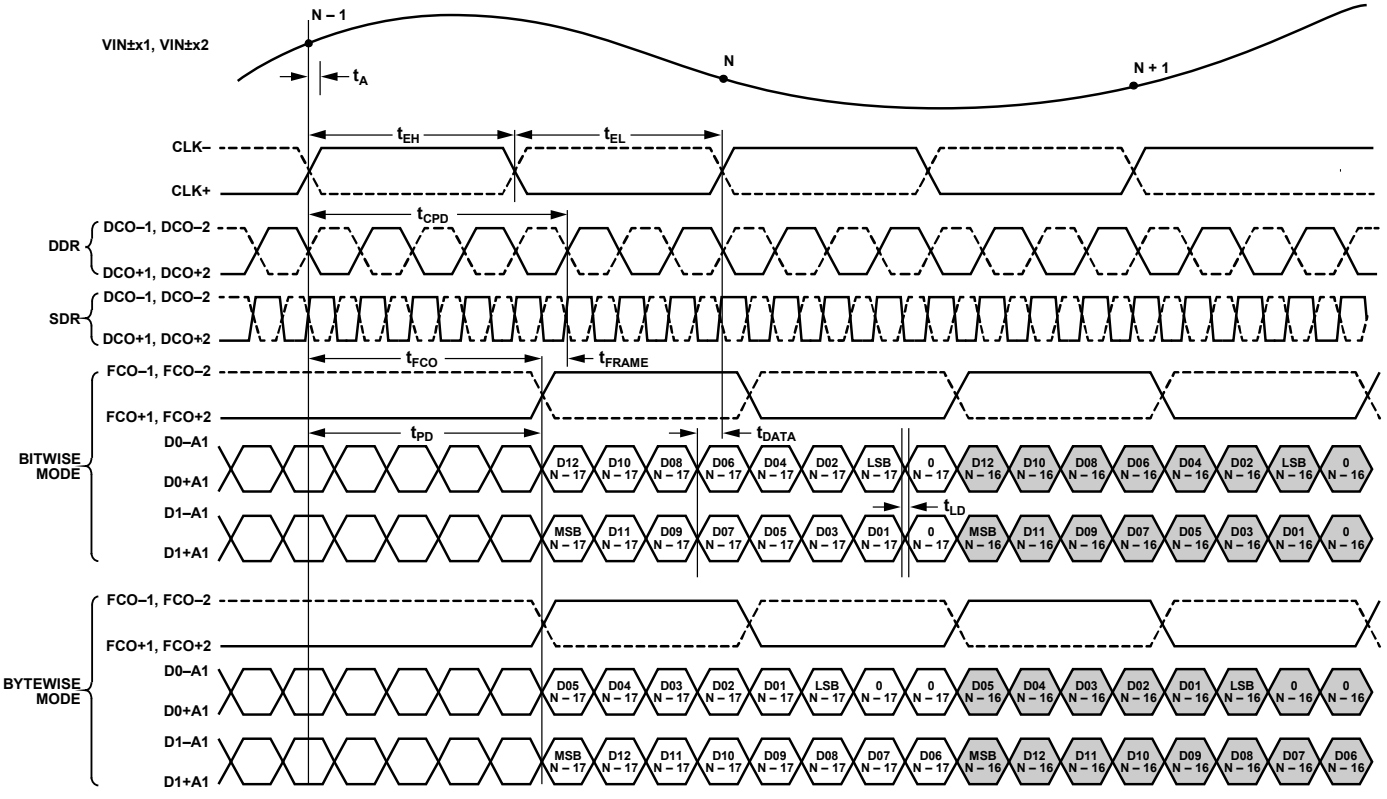

Figure 3. 16-Bit DDR/SDR, Two-Lane, 1× Frame Mode (Default)

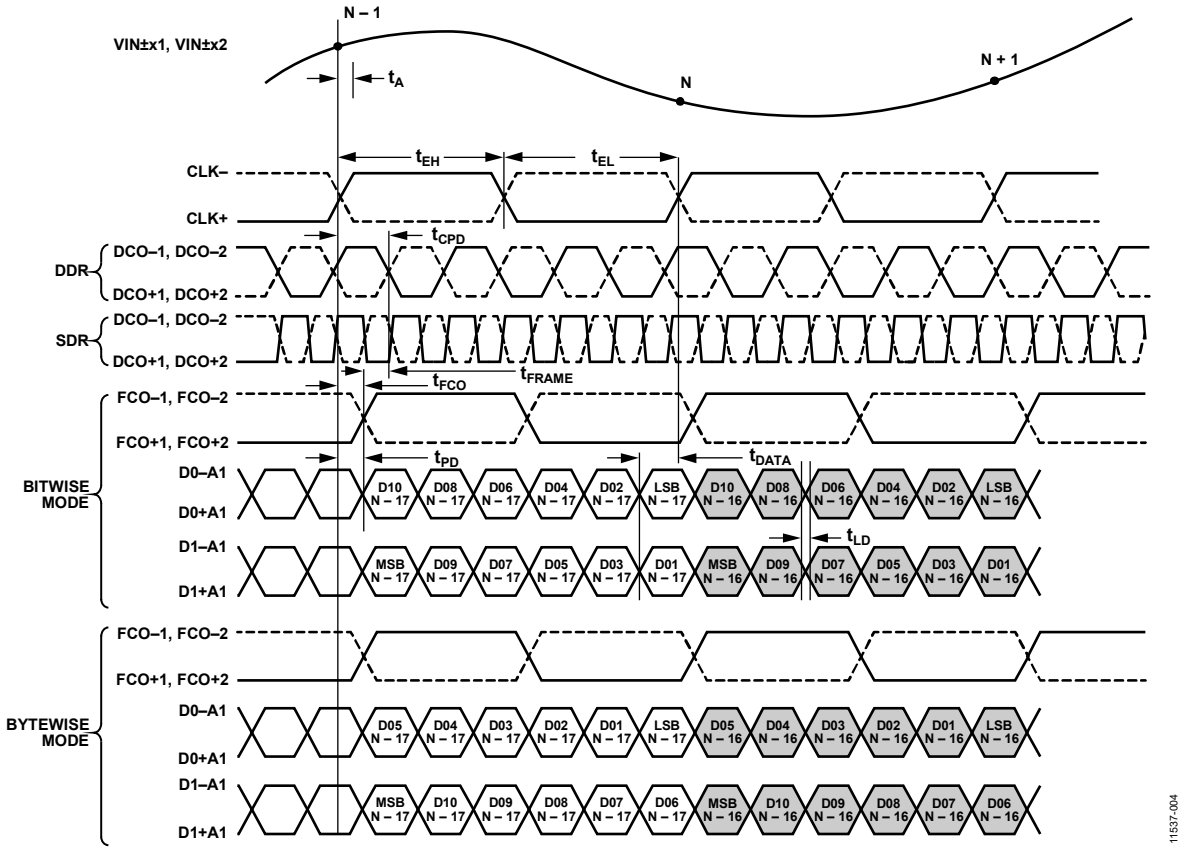

Figure 4. 12-Bit DDR/SDR, Two-Lane, 1× Frame Mode

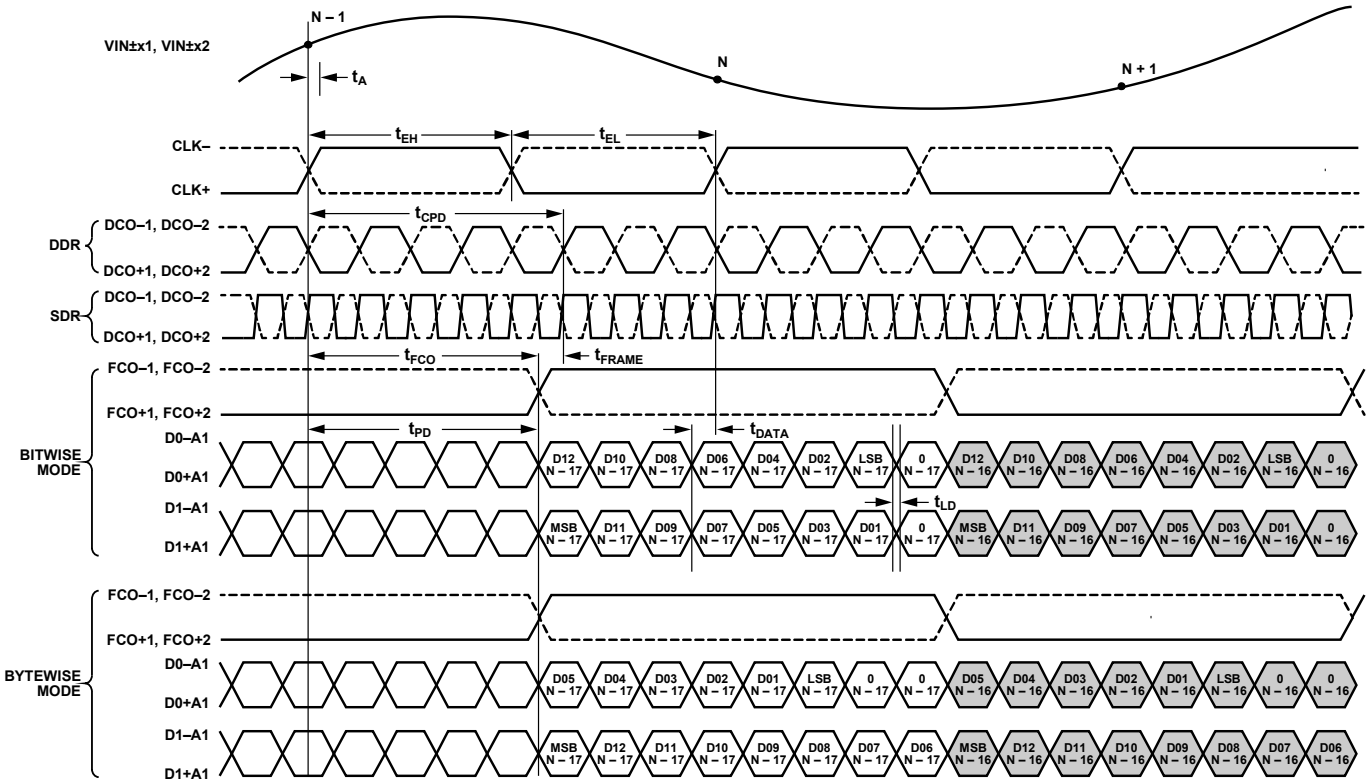

Figure 5. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode

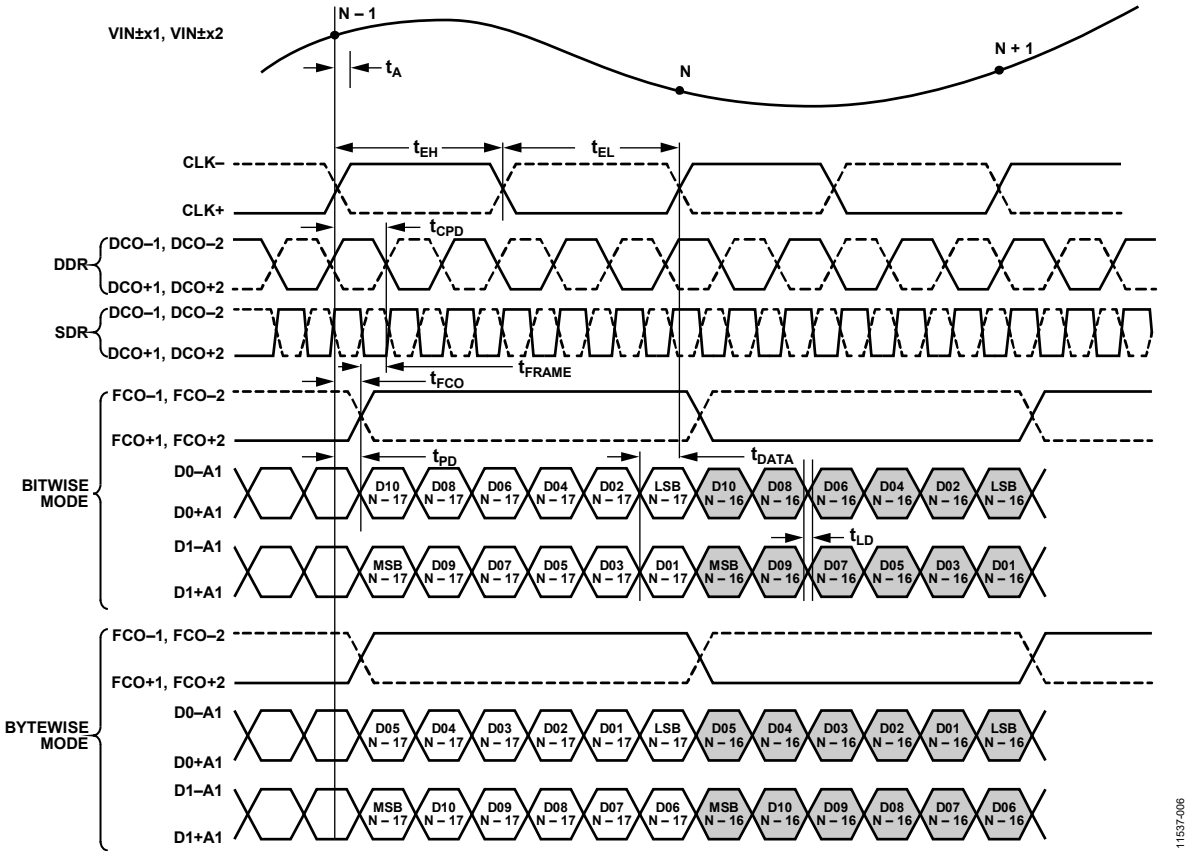

Figure 6. 12-Bit DDR/SDR, Two-Lane, 2× Frame Mode

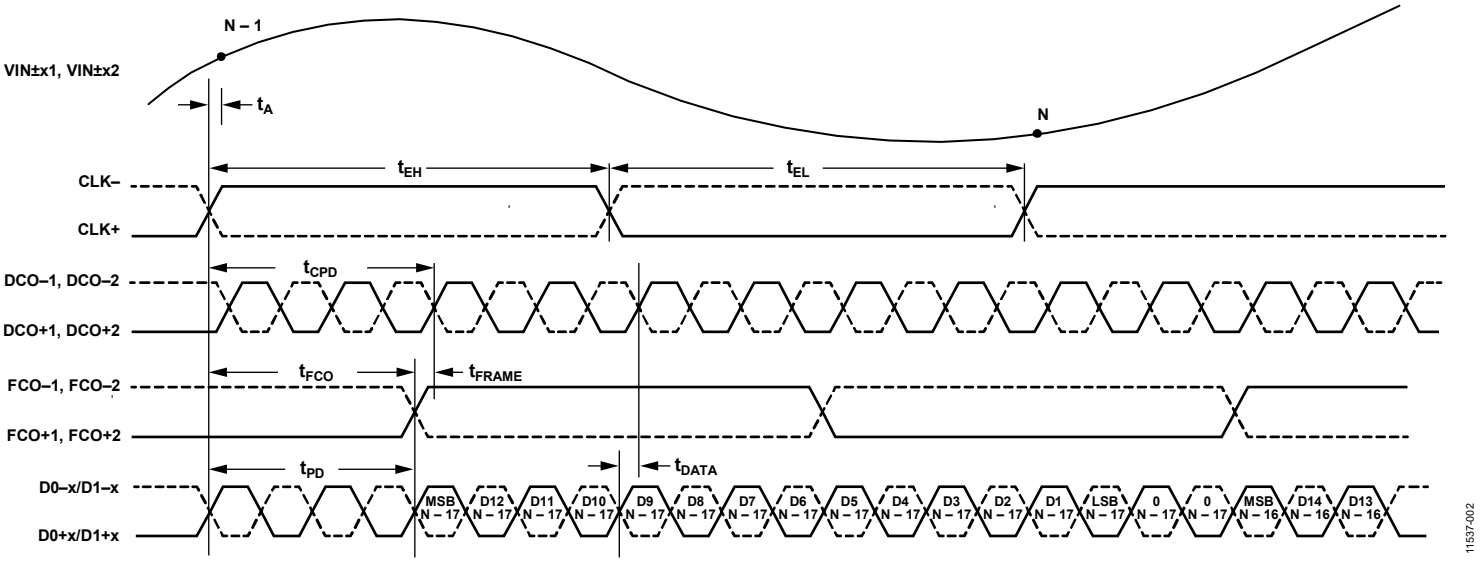

Figure 7. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode (See Table 8 for One-Lane Channel Assignments)

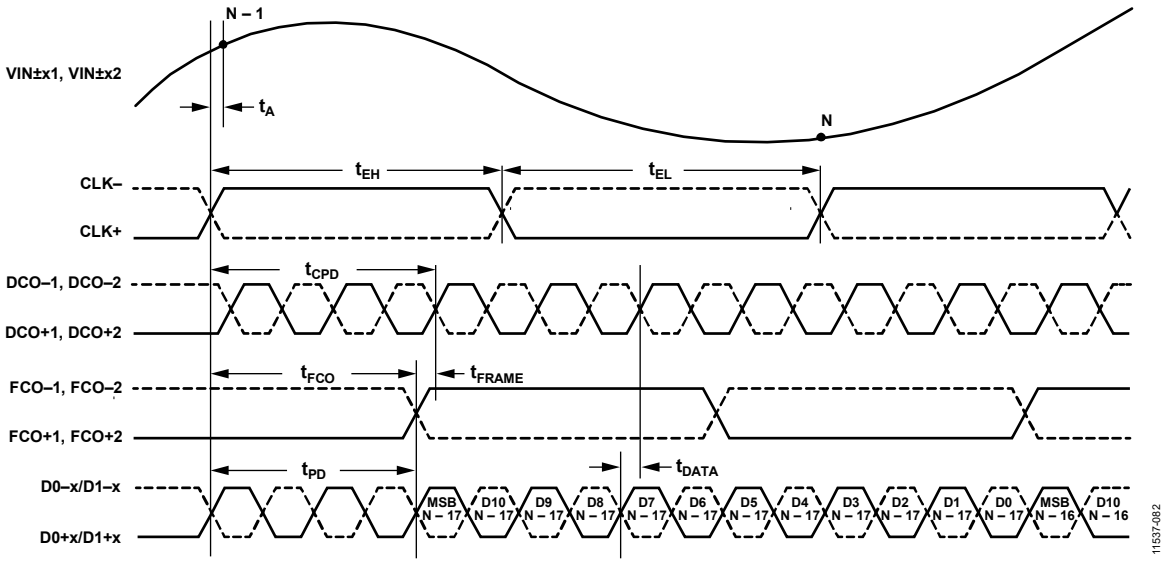

Figure 8. Wordwise DDR, One-Lane, 1× Frame, 12-Bit Output Mode (See Table 8 for One-Lane Channel Assignments)

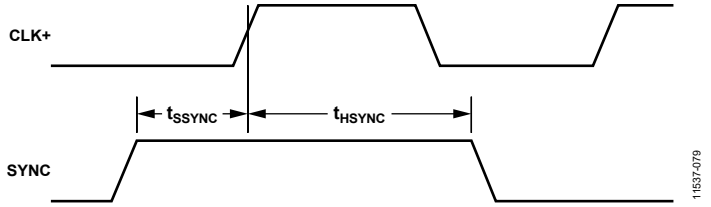

Figure 9. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to GND	−0.3 V to +2.0 V
DRVDD to GND	−0.3 V to +2.0 V
Digital Outputs (D0±xx, D1±xx, DCO±1, DCO±2, FCO±1, FCO±2) to GND	−0.3 V to +2.0 V
CLK+, CLK− to GND	−0.3 V to +2.0 V
VIN±x1, VIN±x2 to GND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/OLM, CSB1, CSB2 to GND	−0.3 V to +2.0 V
SYNC, PDWN to GND	−0.3 V to +2.0 V
RBIAS1, RBIAS2 to GND	−0.3 V to +2.0 V
VREF, VCM1, VCM2, SENSE to GND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. Airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7. Thermal Resistance (Simulated)

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	Ψ_{JT}[1, 2]	Unit
144-Ball, 10 mm × 10 mm CSP-BGA	0	30.2	0.13	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AD9681
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VIN–D1	VIN+D1	NC	VIN–C2	NC	VIN–C1	NC	NC	VIN–B2	NC	VIN+B1	VIN–B1
B	NC	NC	NC	VIN+C2	NC	VIN+C1	NC	NC	VIN+B2	NC	NC	NC
C	VIN–D2	VIN+D2	SYNC	VCM1	VCM2	VREF	SENSE	RBIAS1	RBIAS2	GND	VIN+A2	VIN–A2
D	GND	GND	GND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	NC	NC
E	CLK–	CLK+	GND	AVDD	GND	GND	GND	GND	AVDD	CSB1	VIN+A1	VIN–A1
F	GND	GND	GND	AVDD	GND	GND	GND	GND	AVDD	CSB2	SDIO/OLM	SCLK/DTP
G	D1–D2	D1+D2	GND	AVDD	GND	GND	GND	GND	AVDD	PDWN	D0+A1	D0–A1
H	D0–D2	D0+D2	GND	AVDD	GND	GND	GND	GND	AVDD	GND	D1+A1	D1–A1
J	D1–D1	D1+D1	GND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	D0+A2	D0–A2
K	D0–D1	D0+D1	DRVDD	DRVDD	GND	GND	GND	GND	DRVDD	DRVDD	D1+A2	D1–A2
L	D1–C2	D1+C2	D1+C1	D0+C1	FCO+1	DCO+1	DCO+2	FCO+2	D1+B2	D0+B2	D0+B1	D0–B1
M	D0–C2	D0+C2	D1–C1	D0–C1	FCO–1	DCO–1	DCO–2	FCO–2	D1–B2	D0–B2	D1+B1	D1–B1

NOTES
1. NC = NO CONNECT. THESE PINS ARE NOT ELECTRICALLY CONNECTED TO THE DEVICE. HOWEVER, CONNECT THESE PINS TO BOARD GROUND WHERE POSSIBLE.

11537-009

Figure 10. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
A3, A5, A7, A8, A10, B1 to B3, B5, B7, B8, B10 to B12, D11, D12	NC	No Connect. These pins are not electrically connected to the device. However, connect these pins to board ground where possible.
C10, D1 to D3, D10, E3, E5 to E8, F1 to F3, F5 to F8, G3, G5 to G8, H3, H5 to H8, H10, J3, J10, K5 to K8	GND	Ground.
D4 to D9, E4, E9, F4, F9, G4, G9, H4, H9, J4 to J9	AVDD	1.8 V Analog Supply.
K3, K4, K9, K10	DRVDD	1.8 V Digital Output Driver Supply.
E1, E2	CLK–, CLK+	Input Clock Complement, Input Clock True.
G12, G11	D0−A1, D0+A1	Channel A Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
H12, H11	D1−A1, D1+A1	Channel A Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).

Pin No.	Mnemonic	Description
J12, J11	D0−A2, D0+A2	Channel A Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
K12, K11	D1−A2, D1+A2	Channel A Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
L12, L11	D0−B1, D0+B1	Channel B Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel A Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M12, M11	D1−B1, D1+B1	Channel B Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel B Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M10, L10	D0−B2, D0+B2	Channel B Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode). Channel A Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
M9, L9	D1−B2, D1+B2	Channel B Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Channel B Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
M4, L4	D0−C1, D0+C1	Channel C Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel C Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M3, L3	D1−C1, D1+C1	Channel C Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Channel D Bank 1 Digital Output Complement, Digital Output True (One-Lane Mode).
M1, M2	D0−C2, D0+C2	Channel C Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode) or Channel C Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
L1, L2	D1−C2, D1+C2	Channel C Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Channel D Bank 2 Digital Output Complement, Digital Output True (One-Lane Mode).
K1, K2	D0−D1, D0+D1	Channel D Lane 0 Bank 1 Digital Output Complement, Lane 0 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
J1, J2	D1−D1, D1+D1	Channel D Lane 1 Bank 1 Digital Output Complement, Lane 1 Bank 1 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
H1, H2	D0−D2, D0+D2	Channel D Lane 0 Bank 2 Digital Output Complement, Lane 0 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
G1, G2	D1−D2, D1+D2	Channel D Lane 1 Bank 2 Digital Output Complement, Lane 1 Bank 2 Digital Output True (Default Two-Lane Mode) or Disabled (One-Lane Mode).
M6, L6; M7, L7	DCO−1, DCO+1; DCO−2, DCO+2	Data Clock Digital Output Complement, Data Clock Digital Output True. DCO±1 is used to capture D0±x1/D1±x1 digital output data, and DCO±2 is used to capture D0±x2/D1±x2 digital output data.
M5, L5; M8, L8	FCO−1, FCO+1; FCO−2, FCO+2	Frame Clock Digital Output Complement, Frame Clock Digital Output True. FCO±1 frames D0±x1/D1±x1 digital output data, and FCO±2 frames D0±x2/D1±x2 digital output data.
F12	SCLK/DTP	Serial Clock/Digital Test Pattern.
F11	SDIO/OLM	Serial Data Input/Output/Output Lane Mode.
E10, F10	CSB1, CSB2	Chip Select Bar. CSB1 enables/disables the SPI for four channels in Bank 1; CSB2 enables/ disables the SPI for four channels in Bank 2.
G10	PDWN	Power-Down.
E12, E11	VIN−A1, VIN+A1	Analog Input Complement, Analog Input True.
C12, C11	VIN−A2, VIN+A2	Analog Input Complement, Analog Input True.
A12, A11	VIN−B1, VIN+B1	Analog Input Complement, Analog Input True.
A9, B9	VIN−B2, VIN+B2	Analog Input Complement, Analog Input True.
A6, B6	VIN−C1, VIN+C1	Analog Input Complement, Analog Input True.

Pin No.	Mnemonic	Description
A4, B4	VIN−C2, VIN+C2	Analog Input Complement, Analog Input True.
A1, A2	VIN−D1, VIN+D1	Analog Input Complement, Analog Input True.
C1, C2	VIN−D2, VIN+D2	Analog Input Complement, Analog Input True.
C8, C9	RBIAS1, RBIAS2	Sets analog current bias. Connect each RBIASx pin to a 10 kΩ (1% tolerance) resistor to ground.
C7	SENSE	Reference Mode Selection.
C6	VREF	Voltage Reference Input/Output.
C4, C5	VCM1, VCM2	Analog Output Voltage at Midsupply. Sets the common mode of the analog inputs, external to the ADC, as shown in Figure 38 and Figure 39.
C3	SYNC	Digital Input; Synchronizing Input to Clock Divider. This pin is internally pulled to ground by a 30 kΩ resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

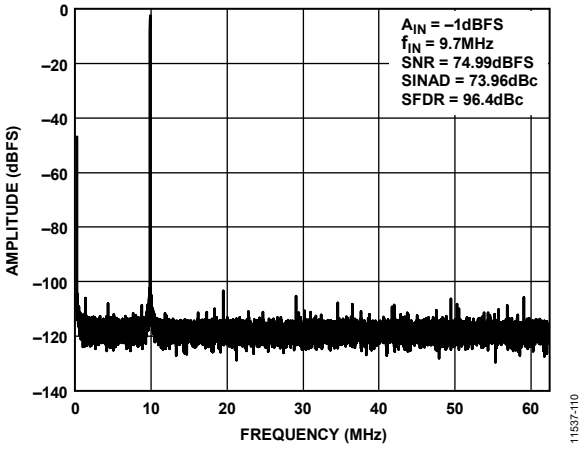

Figure 11. Single-Tone 32k FFT with f_{IN} = 9.7 MHz; f_{SAMPLE} = 125 MSPS

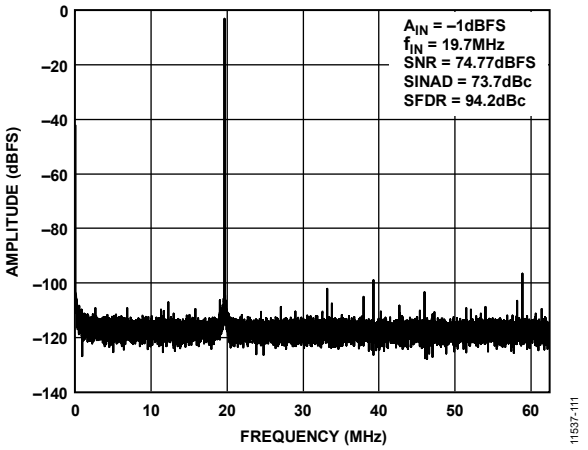

Figure 12. Single-Tone 32k FFT with f_{IN} = 19.7 MHz; f_{SAMPLE} = 125 MSPS

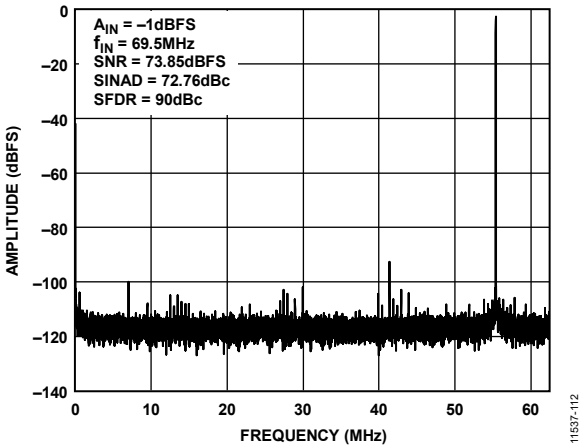

Figure 13. Single-Tone 32k FFT with f_{IN} = 69.5 MHz; f_{SAMPLE} = 125 MSPS

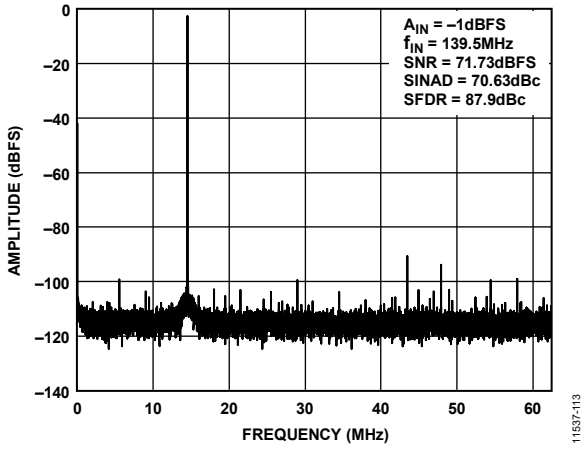

Figure 14. Single-Tone 32k FFT with f_{IN} = 139.5 MHz; f_{SAMPLE} = 125 MSPS

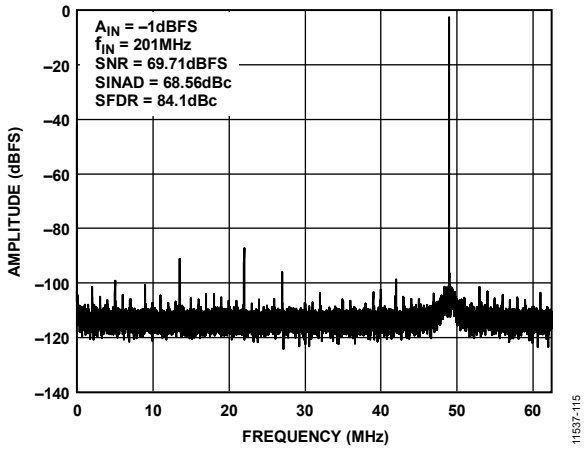

Figure 15. Single-Tone 32k FFT with f_{IN} = 201 MHz; f_{SAMPLE} = 125 MSPS

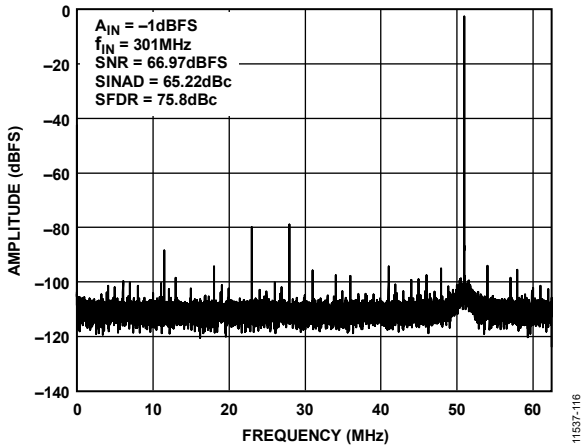

Figure 16. Single-Tone 32k FFT with f_{IN} = 301 MHz; f_{SAMPLE} = 125 MSPS

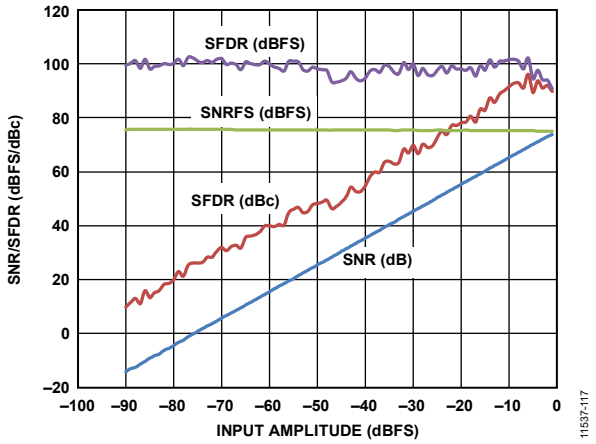

Figure 17. SNR/SFDR vs. Input Amplitude (A_{IN}); f_{IN} = 9.7 MHz; f_{SAMPLE} = 125 MSPS

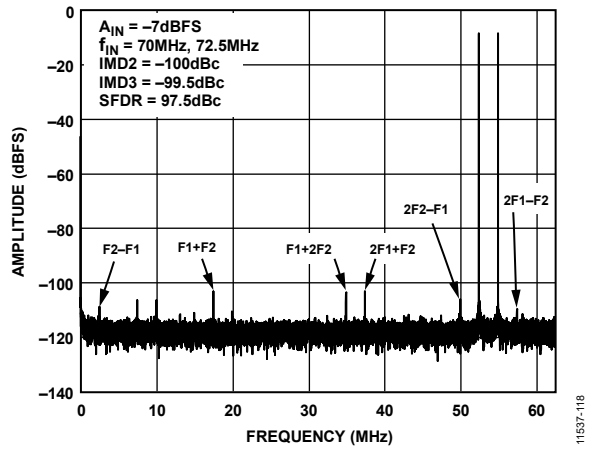

Figure 18. Two-Tone 32k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz; f_{SAMPLE} = 125 MSPS

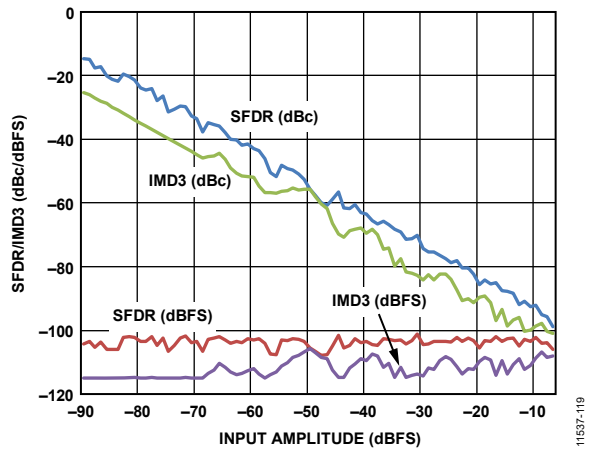

Figure 19. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 70.0 MHz and f_{IN2} = 72.5 MHz; f_{SAMPLE} = 125 MSPS

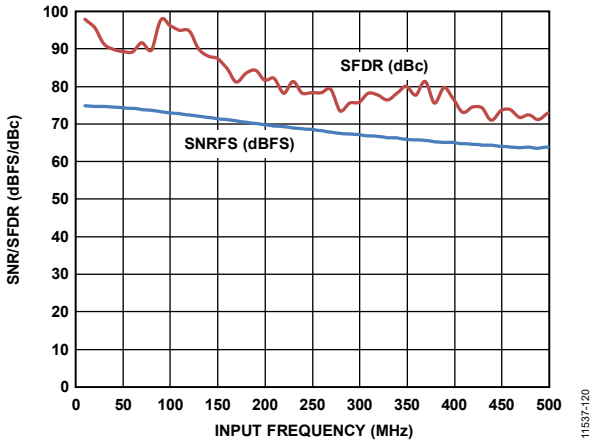

Figure 20. SNR/SFDR vs. f_{IN}; f_{SAMPLE} = 125 MSPS

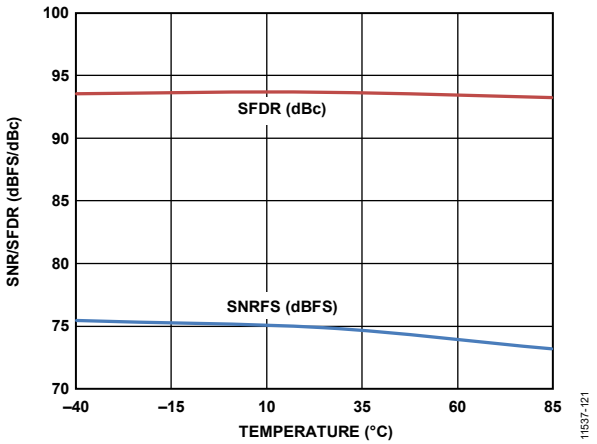

Figure 21. SNR/SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

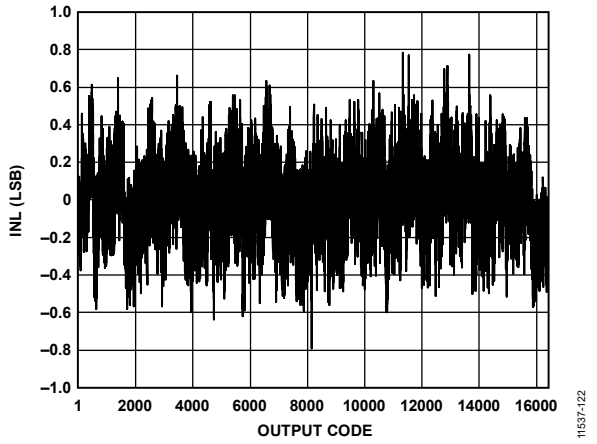

Figure 22. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

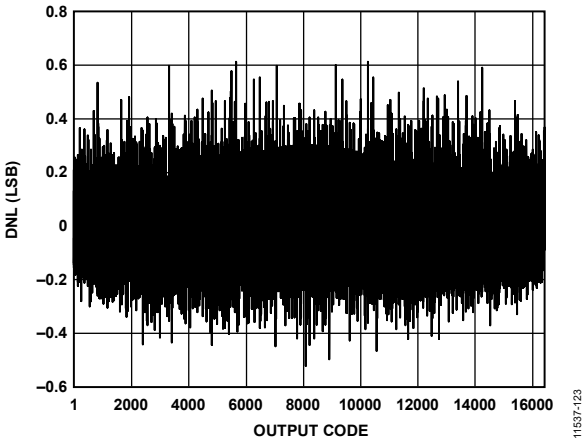

Figure 23. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

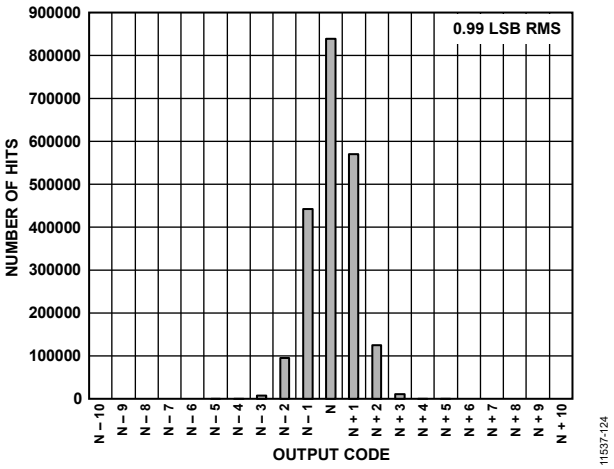

Figure 24. Input Referred Noise Histogram; f_{SAMPLE} = 125 MSPS

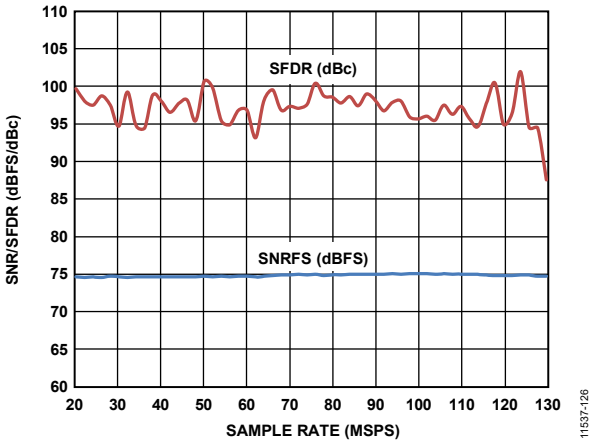

Figure 25. SNR/SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

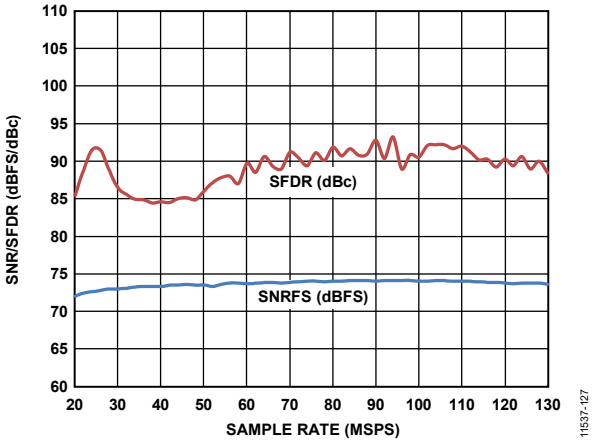

Figure 26. SNR/SFDR vs. Sample Rate; f_{IN} = 70 MHz, f_{SAMPLE} = 125 MSPS

EQUIVALENT CIRCUITS

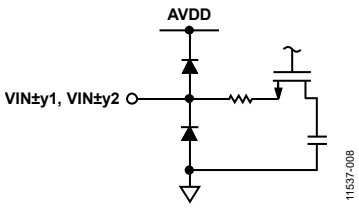

Figure 27. Equivalent Analog Input Circuit

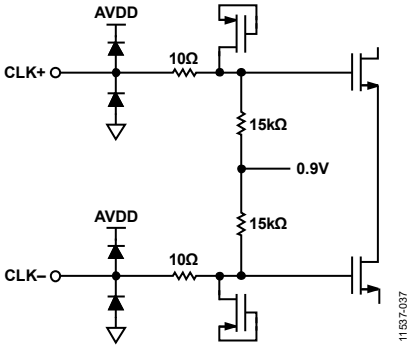

Figure 28. Equivalent Clock Input Circuit

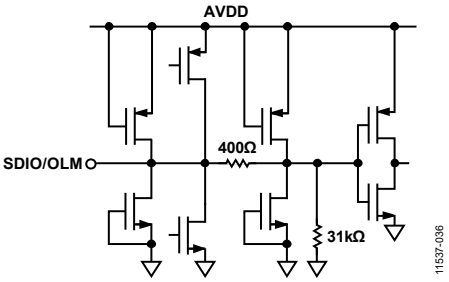

Figure 29. Equivalent SDIO/OLM Input Circuit

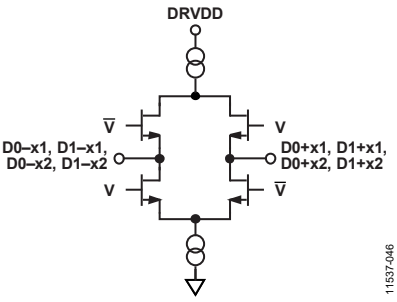

Figure 30. Equivalent Digital Output Circuit

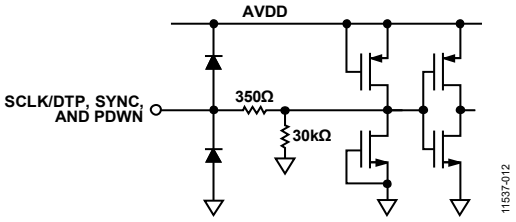

Figure 31. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

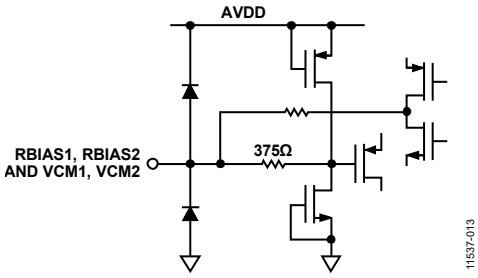

Figure 32. Equivalent RBIASx and VCMx Circuit

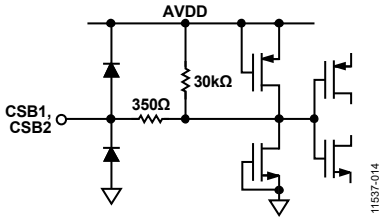

Figure 33. Equivalent CSBx Input Circuit

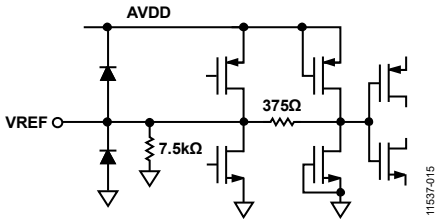

Figure 34. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9681 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9681 is a differential switched capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal dependent errors and achieve optimum performance.

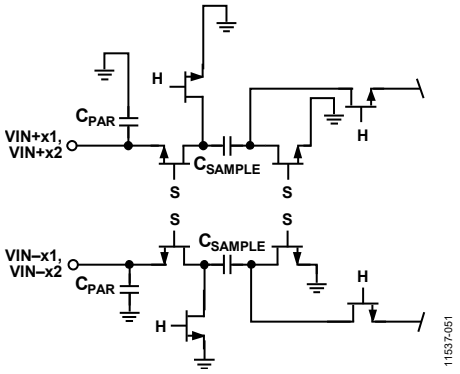

Figure 35. Switched Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 35). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values vary, depending on the application.

Input Common Mode

The analog inputs of the AD9681 are not internally dc biased. Therefore, in ac-coupled applications, the user must provide this bias externally. For optimum performance, set the device so that V_{CM} = AVDD/2. However, the device can function over a wider range with reasonable performance, as shown in Figure 36.

An on-chip, common-mode voltage reference is included in the design and is available at the VCMx pin. Decouple the VCMx pin to ground using a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9681, the largest available input span is 2 V p-p.

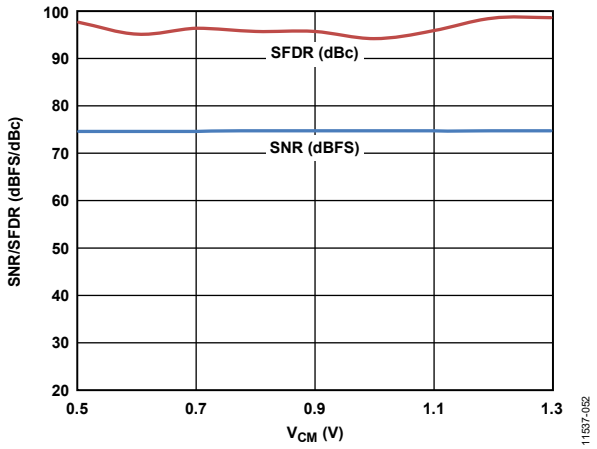

Figure 36. SNR/SFDR vs. Common-Mode Voltage; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

Differential Input Configurations

There are several ways to drive the AD9681, either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9681 provides excellent performance and a flexible interface to the ADC (see Figure 38) for baseband applications. Similarly, differential transformer coupling also provides excellent performance (see Figure 39). Because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9681, use of these passive configurations is recommended wherever possible.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is recommended that the AD9681 inputs not be driven single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9681. Configure VREF using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section. Bypass the VREF pin to ground externally, using a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9681 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 37), setting VREF to 1.0 V.

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	GND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

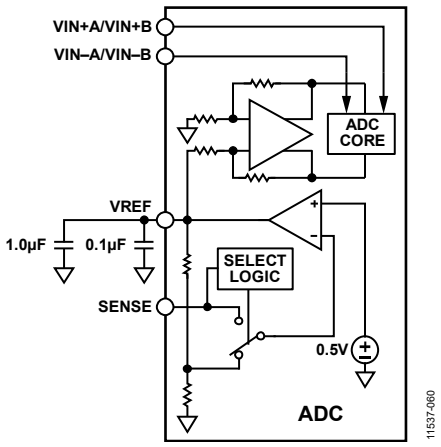

Figure 37. Internal Reference Configuration

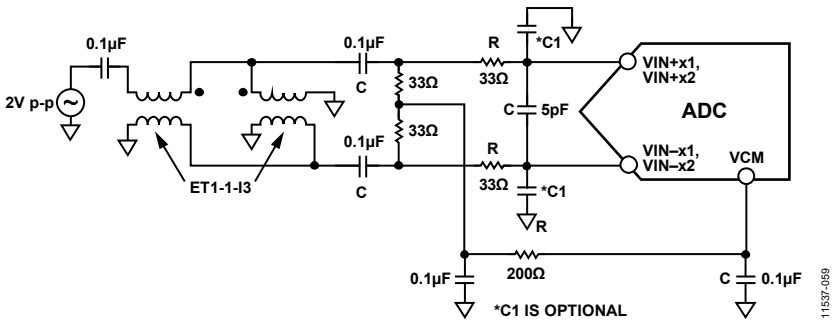

Figure 38. Differential Double Balun Input Configuration for Baseband Applications

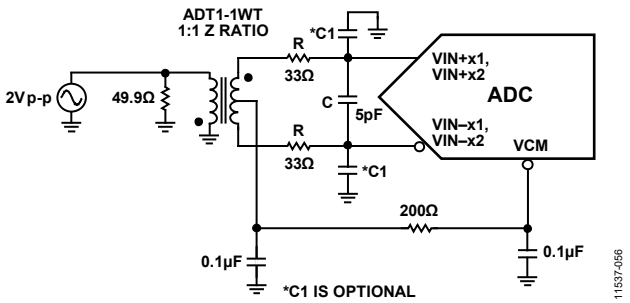

Figure 39. Differential Transformer Coupled Configuration for Baseband Applications

If the internal reference of the AD9681 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 40 shows how the internal reference voltage is affected by loading.

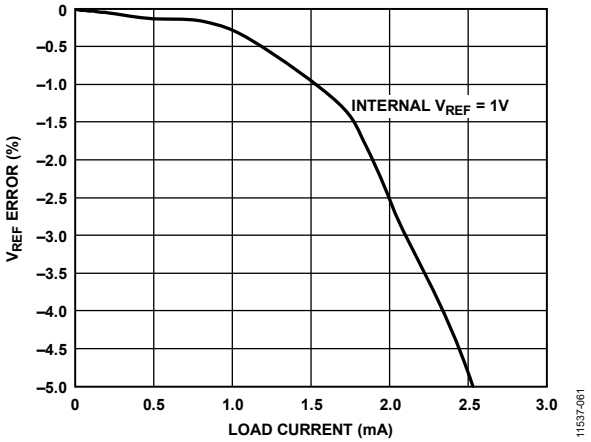

Figure 40. V_{REF} Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 41 shows the typical drift characteristics of the internal reference in 1.0 V mode.

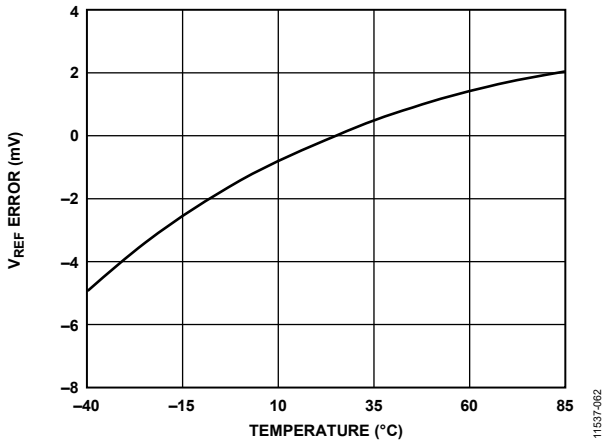

Figure 41. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 34). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, limit the external reference to a maximum of 1.0 V.

Do not leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9681 sample clock inputs, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 28) and require no external bias.

Clock Input Options

The AD9681 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the utmost concern, as described in the Jitter Considerations section.

Figure 42 and Figure 43 show two preferred methods for clocking the AD9681 (at clock rates of up to 1 GHz prior to the internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies from 125 MHz to 1 GHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9681 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9681 while preserving the fast rise and fall times of the signal that are critical to achieving a low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Take care when choosing the appropriate signal limiting diode.

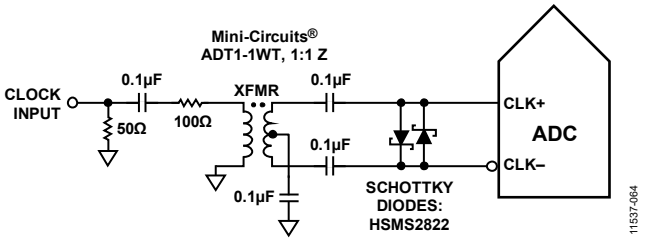

Figure 42. Transformer Coupled Differential Clock (Up to 200 MHz)

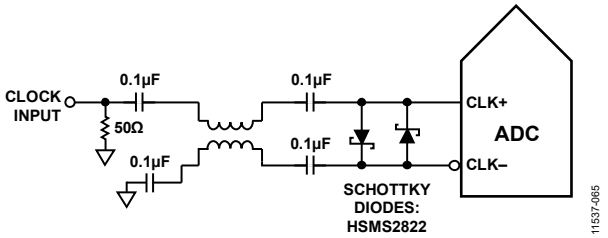

Figure 43. Balun Coupled Differential Clock (Up to 1 GHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 44. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4 clock drivers, noted by AD951x in Figure 44, offer excellent jitter performance.

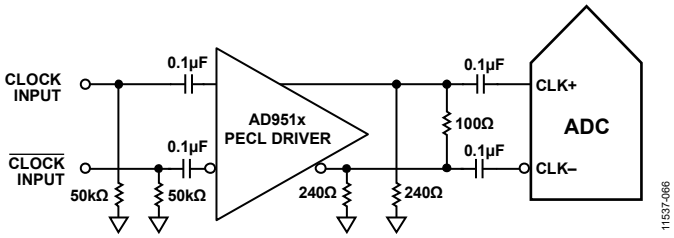

Figure 44. Differential PECL Sample Clock (Up to 1 GHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 45. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4 clock drivers, noted by AD951x in Figure 45 and Figure 46, offer excellent jitter performance.

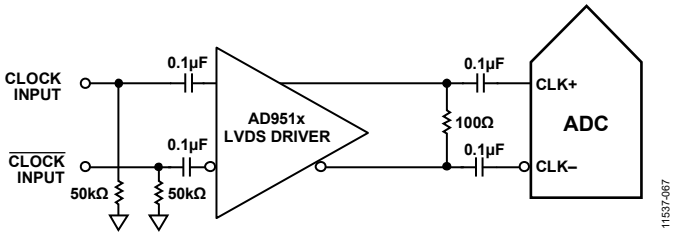

Figure 45. Differential LVDS Sample Clock (Up to 1 GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 46).

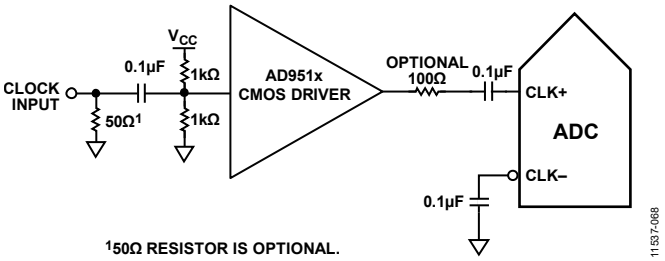

Figure 46. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9681 contains an input clock divider with the ability to divide the input clock by integer values from 1 to 8.

The AD9681 clock divider can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows the clock dividers of multiple devices to be aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9681 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9681. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS turned on.

Jitter on the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) that is due only to aperture jitter (t_J) is expressed by

$$SNR\ Degradation = 20 \log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 47).

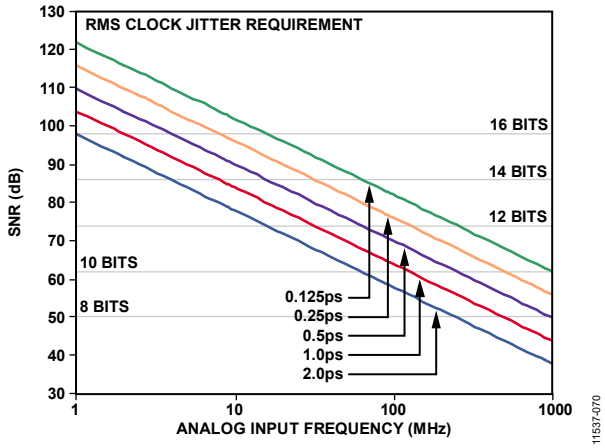

Figure 47. Ideal SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9681. Separate the clock driver power supplies from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators are excellent clock sources. If another type of source generates the clock (by gating, dividing, or another method), ensure that it is retimed by the original clock at the last step.

See the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more in depth information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 48, the power dissipated by the AD9681 is proportional to its sample rate and can be set to one of several power saving modes using Register 0x100, Bits[2:0].

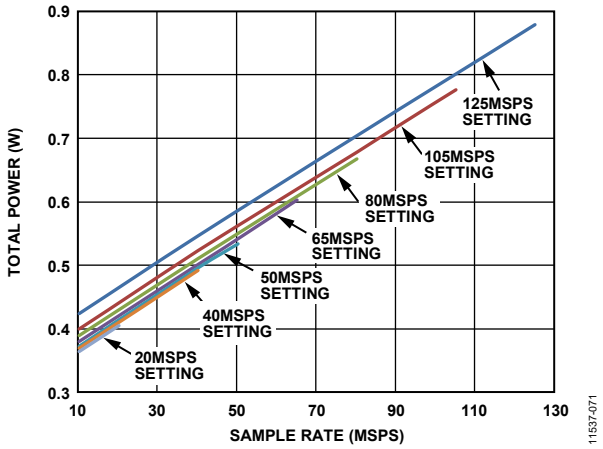

Figure 48. Total Power vs. f_{SAMPLE} for f_{IN} = 9.7 MHz

The AD9681 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In this state, the ADC typically dissipates 2 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9681 to its normal operating mode. Note that PDWN is referenced to the analog supply (AVDD) and must not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. The internal capacitors are discharged when the device enters power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The AD9681 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

When operating in reduced range mode, the output current reduces to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The AD9681 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as near to the receiver as possible. If there is no far end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 24 inches, with all traces the same length. Place the differential output traces as near to each other as possible. An example of the FCO and data stream with proper trace length and position is shown in Figure 49. Figure 50 shows an LVDS output timing example in reduced range mode.

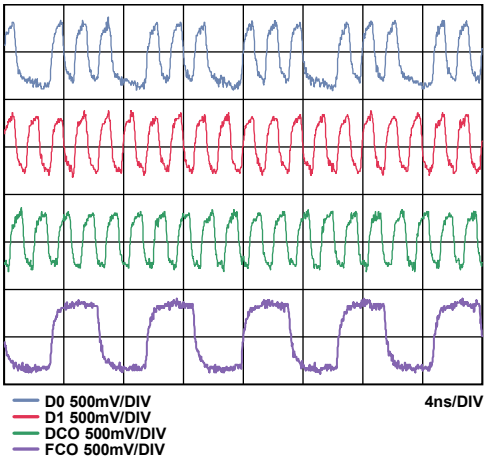

Figure 49. LVDS Output Timing Example in ANSI-644 Mode (Default)

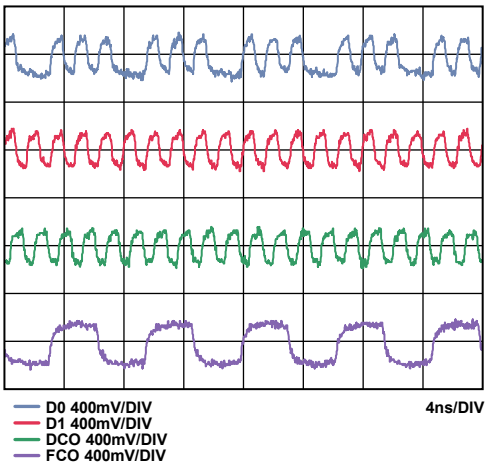

Figure 50. LVDS Output Timing Example in Reduced Range Mode

Figure 51 shows an example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material.

Figure 52 shows an example of trace lengths exceeding 24 inches on standard FR-4 material. Note that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position.

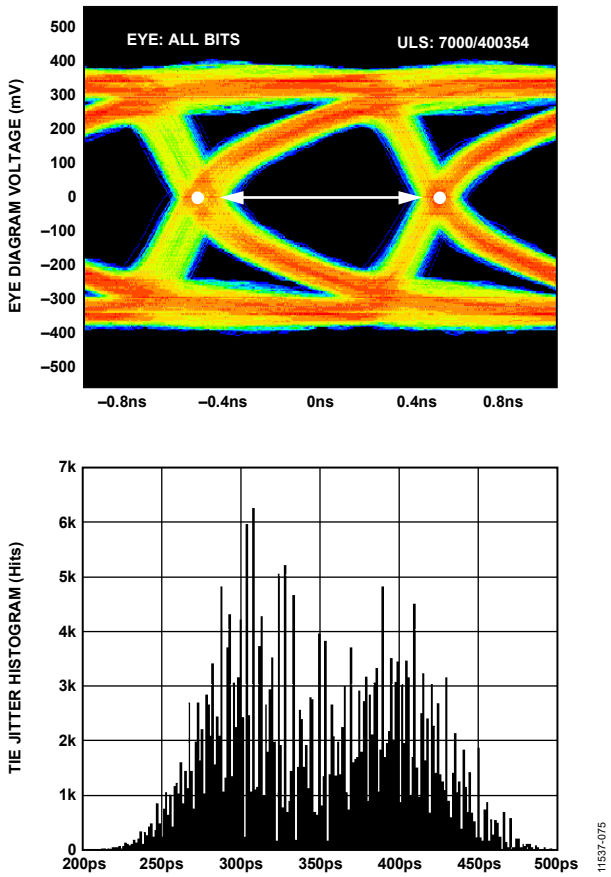

Figure 51. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4 Material, External 100 Ω Far End Termination Only

It is the responsibility of the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all eight outputs to drive longer trace lengths, which can be achieved by program-ming Register 0x15. Although this option produces sharper rise and fall times on the data edges and is less prone to bit errors, it also increases the power dissipation of the DRVDD supply.

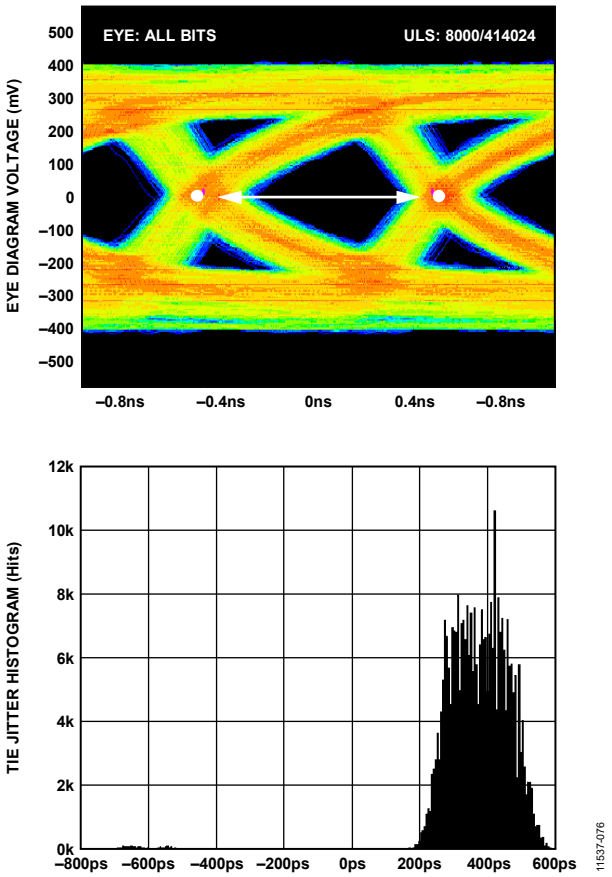

Figure 52. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Greater Than 24 Inches on Standard FR-4 Material, External 100 Ω Far End Termination Only

The default format of the output data is twos complement. Table 10 shows an example of the output coding format. To change the output data format to offset binary, see the Memory Map section, Register 0x14, Bit[0].

Table 10. Digital Output Coding

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VIN+ – VIN–	<–VREF – 0.5 LSB	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ – VIN–	–VREF	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ – VIN–	0 V	1000 0000 0000 0000	0000 0000 0000 0000
VIN+ – VIN–	+VREF – 1.0 LSB	1111 1111 1111 1100	0111 1111 1111 1100
VIN+ – VIN–	>+VREF – 0.5 LSB	1111 1111 1111 1100	0111 1111 1111 1100

Data from each ADC is serialized and provided on a separate channel in two lanes in DDR mode, which is the default condition. In the default condition, the data rate for each serial stream is equal to 8 bits times the sample clock rate, with a maximum of 1 Gbps/lane ((8 bits × 125 MSPS) = 1 Gbps/lane). If one-lane mode is used, the bit rate doubles. To keep within the 1 Gbps limit, the maximum allowable sample rate is 62.5 MSPS in one-lane mode. The lowest typical conversion rate is 10 MSPS. For conversion rates of less than 20 MSPS, the SPI must be used to reconfigure the integrated PLL. See Register 0x21 in the Memory Map section for details on enabling this feature

Two output clock types are provided to assist in capturing data from the AD9681. DCO±1 and DCO±2 are used to clock the output data and their frequency is equal to 4× the sample clock (CLK±) rate for the default mode of operation. Data is clocked out of the AD9681 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. DCO±1 is used to capture the D0±x1/D1±x1 (Bank 1) data; DCO±2 is used to capture the D0±x2/D1±x2 (Bank 2) data. FCO±1 and FCO±2 signal the start of a new output byte and toggle at a rate equal to the sample clock rate in 1× frame mode. FCO±1 frames the D0±x1/D1±x1 (Bank 1) data and FCO±2 frames the D0±x2/ D1±x2 (Bank 2) data. See the Timing Diagrams section for more information.

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to one data cycle (30° relative to one DCO cycle). This enables the user to refine system timing margins if required. The default DCO±1 and DCO±2 to output data edge timing, as shown in Figure 3, is 180° relative to one data cycle (90° relative to one DCO cycle).

A 12-bit serial stream can also be initiated from the SPI. This allows the user to implement and test compatibility to lower resolution systems. When changing the resolution to a 12-bit serial stream, the data stream is shortened. See Figure 4 for the 12-bit example. However, in the default option with the serial output number of bits at 16, the data stream stuffs two 0s at the end of the 14-bit serial data.

In default mode, as shown in Figure 3, the MSB is first in the data output serial stream. This can be inverted so that the LSB is first in the data output serial stream by using the SPI.

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing (see Table 11 for the output bit sequencing options that are available). Some test patterns have two serial sequential words and can alternate in various ways, depending on the test pattern chosen. Note that some patterns do not adhere to the data format select option. In addition, custom user defined test patterns can be assigned in Register 0x19, Register 0x1A, Register 0x1B, and Register 0x1C.

Table 11. Flexible Output Test Modes

Output Test Mode Bit Sequence (Reg. 0x0D)	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select	Notes
0000	Off (default)	Not applicable	Not applicable	Not applicable	
0001	Midscale short	1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	Not applicable	Yes	Offset binary code shown
0010	+Full-scale short	1111 1111 1111 (12-bit) 1111 1111 1111 1100 (16-bit)	Not applicable	Yes	Offset binary code shown
0011	−Full-scale short	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	Not applicable	Yes	Offset binary code shown
0100	Checkerboard	1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit)	0101 0101 0101 (12-bit) 0101 0101 0101 0100 (16-bit)	No	
0101	PN sequence long[1]	Not applicable	Not applicable	Yes	PN23 ITU 0.150 $X^{23} + X^{18} + 1$
0110	PN sequence short[1]	Not applicable	Not applicable	Yes	PN9 ITU 0.150 $X^9 + X^5 + 1$
0111	One-/zero-word toggle	1111 1111 1111 (12-bit) 111 1111 1111 1100 (16-bit)	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	No	
1000	User input	Register 0x19 to Register 0x1A	Register 0x1B to Register 0x1C	No	
1001	1-/0-bit toggle	1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit)	Not applicable	No	
1010	1× sync	0000 0011 1111 (12-bit) 0000 0001 1111 1100 (16-bit)	Not applicable	No	
1011	One bit high	1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	Not applicable	No	Pattern associated with the external pin
1100	Mixed bit frequency	1010 0011 0011 (12-bit) 1010 0001 1001 1100 (16-bit)	Not applicable	No	

[1] All test mode options except PN sequence short and PN sequence long can support 12-bit to 16-bit word lengths to verify data capture to the receiver.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. Refer to Section 5.1 of the ITU-T 0.150 (05/96) standard for a description of the PN sequence and how it is generated. The seed value is all 1s (see Table 12 for the initial values). The output is a parallel representation of the serial PN9 sequence in MSB-first format. The first output word is the first 14 bits of the PN9 sequence in MSB aligned form.

Table 12. PN Sequence

Sequence	Initial Value	Next Three Output Samples (MSB First) Twos Complement
PN Sequence Short	0x7F80	0x77C4, 0xF320, 0xA538
PN Sequence Long	0x7FFC	0x7F80, 0x8004, 0x7000

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. Refer to Section 5.6 of the ITU-T 0.150 (05/96) standard for a description of the PN sequence and how it is generated. The seed value is all 1s (see Table 12 for the initial values), and the AD9681 inverts the bit stream with relation to the ITU standard. The output is a parallel representation of the serial PN23 sequence in MSB-first format. The first output word is the first 14 bits of the PN23 sequence in MSB aligned format.

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO/OLM Pin

For applications that do not require SPI mode operation, the CSB1 and CSB2 pins are tied to AVDD, and the SDIO/OLM pin controls the output lane mode according to Table 13.

For applications where the SDIO/OLM pin is not used, tie CSB1 and CSB2 to AVDD. When using the one-lane mode, use an encode rate of ≤62.5 MSPS to meet the maximum output rate of 1 Gbps.

Table 13. Output Lane Mode Pin Settings

Output Lane Mode Voltage (SDIO/OLM Pin)	Output Mode
AVDD (Default)	Two-lane. 1× frame, 16-bit serial output.
GND	One-lane. 1× frame, 16-bit serial output.

SCLK/DTP Pin

The SCLK/DTP pin can enable a single digital test pattern if it and the CSB1 and CSB2 pins are held high during device power-up. When SCLK/DTP is tied to AVDD, the ADC channel outputs shift out the following pattern: 1000 0000 0000 0000. The FCO±1, FCO±2, DCO±1, and DCO±2 pins function normally while all channels shift out the repeatable test pattern.

This pattern allows the user to perform timing alignment adjustments among the FCO±1, FCO±2, DCO±1, DCO±2, and output data. The SCLK/DTP pin has an internal 30 kΩ resistor to GND and can be left unconnected for normal operation.

Table 14. Digital Test Pattern Pin Settings

Selected Digital Test Pattern	DTP Voltage	Resulting D0±xx and D1±xx
Normal Operation	No connect	Normal operation
DTP	AVDD	1000 0000 0000 0000

Additional and custom test patterns can also be observed when commanded from the SPI port. Consult the Memory Map section for information about the options available.

CSB1 and CSB2 Pins

Tie the CSB1 and CSB2 pins to AVDD for applications that do not require SPI mode operation. Tying CSB1 and CSB2 high causes all SCLK and SDIO SPI communication information to be ignored.

CSB1 selects/deselects SPI circuitry affecting the D0±x1/D1±x1 outputs (Bank 1). CSB2 selects/deselects SPI circuitry affecting the D0±x2/D1±x2 (Bank 2) outputs.

It is recommended that CSB1 and CSB2 be controlled with the same signal; that is, tie them together. In this way, whether tying them to AVDD or selecting SPI functionality, both banks of ADCs are controlled identically and are always in the same state.

RBIAS1 and RBIAS2 Pins

To set the internal core bias current of the ADC, place a 10.0 kΩ, 1% tolerance resistor to ground at each of the RBIAS1 and RBIAS2 pins.

OUTPUT TEST MODES

The AD9681 includes a built-in test feature designed to enable verification of the integrity of each data output channel, as well as to facilitate board level debugging. Various output test modes are provided to place predictable values on the outputs of the AD9681.

The output test modes are described in Table 11 and controlled by the output test mode bits at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SERIAL PORT INTERFACE (SPI)

The AD9681 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI offers the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For general operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. SPI information specific to the AD9681 is found in the AD9681 data sheet and takes precedence over the general information found in the AN-877 Application Note.

CONFIGURATION USING THE SPI

Four pins define the SPI of this ADC: the SCLK/DTP pin (SCLK functionality), the SDIO/OLM pin (SDIO functionality) and the CSB1 and CSB2 pins (see Table 15). SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. SDIO (serial data input/output) serves a dual function, allowing data to be sent to and read from the internal ADC memory map registers. CSB1 and CSB2 (chip select bar) are active low controls that enable or disable the read and write cycles.

Table 15. Serial Port Interface Pins

Pin	Function
SCLK (SCLK/DTP)	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO (SDIO/OLM)	Serial data input/output. A dual-purpose pin that serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB1, CSB2	Chip select bar. An active low control that gates the read and write cycles. CSB1 enables/disables the SPI for four channels in Bank 1; CSB2 enables/disables the SPI for four channels in Bank 2.

The falling edge of CSB1 and/or CSB2, in conjunction with the rising edge of SCLK, determines the start of the framing. For an example of the serial timing and its definitions, see Figure 53 and Table 5.

Other modes involving the CSB1 and CSB2 pins are available. To permanently enable the device, hold CSB1 and CSB2 low indefinitely; this is called streaming. CSB1 and CSB2 can stall high between bytes to allow additional external timing. Tie CSB1 and CSB2 high to place SPI functions in high impedance mode. This mode turns on any SPI secondary pin functions.

It is recommended that CSB1 and CSB2 be controlled with the same signal by tying them together. In this way, whether tying them to AVDD or selecting SPI functionality, both banks of ADCs are controlled identically and are always in the same state.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to both program the chip and read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Input data registers on the rising edge of SCLK, and output data transmits on the falling edge. After the address information passes to the converter requesting a read, the SDIO line transitions from an input to an output within 1/2 of a clock cycle. This timing ensures that when the falling edge of the next clock cycle occurs, data can be safely placed on this serial line for the controller to read.

All data is composed of 8-bit words. Data can be sent in MSB-first mode or in LSB-first mode. MSB-first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

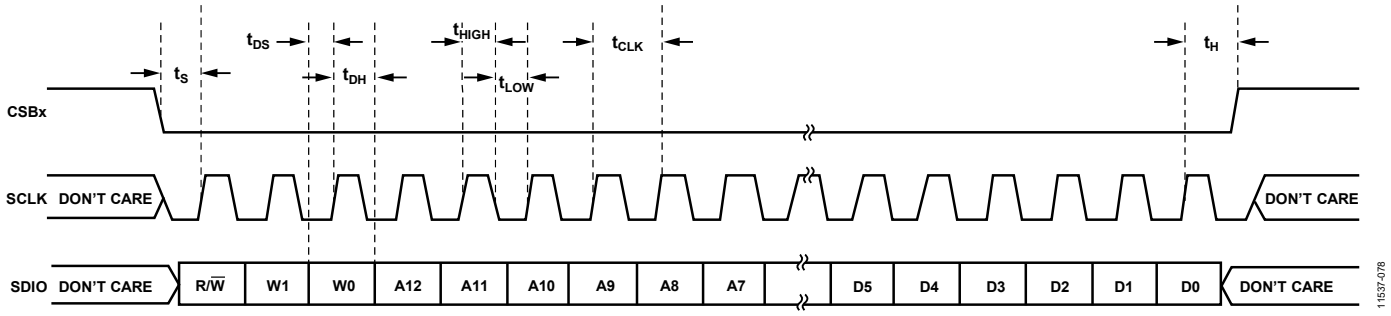

Figure 53. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 15 comprise the physical interface between the user programming device and the serial port of the AD9681. The SCLK/DTP pin (SCLK functionality) and the CSB1 and CSB2 pins function as inputs when using the SPI interface. The SDIO/OLM pin (SDIO functionality) is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB1 and CSB2 signals, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9681 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI interface is not being used. When the pins are strapped to DRVDD or ground during device power-on, they serve a specific function. Table 13 and Table 14 describe the strappable functions that are supported on the AD9681.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/OLM pin, the SCLK/DTP pin, and the PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for output lane mode control, digital test pattern control, and power-down feature control. In this mode, connect CSB1 and CSB2 to AVDD, which disables the serial port interface.

When the device is in SPI mode, the PDWN pin (if enabled) remains active. For SPI control of power-down, set the PDWN pin to its inactive state (low).

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described further in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9681 device-specific features are described in detail in the Memory Map Register Descriptions section following Table 17, the external memory map register table.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Power Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS, set the clock divider, set the clock divider phase, and enable the sync function
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set the output mode
Output Phase	Allows the user to set the output clock polarity
ADC Resolution	Allows scalable power consumption options with respect to the sample rate

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the device index and transfer registers (Address 0x05 and Address 0xFF); and the global ADC function registers, including setup, control, and test (Address 0x08 to Address 0x109).

The memory map register table (see Table 17) lists the default hexadecimal value for each hexadecimal address shown. The column with the Bit 7 (MSB) heading is the start of the default hexadecimal value given. For example, Address 0x05, the device index register, has a hexadecimal default value of 0x3F. This means that in Address 0x05, Bits[7:6] = 0, and the remaining bits, Bits[5:0], = 1. This setting is the default channel index setting. The default value results in all specified ADC channels receiving the next write command. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This application note details the functions controlled by Register 0x00 to Register 0xFF. The remaining registers are documented in the Memory Map Register Descriptions section.

Open Locations

All address and bit locations that are not listed in Table 17 are not currently supported for this device. Write the unused bits of a valid address location with 0s. Writing to these locations is required only when some of the bits of an address location are valid (for example, Address 0x05). Do not write to an address location if the entire address location is open or if the address is not listed in Table 17 (for example, Address 0x13).

Default Values

After the AD9681 is reset (via Bit 5 and Bit 2 of Address 0x00), the registers are loaded with default values. The default values for the registers are listed in the Default Value (Hex) column of Table 17, the memory map register table.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Channel Specific Registers

Some channel setup functions can be programmed independently for each channel. In such cases, channel address locations are internally duplicated for each channel; that is, each channel has its own set of registers. These registers and bits are designated in Table 17 as local. Access these local registers and bits by setting the appropriate data channel bits (A1, A2 through D1, D2) and the clock channel bits (DCO±1, DCO±2 and FCO±1, FCO±2), found in Register 0x05. If all the valid bits are set in Register 0x05, the subsequent write to a local register affects the registers of all the data channels and the DCO±x/FCO±x clock channels. In a read cycle, set only one channel (A1, A2 through D1, D2) to read one local register. If all the bits are set during a SPI read cycle, the device returns the value for Channel A1.

Registers and bits that are designated as global in Table 17 are applicable to the channel features for which independent settings are not allowed; thus, they affect the entire device. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP

The AD9681 uses a 3-wire (bidirectional SDIO) interface and 16-bit addressing. Therefore, Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1. When Bit 5 in Register 0x00 is set high, the SPI enters a soft reset where all of the user registers revert to their default values and Bit 2 is automatically cleared.

Table 17. Memory Map Register Table

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
Chip Configuration Registers											
0x00	SPI port configuration	0 = SDIO active	LSB first	Soft reset	1 = 16-bit address	1 = 16-bit address	Soft reset	LSB first	0 = SDIO active	0x18	Nibbles are mirrored such that a given register value yields the same function for either LSB-first mode or MSB-first mode. The default for ADCs is 16-bit mode.
0x01	Chip ID (global)	8-bit chip ID, Bits[7:0]; 0x8F = the AD9681, an octal, 14-bit, 125 MSPS serial LVDS								0x8F	Unique chip ID used to differentiate devices. Read only.
0x02	Chip grade (global)	Open	Speed grade ID, Bits[6:4]; 110 = 125 MSPS			Open	Open	Open	Open	Read only	Unique speed grade ID used to differentiate graded devices. Read only.
Device Index and Transfer Registers											
0x05	Device index	Open	Open	DCO±1, DCO±2 clock channels	FCO±1, FCO±2 clock channels	D1, D2 data channels	C1, C2 data channels	B1, B2 data channels	A1, A2 data channels	0x3F	Bits are set to determine which device on chip receives the next write command. The default is all devices on chip.
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Initiate override	0x00	Sets resolution/ sample rate override.
Global ADC Function Registers											
0x08	Power modes (global)	Open	Open	External power-down pin function; 0 = full power-down, 1 = standby	Open	Open	Open	Internal power-down mode, Bits[1:0]; 00 = chip run 01 = full power-down 10 = standby 11 = digital reset		0x00	Determines various generic modes of chip operation.
0x09	Clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer; 0 = off 1 = on	0x01	Turns duty cycle stabilizer on or off.
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio, Bits[2:0]; 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Divide ratio is the value plus 1.

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x0C	Enhancement control	Open	Open	Open	Open	Open	Chop mode; 0 = off 1 = on	Open	Open	0x00	Enables/ disables chop mode.
0x0D	Test mode (local except for PN sequence resets)	User input test mode, Bits[7:6]; 00 = single 01 = alternate 10 = single once 11 = alternate once (affects user input test mode only; Register 0x0D, Bits[3:0] = 1000)		Reset PN long gen	Reset PN short gen	Output test mode, Bits[3:0] (local); 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN23 sequence 0110 = PN9 sequence 0111 = one-/zero-word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency				0x00	When set, test data is placed on the output pins in place of normal data.
0x10	Offset adjust (local)	8-bit device offset adjustment, Bits[7:0] (local); offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	Device offset trim.
0x14	Output mode	Open	LVDS-ANSI/ LVDS-IEEE option; 0 = LVDS-ANSI 1 = LVDS-IEEE reduced range link (global); see Table 18	Open	Open	Open	Output invert; 0 = not inverted 1 = inverted (local)	Open	Output format; 0 = offset binary 1 = twos complement (default) (global)	0x01	Configures outputs and format of the data.
0x15	Output adjust	Open	Open	Output driver termination, Bits[5:4]; 00 = none 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω		Open	Open	Open	FCO±x, DCO±x output drive (local); 0 = 1× drive 1 = 2× drive	0x00	Determines LVDS or other output properties.
0x16	Output phase	Open	Input clock phase adjust, Bits[6:4]; (value is number of input clock cycles of phase delay; see Table 19)			Output clock phase adjust, Bits[3:0]; (0000 to 1011; see Table 20)				0x03	On devices that use global clock divide, determines which phase of the divider output supplies the output clock. Internal latching is unaffected.
0x18	V_{REF}	Open	Open	Open	Open	Open	Input full-scale adjustment; digital scheme, Bits[2:0]; 000 = 1.0 V p-p 001 = 1.14 V p-p 010 = 1.33 V p-p 011 = 1.6 V p-p 100 = 2.0 V p-p			0x04	Digital adjustment of input full-scale voltage. Does not affect analog voltage reference.
0x19	USER_PATT1_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 1 LSB.
0x1A	USER_PATT1_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 1 MSB.
0x1B	USER_PATT2_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 2 LSB.
0x1C	USER_PATT2_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 2 MSB.

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x21	Serial output data control (global)	LVDS output LSB first	SDR/DDR one-lane/two-lane, wordwise/bitwise/bytewise, Bits[6:4]; 000 = SDR two-lane, bitwise 001 = SDR two-lane, bytewise 010 = DDR two-lane, bitwise 011 = DDR two-lane, bytewise 100 = DDR one-lane, wordwise			PLL low encode rate mode	Select 2× frame	Serial output number of bits, Bits[1:0]; 00 = 16 bits 10 = 12 bits		0x30	Serial stream control. Default causes MSB first and the native bit stream.
0x22	Serial channel status (local)	Open	Open	Open	Open	Open	Open	Channel output reset	Channel power-down	0x00	Powers down individual sections of a converter.
0x100	Resolution/sample rate override	Open	Resolution/ sample rate override enable	Resolution, Bits[5:4]; 01 = 14 bits 10 = 12 bits		Open	Sample rate, Bits[2:0]; 000 = 20 MSPS 001 = 40 MSPS 010 = 50 MSPS 011 = 65 MSPS 100 = 80 MSPS 101 = 105 MSPS 110 = 125 MSPS			0x00	Resolution/ sample rate override (requires transfer register, Register 0xFF).
0x101	User I/O Control 2	Open	Open	Open	Open	Open	Open	Open	SDIO pull-down	0x00	Disables SDIO pull-down.
0x102	User I/O Control 3	Open	Open	Open	Open	VCM power-down	Open	Open	Open	0x00	VCM control.
0x109	Sync	Open	Open	Open	Open	Open	Open	Sync next only	Enable sync	0x00	

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Device Index (Register 0x05)

There are certain features in the map that can be set independently for each channel, whereas other features apply globally to all channels (depending on context), regardless of which are selected. Bits[3:0] in Register 0x05 select which individual data channels are affected. The output clock channels are selected in Register 0x05 as well. A smaller subset of the independent feature list can be applied to those devices.

Transfer (Register 0xFF)

All registers except Register 0x100 are updated the moment they are written. Setting Bit 0 = 1 in the transfer register initializes the settings in the ADC resolution/sample rate override register (Address 0x100).

Power Modes (Register 0x08)

Bits[7:6]—Open

Bit 5—External Power-Down Pin Function

When set (Bit 5 = 1), the external PDWN pin initiates standby mode. When cleared (Bit 5 = 0), the external PDWN pin initiates full power-down mode.

Bits[4:2]—Open

Bits[1:0]—Internal Power-Down Mode

In normal operation (Bits[1:0] = 00), all ADC channels are active.

In full power-down mode (Bits[1:0] = 01), the digital datapath clocks are disabled and the digital datapath is reset. Outputs are disabled.

In standby mode (Bits[1:0] = 10), the digital datapath clocks and the outputs are disabled.

During a digital reset (Bits[1:0] = 11), all the digital datapath clocks and the outputs (where applicable) on the chip are reset, except the SPI port. Note that the SPI is always left under control of the user; that is, it is never automatically disabled or in reset (except by power-on reset).

Enhancement Control (Register 0x0C)

Bits[7:3]—Open

Bit 2—Chop Mode

For applications that are sensitive to offset voltages and other low frequency noise, such as homodyne or direct conversion receivers, chopping in the first stage of the AD9681 is a feature that can be enabled by setting Bit 2 = 1. In the frequency domain, chopping translates offsets and other low frequency noise to $f_{CLK}/2$, where they can be filtered.

Bits[1:0]—Open

Output Mode (Register 0x14)

Bit 7—Open

Bit 6—LVDS-ANSI/LVDS-IEEE Option

Setting Bit 6 = 1 chooses the LVDS-IEEE (reduced range) option. (The default setting is LVDS-ANSI.) As described in Table 18, when either LVDS-ANSI mode or the LVDS-IEEE reduced range link is selected, the user can select the driver termination resistor in Register 0x15, Bits[5:4]. The driver current is automatically selected to give the proper output swing.

Table 18. LVDS-ANSI/LVDS-IEEE Options

LVDS-ANSI/ LVDS-IEEE Option, Bit 6	Output Mode	Output Driver Termination	Output Driver Current
0	LVDS-ANSI	User selectable	Automatically selected to give proper swing
1	LVDS-IEEE reduced range link	User selectable	Automatically selected to give proper swing

Bits[5:3]—Open

Bit 2—Output Invert

Setting Bit 2 = 1 inverts the output bit stream.

Bit 1—Open

Bit 0—Output Format

By default, setting Bit 0 = 1 sends the data output in twos complement format. Clearing this bit (Bit 0 = 0) changes the output mode to offset binary.

Output Adjust (Register 0x15)

Bits[7:6]—Open

Bits[5:4]—Output Driver Termination

These bits allow the user to select the internal output driver termination resistor.

Bits[3:1]—Open

Bit 0—FCO±x, DCO±x Output Drive

Bit 0 of the output adjust register controls the drive strength on the LVDS driver of the FCO±1, FCO±2, DCO±1, and DCO±2 outputs only. The default value (Bit 0 = 0) sets the drive to 1×. Increase the drive to 2× by setting the appropriate channel bit in Register 0x05 and then setting Bit 0 = 1. These features cannot be used with the output driver termination selected. The termination selection takes precedence over the 2× driver strength on FCO±1, FCO±2, DCO±1, and DCO±2 when both the output driver termination and output drive are selected.

Output Phase (Register 0x16)

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] determine at which phase of the external clock the sampling occurs. This is applicable only when the clock divider is used. It is prohibited to select a value for Bits[6:4] that is greater than the value of Bits[2:0], Register 0x0B. See Table 19 for more information.

Table 19. Input Clock Phase Adjust Options

Input Clock Phase Adjust, Bits[6:4]	Number of Input Clock Cycles of Phase Delay
000 (Default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Bits[3:0]—Output Clock Phase Adjust

See Table 20 for more information.

Table 20. Output Clock Phase Adjust Options

Output Clock Phase Adjust, Bits[3:0]	DCO Phase Adjustment (Degrees Relative to D0±x/D1±x Edge)
0000	0
0001	60
0010	120
0011 (Default)	180
0100	240
0101	300
0110	360
0111	420
1000	480
1001	540
1010	600
1011	660

Serial Output Data Control (Register 0x21)

The serial output data control register programs the AD9681 in various output data modes, depending on the data capture solution. Table 21 describes the various serialization options available in the AD9681.

Resolution/Sample Rate Override (Register 0x100)

This register is designed to allow the user to downgrade the device (that is, establish lower power) for applications that do not require full sample rate. Settings in this register are not initialized until Bit 0 of the transfer register (Register 0xFF) is set to 1.

This function does not affect the sample rate; it affects the maximum sample rate capability of the ADC, as well as the resolution.

User I/O Control 2 (Register 0x101)

Bits[7:1]—Open

Bit 0—SDIO Pull-Down

Set Bit 0 = 1 to disable the internal 30 kΩ pull-down on the SDIO/OLM pin. This feature limits loading when many devices are connected to the SPI bus.

User I/O Control 3 (Register 0x102)

Bits[7:4]—Open

Bit 3—VCM Power-Down

Set Bit 3 = 1 to power down the internal VCM generator. This feature is used when applying an external reference.

Bits[2:0]—Open

Table 21. SPI Register Options

	Serialization Options Selected				
Register 0x21 Contents	**Serial Output Number of Bits (SONB)**	**Frame Mode**	**Serial Data Mode**	**DCO Multiplier**	**Timing Diagram**
0x30	16-bit	1×	DDR two-lane, bytewise	4 × f_S	Figure 3 (default setting)
0x20	16-bit	1×	DDR two-lane, bitwise	4 × f_S	Figure 3
0x10	16-bit	1×	SDR two-lane, bytewise	8 × f_S	Figure 3
0x00	16-bit	1×	SDR two-lane, bitwise	8 × f_S	Figure 3
0x34	16-bit	2×	DDR two-lane, bytewise	4 × f_S	Figure 5
0x24	16-bit	2×	DDR two-lane, bitwise	4 × f_S	Figure 5
0x14	16-bit	2×	SDR two-lane, bytewise	8 × f_S	Figure 5
0x04	16-bit	2×	SDR two-lane, bitwise	8 × f_S	Figure 5
0x40	16-bit	1×	DDR one-lane, wordwise	8 × f_S	Figure 7
0x32	12-bit	1×	DDR two-lane, bytewise	3 × f_S	Figure 4
0x22	12-bit	1×	DDR two-lane, bitwise	3 × f_S	Figure 4
0x12	12-bit	1×	SDR two-lane, bytewise	6 × f_S	Figure 4
0x02	12-bit	1×	SDR two-lane, bitwise	6 × f_S	Figure 4
0x36	12-bit	2×	DDR two-lane, bytewise	3 × f_S	Figure 6
0x26	12-bit	2×	DDR two-lane, bitwise	3 × f_S	Figure 6
0x16	12-bit	2×	SDR two-lane, bytewise	6 × f_S	Figure 6
0x06	12-bit	2×	SDR two-lane, bitwise	6 × f_S	Figure 6
0x42	12-bit	1×	DDR one-lane, wordwise	6 × f_S	Figure 8

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting the design and layout of the AD9681 as a system, it is recommended that the designer become familiar with these guidelines, which describe the special circuit connections and layout requirements that are needed for certain pins.

POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD9681, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, use several different decoupling capacitors for both high and low frequencies. Place these capacitors near the point of entry at the PCB level and near the pins of the device, with minimal trace length.

A single PCB ground plane is typically sufficient when using the AD9681. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

BOARD LAYOUT CONSIDERATIONS

For optimal performance, give special consideration to the AD9681 board layout. The high channel count and small footprint of the AD9681 create a dense configuration that must be managed for matters relating to crosstalk and switching noise.

Sources of Coupling

Trace pairs interfere with each other by inductive coupling and capacitive coupling. Use the following guidelines:

- Inductive coupling is current induced in a trace by a changing magnetic field from an adjacent trace, caused by its changing current flow. Mitigate this effect by making traces orthogonal to each other whenever possible and by increasing the distance between them.
- Capacitive coupling is charge induced in a trace by the changing electric field of an adjacent trace. This effect can be mitigated by minimizing facing areas, increasing the distance between traces, or changing dielectric properties.
- Through-vias are particularly good conduits for both types of coupling and must be used carefully.
- Adjacent trace runs on the same layer may cause unbalanced coupling between channels.
- Traces on one layer should be separated by a plane (ac ground) from the traces on another layer. Significant coupling occurs through gaps in that plane, such as the setback around through-vias.

Crosstalk Between Inputs

To avoid crosstalk between inputs, consider the following guidelines:

- When routing inputs, sequentially alternate input channels on the top and bottom (or other layer) of the board.
- Ensure that the top channels have no vias within 5 mm of any other input channel via.
- For bottom channels, use a via-in-pad to minimize top-metal coupling between channels.
- Avoid running input traces parallel with each other that are nearer than 2 mm apart.
- When possible, lay out traces orthogonal to each other and to any other traces that are not dc.
- Secondhand or indirect coupling may occur through nonrelated dc traces that bridge the distance between two traces or vias.

Coupling of Digital Output Switching Noise to Analog Inputs and Clock

To avoid the coupling of digital output switching noise to the analog inputs and the clock, use the following guidelines:

- Vias on the outputs are a main conduit of noise to the vias on the inputs. Maintain 5 mm of separation between any output via and any input via.
- Place the encode clock traces on the top surface. Vias are not recommended in the clock traces. However, if they are required, ensure that there are no clock trace vias within 5 mm of any input via or output via.
- Place output surface traces (not imbedded between planes) orthogonal to one another as much as possible. Avoid parallel output to input traces within 2 mm.
- Route digital output traces away from the analog input side of the board.
- Coupling among outputs is not a critical issue, but separation between these high speed output pairs increases the noise margin of the signals and is good practice.

CLOCK STABILITY CONSIDERATIONS

When powered on, the AD9681 goes into an initialization phase where an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the AD9681 needs a stable clock. If the ADC clock source is not present or not stable during ADC power-up, the state machine is disrupted and the ADC starts up in an unknown state. To correct this, reinvoke an initialization sequence after the ADC clock is stable by issuing a digital reset using Register 0x08. In the default configuration (internal V_{REF}, ac-coupled input) where V_{REF} and V_{CM} are supplied by the ADC itself, a stable clock during power-up is sufficient. When V_{REF} or V_{CM} is supplied by an external source, it, too, must be stable at power-up. Otherwise, a subsequent digital reset, using Register 0x08, is needed. The pseudocode sequence for a digital reset follows:

```
SPI_Write (0x08, 0x03);   # digital reset
SPI_Write (0x08, 0x00);   # normal operation
```

VCM

Decouple the VCMx pin to ground with a 0.1 µF capacitor.

REFERENCE DECOUPLING

Decouple the VREF pin externally to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI PORT

Ensure that the SPI port is inactive during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB1, CSB2, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9681 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS

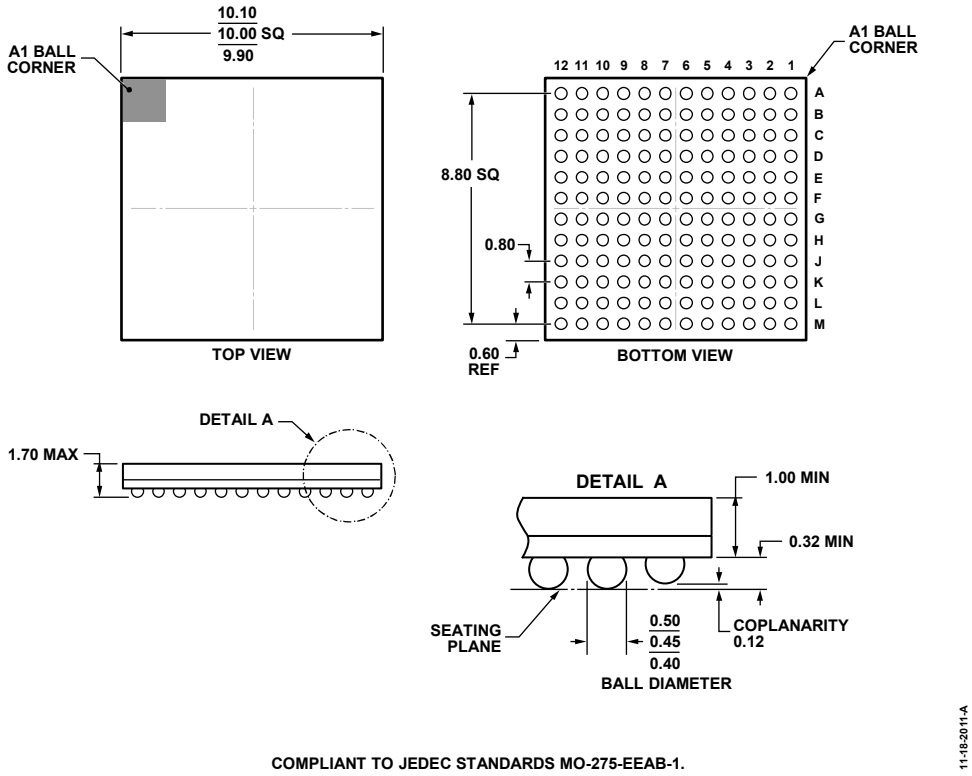

Figure 54. 144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-144-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9681BBCZ-125	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-7
AD9681BBCZRL7-125	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-7
AD9681-125EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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