THE DATASHEET OF

IXBD4411PI

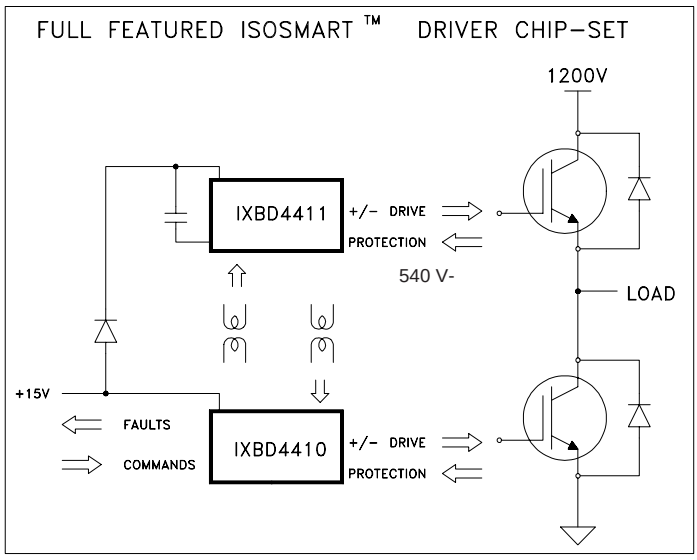
ISOSMART™ Half Bridge Driver Chipset

Type	Description	Package	Temperature Range
IXBD4410PI	Full-Feature Low-Side Driver	16-Pin P-DIP	-40 to +85°C
IXBD4411PI	Full-Feature High-Side Driver	16-Pin P-DIP	-40 to +85°C
IXBD4410SI	Full-Feature Low-Side Driver	16-Pin SO	-40 to +85°C
IXBD4411SI	Full-Feature High-Side Driver	16-Pin SO	-40 to +85°C

The IXBD4410/IXBD4411 ISOSMART chipset is designed to control the gates of two Power MOSFETs or Power IGBTs that are connected in a half-bridge (phase-leg) configuration for driving multiple-phase motors, or used in applications that require half-bridge power circuits. The IXBD4410/ IXBD4411 is a full-feature chipset consisting of two 16-Pin DIP or SO devices interfaced and isolated by two small-signal ferrite pulse transformers. The small-signal transformers provide greater than 1200 V isolation.

Even with commutating noise ambients greater than ±50 V/ns and up to 1200 V potentials, this chipset establishes error-free two-way communications between the system ground-reference IXBD4410 and the inverter output-reference IXBD4411. They incorporate undervoltage V_{DD} or V_{EE} lockout and overcurrent or desaturation shutdown to protect the IGBT or Power MOSFET devices from damage.

The chipset provides the necessary gate drive signals to fully control the grounded-source low-side power device as well as the floating-source high-side power device. Additionally, the IXBD4410/4411 chipset provides a negative-going, off-state gate drive signal for improved turn-off of IGBTs or Power MOSFETs and a system logic-compatible status fault output $\overline{FLT}$ to indicate overcurrent or desaturation, and undervoltage V_{DD} or V_{EE}. During a status fault, both chipset keep their respective gate drive outputs off; at V_{EE}.



Features

- 1200 V or greater low-to-high side isolation.
- Drives Power Systems Operating on up to 575 V AC mains
- dv/dt immunity of greater than ±50V/ns
- Proprietary low-to-high side level translation and communication
- On-chip negative gate-drive supply to ensure Power MOSFET or IGBT turn-off and to prevent gate noise interference
- 5 V logic compatible HCMOS inputs with hysteresis
- Available in either the 16-Pin DIP or the 16-Pin wide-body, small-outline plastic package
- 20 ns switching time with 1000 pF load; 100 ns switching time with 10,000 pF load
- 100 ns propagation delay time
- 2 A peak output drive capability
- Self shut-down of output in response to over-current or short-circuit
- Under-voltage and over-voltage V_{DD} lockout protection
- Protection from cross conduction of the half bridge
- Logic compatible fault indication from both low and high-side driver

Applications

- 1- or 3-Phase Motor Controls
- Switch Mode Power Supplies (SMPS)
- Uninterruptible Power Supplies (UPS)
- Induction Heating and Welding Systems
- Switching Amplifiers
- General Power Conversion Circuits

IXYS reserves the right to change limits, test conditions and dimensions.

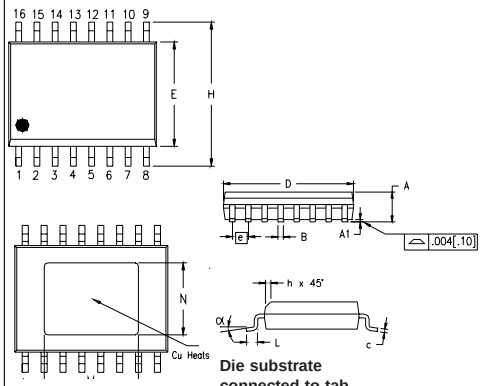
Symbol	Definition	Maximum Ratings	
V_{DD}/V_{EE}	Supply Voltage	-0.5 ... 24	V
V_{in}	Input Voltage (INH, INL)	-0.5...V_{DD} +0.5	V
I_{in}	Input Current (INL, INH, IM)	±10	A
I_o (rev)	Peak Reverse Output Current (OUT)	2	A
P_D	Maximum Power Dissipation (T_A = 25° C)	600	mW
P_D	T_C = 25° C (16-Pin SOIC)	10	W
T_A	Operating Ambient Temperature	-40 ... 85	°C
T_{JM}	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	-55 ... 150	°C
T_L	Lead Soldering Temperature for 10 s	300	°C
R_{thJA}		1.67	K/W
R_{thJC}	(16-Pin SOIC)	10	K/W

Recommended Operating Conditions

V_{DD}/V_{EE}	Supply Voltage	10 ... 20	V
V_{DD}/LG		10 ... 16.5	V
L_{Gh}/L_{Gl}	Maximum Common Mode dv/dt	±50	V/ns

Symbol	Definition/Condition (T_A = 25°C, V_{DD} = 15 V, unless otherwise specified)	Characteristic Values min.	typ.	max.	
INL, INH Inputs (referred to LG)					
V_{t+}	Positive-Going Threshold	3.65			V
V_{t-}	Negative-Going Threshold			1	V
V_{ih}	Input Hysteresis		1		V
I_{in}	Input Leakage Current/V_{in}=V_{DD} or LG	-1		1	µA
C_{in}	Input Capacitance		10		pF
Open Drain Fault Output (referred to LG)					
V_{oh}	HI Output/R_{pu} = 10 kΩ to V_{DD}	V_{DD}-0.05			V
V_{ol}	LO Output/I_o = 4 mA		0.3	0.5	V
OUT Output (referred to LG)					
V_{oh}	HI Output/I_o = -5 mA	V_{DD}-0.05			V
V_{ol}	LO Output/I_o = 5 mA		V_{EE}+0.05		V
R_o	Output HI Res./I_o = -0.1 A		3	5	Ω
R_o	Output LO Res./I_o = 0.1 A		3	4	Ω
I_{pk}	Peak Output Current/C_L = 10 nF	1.5	2		A
IM Input (referred to KG)					
V_{t+}	Positive-Going Threshold	0.24	0.3	0.45	V
C_{in}	Input Capacitance		10		pF
R_s	Shorting Device Output Resistance	50	75	100	Ω
VEE Supply (referred to LG)					
V_{EE}	Output Voltage/I_o = 1 mA, C_o = 1 µF	-5	-6.5	-7.5	V
I_{out}	Output Current/V_{out} = 0.70 • V_{EE}	-20	-25		mA
f_{inv}	Inverting Frequency		600		kHz
V_{EEF}	Undervoltage Fault Indication	-3		-4.8	V

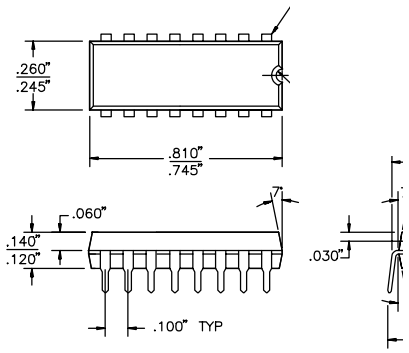
Dimensions in inch (1" = 25.4 mm)
16-Pin SOIC



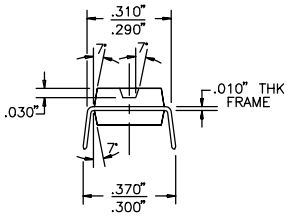
Die substrate connected to tab

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
B	.013	.020	0.33	0.51
C	.009	.013	0.23	0.32
D	.398	.413	10.10	10.50
E	.291	.299	7.40	7.60
e	.050BSC		1.27BSC	
H	.394	.419	10.00	10.65
h	.010	.029	0.25	0.75
L	.016	.050	0.40	1.27
M	.240	.260	6.10	6.60
N	.190	.210	4.83	5.33
α	0°	8°	0°	8°

16-Pin Plastic DIP



End view



Symbol	Definition/Condition		Characteristic Values (T_A = 25°C, V_{DD} = 15 V, unless otherwise specified) min.	typ.	max.	
V_{DD} Undervoltage Lockout						
V_{uv}	Drop Out		9.5	10.5	11.5	V
V_{uh}	Hysteresis		0.1	0.15	0.3	V
Quiescent Power Supply Current						
I_{DD}	V_{DD} Current/V_{in}=V_{DD} or LG, I_o = 0				20	mA
INL and INH Inputs (Fig. 1a - 1c)						
$t_{d(on)}$	Turn-on delay time; 4410	C_L =1nF		110	175	ns
t_r	Rise time;	C_L =10 nF		70	100	ns
		C_L =1 nF		15	20	ns
$t_{d(off)}$	Turn-off delay time 4410	C_L =1nF		70	150	ns
t_f	Fall time	C_L =10nF		70	150	ns
		C_L =1nF		15	20	ns
$t_{dlh(off)}$	4410/4412 Turn-on delay time vs. 4411 Turn-off delay time	C_L =1nF		60	150	ns
$t_{dlh(on)}$	4410 Turn-on delay time vs. 4411 Turn-off delay time	C_L =1nF		60	150	ns
Fault Output Delay for any Fault Conditions (4410/4411)						
t_{FLT}	$\overline{FLT}$ Delay/R_{pu} = 2 kΩ	C_L = 20 pF		200	300	ns
Overcurrent Protection Delay						
t_{oc}	Driver-Off delay time	C_L = 1 nF		200	300	ns

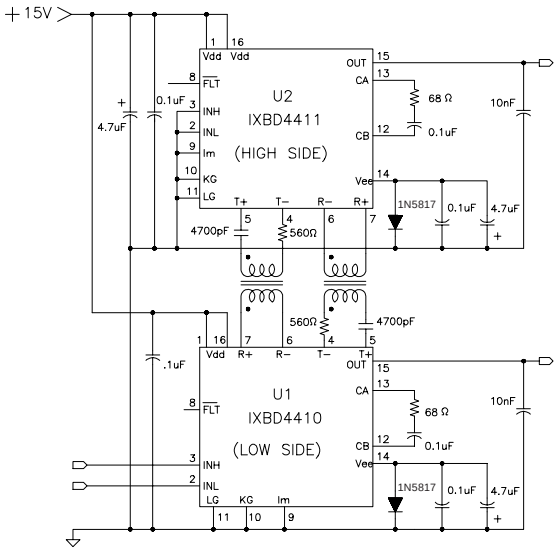


Fig. 1a: IXBD4410/4411 Switching time test circuit

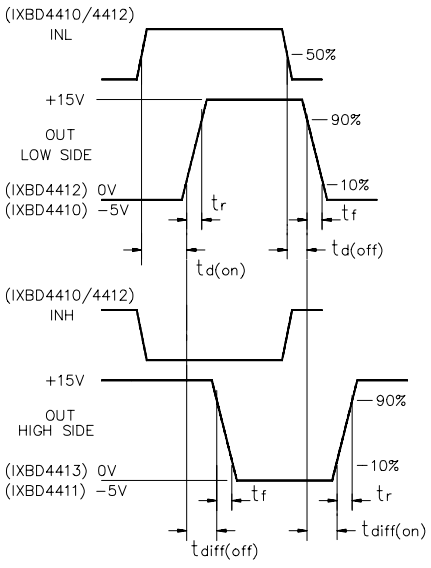


Fig. 1b: Output signal waveform

Chipset Overview

This ISOSMART™ chipset is a pair of integrated circuits providing isolated high- and low-side drivers for phase-leg motor controls, or any other application which utilizes a half bridge, 2- or 3-phase drive configuration. They consist of two drive control inputs (INL and INH) for two Power-MOSFET/IGBT gate-drive outputs. Both inputs operate from a common ground and are activated by HCMOS compatible logic levels. The low-side output operates near input ground, while the high-side output operates from a floating ground that is nominally the source connection of the high-side phase-leg power device. Both outputs typically provide 2 A of transient current drive for fast switching of the phase-leg power device.

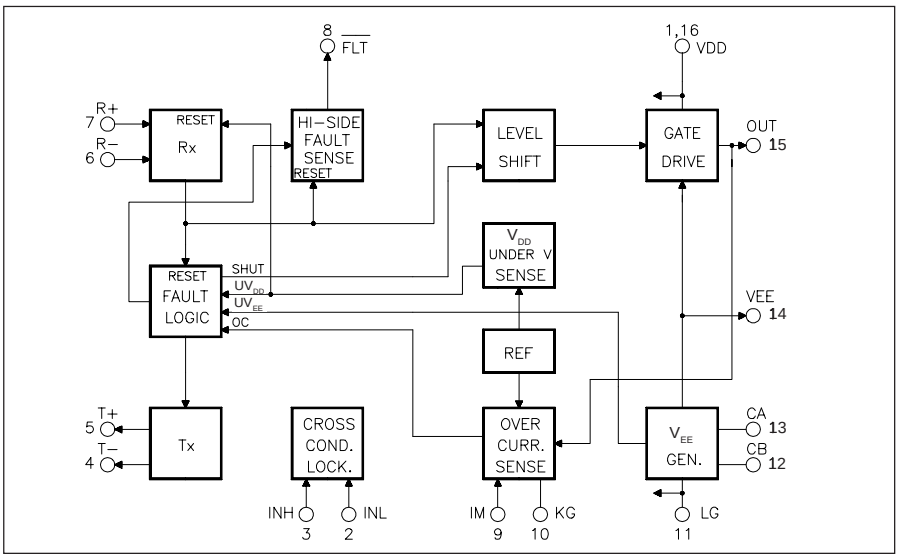


Fig. 2: IXBD4411, high-side driver block diagram

IXBD4410/IXBD4411

The full featured ISOSMART™ driver chipset incorporates a IXBD4410 as the low-side driver (Fig. 3) and a IXBD4411 as the high-side driver (Fig. 2). When input "INL" is set to a positive logic level, the low-side gate output goes high (turns on); when "INH" is set to a positive logic level, the high-side gate drive output goes high. The high-side IC is isolated from the low-side IC by a magnetic barrier, across which the turn on/off signal is transmitted to the high-side gate drive. The IXBD4411 fault signal is also transmitted back to the IXBD4410 driver via these transformers. This isolation only depends on the low cost communications transformer, which is designed to withstand 1200 V or more.

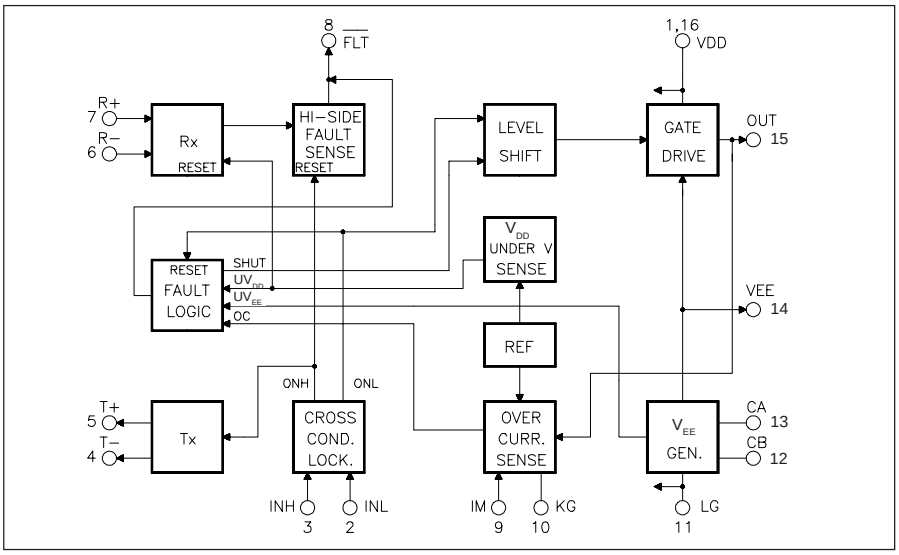


Fig. 3: IXBD4410, low-side driver block diagram

There are two magnetic transmission channels between the low- and high-side IC's for bi-directional communication. One sends a signal from the low-side IXBD4410 IC up to the high-side IXBD4411 IC and the other sends a signal back from the high-side to the low-side IC. The signal that is sent up controls the IXBD4411 gate-drive output. The signal sent from the IXBD4411 back to the IXBD4410 indicates a high-side fault has occurred (overcurrent, or under-voltage of the high-side +power supplies). This is detected at the IXBD4410 driver and sets "$\overline{\text{FLT}}$" pin low, to indicate the high-side fault.

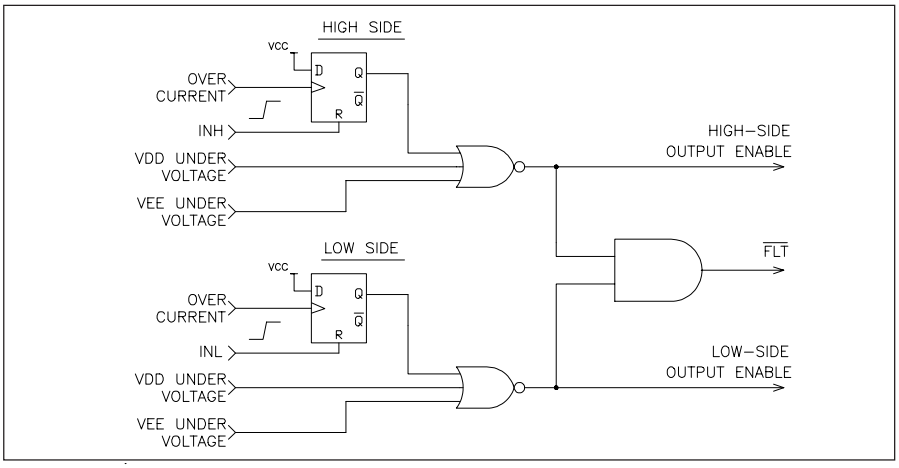


Fig. 4: Logic representation of IXBD4410 $\overline{\text{FLT}}$ signal

The fault signal that is returned from

the IXBD4411 is strictly for status only. Any gate-drive shutdown because of a high-side fault is done locally within the high-side IXBD4411. The IXBD4411 gate-drive will turn-off the power device whenever an overcurrent or under voltage condition arises. The overcurrent sensing is active only while the gate driver output is "high" (on). The overcurrent fault condition is latched and is reset on the next INH gate input positive transition. The FLT (pin 8) of the IXBD4411 is not used and should be grounded.

The low-side IXBD4410 driver provides an output pin 8 (FLT) to indicate a high-side (IXBD4411) **or** a low-side (IXBD4410) fault. This output pin is an "open-drain" output. The IXBD4410 low-side driver fault indications are similar to the IXBD4411 high-side driver indications as outlined above. A "graphic" logic diagram of the chipset's FLT function is presented in Fig.4. Note that this diagram presents the logic of this function at the "low-side" IXBD4410 driver and is not the actual circuit. It describes the combined logic of the "fault logic" and "hi-side fault sense" blocks in both the IXBD4410 and IXBD4411 as shown in Fig. 2 and 3.

The most efficient method of providing power for the high-side driver is by bootstrapping. This method is illustrated in the functional drawing on page 4 and in the application example (Fig. 6 and 9) by diode D1 and capacitor C1. Using this method, the power is drawn through a high-voltage diode onto a reservoir capacitor whenever the floating high-side ground returns to near the real ground of the low-side driver. When the high-side gate is turned on and the floating ground moves towards a higher potential, the bootstrapping diode back-biases, and the high-side driver draws its power solely from the reservoir capacitor. Power may also be provided via any isolated power supply (usually an extra secondary on the system housekeeping supply switching transformer).

Both the IXBD4410 and IXBD4411 contain on-board negative charge pumps to provide negative gate drive, which ensures turn-off of the high- or low-side power device in the presence of currents induced by power device Miller capacitance or from inductive ground transients. These charge pumps provide -5 V relative to the local driver ground when V_{DD} is at +15 V, and at rated average currents of 25 mA. The charge pump requires two external capacitors, C7 and C11 in Fig. 6. The charge pump frequency is nominally 600 kHz. The charge pump clock is turned off whenever the difference between the V_{DD} and V_{EE} supplies exceed 20 V, to prevent exceeding the breakdown rating of the IC.

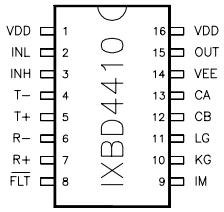
Both the IXBD4410 and IXBD4411 drivers possess two local grounds each, a common logic ground, and "Kelvin" ground. The Kelvin ground and logic grounds are first connected directly to each other, and then to the Kelvin-source of the power device for accurate over-current measurement in the presence of inductive transients on the power device source terminal.

Power MOSFET or IGBT overcurrent sensing utilizes an on-chip comparator with a typical 300 mV threshold. In a typical application, the current mirror pin of the Power MOSFET or IGBT is connected to a grounded, low-value resistor, and to the overcurrent comparator input on the high- or low-side driver. The comparator will respond typically within 150 ns to an overcurrent condition to shutdown the driver output. The power switches could be protected also by desa-turation detection (see Fig. 6, 7 and 9).

To assure maximum protection for the phase-leg power devices, the chipset incorporates the following Power MOSFET and IGBT protection circuits:

- Power device overcurrent or desa-turation protection. The IXBD4410/ 4411will turn off the driven device within 150 ns of sensing an output overcurrent or desaturation condition.
- Gate-drive lockout circuitry to prevent cross conduction (simultaneous conduction of the low- and high-side phase-leg power devices), either under normal operating conditions or when a fault occurs.
- During power-up, the chipset's gate-drive outputs will be low (off), until the voltage reaches the under-voltage trip point.
- Under-voltage gate-drive lockout on the low- and/or high- side driver whenever the respective positive power supply falls below 9.5 V typically.
- Under-voltage gate-drive lockout on the low- and high- side driver whenever the respective negative power supply rises above -3 V typically.

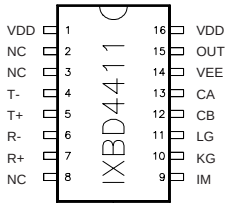
Pin Description
IXBD4410 (Low-Side Driver)



Sym. Pin Description of IXBD 4410/4411

VDD	1 16	Positive power supply.
INL **NC**	2	Logic input signal referenced to LG (logic ground). In the IXBD4410. A "high" to this pin turns on its gate drive output and resets its fault logic. A "low" to this pin turns off the gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). **N**o **C**onnection (IXBD 4411)
INH **NC**	3	Logic input signal referenced to LG (logic ground). In the IXBD4410, this signal is transmitted to the IXBD4411 "high-side" driver through pins 4 and 5 (T- and T+). A "high" to this pin turns on the IXBD4411 gate drive output and resets its fault logic. A "low" to this pin turns off the IXBD4411 gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). **N**o **C**onnection (IXBD 4411)
T- **T+**	4 5	Transmitter output complementary drive signals. Direct drive of the low signal transformer, which is connected to the receiver of the chipset's companion device. In the IXBD4410, this signal transmits the on/off command to its companion IXBD4411. In the IXBD4411, this signal transmits the fault indication to its companion IXBD4410 driver.
R- **R+**	6 7	Receiver input complementary signal. Directly connected to the low signal transformer, which is driven by the chipset's companion device. In the IXBD4410, this input receives the fault indication from its companion IXBD4411 driver. In the IXBD4411, this input receives the on/off command from its companion IXBD4410 driver.
VEE	TAB	Connected to Pin 14 (substrate)

Pin Description
IXBD4411 (High-Side Driver)



Sym. Pin Description of IXBD 4410/4411

$\overline{\text{FLT}}$ **NC**	8	Low/high side fault output. In the IXBD4410, this output indicates a fault condition of either device of the chipset. A "high" indicates no fault, A "low" indicates that either overcurrent, V_{DD} or V_{EE} under-voltage occurred. In case of overcurrent, this output will remain active "low" until the next input cycle of the respective driver. In case of under-voltage, this output will remain "low" until the proper voltage is restored. The IXBD4411 does not have a $\overline{\text{FLT}}$ output,and its pin 8 should be tied to LG **N**o **C**onnection (IXBD 4411)
IM	9	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 70 Ω resistor. Any voltage at this pin above the threshold of .3 V typical, will turn the output (pin 15) off. This pin is used for power device overcurrent protection.
KG	10	Kelvin ground. This ground is used as Kelvin connection for overcurrent or desaturation sensing.
LG	11	Logic and power ground.
CB **CA**	12 13	Capacitor terminals for negative charge pump (V_{EE}); "+" terminal is CB (pin 12).
VEE	14	Negative supply terminal(substrate)
OUT	15	Gate drive output. In the IXBD4410 this output responds to the INL signal. A "high" at INL will turn it on ("high"), a "low" will turn it off ("low"). In the IXBD4411, this output responds to the transmitted signal from the companion IXBD4410. A "high" at INH of the IXBD4410 drives will turn it on ("high"). A "low" will turn it off ("low"). This output will turn off ("low") also in response to any fault condition.

Application

The IXBD4410/4411 chipset devices are specifically designed as MOS-gated transistor drivers in half-bridge power converters, 1- and 3-phase motor controls, and UPS applications. The phase-leg PWM command is normally generated by previous (user provided) circuitry. It must be decomposed into two separate logic signals, one for the high-side and one for the low-side power transistors, with appropriate deadtime for each state transition. The deadtime insures non-overlapping conduction even if the turn-on and turn-off delay times of the power devices are unequal. The minimum deadtime should be greater than t_{dlh}. A separate circuit, or an IC device like the IXYS deadtime generator IXDP630, can be used to perform this function. The ISOSMART™ chipset family of devices do not generate deadtime, although there is an internal lockout that prohibits one device form being commanded "on" before the other is commanded "off". This simplifies start-up and shutdown protection circuitry, preventing logic error during power-up from turning on both high-and low-side transistors simultaneously.

Negative V_{EE} Charge Pump Circuit Design

The on-chip V_{EE} generator provided in the IXBD4410/4411 generates a negative power supply, regulated at 20 V below the positive V_{DD} rail. If V_{DD} is +10 V, V_{EE} will be -10 V. If V_{DD} is +15 V, V_{EE} will be -5 V. This negative drive potential in the off-state is either desirable or required in many instances. When switching a clamped inductive load (Fig. 5), the turn-on of Q2 will commutate the freewheeling diode around Q1. Whether this diode is intrinsic (as in a MOSFET) or extrinsic (IGBT or bipolar), its reverse recovery is critical to proper circuit operation.

At high turn-on di/dt in Q2 and near its rated voltage, the recovery of D1 can get quite "snappy" (the di/dt in the second half of the recovery process, after the diode has begun to recover its blocking capability, can get very large), creating a very high dv/dt across Q1. This dv/dt is impressed across the Miller capacitance of Q1, forcing a large current to flow out the gate

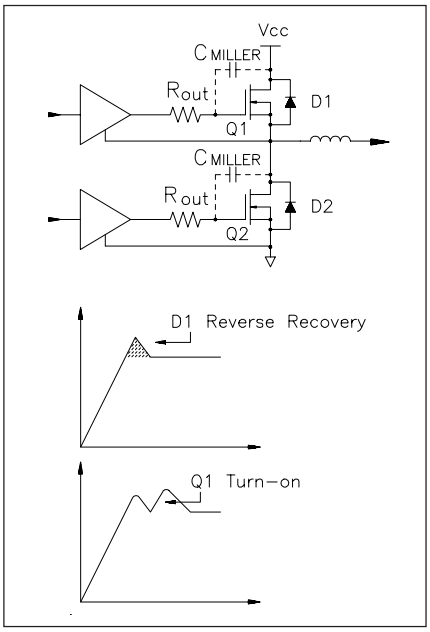


Fig. 5: Switching a clamped inductive load

terminal of the device. If this current pulse causes a high enough voltage drop across the output impedance of the gate drive circuit, R_{out}, Q1 will be turned on.

The Q1 conduction in every instance Q2 is turned on (and vice versa), aside from degrading efficiency, can lead to catastrophic failure of both power transistors. At high temperature, where the -6 to -7 mV/°C temperature coefficient of IGBT/MOSFET threshold reduces the voltage required to create a failure, this problem is even more likely to occur. In an industrial module package (e.g.: a 150 A/1200 V IGBT phase-leg module), the series inductance contributed by the long gate leads and connectors further complicate the design.

In a heavily snubbered converter, or in a power supply design with low transformer leakage inductance, the design problem is relatively simple and negative drive is seldom required. However, in a modern snubberless or lightly snubbered converter design, it is important to keep the gate drive impedance high enough during transistor turnoff to limit the reapplied dv/dt (the transistor is its own 'active' snubber). This is always important for EMI control, and in the case of IGBT may be required to achieve the necessary RBSOA. At the same time, it is mandatory to keep the off-state gate drive impedance very low to assure the transistor remain off during induced dv/dt (including diode recovery dv/dt). In some instances, it is simply not possible to satisfy both criteria with 0 V applied in the off-state. In these cases the IXBD4410/4411 with V_{EE} negative bias generator must be used.

The internal V_{EE} generator is a charge pump circuit. Referring to Fig. 6, an external charge pump capacitor is required between the CA and CB

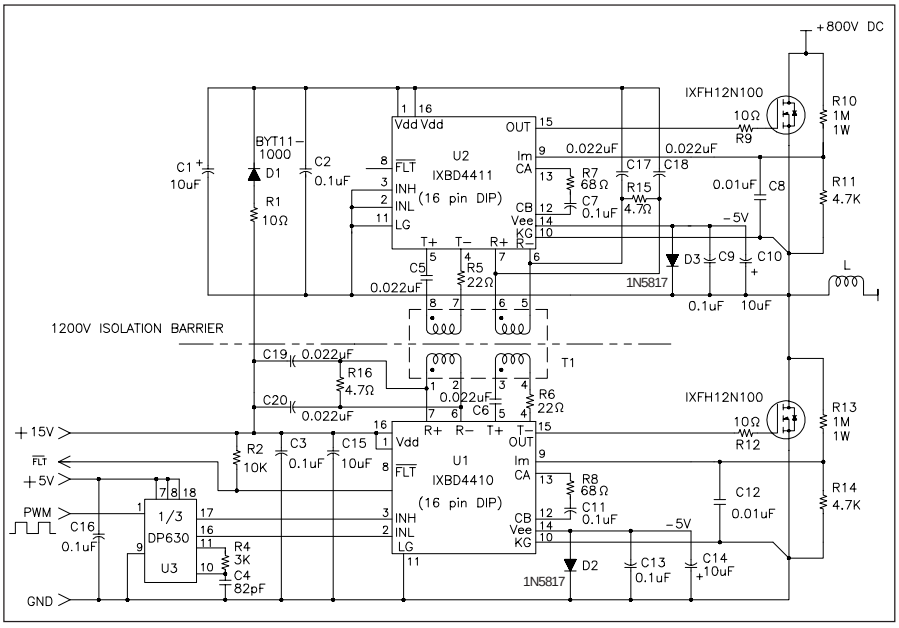


Fig. 6: IXBD4410/4411 Detailed one phase circuit with dead time generator IXDP 630

terminals (C7, C11), and an output reservoir capacitor between V_{EE} and GND (C10, C14). A 0.1 µF charge pump capacitor (C7, C11) is recommended. The voltage regulation method used in the IXBD4410/4411 allows a 1 to 2 V ripple frequency depends on the size of the V_{EE} output reservoir capacitor (C10, C14) and the average load current. The minimum recommended output reservoir (C10, C14) is 4.7 µF tantalum, or 10 µF if aluminium electrolytic construction is chosen. Note that this reservoir capacitor is in addition to a good quality high frequency bypass capacitor (0.1 µF) that should be placed from VEE to GND (C9, C13).

A small resistor in series with the charge pump capacitor, (R7, R8) reduces the peak charging currents of the charge pump. A value or 68 Ω or greater is recommended, as illustrated in the applications example in Fig. 6.

Current Sense / Desaturation Detection Circuit

All members of the ISOSMART™ driver family provide a very flexible overcurrent/short circuit protection capability that works with both standard three-terminal power transistors, and with 4- and 5-terminal current sensing power devices. Overcurrent detection is accomplished as illustrated in Fig. 7a (for a current mirror power device) and Fig. 7b (for a standard three terminal power transistor). Desaturation detection is accomplished with the same internal circuits by measuring the voltage across the power transistor in the on-state with an external resistor divider (Fig. 7c).

The IM input trip point V_{TIM}, typically 300 mV, is referenced to the Kelvin ground pin KG.

Current Mirror MOSFET and IGBT allow good control of peak let-through currents and excellent short circuit protection when combined with the ISOSMART™ driver family of devices. The sense resistor is chosen to develop 300 mV at the desired peak transistor current, assuming a mirror ration of 1400:1, and a trip point of 30 A is desired:

R_s = 300 mV • 1400/30 A = 14 Ω
(use 15 Ω CC).

It is important to realize that C_{oss} per unit area of the mirror cells is much larger that C_{oss} per unit area of the bulk of the chip due to periphery effects. This causes a large transient current pulse at the mirror output whenever the transistor switches (C • dv/dt currents), which can cause false overcurrent trigger. The RC filter indicated in Fig. 7a will eliminate this problem.

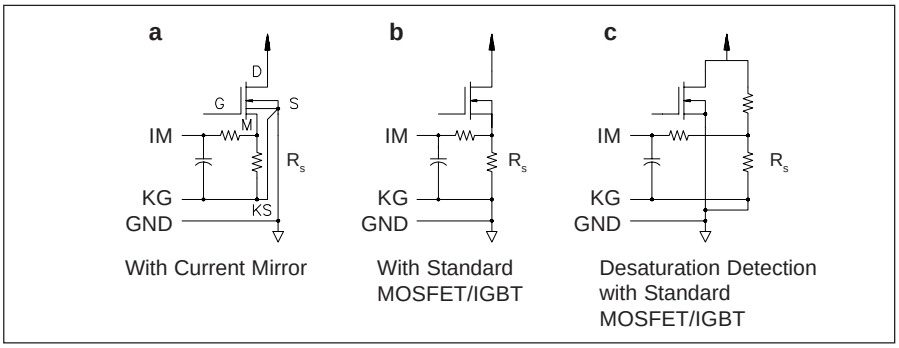


Fig. 7: Alternative overcurrent protection circuits

Standard three-terminal MOSFET and IGBT devices (in discrete as well as modern industrial single transistor and phase-leg modules) can also be protected from short circuit with the ISOSMART™ driver family devices. In discrete device designs, where the source/emitter terminal is available, overcurrent protection with an external power resistor can be implemented. The resistor is placed in series with the device emitter, with the full device current flowing through it (Fig. 7b). The sense resistor is again selected to develop 300 mV at the desired peak transistor current, assuming a trip point of 30 A is desired:

R_s = 300 mV / 30 A = 10 mΩ
(use 10 mΩ, noninductive current sense resistor).

It is important to recognize that "noninductive" is a relative term, especially when applied to current sense resistor construction and characterization. There is always significant series inductance inserted with the sense resistor, and L • di/dt voltage transients can cause false overcurrent trigger.

The RC filter indicated in Figure 7b will eliminate this problem. Choosing the RC pole at the current sense resistor RL zero should exactly compensate for series inductance. Because the exact value is not normally known (and can vary depending on PC layout and component lead dress) this is not normally a good idea. Usually, the RC time constant should be two to ten times longer than the suspected RL time constant.

Desaturation detection as in Figure 7c is probably the most common method of short circuit protection in use today. While not strictly an "overcurrent" detector, if the power transistor gain, and consequently short circuit let-through current, is well controlled (as with modern MOSFET and IGBT) this methodology offers very effective protection.

The IXBD4410/4411 half-bridge circuits in Fig. 6 uses desaturation detection. In Fig. 6, the voltage across the two power MOSFET devices (or IGBTs) are monitored by two sets of voltage-divider networks, R10 and R11 for the high-side gate driver, and R13 and R14 for the low-side gate driver. The dividers are set to trip the IM input comparators when either Power MOSFET device V_{DS} exceeds a reasonable value, perhaps 50 V (usually a value of 10 % of the nominal DC bus voltage works well). R10 or R13 are chosen to tolerate the applied steady state DC bus voltage at an acceptable power dissipation. Dielectric withstand capability, power handling, temperature rise, and PC board creep and strike spacings, must all be carefully considered in the design of the voltage-divider networks.

In the off-state, the voltage across the Power MOSFET device may go as high as the DC bus potential. To keep this normal condition from setting the internal fault flip-flop of the IXBD4410 or the IXBD4411, an internal CMOS switch is turned on and placed across IM and KG pins shorting them together. This effectively discharges C8 or C12 in Fig. 6 and maintains zero potential

with respect to KG at IM.

When the command arrives to switch on the Power MOSFET device, the CMOS switch shorting IM to KG is turned off. The driven Power MOSFET device is switched on approximately 100 ns to 1 µs later, and with typical load conditions, its drain-to-source potential, V_{DS}, may take an additional 10 µs of delay to collapse to the normal on-state voltage level. To prevent false triggering due to this, C8 or C12 in parallel combination with R10 and R11, or R13 and R14, delays the IM input signal. During this turn-on interval, the voltage across C8 or C12 will rise until the Power MOSFET device finally comes on and pulls the voltage across C8 or C12 back down. If the MOSFET device load circuit is shorted, its V_{DS} voltage cannot collapse at turn-on. In this case, the voltage across C8 or C12 rises rapidly until it reaches 300 mV, tripping the fault flip-flop and shutting down the driver output. At the same time, C8 or C12 must be kept small enough that the added delay does not slow down the detection of a short circuit event so much that the Power MOSFET device fails before the driver realizes that it is in trouble.

Three Phase Motor Controls

Fig. 8 is a block diagram of a typical 3-phase PWM voltage-source inverter motor control. The power circuit consists of six power switching transistors with freewheeling diodes around each of them. The control function may be performed digitally by a microprocessor, microcontroller, DSP chip, or user custom IC; or it may be performed by a PC board full of random logic and analog circuits. In any of these cases, the PWM command for all six power transistors is generated in one circuit, and this circuit is usually referred to system ground potential - the bottom terminal of the power bridge.

The ISOSMART™ family of drivers is the interface between the world of control logic and the world of power, 5 V input logic commands precisely control actions at high voltage and current (1200 V and 100 A in a typical application). Fig. 6 is a detailed schematic of one phase of three 3-phase motor control, showing the interconnection of the IXBD4410/4411 and its associated circuitry.

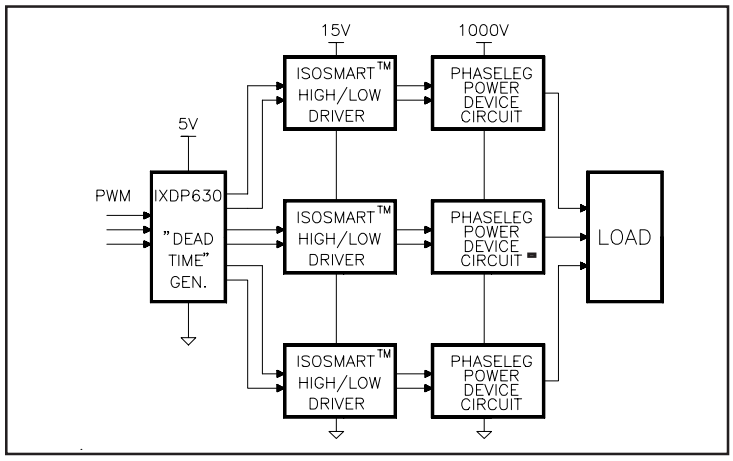


Fig. 8: Typical 3-phase motor control system block diagram

PCB Layout Considerations

The IXBD4410/4411 is intended to be used in high voltage, high speed, high dv/dt applications.

To ensure proper operation, great care must be taken in laying out the printed circuit board. The layout critical areas include the communication links, current sense, gate drive, and supply bypassing.

The communication path should be as short as possible. Added inductance disturbs the frequency response of the signal path, and these distortions may cause false triggering in the receiver. The transformer should be placed between the two ICs with the orientation of one IC reversed (Fig. 9).

Capacitance between the high- and low-side should be minimized. No signal trace should run underneath the communication path, and high- and low-side traces should be separated on the PCB. The dv/dt of the high-side during power stage switching may cause false logic transitions in low-side circuits due to capacitive coupling.

The low signal pulse transformer provides the isolation between high-and low-side circuits. For 460 V~ line operation, a spacing of 4 mm is recommended between low- and high-side circuits, and a transformer HIPOT specification of at least 1500 V~ is required. This creep spacing is usually adequate to control leakage currents on the PCB with up to 1200 V~ applied after 10 to 15 years of accumulated dust and particulates in a standard industrial environment. In other environments, or at other line voltages, this spacing should be appropriately modified.

The current sense/desaturation detect input is noise sensitive. The 300 mV trip point is referred to the KG (Kelvin ground) pin, and the applied signal must be kept as clean as possible, A filter is recommended, preferably a monolithic ceramic capacitor placed as close to the IC as possible directly between IM and KG. To preserve maximum noise immunity, the KG pin should first be connected directly to the LG pin, and the pair then sent directly to the power transistor source/emitter terminal, or (if a desaturation detection circuit is used) to the bottom of the divider resistor chain.

All supply pins must be bypassed with a low impedance capacitor (preferably monolithic ceramic construction) with minimum lead length. The output driver stage draws 2 A (typical) currents during transitions at di/dt values in excess of 100 A/µs. Supply line inductance will cause supply and ground bounce on the chip that can cause problems (logic oscillations and, in severe cases, possible latch-up failure) without proper bypassing. These bypass elements are in addition to the reservoir capacitors required for the negative Vee supply and the high-side bootstrapped supply if these features are used.

Power Circuit Noise Considerations

In a typical transistor inverter, the output MOSFET may switch on or off with di/dt >500 A/µs. Referring to Fig.10 and assuming that the MOSFET source terminal has a one inch path on the PCB to system ground, a voltage as high as V = 27 nH • 500 A/µs = 13.5 V can be developed.

If the MOSFET switched 25 A, the transient will last as long as (25/500) µs or 50 ns, which is more than the typical 6 or 7 ns propagations or of a 74HC series gate.

Fig. 10 illustrates an example layout problem. The power circuit consists of three power transistors (MOSFETs in this example). With the ISOSMART™ gate driver chipset grounded as in option (b) in Fig. 10, the communication path from the IXDP630 will operate without errors. The PC trace induced voltages are not common with the digital

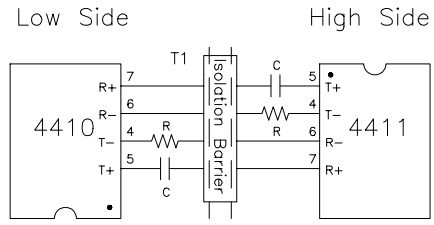


Fig. 9: Suggested IC Orientation

path, so the input of the gate driver will not see or respond to them.

Unfortunately, the MOSFET will not operate properly. The voltage induced across LS1 when Q1 is turned on, acts as source degeneration, modifying the turn-on behavior of the MOSFET. If LS1= 27 nH, and V_{CC} is 15 V (assuming the gate plateau of the MOSFET is 6 V), the di/dt at turn-on will be regulated by the driver/MOSFET/LS1 loop to about 200 A/µs; quite a surprise when your circuit requires 500 A/µs to operate correctly.

It is possible to make use of this behavior to create a turn-on or turn-off di/dt limiter (perhaps to snub the upper free wheeling diode reverse recovery). While possible, this is normally not desirable or practical where two or more transistors are controlled. Equalizing the parasitic impedances of three traces while positioning the transistors next to their heat sink and meeting UL/VDE voltage spacings is just too difficult.

Grounding the gate driver as in option (a) in Fig. 10 solves the MOSFET turn on problem by eliminating LS1 from the source feedback loop. Now, unfortunately, the gate driver will oscillate every time it is turned on or off. As the IXDP630 output goes "high", the gate drive output follows (after its propagation delay) and the MOSFET starts to conduct. The voltage transient induced across LS1 (V = LS1 • di/dt) raises the local ground (point a) until it exceeds V_{oh} (630) - V_{il} and the driver (after its propagation delay) turns the MOSFET off. Now the MOSFET current falls, V(LS1) drops, point (a) drops to system ground (or slightly below), and the driver detects a "1" at its input. After its propagation delay, it again turns the

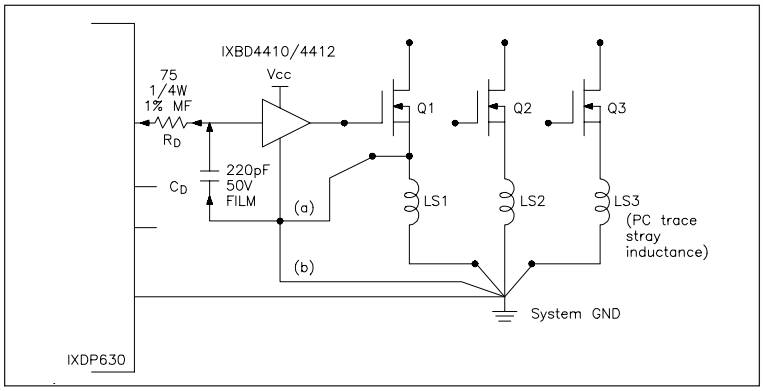


Fig. 10: Potential layout problems that create functional problems

MOSFET on, continuing the oscillation for one more cycle.

To eliminate this problem, a ground level transformation circuit must be added, that rejects this common mode transient. The simplest is a de-coupling circuit, also illustrated in Fig. 10. The capacitor voltage on C_d remains constant while the transient voltage is dropped across R_d and the driver detects no input transition, eliminating the oscillation. This circuit does add significantly to turn-on and turn-off delay time, and cannot be used if the transient lasts longer than the allowable delays. Delay times must be considered in selection of system dead time.

The most complex (and most effective) method of eliminating the effects of transients between grounds is isolation. Optocouplers and pulse transformers are the most commonly used isolation techniques, and work very well in this case. The IXDP630/631 has been specifically designed to directly drive a high speed optocoupler like the Hewlett Packard HCPL22XX family or the General Instrument 740L60XX optologic family. These optos are especially well suited to motor control and power conversion equipment due to their very high common mode dv/dt rejection capabilities.

Transformer Considerations

The transformer is the communication link and isolation barrier between the high- and low-side ICs. The high-side gate and fault signals are transmitted through the transformer while maintaining the proper isolation. The transmitter signal is in the form of a square wave, but the receiver responds only to the logic edges. This allows for much smaller transformer designs, since a 10 kHz switching frequency does not require a 10 kHz pulse transformer.

The recommended transformer for this ISOSMART™ driver chipset is fabricated using a very small ferrite shield bead (see Fig. 11), onto which a six-turn primary and a two-turn secondary winding of 36 AWG magnet wire are made. The two windings are segment wound to achieve primary-to-secondary isolation of up to 2500 V~. The six-turn primaries are connected to the respective IXBD4410/4411 transmitter outputs and the two-turn secondaries are connected to their respective receiver inputs.

The nominal electrical specifications of the transformer are as follows:

- Open circuit inductance (100 kHz; 20 mV): 3 µH
- Interwinding capacitance: 2 pF
- Primary leakage inductance: 0.1 µH
- Turns ratio: 6:2
- Primary-to-secondary isolation (1min): 1500 V~
- Core permeability (μ_i): 125

The recommended ferrite bead is Fair Rite Products part number 2661000101, which is manufactured by:

Fair-Rite Products Corp.
Wallkill, NY
Phone: (800) 836-0427
Web site: www.fair-rite.com

As seen in the application drawings (Fig. 6, 9 and 12) a coupling capacitor (22 nF) and a damping resistor (22 Ω) are added in series with the primary side of the transformer. The capacitor will control the small amount of energy needed to transfer the signal to the companion driver. The resistor will control the damping of the signal and limit the peak transmitter output current. The receiver is designed to operate

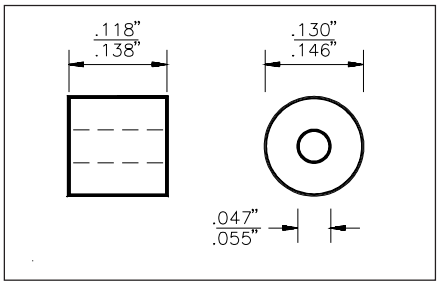


Fig. 11: Ferrite bead dimensions

over a wide common mode input range. To reduce noise pickup, the receiver has ±250 mV of input hysteresis.

If the signal is being distorted at the transmitter, the transmitter is probably running into current limit. A decrease in the coupling capacitance or an increase in the damping resistance should solve this problem. The receiver operates over a wide input range. The minimum amplitude for one side of the receiver is about 1 V and a maximum of about 3 V. It is critical that there be no overshoot on the transformer secondary waveform. Each signal should be slightly overdamped. If significant overshoot exists, the received signal may be logically inverted. An increase of the damping resistor will solve this problem.

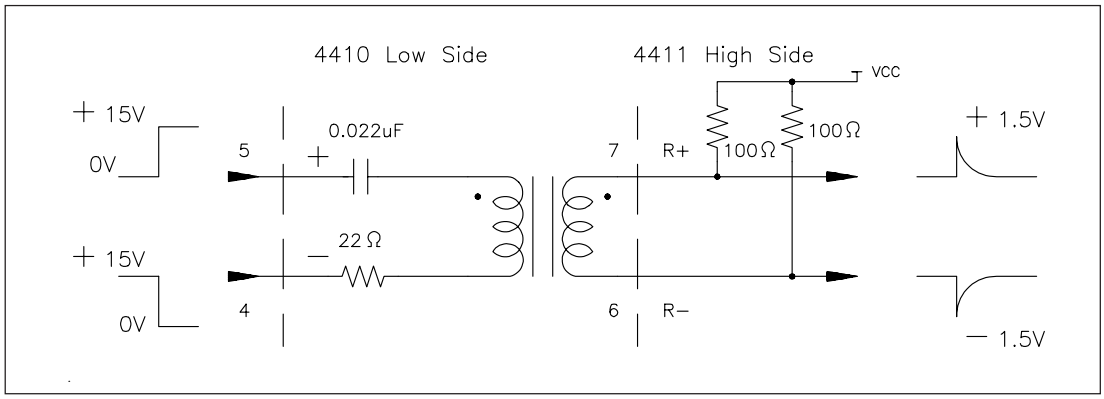


Fig. 12: Transmitter/Receiver Waveforms

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