THE DATASHEET OF

IS61C25616AL-10TLI

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IS61C25616AL IS61C25616AS
IS64C25616AL IS64C25616AS

256K x 16 HIGH-SPEED CMOS STATIC RAM

MARCH 2020

FEATURES

HIGH SPEED: (IS61/64C25616AL)

- High-speed access time: 10ns, 12 ns
- Low Active Power: 150 mW (typical)
- Low Standby Power: 10 mW (typical) CMOS standby

LOW POWER: (IS61/64C25616AS)

- High-speed access time: 25 ns
- Low Active Power: 75 mW (typical)
- Low Standby Power: 1 mW (typical) CMOS standby

- TTL compatible interface levels
- Single 5V ± 10% power supply
- Fully static operation: no clock or refresh required
- Available in 44-pin SOJ package and 44-pin TSOP (Type II)
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

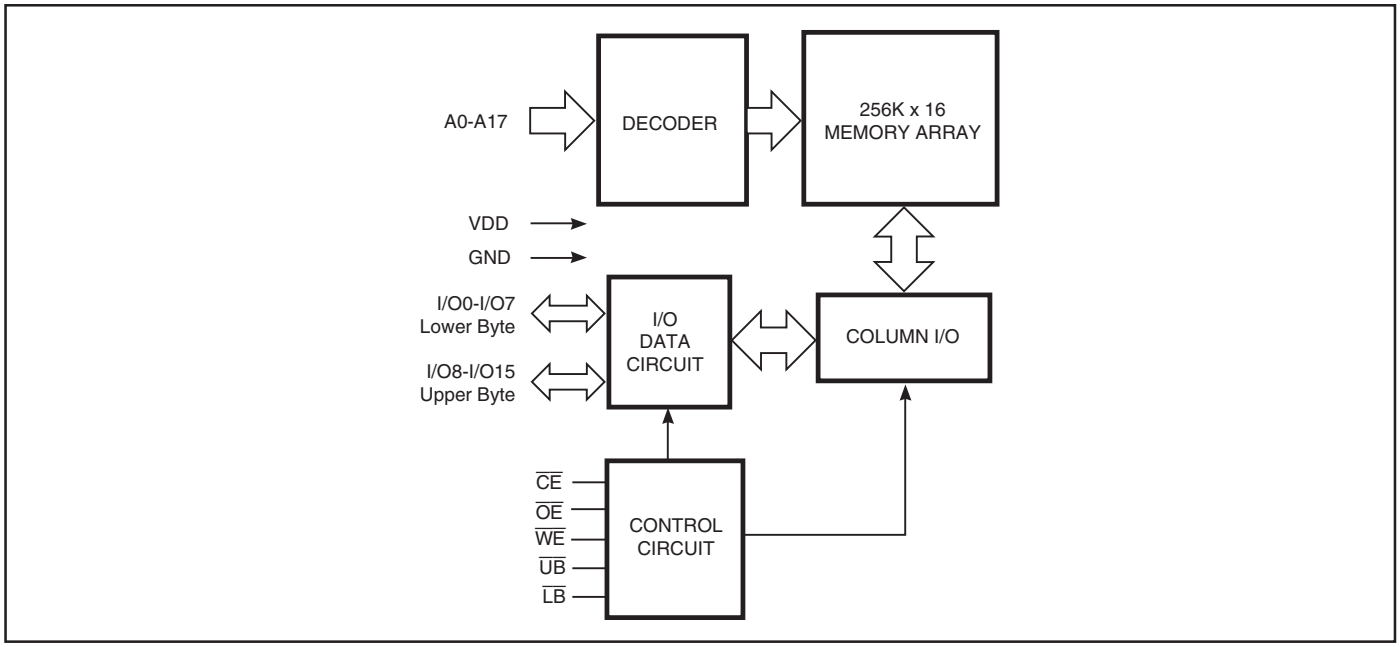
The *ISSI* IS61C25616AL/AS and IS64C25616AL/AS are high-speed, 4,194,304-bit static RAMs organized as 262,144 words by 16 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61C25616AL/AS and IS64C25616AL/AS are packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type II).

FUNCTIONAL BLOCK DIAGRAM



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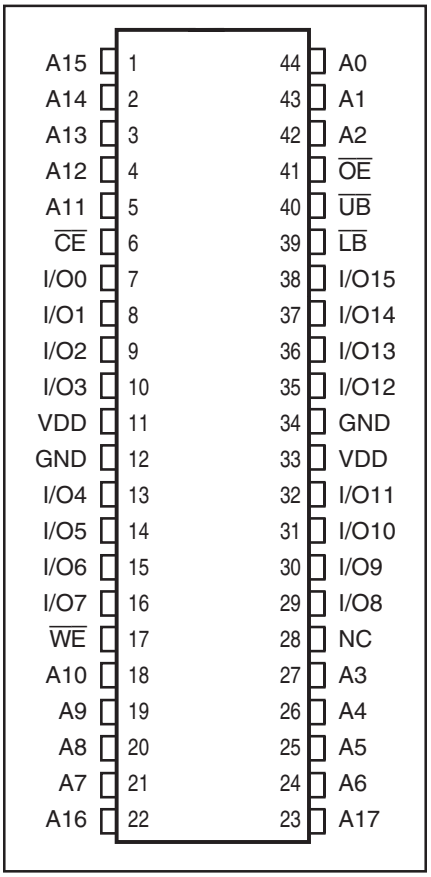
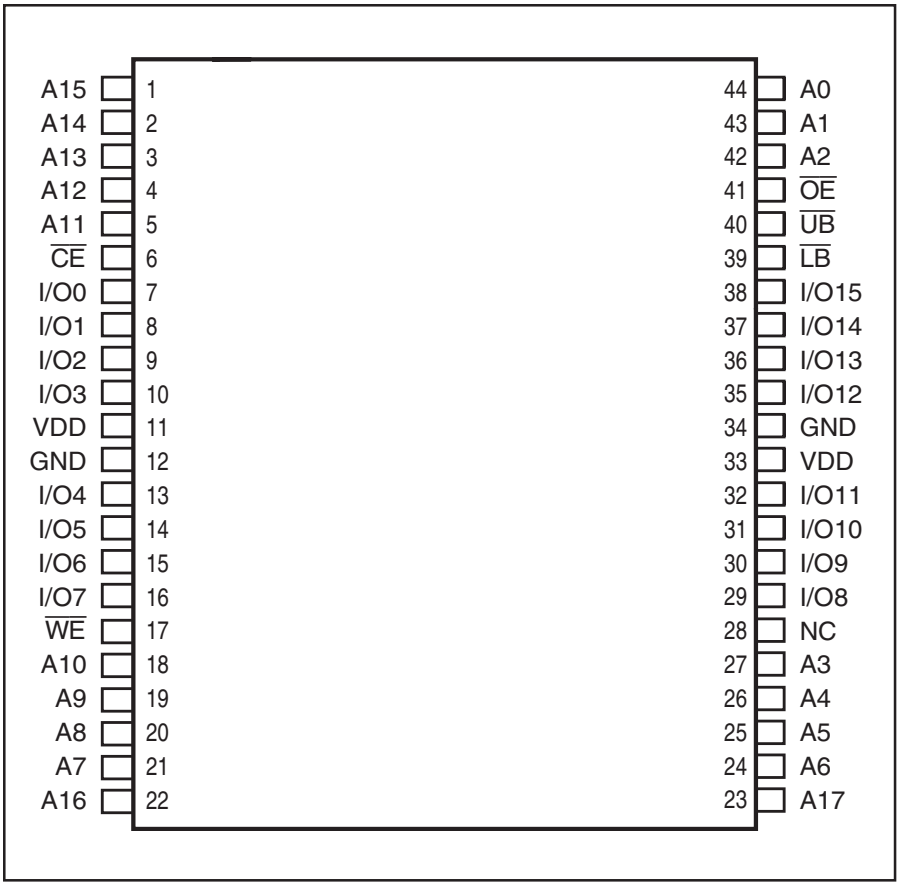
PIN CONFIGURATIONS

44-Pin SOJ



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC1}, I_{CC2}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC1}, I_{CC2}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC1}, I_{CC2}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage(1)			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
			Auto.	–5	5	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}	Com.	–1	1	µA
		Outputs Disabled	Ind.	–2	2	
			Auto.	–5	5	

Note: 1. V_{IL} = –3.0V for pulse width less than 10 ns.

OPERATING RANGE: HIGH SPEED OPTION (IS61/64C25616AL)

Range	Ambient Temperature	V_{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	10
Industrial	-40°C to +85°C	5V ± 10%	10
Automotive	-40°C to +125°C	5V ± 10%	12

OPERATING RANGE: LOW POWER OPTION (IS61/64C25616AS)

Range	Ambient Temperature	V_{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	25
Industrial	-40°C to +85°C	5V ± 10%	25
Automotive	-40°C to +125°C	5V ± 10%	25

HIGH SPEED OPTION (IS61/64C25616AL)

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0$ mA, f = 0	Com. Ind. Auto.	— — —	45 50 55	— — —	45 50 55	mA
I_{CC2}	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0$ mA, f = f_{MAX}	Com. Ind. Auto. typ.[2]	— — — 30	50 55 70	— — — 25	45 50 60	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	$V_{DD} = V_{DD\ MAX.}$, $V_{IN} = V_{IH}$ or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com. Ind. Auto.	— — —	15 20 30	— — —	15 20 30	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} \leq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com. Ind. Auto. typ.[2]	— — — 2	8 12 20	— — —	8 12 20	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

LOW POWER OPTION (IS61/64C25616AS)

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 ns Min.	-25 ns Max.	Unit
I_{CC}	Average operating Current	$\overline{CE} = V_{IL}$, V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com. Ind. Auto.	— — —	10 15 20	mA
I_{CC1}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE} = V_{IL}$ I_{OUT} = 0 mA, f = f_{MAX} $V_{IN} = V_{IH}$ or V_{IL}	Com. Ind. Auto. typ.[2]	— — — 15	25 30 40	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} \geq V_{IH}$, f = 0	Com. Ind. Auto.	— — —	1 1.5 2	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$, f = 0	Com. Ind. Auto. typ.[2]	— — — 0.2	0.8 0.9 2	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-25 Min.	-25 Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	25	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	6	—	15	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	5	0	6	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	2	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	5	0	6	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	2	—	2	—	2	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	5	—	6	—	25	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	5	0	6	0	8	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

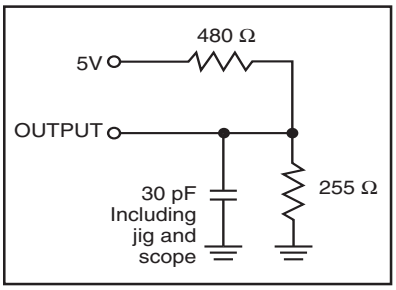


Figure 1

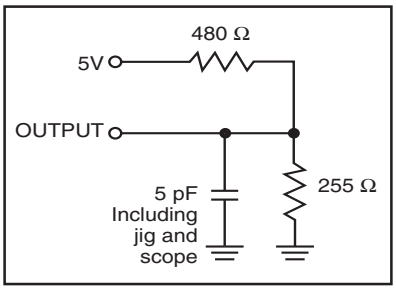
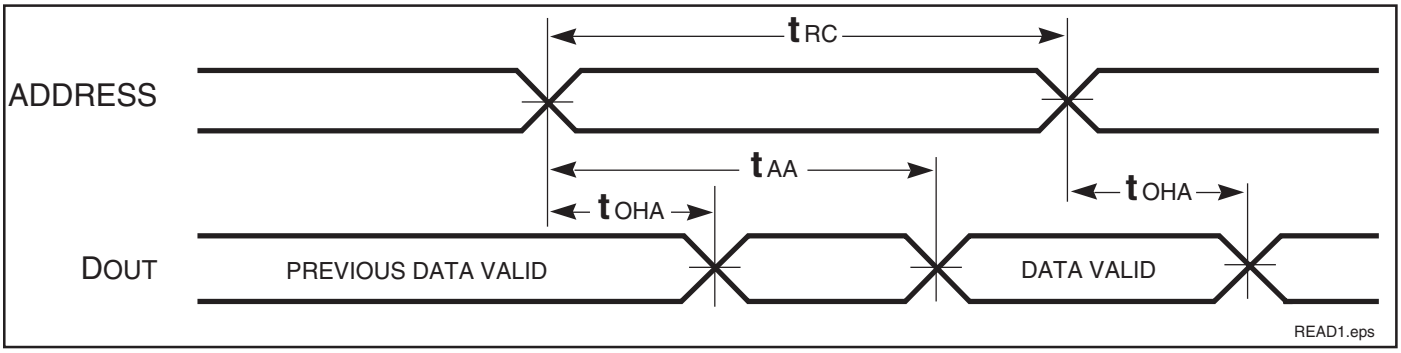


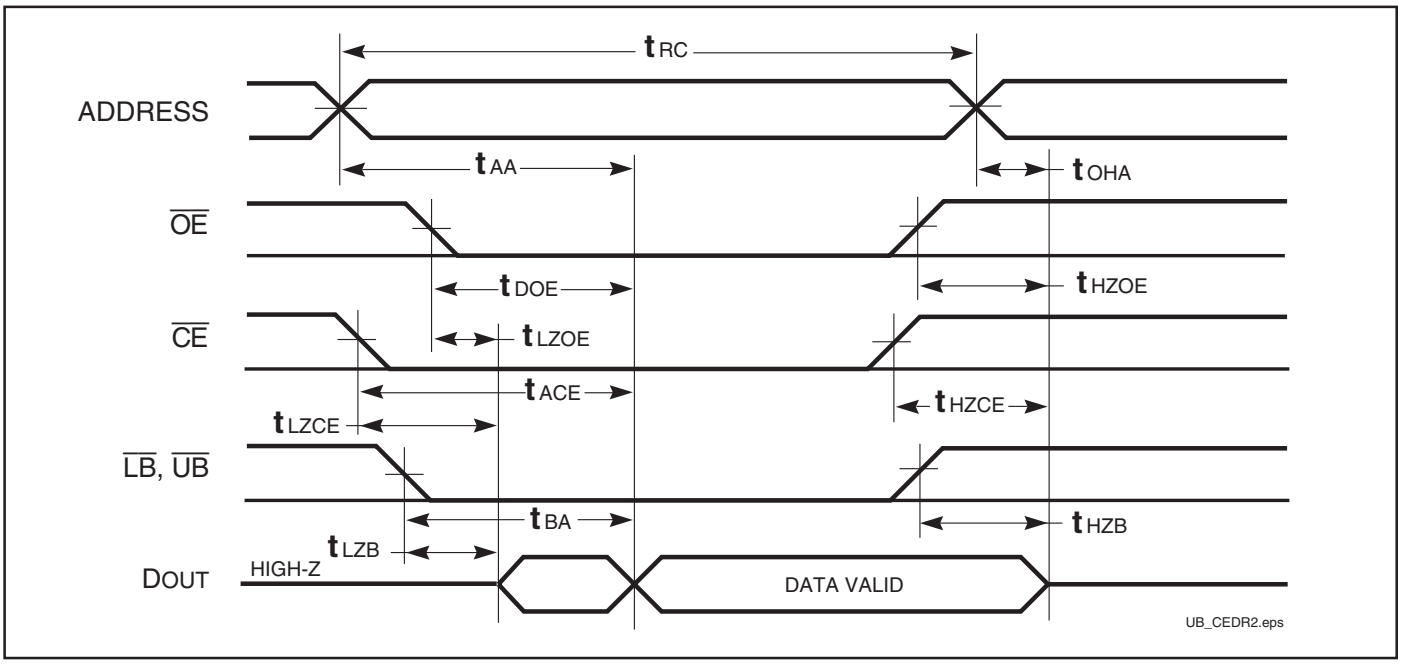
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

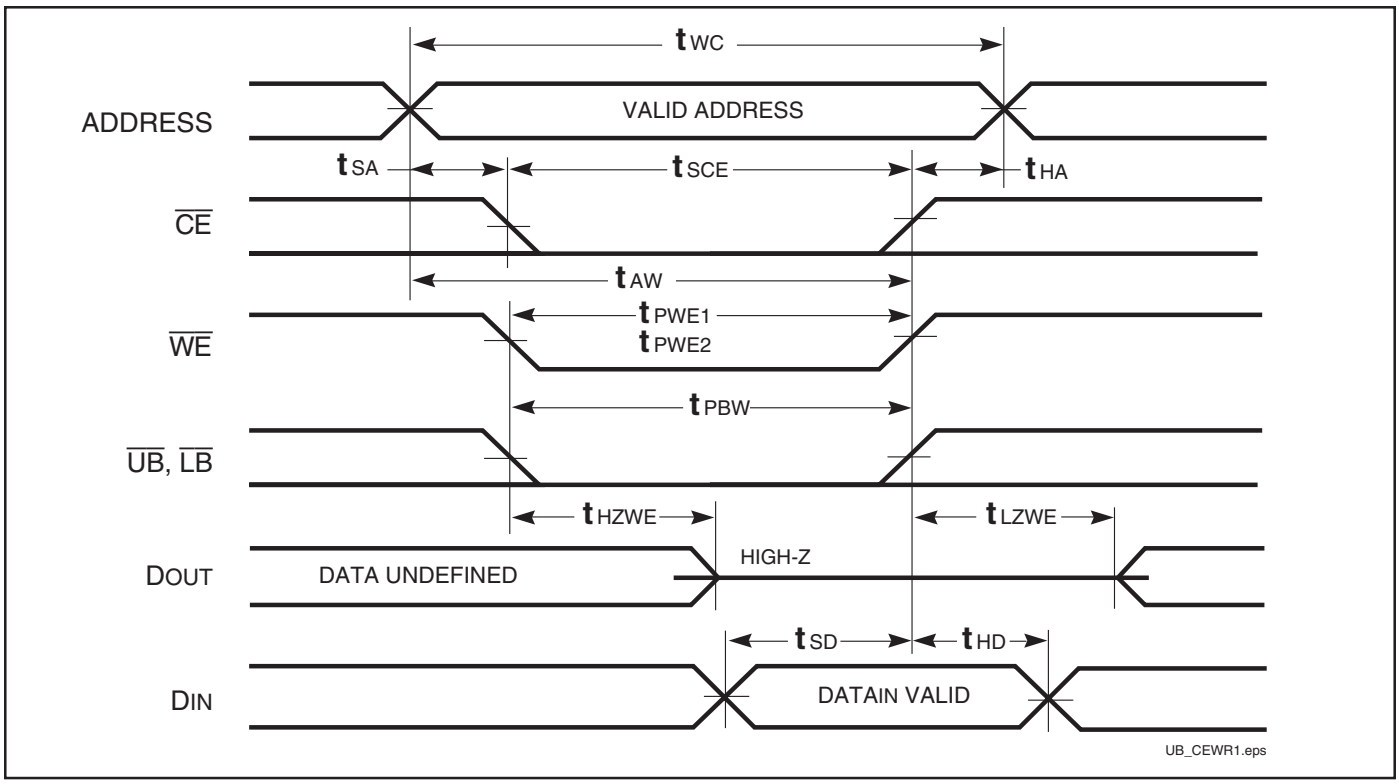
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-25 Min.	-25 Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	25	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	9	—	18	—	ns
t_{AW}	Address Setup Time to Write End	7	—	9	—	18	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	7	—	9	—	18	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	7	—	9	—	15	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$=Low)	7	—	9	—	17	—	ns
t_{SD}	Data Setup to Write End	6	—	6	—	15	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	15	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	5	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

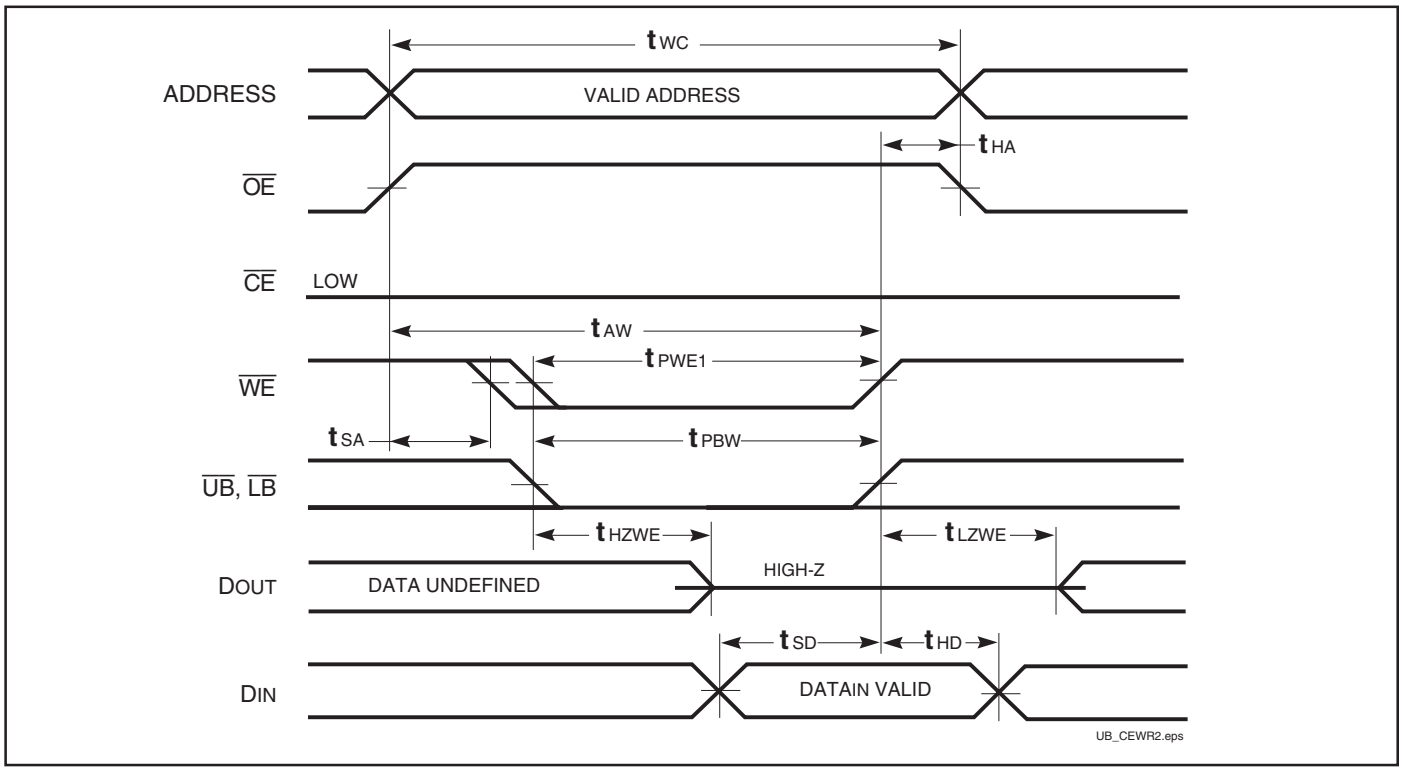
AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)(1,2)

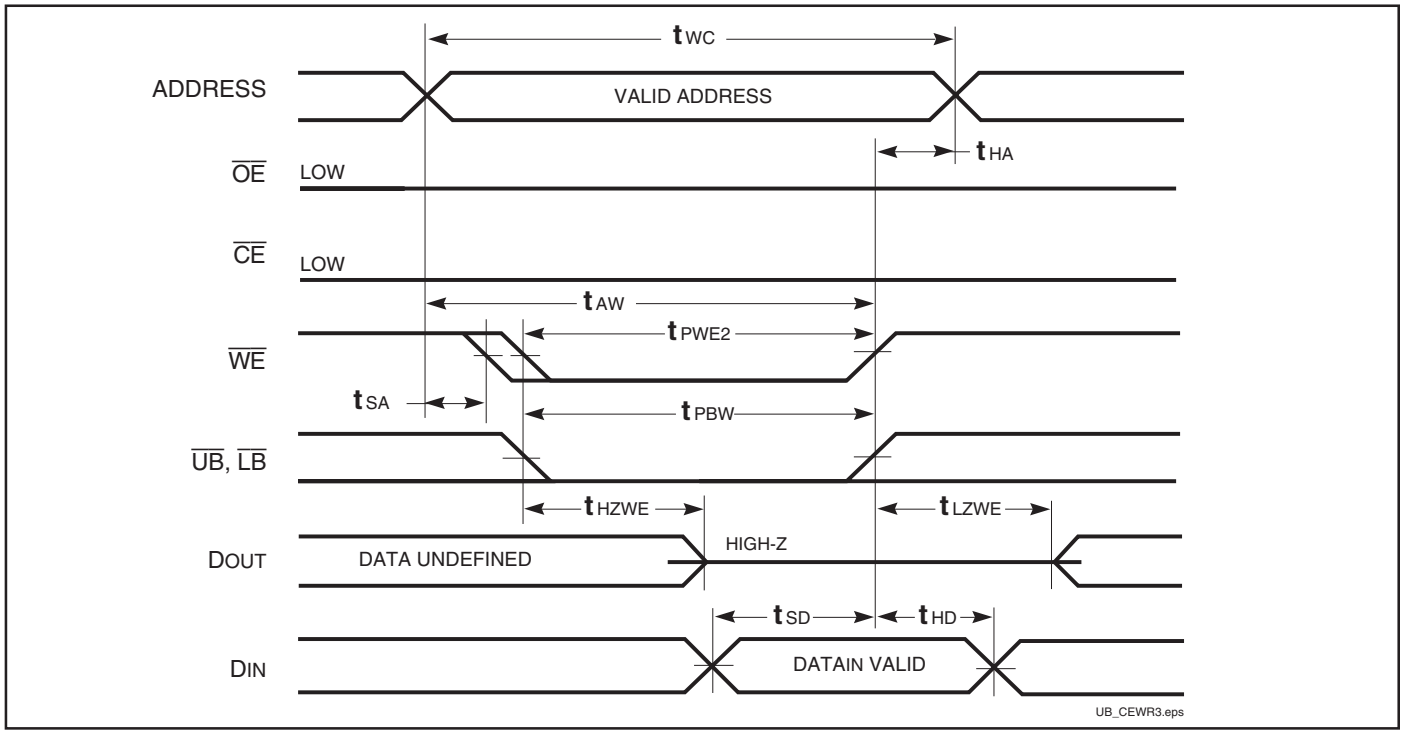


Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



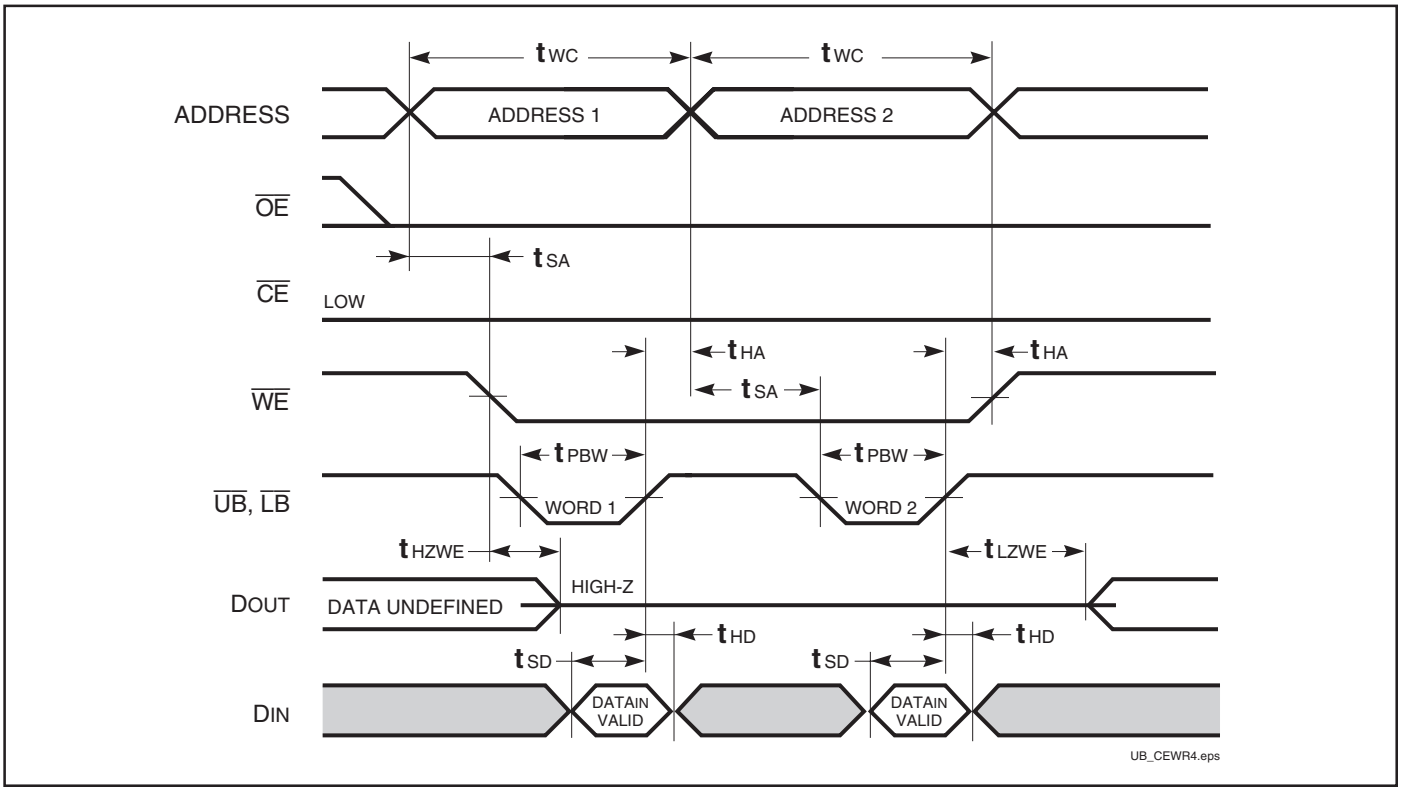
WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Back to Back Write)



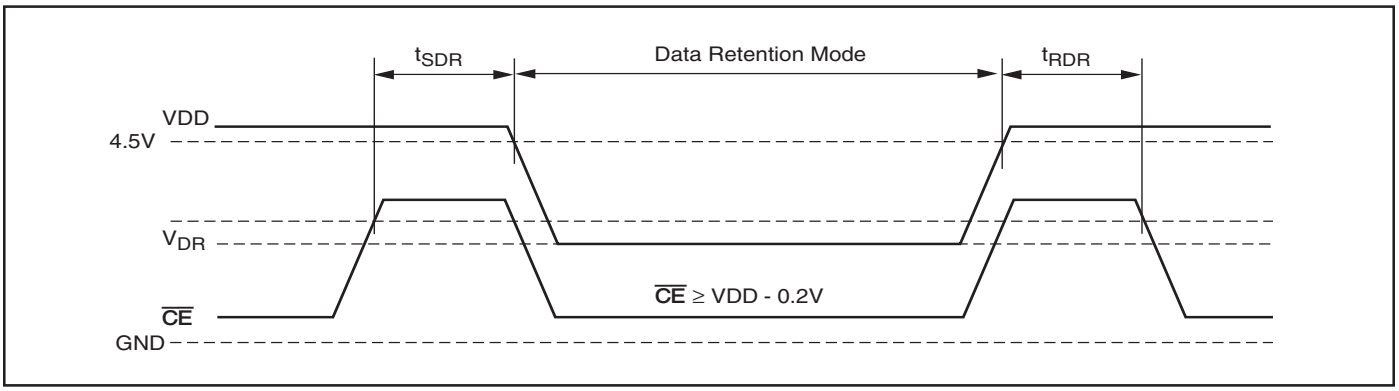
DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61/64C25616AL)

Symbol	Parameter	Test Condition		Min.		Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.9		5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.9V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—		8	mA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—		10	
			Auto.	—		15	
			typ. (1)		1		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

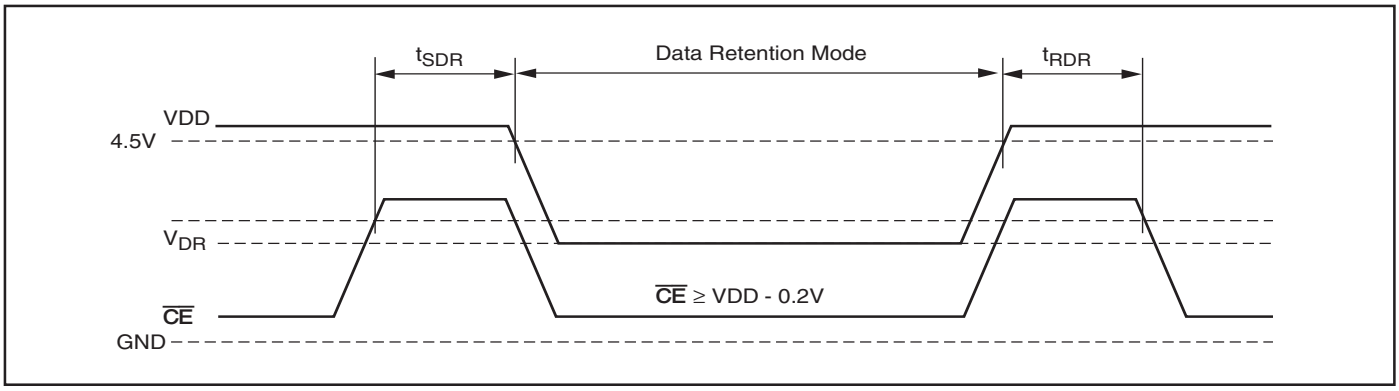


DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61/64C25616AS)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.9	5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.9V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	0.8	mA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	0.9	
			Auto.	—	2	
			typ. (1)	0.2		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:
1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



HIGH SPEED

ORDERING INFORMATION: IS61/64C25616AL

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IS61C25616AL-10TL	44-pin TSOP-II, Lead-free

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61C25616AL-10KLI	400-mil Plastic SOJ, Lead-free
	IS61C25616AL-10TLI	44-pin TSOP-II, Lead-free

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
12	IS64C25616AL-12CTLA3	44-pin TSOP-II, Lead-free, Copper Leadframe

LOW POWER

ORDERING INFORMATION: IS61C25616AS

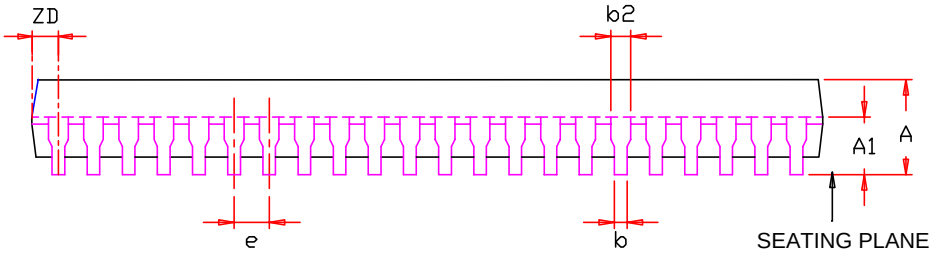
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
25	IS61C25616AS-25KLI	400-mil Plastic SOJ, Lead-free
	IS61C25616AS-25TLI	44-pin TSOP-II, Lead-free

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
25	IS64C25616AS-25TLA3	44-pin TSOP-II, Lead-free

SYMBOL	
A	
A1	
A3	
b	
b2	
D	
E	
E1	
E2	
e	
ZD	



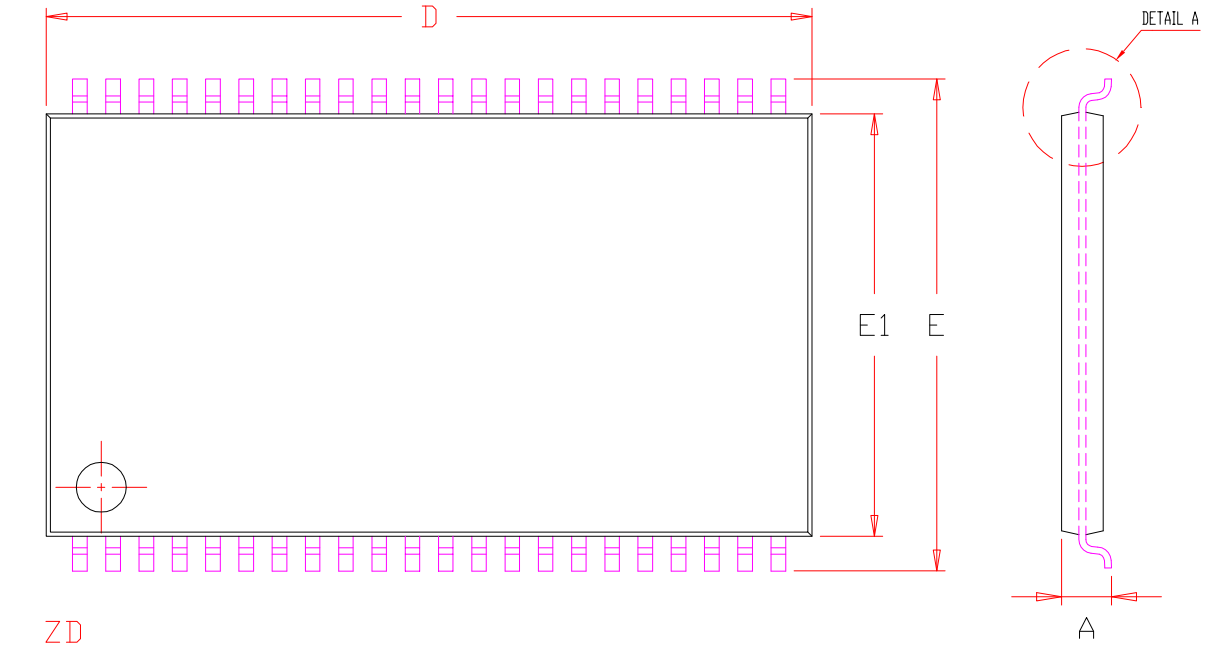
NOTE :

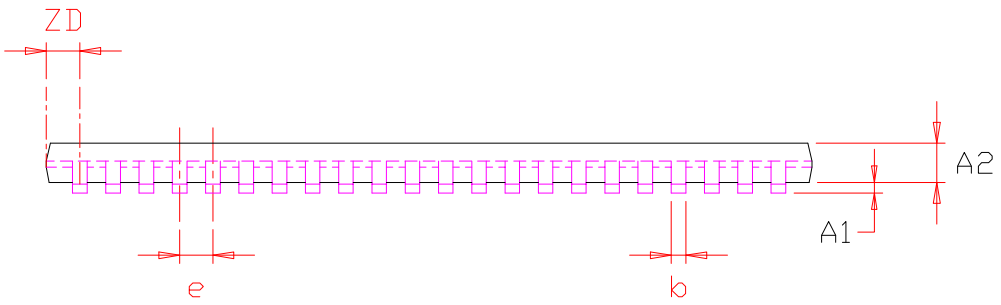
1. Controlling dimension : mm
2. Dimension D and E1 do not include m
3. Dimension b2 does not include damba
4. Formed leads shall be planar with resp
   at the seating plane after final test.
5. Reference document : JEDEC SPEC

ISSI

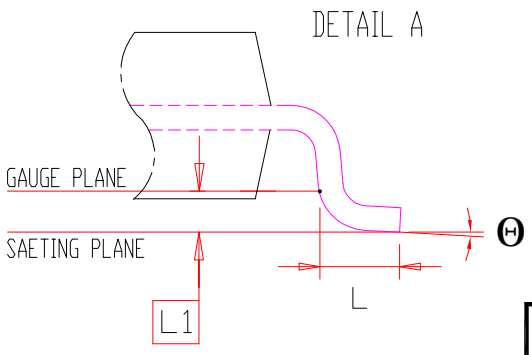
TITLE

44L 400mil SOJ
Package Outline





SYMBOL	DIMENSION I	
	MIN.	NOM.
A	1.00	
A1	0.05	
A2	0.95	1.00
b	0.30	
D	18.28	18.41
E	11.56	11.76
E1	10.03	10.16
e	0.80 BS	
L	0.40	
L1	0.25 BS	
ZD	0.805 R	
Θ	0	



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PR
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROT

ISSI	TITLE	44L 400mil TSOP-2 Package Outline	REV.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

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- ISSI, Integrated Silicon Solution Inc Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management