



THIS SPEC IS OBSOLETE

Spec No: 38-05353

Spec Title: CY7C1460AV33/CY7C1462AV33, 36-MBIT (1M X 36/2M X 18) PIPELINED SRAM WITH NOBL(TM) ARCHITECTURE

Replaced by: None

36-Mbit (1M × 36/2M × 18) Pipelined SRAM with NoBL™ Architecture

Features

- Pin compatible and functionally equivalent to ZBT
- Supports 250 MHz bus operations with zero wait states
 - Available speed grades are 250, 200 and 167 MHz
- Internally self timed output buffer control to eliminate the need to use asynchronous OE
- Fully registered (inputs and outputs) for pipelined operation
- Byte write capability
- 3.3 V power supply
- 3.3 V/2.5 V I/O power supply
- Fast clock-to-output times
 - 2.6 ns (for 250 MHz device)
- Clock enable ($\overline{\text{CEN}}$) pin to suspend operation
- Synchronous self timed writes
- CY7C1460AV33 available in JEDEC-standard Pb-free 100-pin TQFP and non Pb-free 165-ball FBGA package. CY7C1462AV33 available in JEDEC-standard Pb-free 100-pin TQFP.
- IEEE 1149.1 JTAG-compatible boundary scan
- Burst capability – linear or interleaved burst order
- “ZZ” sleep mode option and stop clock option

Functional Description

The CY7C1460AV33/CY7C1462AV33 are 3.3 V, 1M × 36/2M × 18 synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read/write operations with no wait states. The CY7C1460AV33/CY7C1462AV33 are equipped with the advanced (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write/read transitions. The CY7C1460AV33/CY7C1462AV33 are pin compatible and functionally equivalent to ZBT devices.

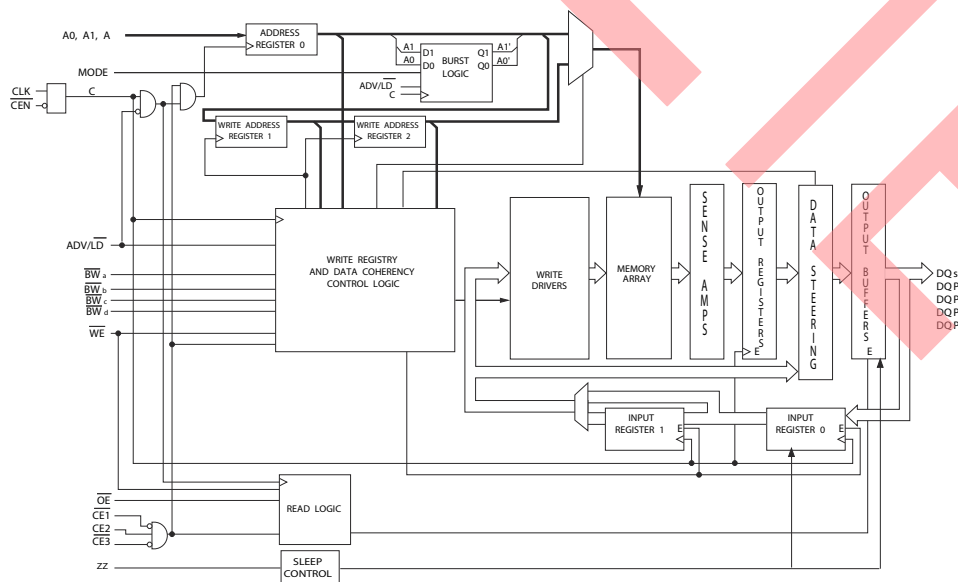
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable (CEN) signal, which when deasserted suspends operation and extends the previous clock cycle.

Write operations are controlled by the byte write selects (BW_a – BW_d for CY7C1460AV33 and BW_a – BW_b for CY7C1462AV33) and a write enable (WE) input. All writes are conducted with on-chip synchronous self timed write circuitry.

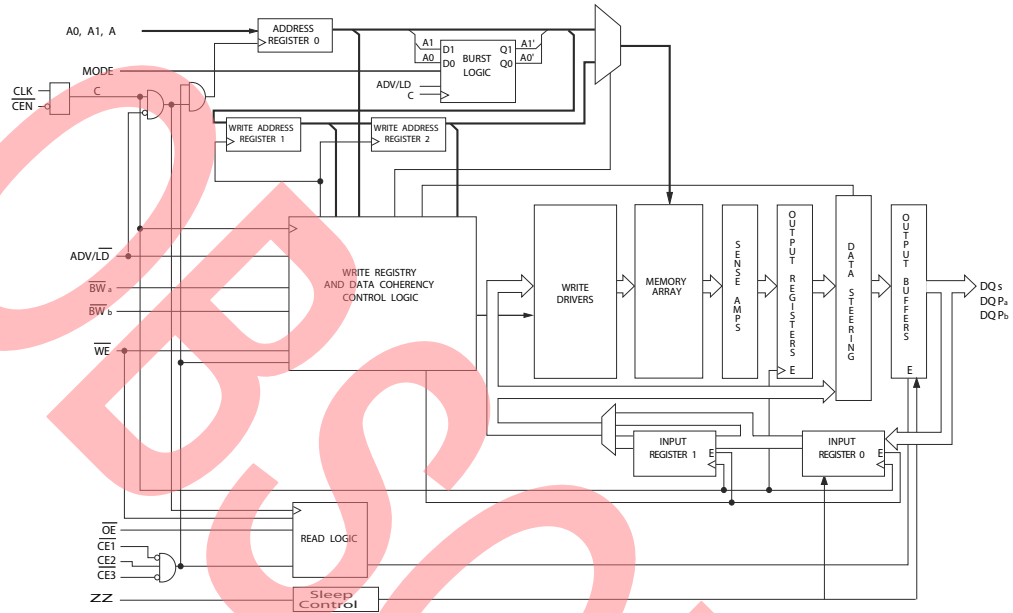
Three synchronous chip enables ($\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, $\overline{\text{CE}}_3$) and an asynchronous output enable (OE) provide for easy bank selection and output tristate control. To avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

For a complete list of related documentation, click [here](#).

Logic Block Diagram – CY7C1460AV33



Logic Block Diagram – CY7C1462AV33



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Pin Configurations (continued)

Figure 2. 165-ball FBGA (15 × 17 × 1.40 mm) pinout

CY7C1460AV33 (1M × 36)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|----------|------------------|-----------------|-------------------|-------------------|-------------------|-------------------|------------------|-----------------|------------------|-----------------|------------------|
| A | NC/576M | A | \overline{CE}_1 | \overline{BW}_c | \overline{BW}_b | \overline{CE}_3 | \overline{CEN} | ADV/LD | A | A | NC |
| B | NC/1G | A | CE_2 | \overline{BW}_d | \overline{BW}_a | CLK | \overline{WE} | \overline{OE} | A | A | NC |
| C | DQP _c | NC | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | DQP _b |
| D | DQ _c | DQ _c | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _b | DQ _b |
| E | DQ _c | DQ _c | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _b | DQ _b |
| F | DQ _c | DQ _c | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _b | DQ _b |
| G | DQ _c | DQ _c | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _b | DQ _b |
| H | NC | NC | NC | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | NC | NC | ZZ |
| J | DQ _d | DQ _d | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | DQ _a |
| K | DQ _d | DQ _d | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | DQ _a |
| L | DQ _d | DQ _d | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | DQ _a |
| M | DQ _d | DQ _d | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | DQ _a |
| N | DQP _d | NC | V _{DDQ} | V _{SS} | NC | NC | NC | V _{SS} | V _{DDQ} | NC | DQP _a |
| P | NC/144M | NC/72M | A | A | TDI | A1 | TDO | A | A | A | NC/288M |
| R | MODE | A | A | A | TMS | A0 | TCK | A | A | A | A |

Pin Definitions

| Pin Name | I/O Type | Pin Description |
|--|--------------------------------|---|
| A ₀ , A ₁ , A | Input-synchronous | Address inputs used to select one of the address locations. Sampled at the rising edge of the CLK. |
| \overline{BW}_a , \overline{BW}_b , \overline{BW}_c , \overline{BW}_d , \overline{BW}_e , \overline{BW}_f , \overline{BW}_g , \overline{BW}_h | Input-synchronous | Byte write select inputs, active LOW. Qualified with \overline{WE} to conduct writes to the SRAM. Sampled on the rising edge of CLK. \overline{BW}_a controls DQ _a and DQP _a , \overline{BW}_b controls DQ _b and DQP _b , \overline{BW}_c controls DQ _c and DQP _c , \overline{BW}_d controls DQ _d and DQP _d , \overline{BW}_e controls DQ _e and DQP _e , \overline{BW}_f controls DQ _f and DQP _f , \overline{BW}_g controls DQ _g and DQP _g , \overline{BW}_h controls DQ _h and DQP _h . |
| \overline{WE} | Input-synchronous | Write enable input, active LOW. Sampled on the rising edge of CLK if \overline{CEN} is active LOW. This signal must be asserted LOW to initiate a write sequence. |
| $\overline{ADV/LD}$ | Input-synchronous | Advance/load input used to advance the on-chip address counter or load a new address. When HIGH (and \overline{CEN} is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, $\overline{ADV/LD}$ should be driven LOW to load a new address. |
| CLK | Input-clock | Clock input. Used to capture all synchronous inputs to the device. CLK is qualified with \overline{CEN} . CLK is only recognized if \overline{CEN} is active LOW. |
| \overline{CE}_1 | Input-synchronous | Chip enable 1 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 and \overline{CE}_3 to select/deselect the device. |
| \overline{CE}_2 | Input-synchronous | Chip enable 2 input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select/deselect the device. |
| \overline{CE}_3 | Input-synchronous | Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select/deselect the device. |
| \overline{OE} | Input-asynchronous | Output enable, active LOW. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. \overline{OE} is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected. |
| \overline{CEN} | Input-synchronous | Clock enable input, active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting \overline{CEN} does not deselect the device, \overline{CEN} can be used to extend the previous cycle when required. |
| DQ _a , DQ _b , DQ _c , DQ _d , DQ _e , DQ _f , DQ _g , DQ _h | I/O-synchronous | Bidirectional data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A _X during the previous clock rise of the read cycle. The direction of the pins is controlled by \overline{OE} and the internal control logic. When \overline{OE} is asserted LOW, the pins can behave as outputs. When HIGH, DQ _a –DQ _d are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of \overline{OE} . |
| DQP _a , DQP _b , DQP _c , DQP _d , DQP _e , DQP _f , DQP _g , DQP _h | I/O-synchronous | Bidirectional data parity I/O lines. Functionally, these signals are identical to DQ _[31:0] . During write sequences, DQP _a is controlled by \overline{BW}_a , DQP _b is controlled by \overline{BW}_b , DQP _c is controlled by \overline{BW}_c , and DQP _d is controlled by \overline{BW}_d , DQP _e is controlled by \overline{BW}_e , DQP _f is controlled by \overline{BW}_f , DQP _g is controlled by \overline{BW}_g , DQP _h is controlled by \overline{BW}_h . |
| MODE | Input strap pin | Mode input. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE defaults HIGH, to an interleaved burst order. |
| TDO | JTAG serial output synchronous | Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK. |
| TDI | JTAG serial input synchronous | Serial data-in to the JTAG circuit. Sampled on the rising edge of TCK. |

Pin Definitions *(continued)*

| Pin Name | I/O Type | Pin Description |
|------------------|------------------------------|---|
| TMS | Test mode select synchronous | This pin controls the test access port state machine. Sampled on the rising edge of TCK. |
| TCK | JTAG-clock | Clock input to the JTAG circuitry. |
| V _{DD} | Power supply | Power supply inputs to the core of the device. |
| V _{DDQ} | I/O power supply | Power supply for the I/O circuitry. |
| V _{SS} | Ground | Ground for the device. Should be connected to ground of the system. |
| NC | N/A | No connects. This pin is not connected to the die. |
| NC/72M | N/A | Not connected to the die. Can be tied to any voltage level. |
| NC/144M | N/A | Not connected to the die. Can be tied to any voltage level. |
| NC/288M | N/A | Not connected to the die. Can be tied to any voltage level. |
| NC/576M | N/A | Not connected to the die. Can be tied to any voltage level. |
| NC/1G | N/A | Not connected to the die. Can be tied to any voltage level. |
| ZZ | Input-asynchronous | ZZ “sleep” input. This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved. During normal operation, this pin can be connected to V _{SS} or left floating. ZZ pin has an internal pull-down. |

Functional Overview

The CY7C1460AV33/CY7C1462AV33 are synchronous-pipelined burst NoBL SRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.6 ns (250 MHz device).

Accesses can be initiated by asserting all three chip enables (CE₁, CE₂, CE₃) active at the rising edge of the clock. If clock enable (CEN) is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable (WE). BW_[x] can be used to conduct byte write operations.

Write operations are qualified by the write enable (WE). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables (CE₁, CE₂, CE₃) and an asynchronous output enable (OE) simplify depth expansion. All operations (reads, writes, and deselections) are pipelined. ADV/LD should be driven LOW after the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE₁, CE₂, and CE₃ are all asserted active, (3) the write enable input signal WE is deasserted HIGH, and (4) ADV/LD is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in

progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.6 ns (250 MHz device) provided OE is active LOW. After the first clock of the read access the output buffers are controlled by OE and the internal control logic. OE must be driven LOW for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tristates following the next clock rise.

Burst Read Accesses

The CY7C1460AV33/CY7C1462AV33 have an on-chip burst counter that enables the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW in order to load a new address into the SRAM, as described in the section [Single Read Accesses](#) earlier. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enables inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE₁, CE₂, and CE₃ are all asserted active, and (3) the write signal WE is asserted LOW. The address presented to the address inputs is

loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically tristated regardless of the state of the OE input signal. This enables the external logic to present the data on DQ and DQP (DQ_{a,b,c,d}/DQP_{a,b,c,d} for CY7C1460AV33 and DQ_{a,b}/DQP_{a,b} for CY7C1462AV33). In addition, the address for the subsequent access (read/write/deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP (DQ_{a,b,c,d}/DQP_{a,b,c,d} for CY7C1460AV33 and DQ_{a,b}/DQP_{a,b} for CY7C1462AV33) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by BW (BW_{a,b,c,d} for CY7C1460AV33 and BW_{a,b} for CY7C1462AV33) signals. The CY7C1460AV33/CY7C1462AV33 provides byte write capability that is described in the Write Cycle Description table. Asserting the write enable input (WE) with the selected byte write select (BW) input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1460AV33/CY7C1462AV33 are common I/O devices, data should not be driven into the device while the outputs are active. The output enable (OE) can be deasserted HIGH before presenting data to the DQ and DQP (DQ_{a,b,c,d}/DQP_{a,b,c,d} for CY7C1460AV33 and DQ_{a,b}/DQP_{a,b} for CY7C1462AV33) inputs. Doing so tristates the output drivers. As a safety precaution, DQ and DQP (DQ_{a,b,c,d}/DQP_{a,b,c,d} for CY7C1460AV33 and DQ_{a,b}/DQP_{a,b} for CY7C1462AV33) are automatically tristated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CY7C1460AV33/CY7C1462AV33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in the section [Single Write Accesses](#)

on page 7 earlier. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables (CE₁, CE₂, and CE₃) and WE inputs are ignored and the burst counter is incremented. The correct BW (BW_{a,b,c,d} for CY7C1460AV33 and BW_{a,b} for CY7C1462AV33) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE₁, CE₂, and CE₃, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

| First Address A1, A0 | Second Address A1, A0 | Third Address A1, A0 | Fourth Address A1, A0 |
|----------------------|-----------------------|----------------------|-----------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

Linear Burst Address Table

(MODE = GND)

| First Address A1, A0 | Second Address A1, A0 | Third Address A1, A0 | Fourth Address A1, A0 |
|----------------------|-----------------------|----------------------|-----------------------|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--------------------|-----------------------------------|------------------------------|-------------------|-------------------|------|
| I _{DDZZ} | Sleep mode standby current | ZZ ≥ V _{DD} - 0.2 V | – | 100 | mA |
| t _{ZZS} | Device operation to ZZ | ZZ ≥ V _{DD} - 0.2 V | – | 2t _{CYC} | ns |
| t _{ZZREC} | ZZ recovery time | ZZ ≤ 0.2 V | 2t _{CYC} | – | ns |
| t _{ZZI} | ZZ active to sleep current | This parameter is sampled | – | 2t _{CYC} | ns |
| t _{RZZI} | ZZ inactive to exit sleep current | This parameter is sampled | 0 | – | ns |

Truth Table

The Truth Table for CY7C1460AV33/CY7C1462AV33 follows. [1, 2, 3, 4, 5, 6, 7]

| Operation | Address Used | \overline{CE} | ZZ | ADV/LD | \overline{WE} | \overline{BW}_x | \overline{OE} | CEN | CLK | DQ |
|-------------------------------|--------------|-----------------|----|--------|-----------------|-------------------|-----------------|-----|-----|--------------|
| Deselect cycle | None | H | L | L | X | X | X | L | L-H | Tri-state |
| Continue deselect cycle | None | X | L | H | X | X | X | L | L-H | Tri-state |
| Read cycle (begin burst) | External | L | L | L | H | X | L | L | L-H | Data out (Q) |
| Read cycle (continue burst) | Next | X | L | H | X | X | L | L | L-H | Data out (Q) |
| NOP/dummy read (begin burst) | External | L | L | L | H | X | H | L | L-H | Tri-state |
| Dummy read (continue burst) | Next | X | L | H | X | X | H | L | L-H | Tri-state |
| Write cycle (begin burst) | External | L | L | L | L | L | X | L | L-H | Data in (D) |
| Write cycle (continue burst) | Next | X | L | H | X | L | X | L | L-H | Data in (D) |
| NOP/WRITE ABORT (begin burst) | None | L | L | L | L | H | X | L | L-H | Tri-state |
| WRITE ABORT (continue burst) | Next | X | L | H | X | H | X | L | L-H | Tri-state |
| IGNORE CLOCK EDGE (stall) | Current | X | L | X | X | X | X | H | L-H | - |
| SLEEP MODE | None | X | H | X | X | X | X | X | X | Tri-state |

Notes

1. X = "Don't Care", H = Logic HIGH, L = Logic LOW, \overline{CE} stands for all chip enables active. $\overline{BW}_x = L$ signifies at least one byte write select is active, $\overline{BW}_x = \text{valid}$ signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by \overline{WE} and \overline{BW}_x . See Write Cycle Description table for details.
3. When a write cycle is detected, all I/Os are tristated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the \overline{OE} signal.
5. CEN = H inserts wait states.
6. Device powers up deselected and the I/Os in a tristate condition, regardless of \overline{OE} .
7. \overline{OE} is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ_s and $DQP_x = \text{Tristate}$ when \overline{OE} is inactive or when the device is deselected, and $DQ_s = \text{data}$ when \overline{OE} is active.

Partial Write Cycle Description

The Partial Write Cycle Description for CY7C1460AV33 follows. [8, 9, 10, 11]

| Function (CY7C1460AV33) | \overline{WE} | \overline{BW}_d | \overline{BW}_c | \overline{BW}_b | \overline{BW}_a |
|--|-----------------|-------------------|-------------------|-------------------|-------------------|
| Read | H | X | X | X | X |
| Write – no bytes written | L | H | H | H | H |
| Write byte a – (DQ _a and DQP _a) | L | H | H | H | L |
| Write byte b – (DQ _b and DQP _b) | L | H | H | L | H |
| Write bytes b, a | L | H | H | L | L |
| Write byte c – (DQ _c and DQP _c) | L | H | L | H | H |
| Write bytes c, a | L | H | L | H | L |
| Write bytes c, b | L | H | LL | L | H |
| Write bytes c, b, a | L | H | L | L | L |
| Write byte d – (DQ _d and DQP _d) | L | L | H | H | H |
| Write bytes d, a | L | L | H | H | L |
| Write bytes d, b | L | L | H | L | H |
| Write bytes d, b, a | L | L | H | L | L |
| Write bytes d, c | L | L | L | H | H |
| Write bytes d, c, a | L | L | L | H | L |
| Write bytes d, c, b | L | L | L | L | H |
| Write all bytes | L | L | L | L | L |

Partial Write Cycle Description

The Partial Write Cycle Description for CY7C1462AV33 follows. [9, 11]

| Function (CY7C1462AV33) | \overline{WE} | \overline{BW}_b | \overline{BW}_a |
|--|-----------------|-------------------|-------------------|
| Read | H | x | x |
| Write – no bytes written | L | H | H |
| Write byte a – (DQ _a and DQP _a) | L | H | L |
| Write byte b – (DQ _b and DQP _b) | L | L | H |
| Write both bytes | L | L | L |

Notes

8. X = "Don't Care", H = Logic HIGH, L = Logic LOW, \overline{CE} stands for all chip enables active. $\overline{BW}_x = L$ signifies at least one byte write select is active, $\overline{BW}_x = \text{valid}$ signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
9. Write is defined by \overline{WE} and \overline{BW}_x . See Write Cycle Description table for details.
10. When a write cycle is detected, all I/Os are tristated, even during byte writes.
11. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_{[a:d]}$ is valid. Appropriate write is done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1460AV33 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic level.

The CY7C1460AV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the [TAP Controller State Diagram on page 13](#). TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see [Instruction Codes on page 17](#)). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the

instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the [TAP Controller Block Diagram on page 14](#). Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The length of the boundary scan register for the SRAM in different packages is listed in the [Scan Register Sizes](#) table.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The [Boundary Scan Order on page 18](#) and show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the [Identification Register Definitions on page 17](#).

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the [Instruction Codes](#) table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions described in detail are as follows.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the

instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a high Z state until the next command is given during the "Update IR" state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

EXTEST OUTPUT BUS TRISTATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

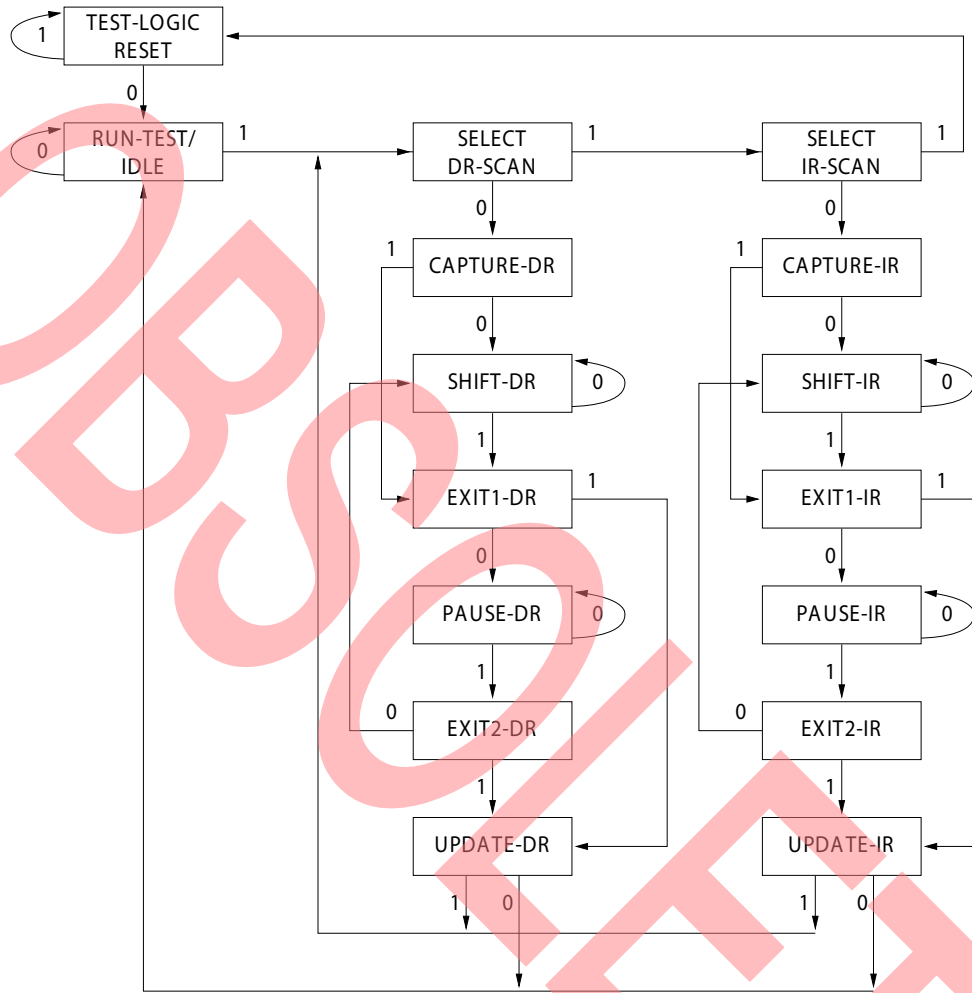
The boundary scan register has a special bit located at bit #89 (for 165-ball FBGA package) or bit #138 (for 209-ball FBGA package). When this scan cell, called the "extest output bus tristate," is latched into the preload register during the "Update-DR" state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the "Shift-DR" state. During "Update-DR," the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the "Test-Logic-Reset" state.

Reserved

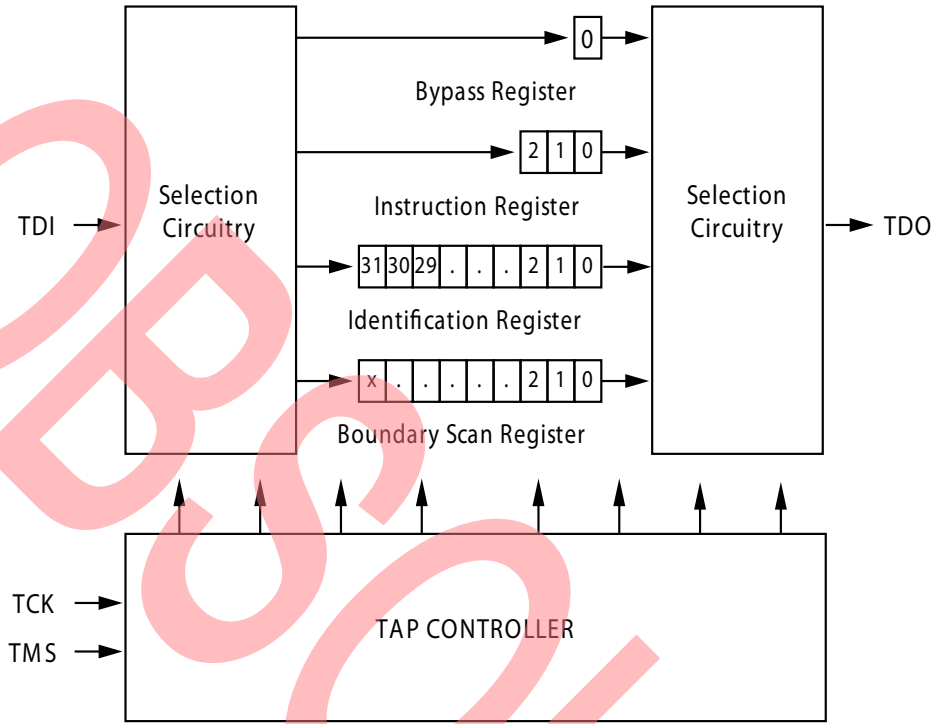
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

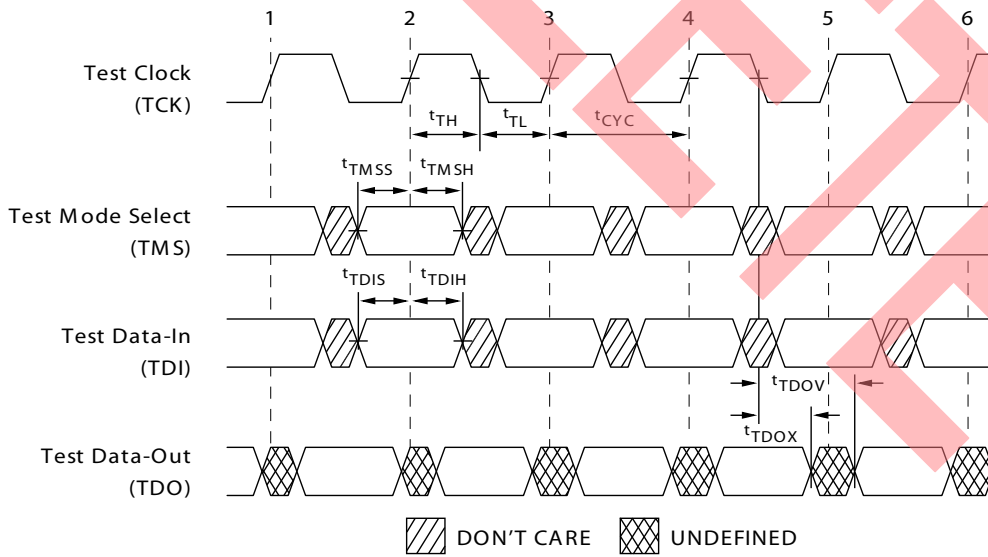


The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing Diagram



TAP AC Switching Characteristics

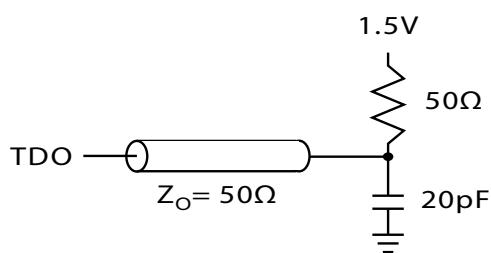
Over the Operating Range

| Parameter ^[12, 13] | Description | Min | Max | Unit |
|-------------------------------|-------------------------------|-----|-----|------|
| Clock | | | | |
| t_{TCYC} | TCK clock cycle time | 50 | – | ns |
| t_{TF} | TCK clock frequency | – | 20 | MHz |
| t_{TH} | TCK clock HIGH time | 20 | – | ns |
| t_{TL} | TCK clock LOW time | 20 | – | ns |
| Output Times | | | | |
| t_{TDOV} | TCK clock LOW to TDO valid | – | 10 | ns |
| t_{TDOX} | TCK clock LOW to TDO invalid | 0 | – | ns |
| Setup Times | | | | |
| t_{TMSS} | TMS setup to TCK clock rise | 5 | – | ns |
| t_{TDIS} | TDI setup to TCK clock rise | 5 | – | ns |
| t_{CS} | Capture setup to TCK rise | 5 | – | ns |
| Hold Times | | | | |
| t_{TMSH} | TMS hold after TCK clock rise | 5 | – | ns |
| t_{TDIH} | TDI hold after clock rise | 5 | – | ns |
| t_{CH} | Capture hold after clock rise | 5 | – | ns |

3.3 V TAP AC Test Conditions

Input pulse levels V_{SS} to 3.3 V
 Input rise and fall times 1 ns
 Input timing reference levels 1.5 V
 Output reference levels 1.5 V
 Test load termination supply voltage 1.5 V

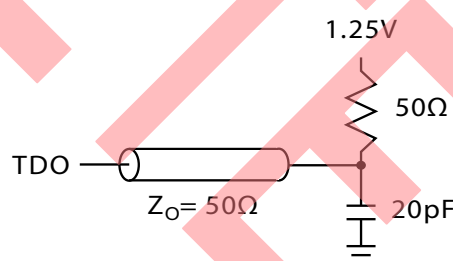
3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Test Conditions

Input pulse levels V_{SS} to 2.5 V
 Input rise and fall time 1 ns
 Input timing reference levels 1.25 V
 Output reference levels 1.25 V
 Test load termination supply voltage 1.25 V

2.5 V TAP AC Output Load Equivalent



Notes

12. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
 13. Test conditions are specified using the load in TAP AC test Conditions. $t_R/t_F = 1$ ns.

TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.135 V to 3.6 V unless otherwise noted)

| Parameter ^[14] | Description | Test Conditions | Min | Max | Unit | |
|---------------------------|---------------------|---|--------------------------|------|-----------------------|---|
| V _{OH1} | Output HIGH voltage | I _{OH} = -4.0 mA, V _{DDQ} = 3.3 V | 2.4 | - | V | |
| | | I _{OH} = -1.0 mA, V _{DDQ} = 2.5 V | 2.0 | - | V | |
| V _{OH2} | Output HIGH voltage | I _{OH} = -100 μA | V _{DDQ} = 3.3 V | 2.9 | - | V |
| | | | V _{DDQ} = 2.5 V | 2.1 | - | V |
| V _{OL1} | Output LOW voltage | I _{OL} = 8.0 mA | V _{DDQ} = 3.3 V | - | 0.4 | V |
| | | I _{OL} = 1.0 mA | V _{DDQ} = 2.5 V | - | 0.4 | V |
| V _{OL2} | Output LOW voltage | I _{OL} = 100 μA | V _{DDQ} = 3.3 V | - | 0.2 | V |
| | | | V _{DDQ} = 2.5 V | - | 0.2 | V |
| V _{IH} | Input HIGH voltage | | V _{DDQ} = 3.3 V | 2.0 | V _{DD} + 0.3 | V |
| | | | V _{DDQ} = 2.5 V | 1.7 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW voltage | | V _{DDQ} = 3.3 V | -0.3 | 0.8 | V |
| | | | V _{DDQ} = 2.5 V | -0.3 | 0.7 | V |
| I _X | Input load current | GND ≤ V _{IN} ≤ V _{DDQ} | -5 | 5 | μA | |

Note

14. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

| Instruction Field | CY7C1460AV33 (1M × 36) | Description |
|--------------------------------------|---------------------------|--|
| Revision number (31:29) | 000 | Describes the version number. |
| Device depth (28:24) ^[15] | 01011 | Reserved for internal use |
| Architecture/memory type(23:18) | 001000 | Defines memory type and architecture |
| Bus width/density(17:12) | 100111 | Defines width and density |
| Cypress JEDEC ID code (11:1) | 00000110100 | Allows unique identification of SRAM vendor. |
| ID register presence indicator (0) | 1 | Indicates the presence of an ID register. |

Scan Register Sizes

| Register Name | Bit Size (× 36) |
|---|-----------------|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary scan order (165-ball FBGA package) | 89 |

Instruction Codes

| Instruction | Code | Description |
|----------------|------|--|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operations. |

Note

15. Bit #24 is "1" in the ID Register Definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Order

165-ball FBGA ^[16]

CY7C1460AV33 (1M × 36)

| Bit# | Ball ID | Bit# | Ball ID | Bit# | Ball ID | Bit# | Ball ID |
|------|---------|------|---------|------|---------|------|----------|
| 1 | N6 | 26 | E11 | 51 | A3 | 76 | N1 |
| 2 | N7 | 27 | D11 | 52 | A2 | 77 | N2 |
| 3 | 10N | 28 | G10 | 53 | B2 | 78 | P1 |
| 4 | P11 | 29 | F10 | 54 | C2 | 79 | R1 |
| 5 | P8 | 30 | E10 | 55 | B1 | 80 | R2 |
| 6 | R8 | 31 | D10 | 56 | A1 | 81 | P3 |
| 7 | R9 | 32 | C11 | 57 | C1 | 82 | R3 |
| 8 | P9 | 33 | A11 | 58 | D1 | 83 | P2 |
| 9 | P10 | 34 | B11 | 59 | E1 | 84 | R4 |
| 10 | R10 | 35 | A10 | 60 | F1 | 85 | P4 |
| 11 | R11 | 36 | B10 | 61 | G1 | 86 | N5 |
| 12 | H11 | 37 | A9 | 62 | D2 | 87 | P6 |
| 13 | N11 | 38 | B9 | 63 | E2 | 88 | R6 |
| 14 | M11 | 39 | C10 | 64 | F2 | 89 | Internal |
| 15 | L11 | 40 | A8 | 65 | G2 | | |
| 16 | K11 | 41 | B8 | 66 | H1 | | |
| 17 | J11 | 42 | A7 | 67 | H3 | | |
| 18 | M10 | 43 | B7 | 68 | J1 | | |
| 19 | L10 | 44 | B6 | 69 | K1 | | |
| 20 | K10 | 45 | A6 | 70 | L1 | | |
| 21 | J10 | 46 | B5 | 71 | M1 | | |
| 22 | H9 | 47 | A5 | 72 | J2 | | |
| 23 | H10 | 48 | A4 | 73 | K2 | | |
| 24 | G11 | 49 | B4 | 74 | L2 | | |
| 25 | F11 | 50 | B3 | 75 | M2 | | |

Note
16. Bit# 89 is preset HIGH.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| | |
|---|------------------------------------|
| Storage temperature | -65 °C to +150 °C |
| Ambient temperature with power applied | -55 °C to +125 °C |
| Supply voltage on V _{DD} relative to GND | -0.5 V to +4.6 V |
| Supply voltage on V _{DDQ} relative to GND | -0.5 V to +V _{DD} |
| DC to outputs in tri-state | -0.5 V to V _{DDQ} + 0.5 V |
| DC input voltage | -0.5 V to V _{DD} + 0.5 V |
| Current into outputs (LOW) | 20 mA |
| Static discharge voltage (per MIL-STD-883, method 3015) | > 2001 V |
| Latch-up current | > 200 mA |

Operating Range

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|--------------------|-------------------------------|
| Commercial | 0 °C to +70 °C | 3.3 V – 5% / + 10% | 2.5 V – 5% to V _{DD} |
| Industrial | -40 °C to +85 °C | | |

Neutron Soft Error Immunity

| Parameter | Description | Test Conditions | Typ | Max* | Unit |
|-----------|---------------------------|-----------------|-----|------|---------|
| LSBU | Logical single bit upsets | 25 °C | 361 | 394 | FIT/Mb |
| LMBU | Logical multi bit upsets | 25 °C | 0 | 0.01 | FIT/Mb |
| SEL | Single event latch-up | 85 °C | 0 | 0.1 | FIT/Dev |

* No LMBU or SEL events occurred during testing; this column represents a statistical χ^2 , 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Electrical Characteristics

Over the Operating Range

| Parameter ^[17, 18] | Description | Test Conditions | Min | Max | Unit |
|-------------------------------|--|---|-------|-------------------------|------|
| V _{DD} | Power supply voltage | | 3.135 | 3.6 | V |
| V _{DDQ} | I/O supply voltage | for 3.3 V I/O | 3.135 | V _{DD} | V |
| | | for 2.5 V I/O | 2.375 | 2.625 | V |
| V _{OH} | Output HIGH voltage | for 3.3 V I/O, I _{OH} = -4.0 mA | 2.4 | - | V |
| | | for 2.5 V I/O, I _{OH} = -1.0 mA | 2.0 | - | V |
| V _{OL} | Output LOW voltage | for 3.3 V I/O, I _{OL} = 8.0 mA | - | 0.4 | V |
| | | for 2.5 V I/O, I _{OL} = 1.0 mA | - | 0.4 | V |
| V _{IH} | Input HIGH voltage ^[17] | for 3.3 V I/O | 2.0 | V _{DD} + 0.3 V | V |
| | | for 2.5 V I/O | 1.7 | V _{DD} + 0.3 V | V |
| V _{IL} | Input LOW voltage ^[17] | for 3.3 V I/O | -0.3 | 0.8 | V |
| | | for 2.5 V I/O | -0.3 | 0.7 | V |
| I _X | Input leakage current except ZZ and MODE | GND ≤ V _I ≤ V _{DDQ} | -5 | 5 | μA |
| | Input current of MODE | Input = V _{SS} | -30 | - | μA |
| | | Input = V _{DD} | - | 5 | μA |
| | Input current of ZZ | Input = V _{SS} | -5 | - | μA |
| Input = V _{DD} | | - | 30 | μA | |
| I _{OZ} | Output leakage current | GND ≤ V _I ≤ V _{DDQ} , output disabled | -5 | 5 | μA |

Notes

17. Overshoot: V_{IH(AC)} < V_{DD} + 1.5 V (Pulse width less than t_{CYC/2}), undershoot: V_{IL(AC)} > -2 V (Pulse width less than t_{CYC/2}).
18. T_{power up}: Assumes a linear ramp from 0 V to V_{DD(Min)} within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter ^[17, 18] | Description | Test Conditions | Min | Max | Unit | |
|-------------------------------|---|---|------------------------|-----|------|----|
| I _{DD} | V _{DD} operating supply | V _{DD} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{CYC} | 4 ns cycle, 250 MHz | – | 475 | mA |
| | | | 5 ns cycle, 200 MHz | – | 425 | mA |
| | | | 6 ns cycle, 167 MHz | – | 375 | mA |
| I _{SB1} | Automatic CE power-down current – TTL inputs | Max V _{DD} , device deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} = 1/t _{CYC} | All speed grades | – | 225 | mA |
| I _{SB2} | Automatic CE power-down current – CMOS inputs | Max V _{DD} , device deselected, V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{DDQ} – 0.3 V, f = 0 | All speed grades | – | 120 | mA |
| I _{SB3} | Automatic CE power-down current – CMOS inputs | Max V _{DD} , device deselected, V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{DDQ} – 0.3 V, f = f _{MAX} = 1/t _{CYC} | All speed grades | – | 200 | mA |
| I _{SB4} | Automatic CE power-down current – TTL inputs | Max V _{DD} , device deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = 0 | All speed grades | – | 135 | mA |

Capacitance

| Parameter ^[19] | Description | Test Conditions | 100-pin TQFP Max | 165-ball FBGA Max | Unit |
|---------------------------|--------------------------|---|------------------|-------------------|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{DD} = 2.5 V, V _{DDQ} = 2.5 V | 6.5 | 7 | pF |
| C _{CLK} | Clock input capacitance | | 3 | 7 | pF |
| C _{I/O} | Input/output capacitance | | 5.5 | 6 | pF |

Thermal Resistance

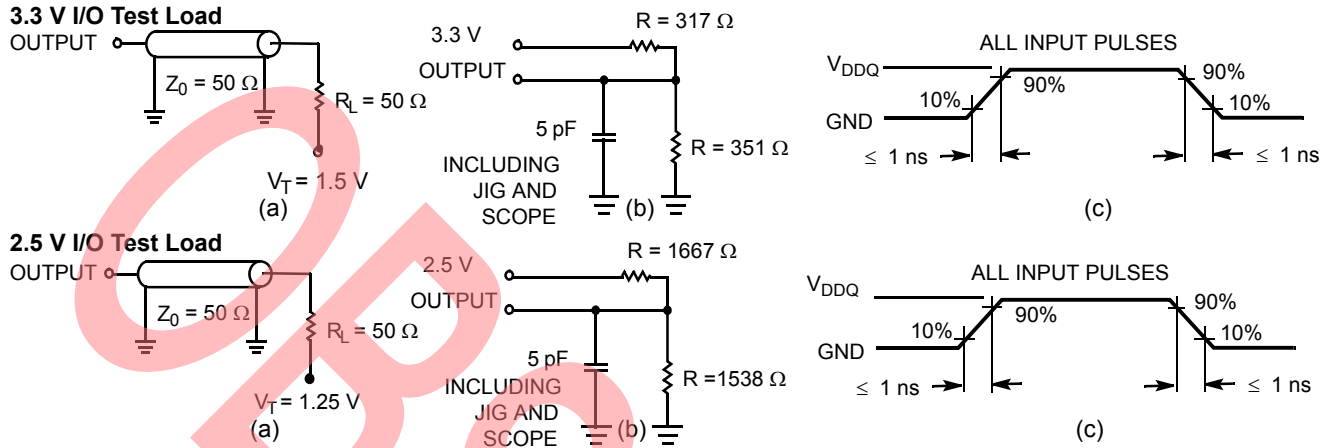
| Parameter ^[19] | Description | Test Conditions | 100-pin TQFP Package | 165-ball FBGA Package | Unit |
|---------------------------|--|--|----------------------|-----------------------|------|
| Θ _{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 25.21 | 20.8 | °C/W |
| Θ _{JC} | Thermal resistance (junction to case) | | 2.28 | 3.2 | °C/W |

Note

19. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range

| Parameter ^[20, 21] | Description | -250 | | -200 | | -167 | | Unit |
|-------------------------------|---|------|-----|------|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| t_{Power} ^[22] | $V_{CC}(\text{typical})$ to the first access read or write | 1 | – | 1 | – | 1 | – | ms |
| Clock | | | | | | | | |
| t_{CYC} | Clock cycle time | 4.0 | – | 5.0 | – | 6.0 | – | ns |
| F_{MAX} | Maximum operating frequency | – | 250 | – | 200 | – | 167 | MHz |
| t_{CH} | Clock HIGH | 1.5 | – | 2.0 | – | 2.4 | – | ns |
| t_{CL} | Clock LOW | 1.5 | – | 2.0 | – | 2.4 | – | ns |
| Output Times | | | | | | | | |
| t_{CO} | Data output valid after CLK rise | – | 2.6 | – | 3.2 | – | 3.4 | ns |
| t_{EOV} | \overline{OE} LOW to output valid | – | 2.6 | – | 3.0 | – | 3.4 | ns |
| t_{DOH} | Data output hold after CLK rise | 1.0 | – | 1.5 | – | 1.5 | – | ns |
| t_{CHZ} | Clock to high Z ^[23, 24, 25] | – | 2.6 | – | 3.0 | – | 3.4 | ns |
| t_{CLZ} | Clock to low Z ^[23, 24, 25] | 1.0 | – | 1.3 | – | 1.5 | – | ns |
| t_{EOHZ} | \overline{OE} HIGH to output high Z ^[23, 24, 25] | – | 2.6 | – | 3.0 | – | 3.4 | ns |
| t_{EOLZ} | \overline{OE} LOW to output low Z ^[23, 24, 25] | 0 | – | 0 | – | 0 | – | ns |
| Setup Times | | | | | | | | |
| t_{AS} | Address setup before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| t_{DS} | Data input setup before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| t_{CENS} | \overline{CEN} setup before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| t_{WES} | \overline{WE} , \overline{BW}_x setup before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| t_{ALS} | ADV/LD setup before CLK rise | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| t_{CES} | Chip select setup | 1.2 | – | 1.4 | – | 1.5 | – | ns |
| Hold Times | | | | | | | | |
| t_{AH} | Address hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| t_{DH} | Data input hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| t_{CENH} | \overline{CEN} hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| t_{WEH} | \overline{WE} , \overline{BW}_x hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| t_{ALH} | ADV/LD hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |
| t_{CEH} | Chip select hold after CLK rise | 0.3 | – | 0.4 | – | 0.5 | – | ns |

Notes

20. Timing reference is 1.5 V when $V_{DDQ} = 3.3$ V and is 1.25 V when $V_{DDQ} = 2.5$ V.

21. Test conditions shown in (a) of Figure 3 on page 21 unless otherwise noted.

22. This part has a voltage regulator internally; t_{Power} is the time power needs to be supplied above $V_{DD(\text{minimum})}$ initially, before a Read or Write operation can be initiated.

23. t_{CHZ} , t_{CLZ} , t_{EOLZ} , and t_{EOHZ} are specified with AC test conditions shown in (b) of Figure 3 on page 21. Transition is measured ± 200 mV from steady-state voltage.

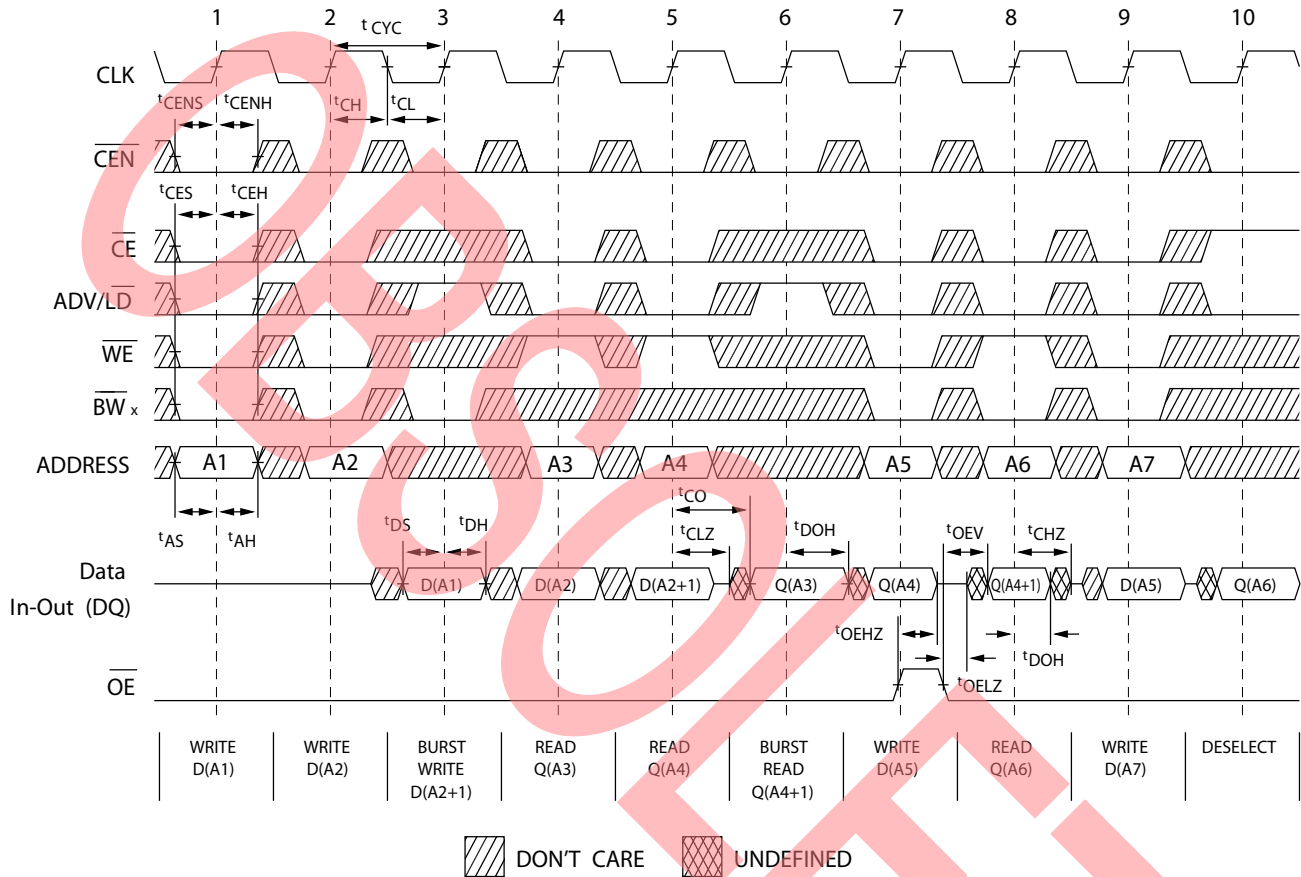
24. At any voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus.

These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

25. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 4. Read/Write/Timing [26, 27, 28]



Notes

26. For this waveform \overline{ZZ} is tied low.

27. When \overline{CE} is LOW, \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH, \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW or \overline{CE}_3 is HIGH.

28. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

Figure 5. NOP, STALL and DESELECT Cycles [29, 30, 31]

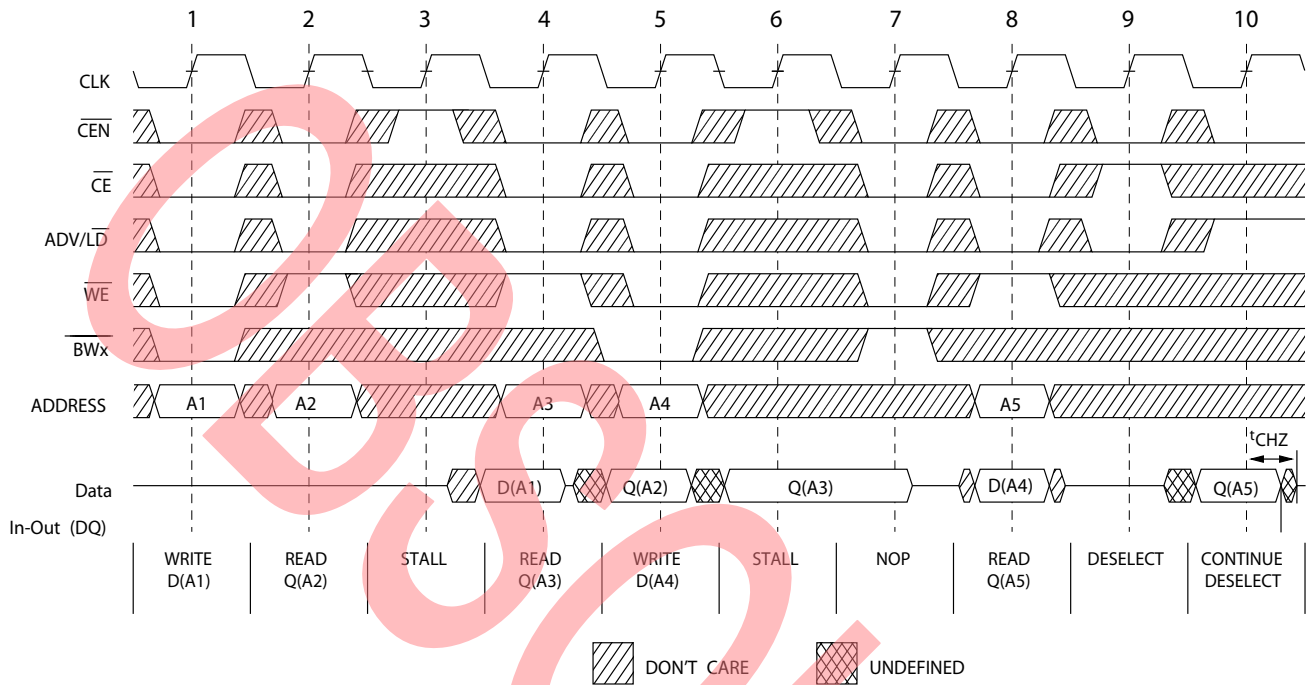
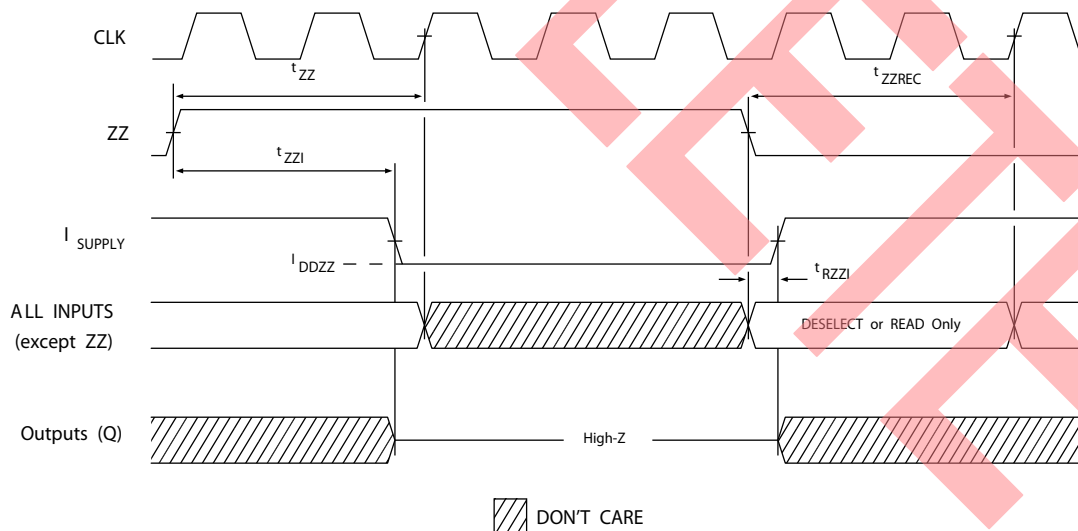


Figure 6. ZZ Mode Timing [32, 33]



Notes

- 29. For this waveform ZZ is tied low.
- 30. When CE is LOW, CE₁ is LOW, CE₂ is HIGH and CE₃ is LOW. When CE is HIGH, CE₁ is HIGH or CE₂ is LOW or CE₃ is HIGH.
- 31. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated CEN being used to create a pause. A write is not performed during this cycle.
- 32. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
- 33. I/Os are in high Z when exiting ZZ sleep mode.

Ordering Information

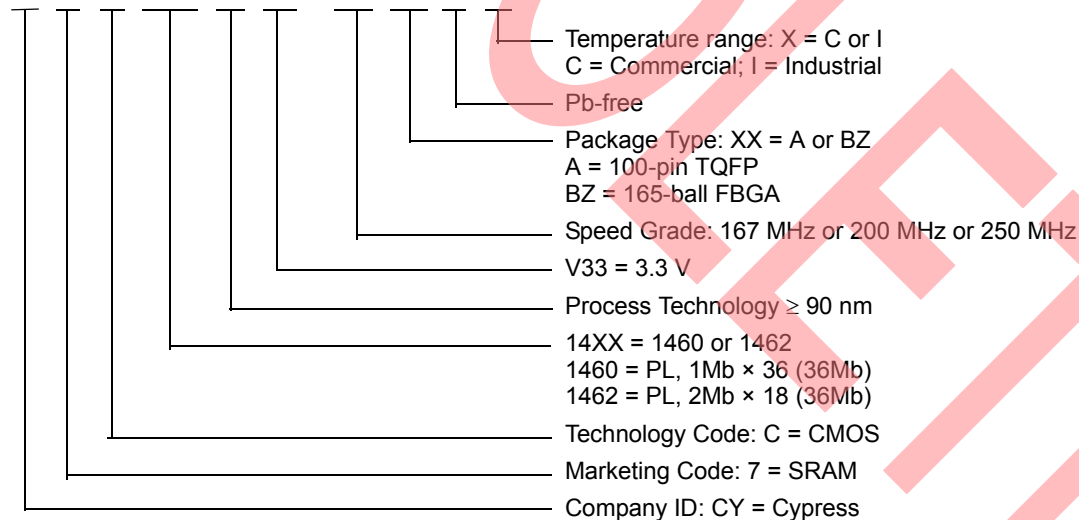
The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>

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| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|-------------|---------------------|-----------------|---|-----------------|
| 167 | CY7C1460AV33-167AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| | CY7C1462AV33-167AXC | | | |
| | CY7C1460AV33-167BZC | 51-85195 | 165-ball FBGA (15 × 17 × 1.4 mm) | Industrial |
| | CY7C1460AV33-167AXI | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | |
| 200 | CY7C1460AV33-200AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| | CY7C1462AV33-200AXI | | | Industrial |
| 250 | CY7C1460AV33-250AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| | CY7C1460AV33-250AXI | | | Industrial |

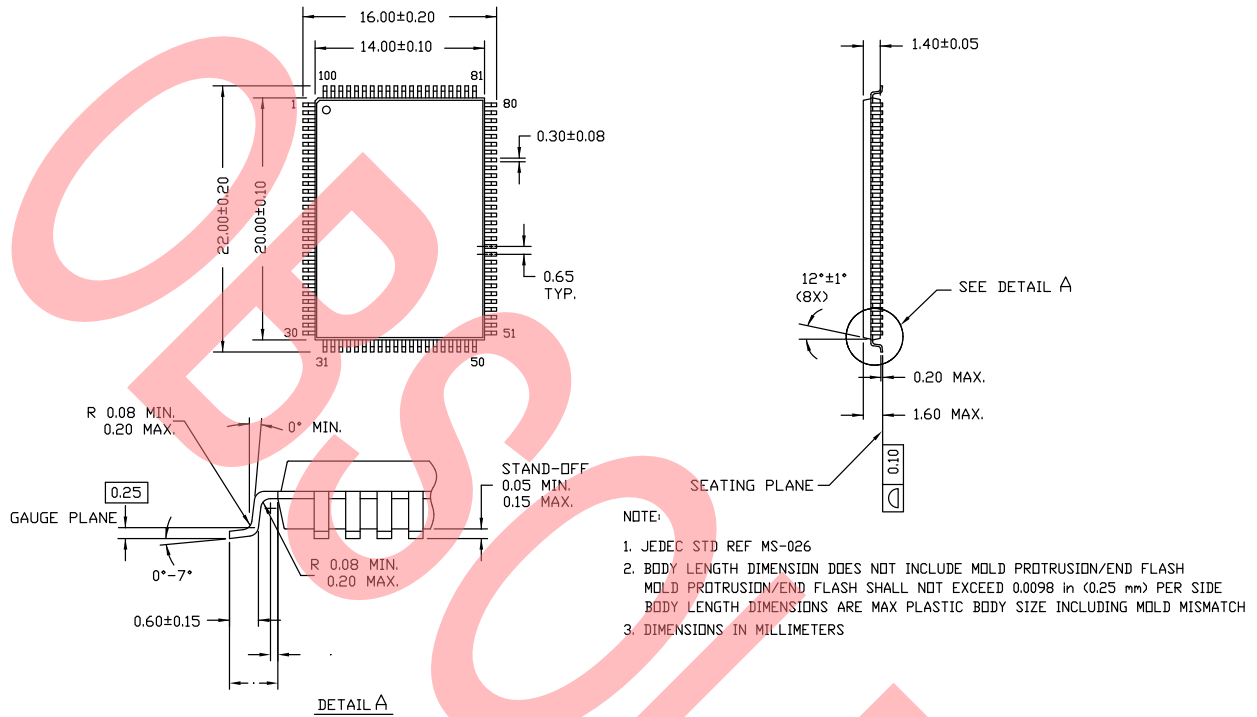
Ordering Code Definitions

CY 7 C 14XX A V33 - 167 XX X X



Package Diagrams

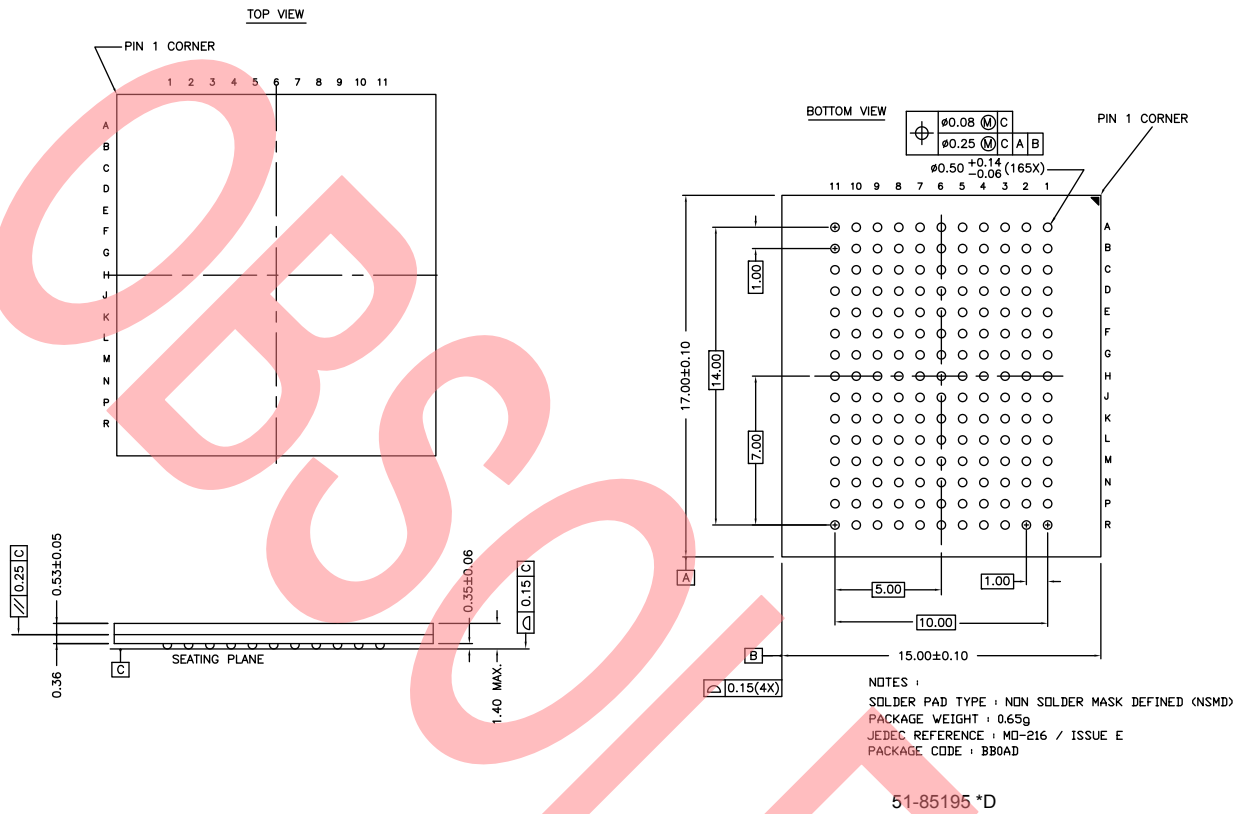
Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 *E

Package Diagrams (continued)

Figure 8. 165-ball FBGA (15 × 17 × 1.40 mm) (0.50 Ball Diameter) Package Outline, 51-85195



Acronyms

| Acronym | Description |
|-------------------------|--|
| CE | Chip Enable |
| $\overline{\text{CEN}}$ | Clock Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| EIA | Electronic Industries Alliance |
| FBGA | Fine-Pitch Ball Grid Array |
| I/O | Input/Output |
| JEDEC | Joint Electron Devices Engineering Council |
| JTAG | Joint Test Action Group |
| LMBU | Logical Multi Bit Upsets |
| LSB | Least Significant Bit |
| LSBU | Logical Single Bit Upsets |
| MSB | Most Significant Bit |
| NoBL | No Bus Latency |
| $\overline{\text{OE}}$ | Output Enable |
| SEL | Single Event Latch-up |
| SRAM | Static Random Access Memory |
| TAP | Test Access Port |
| TCK | Test Clock |
| TMS | Test Mode Select |
| TDI | Test Data-In |
| TDO | Test Data-Out |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |
| $\overline{\text{WE}}$ | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| ms | millisecond |
| mm | millimeter |
| mV | millivolt |
| nm | nanometer |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY7C1460AV33/CY7C1462AV33, 36-Mbit (1M × 36/2M × 18) Pipelined SRAM with NoBL™ Architecture | | | | |
|---|--------|-----------------|-----------------|--|
| Document Number: 38-05353 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 254911 | SYT | See ECN | New data sheet. Part number changed from previous revision. New and old part number differ by the letter "A". |
| *A | 303533 | SYT | See ECN | Updated Pin Configurations (Changed H9 pin from V _{SSQ} to V _{SS} on 209-ball FBGA). Updated Electrical Characteristics (Changed the test condition from V _{DD} = Min to V _{DD} = Max for V _{OL} parameter, changed maximum value of I _{DD} parameter from 450, 400 and 350 mA to 475, 425 and 375 mA for 250, 200 and 167 MHz respectively, changed maximum value of I _{SB1} parameter from 190, 180 and 170 mA to 225 mA for 250, 200 and 167 MHz respectively, changed maximum value of I _{SB2} parameter from 80 mA to 100 mA for all frequencies, changed maximum value of I _{SB3} parameter from 180, 170 and 160 mA to 200 mA for 250, 200 and 167 MHz respectively, changed maximum value of I _{SB4} parameter from 100 mA to 110 mA for all frequencies). Updated Capacitance (Changed the values of C _{IN} , C _{CLK} and C _{I/O} parameters to 6.5, 3 and 5.5 pF from 5, 5 and 7 pF for 100-pin TQFP package). Updated Thermal Resistance (Replaced the values of Θ _{JA} and Θ _{JC} parameters from TBD to respective Thermal Values for all packages). Updated Switching Characteristics (Changed maximum value of t _{CO} parameter from 3.0 ns to 3.2 ns and minimum value of t _{DOH} parameter from 1.3 ns to 1.5 ns for 200 MHz speed bin). Updated Ordering Information (Added Pb-free information for 100-pin TQFP and 165-ball FBGA and 209-ball BGA packages). |
| *B | 331778 | SYT | See ECN | Updated Pin Configurations (Modified Address Expansion balls in the pinouts for 165-ball FBGA and 209-ball BGA Package as per JEDEC standards) and updated Pin Definitions accordingly. Updated Operating Range (Added Industrial Temperature Grade). Updated Electrical Characteristics (Modified test conditions for V _{OL} and V _{OH} parameters, changed maximum value of I _{SB2} parameter from 100 mA to 120 mA and maximum value of I _{SB4} parameter from 110 mA to 135 mA). Updated Capacitance (Changed C _{IN} , C _{CLK} and C _{I/O} to 7, 7 and 6 pF from 5, 5 and 7 pF for 165-ball FBGA Package). Updated Ordering Information (by Shading and Unshading MPNs as per availability). |
| *C | 417509 | R XU | See ECN | Changed status from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Updated Electrical Characteristics (Modified the description of I _X parameter "Input Load Current except ZZ and MODE" to "Input Leakage Current except ZZ and MODE", changed minimum value of I _X parameter from -5 μA to -30 μA and maximum value of I _X parameter from 30 μA to 5 μA respectively for "Input Current of MODE", and also changed minimum value of I _X parameter from -30 μA to -5 μA and maximum value of I _X parameter from 5 μA to 30 μA respectively for "Input Current of ZZ", Modified test condition from V _{IH} ≤ V _{DD} to V _{IH} < V _{DD}). Updated Ordering Information (Replaced Package Name column with Package Diagram in the Ordering Information table). Updated Package Diagrams (for spec 51-85050). |
| *D | 473229 | NXR | See ECN | Updated TAP AC Switching Characteristics (Changed minimum value of t _{TH} , t _{TL} parameters from 25 ns to 20 ns and maximum value of t _{TDOV} parameter from 5 ns to 10 ns). |

Document History Page (continued)

| Document Title: CY7C1460AV33/CY7C1462AV33, 36-Mbit (1M × 36/2M × 18) Pipelined SRAM with NoBL™ Architecture | | | | |
|---|---------|-----------------|-----------------|---|
| Document Number: 38-05353 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *D (cont.) | 473229 | NXR | See ECN | Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on V _{DDQ} Relative to GND). Updated Ordering Information (Updated part numbers). |
| *E | 2756998 | VKN | 08/28/09 | Included Neutron Soft Error Immunity . Updated Ordering Information (by including parts that are available) and modified the disclaimer for the Ordering Information . Updated Package Diagrams (for spec 51-85165). |
| *F | 2900822 | NJY | 03/29/2010 | Updated Ordering Information (Added part number CY7C1460AV33-167AXI). Updated Package Diagrams (100-pin TQFP and 209-ball FBGA). Updated links in Sales, Solutions, and Legal Information . |
| *G | 3043005 | NJY | 09/30/2010 | Added Ordering Code Definitions . Added Acronyms and Units of Measure . Minor edits. Updated to new template. |
| *H | 3051765 | NJY | 10/07/2010 | Removed all information of CY7C1464 and 209-ball FBGA across the document as those part numbers are pruned. Corrected typos in Units of Measure . |
| *I | 3207715 | NJY | 03/28/2011 | Updated Ordering Information (Updated part numbers). Updated Package Diagrams . |
| *J | 3365114 | PRIT | 09/14/2011 | Updated Package Diagrams . |
| *K | 3538377 | PRIT | 03/02/2012 | Updated Features (Removed all information related to CY7C1462AV33 165-ball FBGA packages). Updated Pin Configurations (Removed all information related to CY7C1462AV33 165-ball FBGA packages). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed all information related to CY7C1462AV33 165-ball FBGA packages). Updated Identification Register Definitions (Removed all information related to CY7C1462AV33 165-ball FBGA packages). Updated Scan Register Sizes (Removed all information related to CY7C1462AV33 165-ball FBGA packages). Updated Boundary Scan Order (Removed all information related to CY7C1462AV33 165-ball FBGA packages). Updated Ordering Information (Added part number CY7C1462AV33-200AXI). Updated Package Diagrams . |
| *L | 3767562 | PRIT | 10/05/2012 | No technical updates. Completing Sunset Review. |
| *M | 4541859 | PRIT | 10/17/2014 | Updated Package Diagrams : spec 51-85050 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review. |
| *N | 4569232 | PRIT | 11/14/2014 | Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end. |
| *O | 4976716 | PRIT | 10/20/2015 | Added watermark “Not recommended for New Designs” across the document. Updated Package Diagrams : spec 51-85195 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review. |
| *P | 5506925 | PRIT | 11/02/2016 | Obsolete document. Completing Sunset Review. |

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