



**THE DATASHEET OF  
CD54AC273F3A**



## CDx4AC273, CDx4ACT273 Octal D Flip-Flop with Reset

### 1 Features

- Buffered inputs
- Typical propagation delay
  - 6.5ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$
- SCR-latchup-resistant CMOS process and circuit design
- Speed of Bipolar FAST™/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5v to 5.5v operation and balanced noise immunity at 30% of the supply
- $\pm 24mA$  output drive current
  - Fanout to 15 FAST™ ICs
  - Drives  $50\Omega$  transmission lines

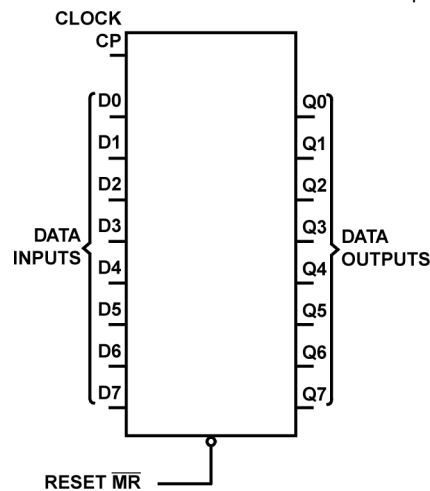
### 2 Description

The 'AC273 and 'ACT273 devices are octal D-type flip-flops with reset that utilize advanced CMOS logic technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset ( $\overline{MR}$ ). Resetting is accomplished by a low voltage level independent of the clock.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
CD74AC273/ CD74ACT273	DW (SOIC, 20)	12.8 mm x 10.3 mm	12.8 mm x 7.5 mm
	DB (SSOP, 20)	7.2 mm x 7.8 mm	7.2 mm x 5.3 mm
	N (PDIP, 20)	24.33 mm x 9.4 mm	24.33 mm x 6.35 mm
	PW (TSSOP, 20)	5.00 mm x 6.4 mm	5.00 mm x 4.4 mm

- (1) For more information, see [Section 10](#).
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.
- (3) The body size (length x width) is a nominal value and does not include pins.



**Functional Block Diagram**



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### 3 Pin Configuration and Functions

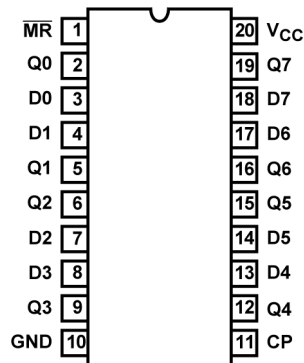


Figure 3-1. CD54AC273, CD54ACT273 (CDIP) CD74AC273, CD74ACT273 (PDIP, SOIC) Top View

#### Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
!MR	1	I	Master reset, active low
Q0	2	O	Output Q0
D0	3	I	Input D0
D1	4	I	Input D1
Q1	5	O	Output Q1
Q2	6	O	Output Q2
D2	7	I	Input D2
D3	8	I	Input D3
Q3	9	O	Output Q3
GND	10	-	Ground
CP	11	I	Clock, rising edge triggered
Q4	12	O	Output Q4
D4	13	I	Input D4
D5	14	I	Input D5
Q5	15	O	Output Q5
Q6	16	O	Output Q6
D6	17	I	Input D6
D7	18	I	Input D7
Q7	19	O	Output Q7
V <sub>CC</sub>	20	-	Supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

## 4 Specifications

### 4.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
$V_{CC}$	DC Supply Voltage	-0.5	6	V
$I_{IK}$	DC Input Diode Current	$V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$		±20 mA
$I_{OK}$	DC Output Diode Current	$V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		±50 mA
$I_O$	DC Output Source or Sink Current per Output Pin	$V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$		±50 mA
	DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ <sup>(1)</sup>		±100	mA
$T_{stg}$	Storage temperature	-65	150	°C

(1) For up to 4 outputs per device, add ±25mA for each additional output.

Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### 4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	±2000 V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$T_A$	Temperature Range	-55	125	°C
$V_{CC}$ <sup>(1)</sup>	Supply Voltage Range			
	AC Types	1.5	5.5	V
	ACT Types	4.5	5.5	V
$V_I, V_O$	DC Input or Output Voltage	0	$V_{CC}$	V
$dt/dv$	Input Rise and Fall Slew Rate			
	AC Types	1.5V to 3V	50	ns (Max)
	AC Types	3.6V to 5.5V	20	ns (Max)
	ACT Types	4.5V to 5.5V	10	ns (Max)

(1) Unless otherwise specified, all voltages are referenced to ground.

### 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CDx4AC273, CDx4ACT273			UNIT
		N (PDIP)	DW (SOIC)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	
$\theta_{JA}$	Thermal Resistance	69	101.2	126.2	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51.

### 4.5 Electrical Characteristics

PARAMETER	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNITS	
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
<b>AC TYPES</b>											
V <sub>IH</sub>	High Level Input Voltage	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
V <sub>IL</sub>	Low Level Input Voltage	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 <sup>(1) (2)</sup>	5.5	-	-	3.85	-	-	-	V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>IH</sub> or V <sub>IL</sub>	-50 <sup>(1) (2)</sup>	5.5	-	-	-	-	3.85	-	V
			0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
I <sub>I</sub>	Input Leakage Current	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	Quiescent Supply Current MSI	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	µA
<b>ACT TYPES</b>											
V <sub>IH</sub>	High Level Input Voltage	-	-	4.5 to 5.5	2	-	2	-	2	-	V
V <sub>IL</sub>	Low Level Input Voltage	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 <sup>(1) (2)</sup>	5.5	-	-	3.85	-	-	-	V
			-50 <sup>(1) (2)</sup>	5.5	-	-	-	-	3.85	-	V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 <sup>(1) (2)</sup>	5.5	-	-	-	1.65	-	-	V
			50 <sup>(1) (2)</sup>	5.5	-	-	-	-	-	1.65	V
I <sub>I</sub>	Input Leakage Current	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	Quiescent Supply Current MSI	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	µA

PARAMETER	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNITS	
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
ΔI <sub>CC</sub>	Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

- (1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- (2) Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

**Table 4-1. ACT Input Load Table**

INPUT	UNIT LOAD
Dn	0.5
$\overline{\text{MR}}$	0.57
CP	1

#### 4.6 Prerequisite for Switching Function

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
<b>AC TYPES</b>							
Data to CP Set-Up Time	t <sub>SU</sub>	1.5	2	-	2	-	ns
		3.3 <sup>(1)</sup>	2	-	2	-	ns
		5 <sup>(2)</sup>	2	-	2	-	ns
Hold Time	t <sub>H</sub>	1.5	2	-	2	-	ns
		3.3	2	-	2	-	ns
		5	2	-	2	-	ns
Removal Time, $\overline{\text{MR}}$ to CP	t <sub>REM</sub>	1.5	2	-	2	-	ns
		3.3	2	-	2	-	ns
		5	2	-	2	-	ns
$\overline{\text{MR}}$ Pulse Width	t <sub>W</sub>	1.5	55	-	63	-	ns
		3.3	6.1	-	7	-	ns
		5	4.4	-	5	-	ns
CP Pulse Width	t <sub>W</sub>	1.5	55	-	63	-	ns
		3.3	6.1	-	7	-	ns
		5	4.4	-	5	-	ns
CP Frequency	f <sub>MAX</sub>	1.5	9	-	8	-	MHz
		3.3	81	-	71	-	MHz
		5	114	-	100	-	MHz
<b>ACT TYPES</b>							
Data to CP Set-Up Time	t <sub>SU</sub>	5 <sup>(2)</sup>	2	-	2	-	ns
Hold Time	t <sub>H</sub>	5	2	-	2	-	ns
Removal Time $\overline{\text{MR}}$ to CP	t <sub>REM</sub>	5	2	-	2	-	ns
$\overline{\text{MR}}$ Pulse Width	t <sub>W</sub>	5	4.4	-	5	-	ns
CP Pulse Width	t <sub>W</sub>	5	5.3	-	6	-	ns
CP Frequency	f <sub>MAX</sub>	5	97	-	85	-	MHz

- (1) 3.3V Min is at 3.6V, Max is at 3V.
- (2) 5V Min is at 5.5V, Max is at 4.5V.

## 4.7 Switching Characteristics

Input  $t_r$ ,  $t_f = 3\text{ns}$ ,  $C_L = 50\text{pF}$  (Worst Case)

PARAMETER		$V_{CC}$ (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>AC TYPES</b>									
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, CP to Qn	1.5	-	-	154	-	-	169	ns
		3.3 <sup>(1)</sup>	4.9	-	17.2	4.7	-	18.9	ns
		5 <sup>(2)</sup>	3.5	-	12.3	3.4	-	13.5	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, $\overline{MR}$ to Qn	1.5	-	-	154	-	-	169	ns
		3.3	4.9	-	17.2	4.7	-	18.9	ns
		5	3.5	-	12.3	3.4	-	13.5	ns
$C_I$	Input Capacitance	-	-	-	10	-	-	10	pF
$C_{PD}$ <sup>(3)</sup>	Power Dissipation Capacitance	-	-	45	-	-	45	-	pF
<b>ACT TYPES</b>									
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, CP to Qn	5 <sup>(2)</sup>	3.5	-	12.3	3.4	-	13.5	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, $\overline{MR}$ to Qn	5	3.5	-	12.3	3.4	-	13.5	ns
$C_I$	Input Capacitance	-	-	-	10	-	-	10	pF
$C_{PD}$ <sup>(3)</sup>	Power Dissipation Capacitance	-	-	45	-	-	45	-	pF

- (1) 3.3V Min is at 3.6V, Max is at 3V.  
 (2) 5V Min is at 5.5V, Max is at 4.5V.  
 (3)  $C_{PD}$  is used to determine the dynamic power consumption per flip-flop.

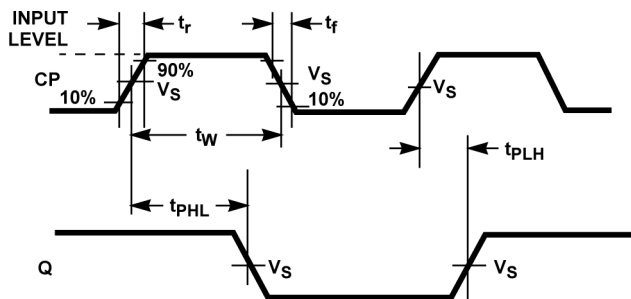
### Note

$$\text{AC: } P_D = C_{PD} V_{CC}^2 f_i = \sum (C_L V_{CC}^2 f_o)$$

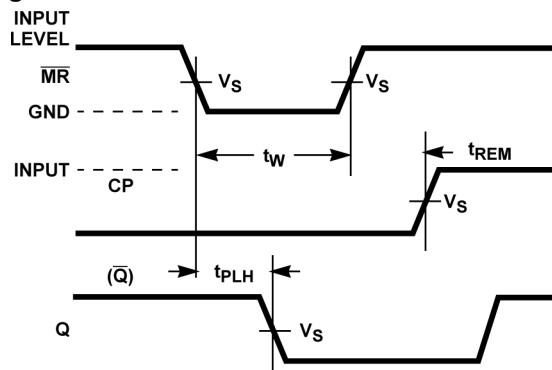
$$\text{ACT: } P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency, } f_o = \text{output frequency, } C_L = \text{output load capacitance, } V_{CC} = \text{supply voltage.}$$

## 5 Parameter Measurement Information

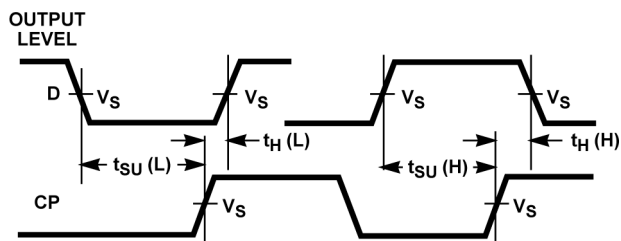
### Load Circuit and Voltage Waveforms



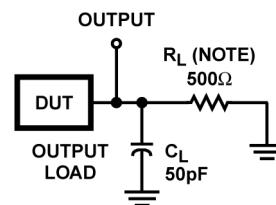
Propagation Delay Times and Clock Pulse Width



Prerequisite and Propagation Delay Times for Master Reset



Prerequisite for Clock



A. For AC Series Only: When  $V_{CC} = 1.5V$ ,  $R_L = 1k\Omega$ .

Propagation Delay Times

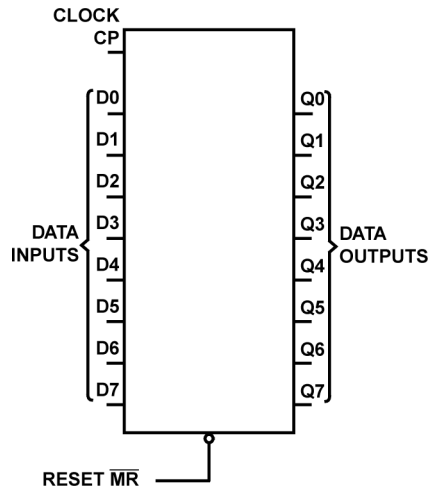
	AC	ACT
Input Level	$V_{CC}$	3V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

## 6 Detailed Description

### 6.1 Overview

The 'AC273 and 'ACT273 devices are octal D-type flip-flops with reset that utilize advanced CMOS logic technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset ( $\overline{MR}$ ). Resetting is accomplished by a low voltage level independent of the clock.

### 6.2 Functional Block Diagram



### 6.3 Device Functional Modes

Table 6-1. Truth Table

INPUTS			OUTPUTS
RESET ( $\overline{MR}$ )	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

## 7 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [Section 4.3](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1  $\mu\text{F}$  and if there are multiple  $V_{CC}$  terminals, then TI recommends .01  $\mu\text{F}$  or .022  $\mu\text{F}$  for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC273	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
CD74AC273	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
CD54ACT273	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
CD74ACT273	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 1998) to Revision C (May 2024)	Page
• Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Updated RθJA values: DW = 58 to 101.2; added PW = 126.2, all values in °C/W .....	4

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54AC273F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54AC273F3A	<a href="#">Samples</a>
CD54ACT273F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT273F3A	<a href="#">Samples</a>
CD74AC273E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC273E	<a href="#">Samples</a>
CD74AC273M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC273M	<a href="#">Samples</a>
CD74ACT273E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT273E	<a href="#">Samples</a>
CD74ACT273EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT273E	<a href="#">Samples</a>
CD74ACT273M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT273M	<a href="#">Samples</a>
CD74ACT273M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT273M	<a href="#">Samples</a>
CD74ACT273PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HM273	<a href="#">Samples</a>
CD74ACT273SM96	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT273SM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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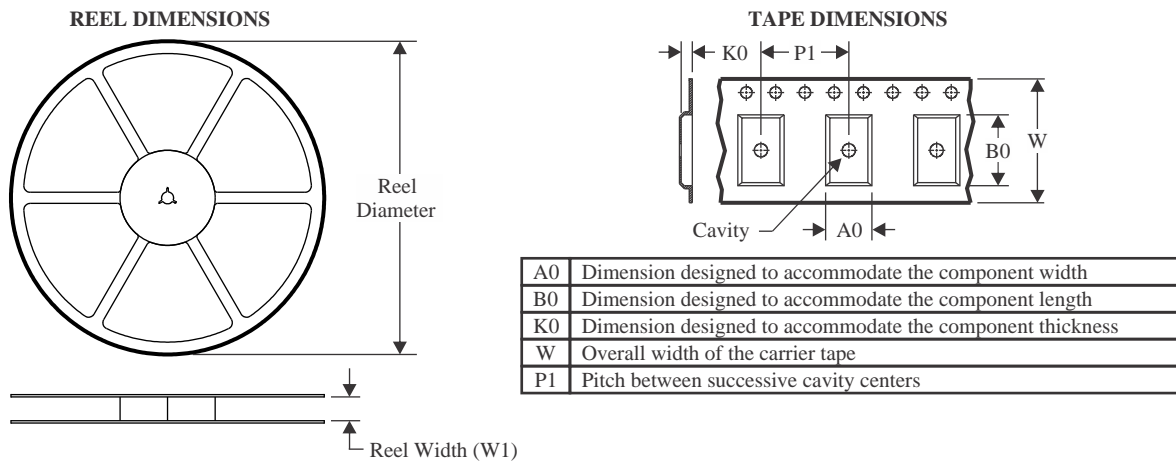
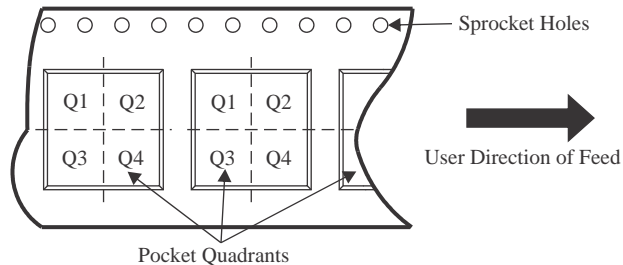
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC273, CD54ACT273, CD74AC273, CD74ACT273 :**

- Catalog : [CD74AC273](#), [CD74ACT273](#)
- Military : [CD54AC273](#), [CD54ACT273](#)

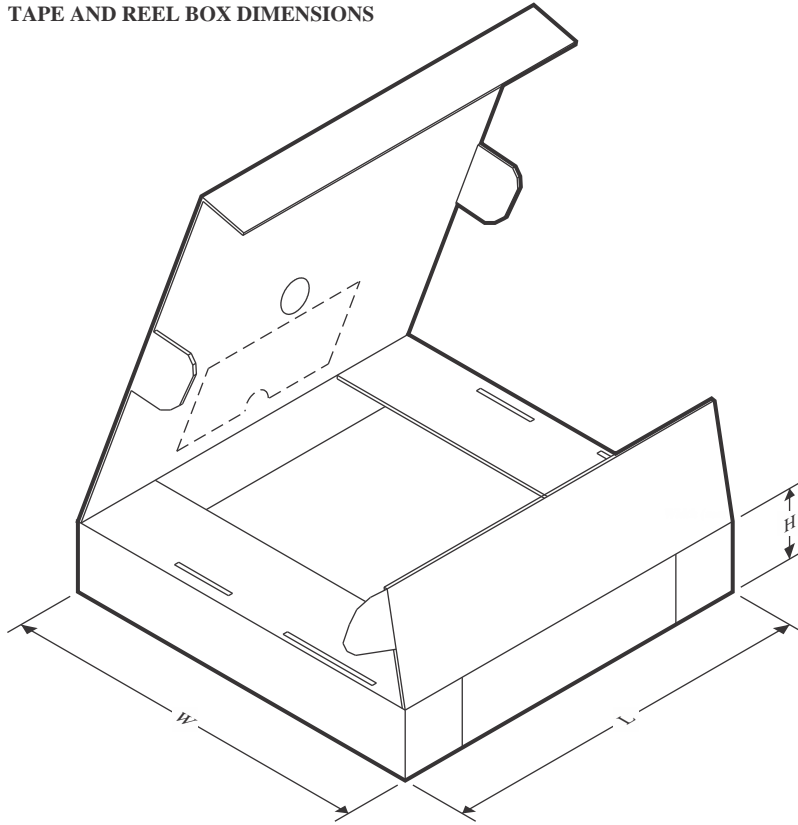
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


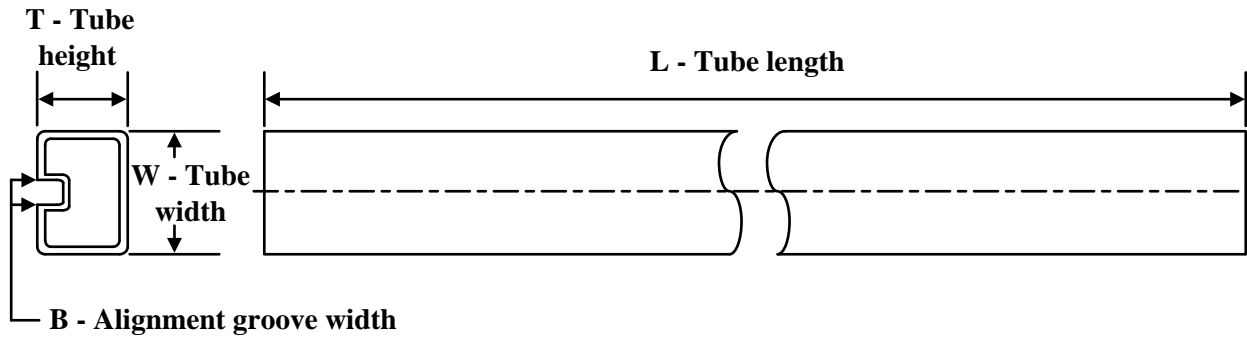
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC273M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74AC273M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74ACT273M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74ACT273M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74ACT273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
CD74ACT273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
CD74ACT273SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
CD74ACT273SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC273M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74AC273M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT273M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT273M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT273PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
CD74ACT273PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
CD74ACT273SM96	SSOP	DB	20	2000	353.0	353.0	32.0
CD74ACT273SM96	SSOP	DB	20	2000	356.0	356.0	35.0

**TUBE**


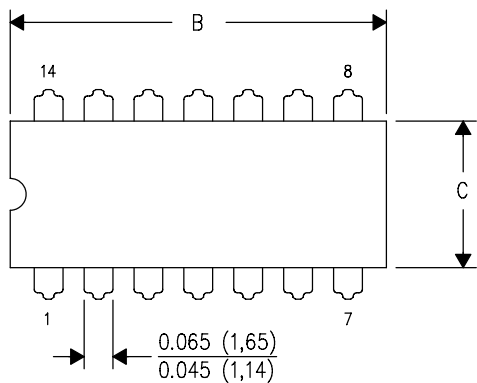
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74AC273E	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT273E	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT273EE4	N	PDIP	20	20	506	13.97	11230	4.32

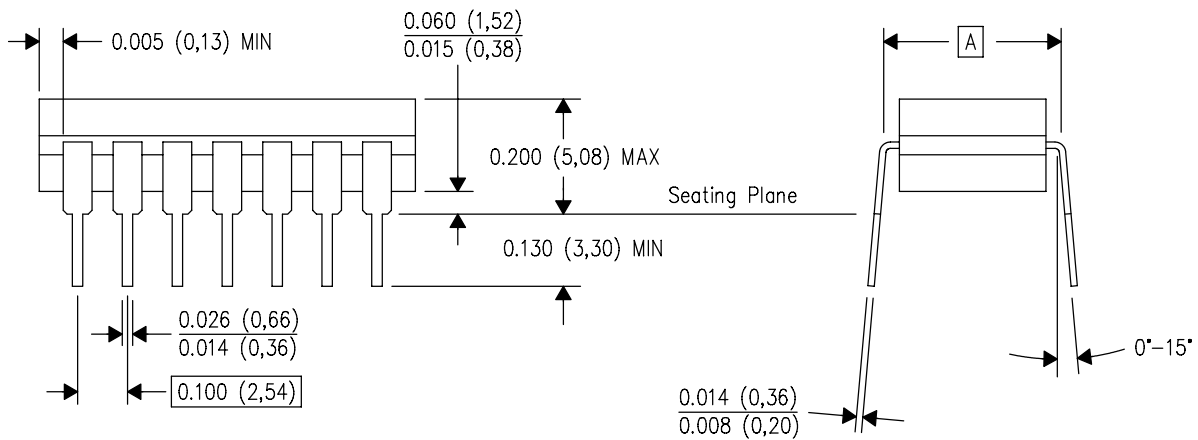
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



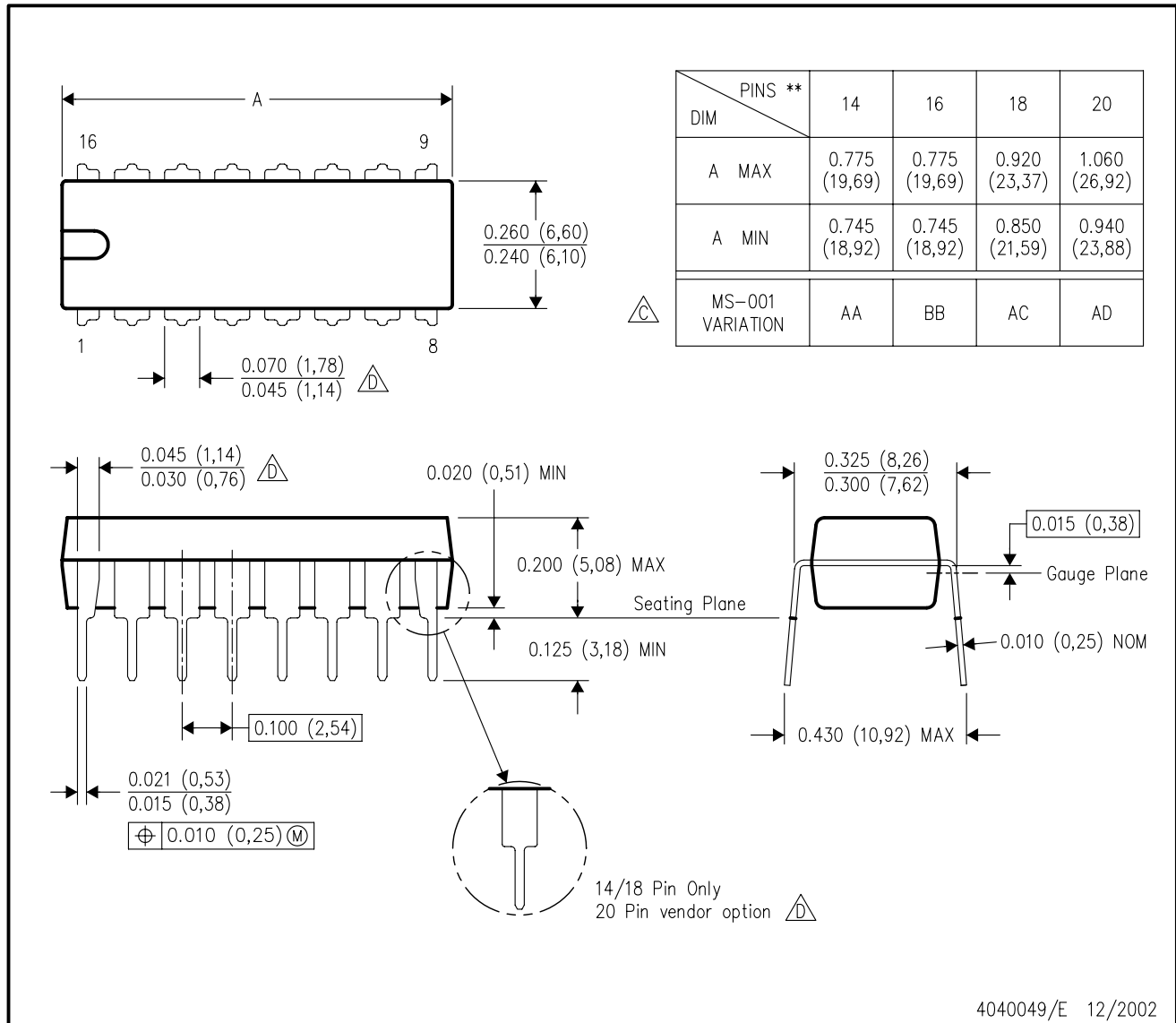
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

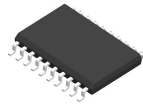
PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

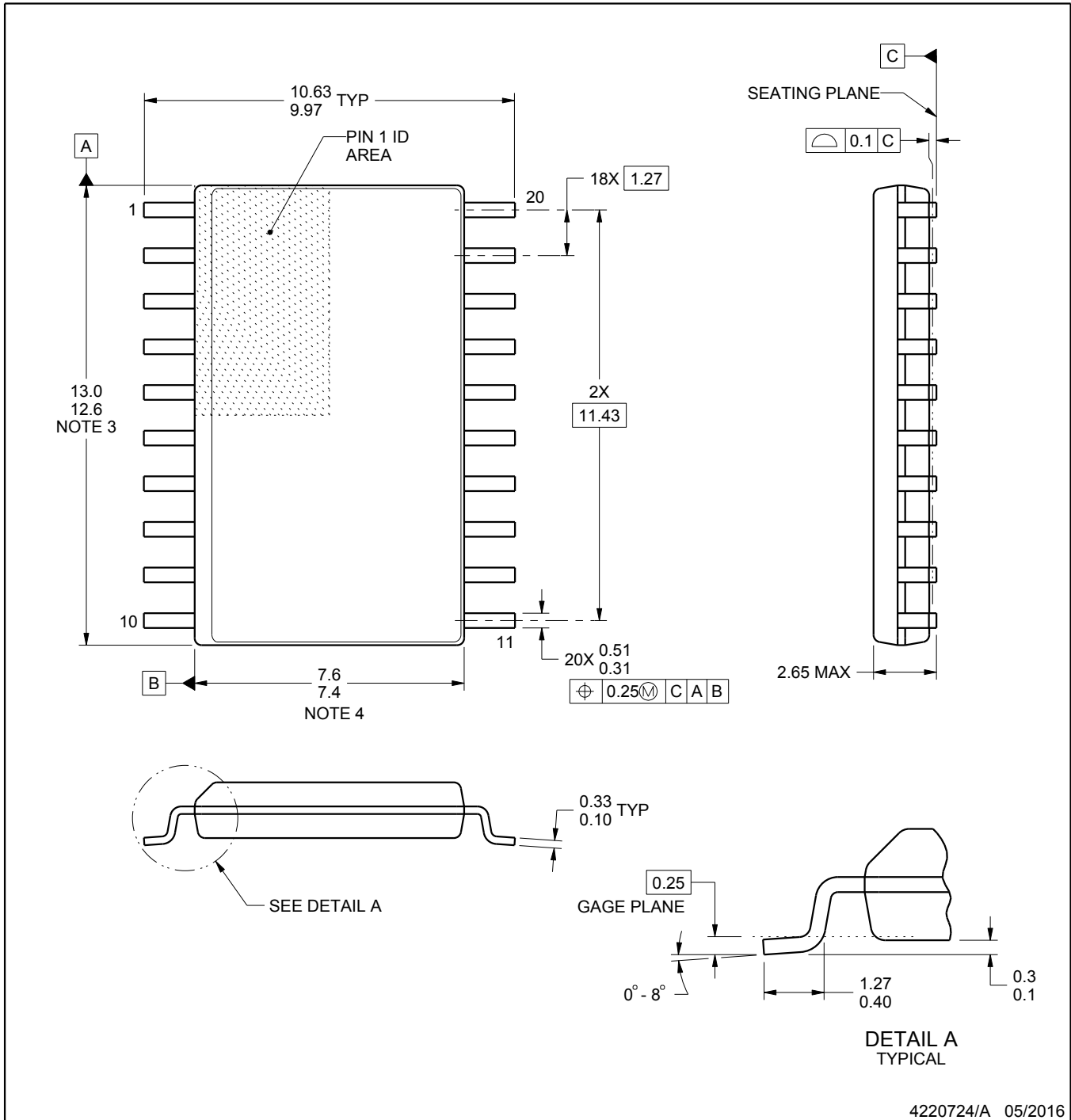
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



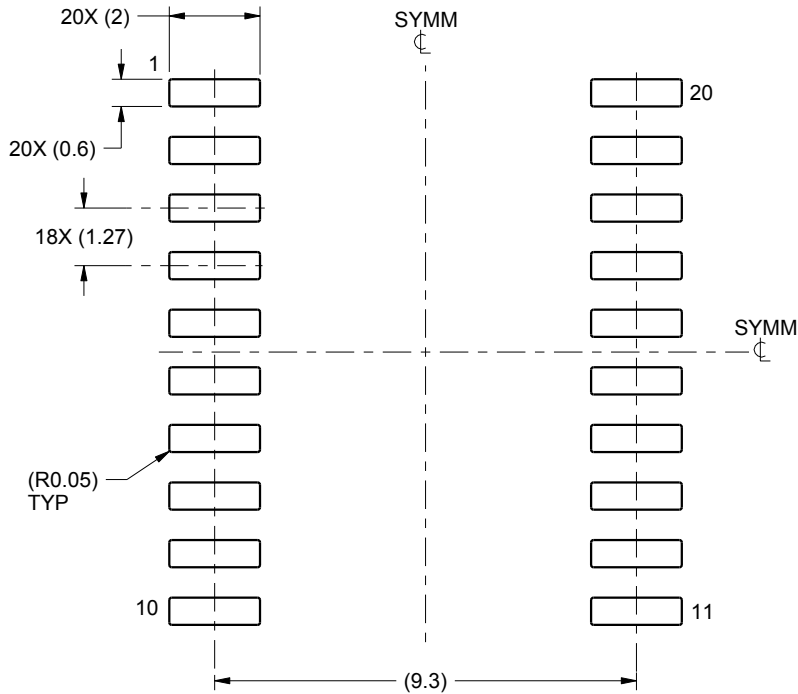
4220724/A 05/2016

# EXAMPLE BOARD LAYOUT

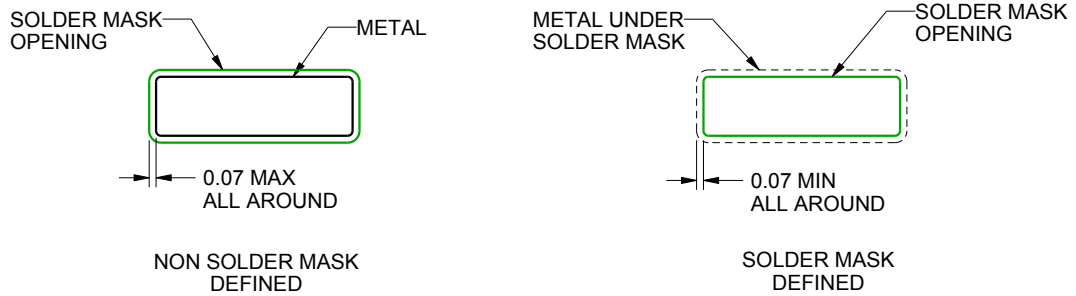
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

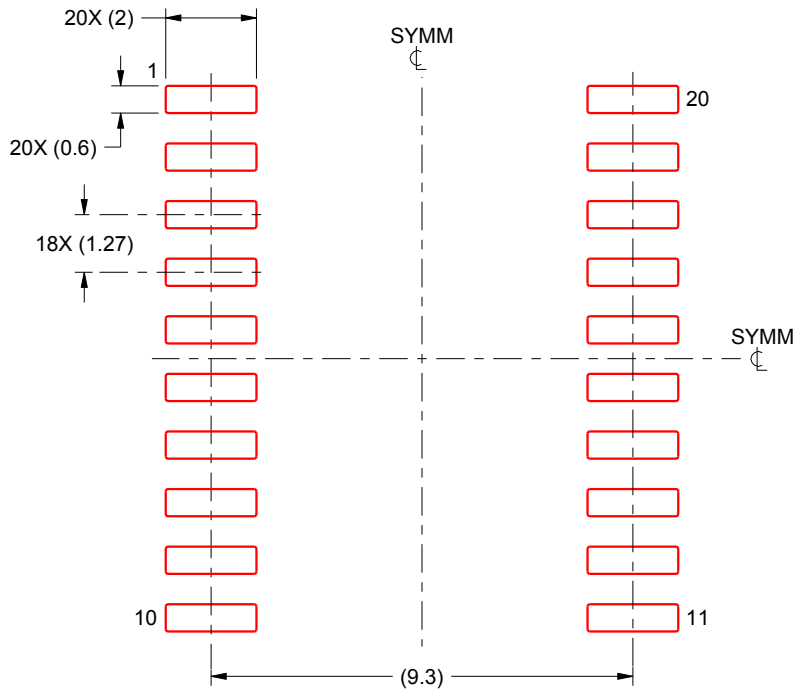
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



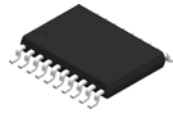
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

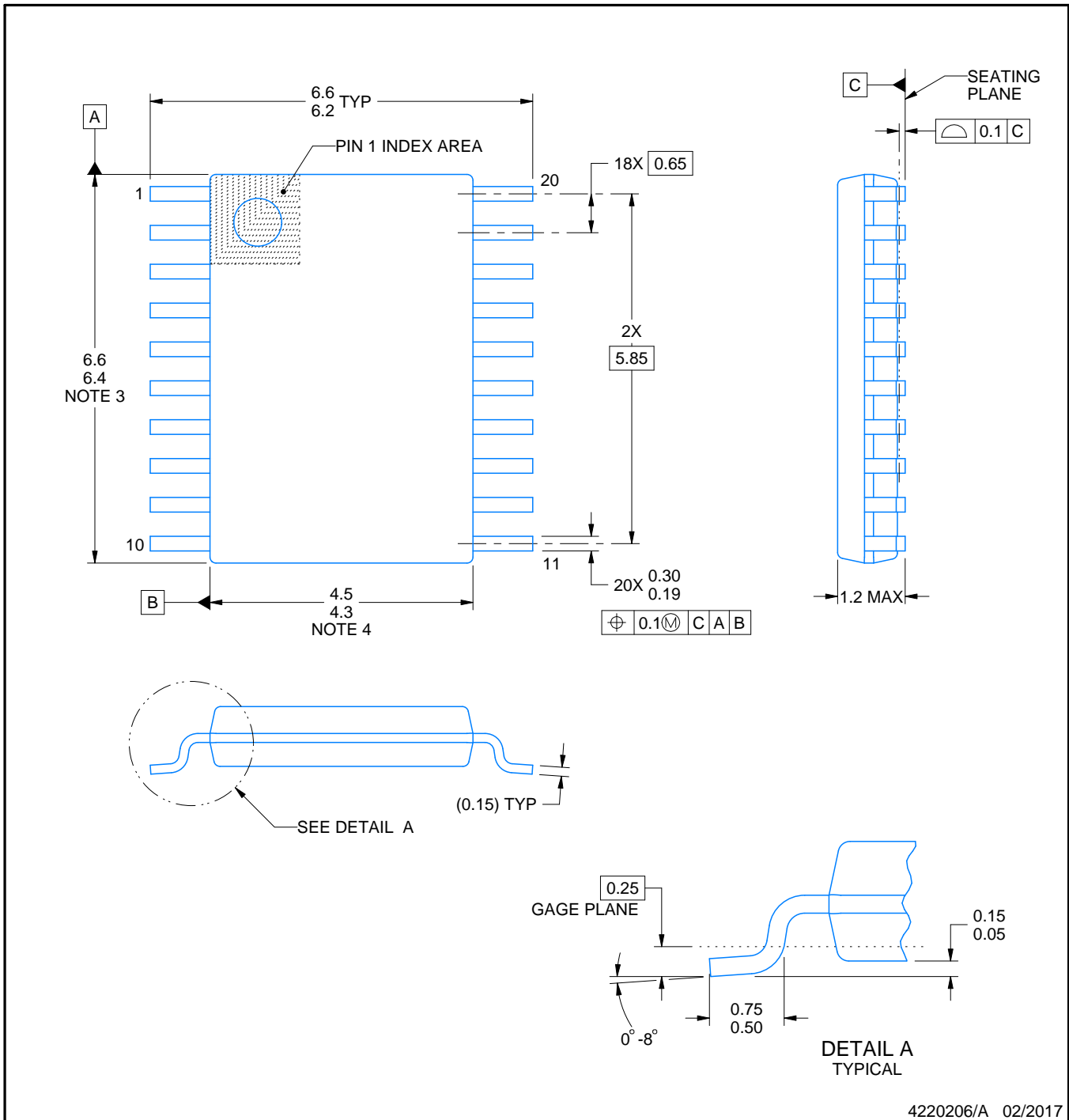
# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

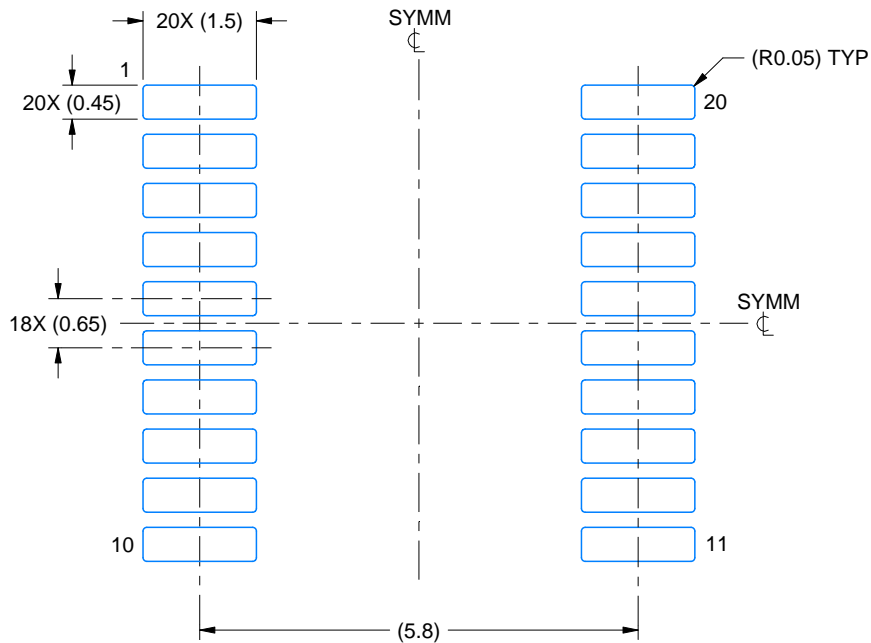
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

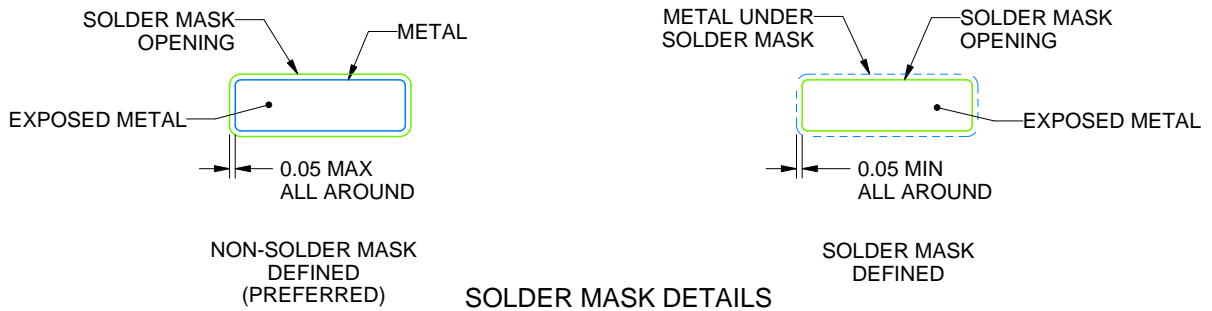
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

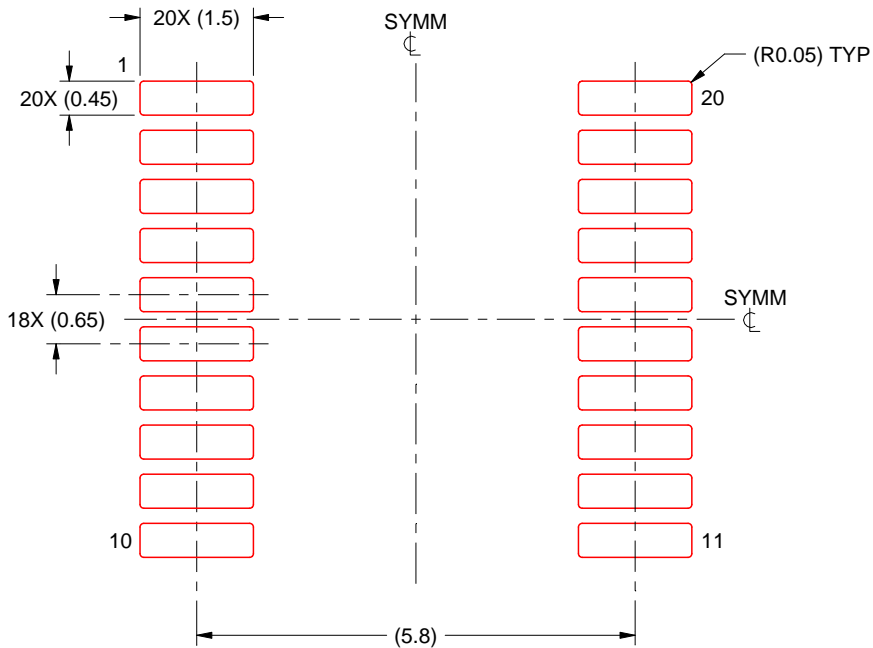
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

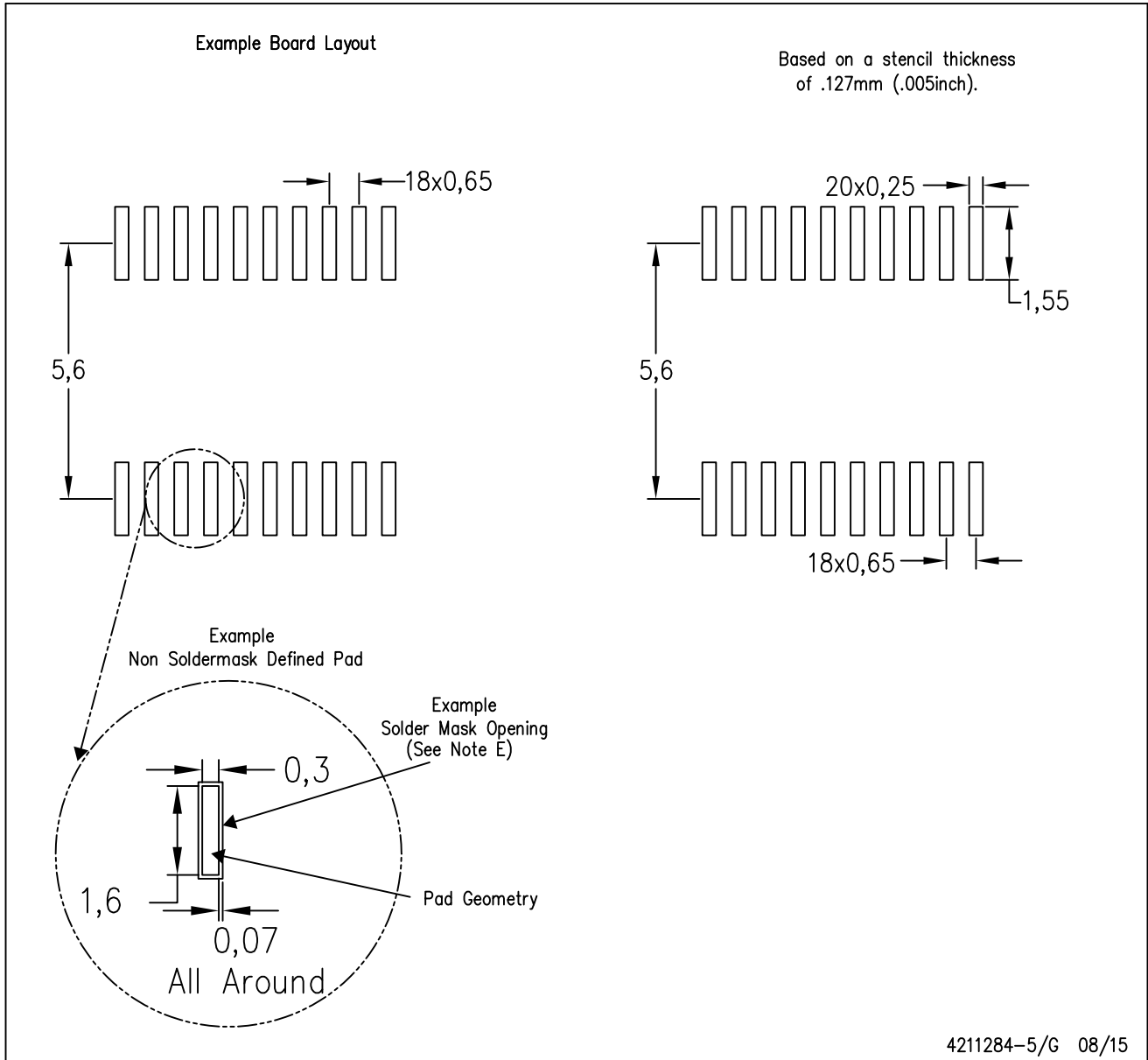
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

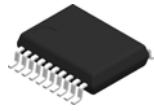
PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

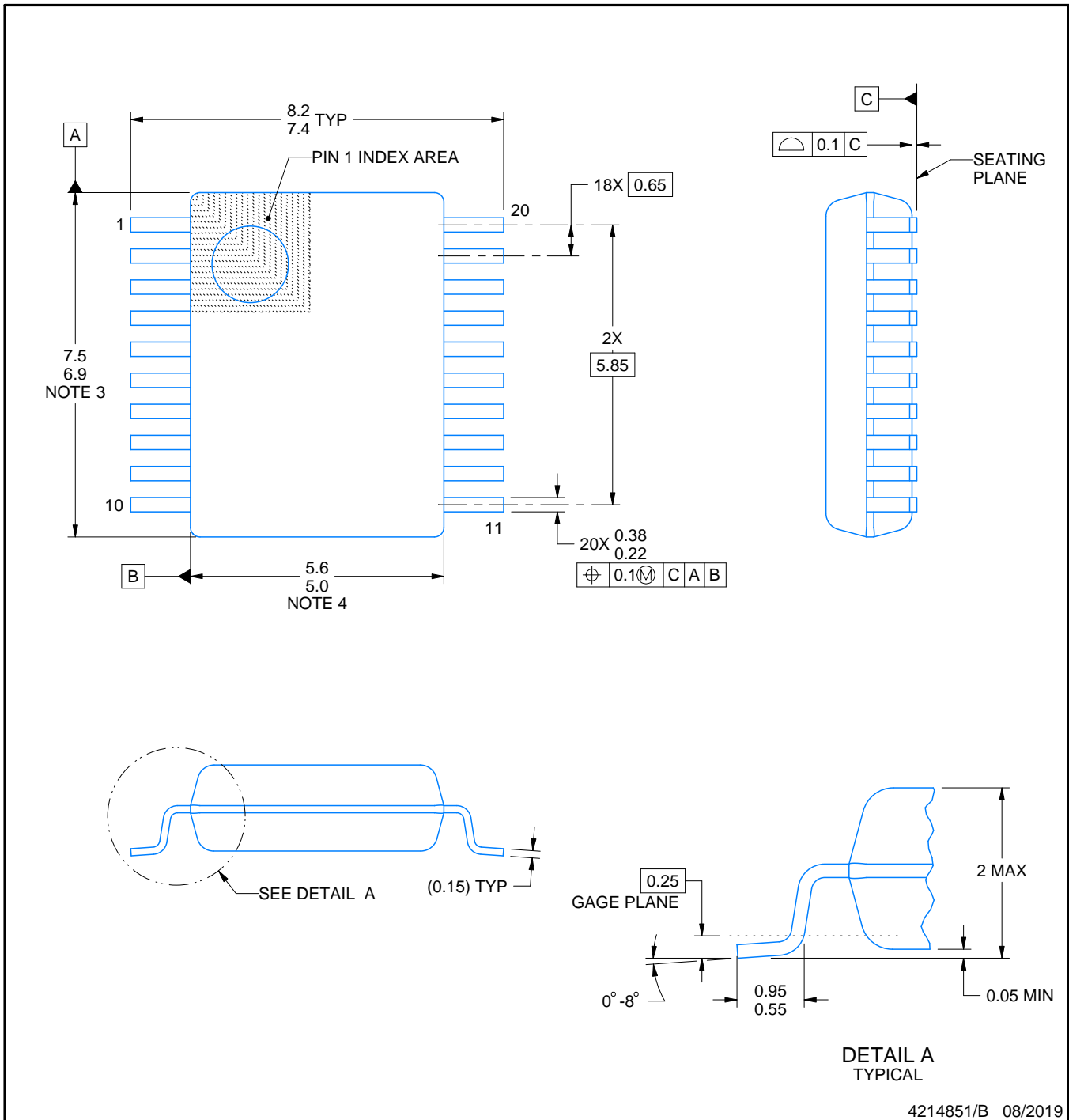
# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

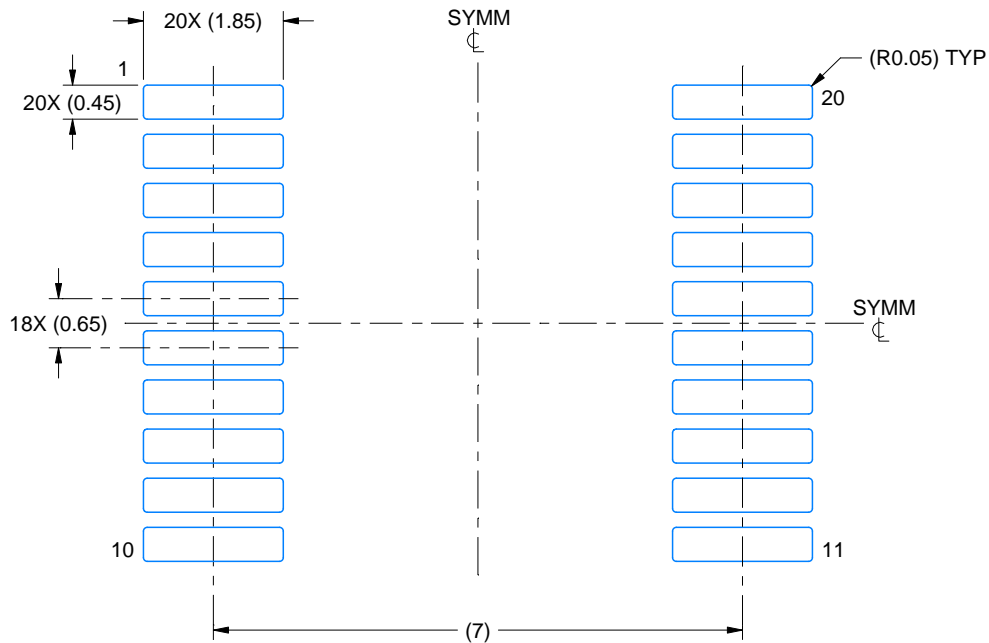
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

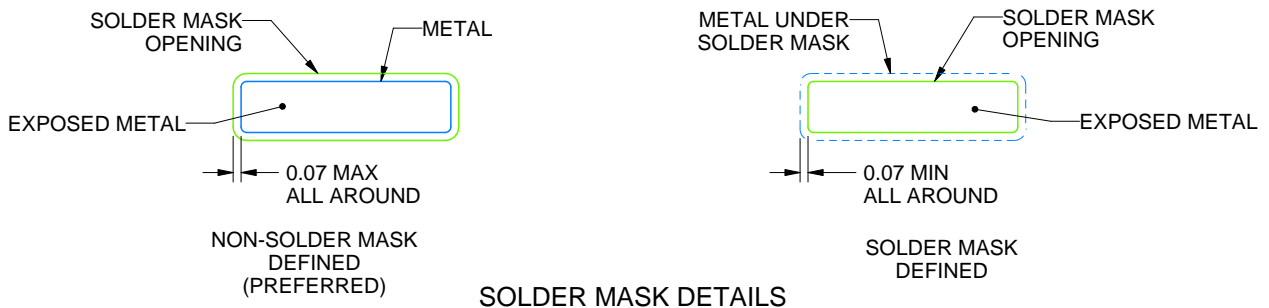
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

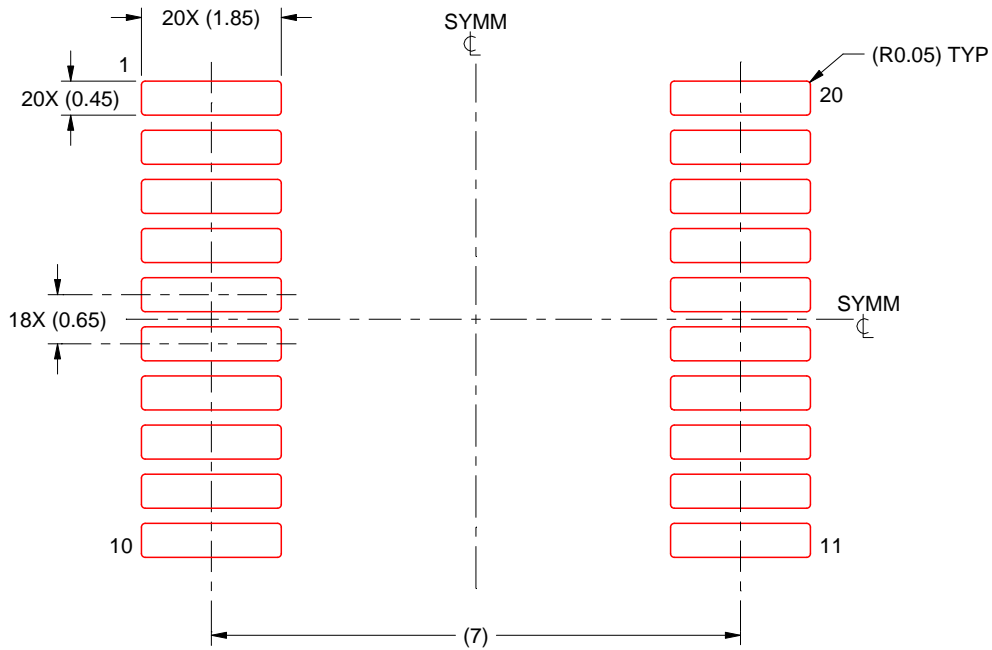
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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