



**THE DATASHEET OF  
ADS7835E/250**





ADS7835

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## 12-Bit, High-Speed, Low Power Sampling ANALOG-TO-DIGITAL CONVERTER

### FEATURES

- 500kHz THROUGHPUT RATE
- 2.5V INTERNAL REFERENCE
- LOW POWER: 17.5mW
- SINGLE SUPPLY +5V OPERATION
- SERIAL INTERFACE
- GUARANTEED NO MISSING CODES
- MSOP-8
- $\pm V_{REF}$  INPUT RANGE

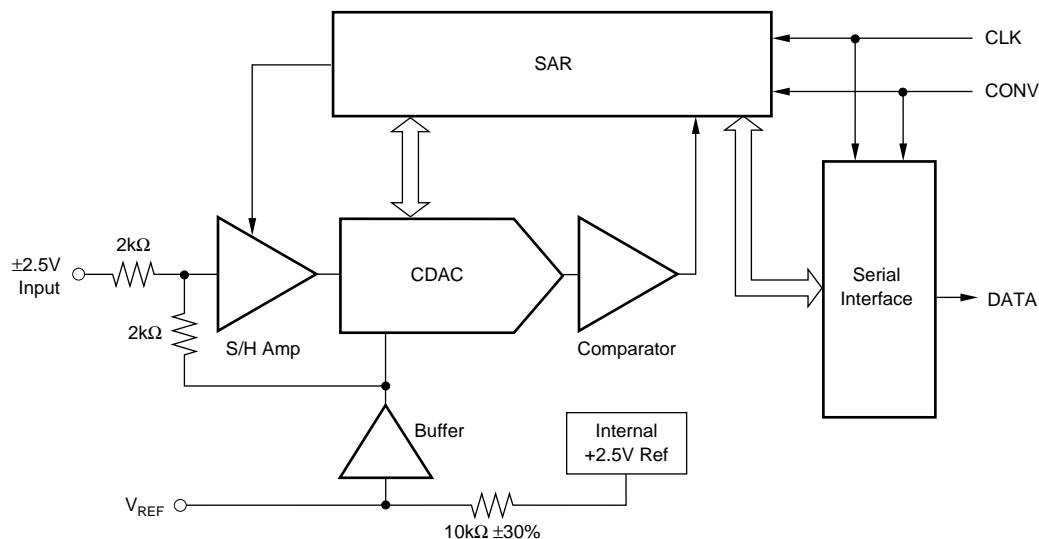
### APPLICATIONS

- BATTERY-OPERATED SYSTEMS
- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION
- WIRELESS COMMUNICATION SYSTEMS

### DESCRIPTION

The ADS7835 is a 12-bit, sampling analog-to-digital converter (A/D) complete with sample-and-hold (S/H), internal 2.5V reference, and synchronous serial interface. Typical power dissipation is 17.5mW at a 500kHz throughput rate. The device can be placed into a power-down mode which reduces dissipation to just 2.5mW. The input range is  $-V_{REF}$  to  $+V_{REF}$ , and the internal reference can be overdriven by an external voltage.

Low power, small size, and high speed make the ADS7835 ideal for battery-operated systems such as wireless communication devices, portable multi-channel data loggers, and spectrum analyzers. The serial interface also provides low cost isolation for remote data acquisition. The ADS7835 is available in an MSOP-8 package and is guaranteed over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.



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Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $+V_{CC} = +5\text{V}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ ,  $f_{\text{CLK}} = 16 \cdot f_{\text{SAMPLE}}$ , and internal  $+2.5\text{V}$  reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7835E			ADS7835EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>RESOLUTION</b>			12			*		Bits
<b>ANALOG INPUT<sup>(1)</sup></b> Input Voltage Range	$\pm 2.5\text{V}$ with the $2.5\text{V}$ Internal Reference	$-V_{\text{REF}}$		$+V_{\text{REF}}$	*		*	V
Input Capacitance			25			*		pF
Input Resistance	During Conversion (CONV = LOW)		2			*		k $\Omega$
<b>SYSTEM PERFORMANCE</b> No Missing Codes Integral Linearity Differential Linearity Bipolar Offset Error Positive Full-Scale Error <sup>(3)</sup> Negative Full-Scale Error <sup>(3)</sup> Noise Power Supply Rejection Ratio	At $25^\circ\text{C}$ $-40^\circ\text{C}$ to $+85^\circ\text{C}$ At $25^\circ\text{C}$ $-40^\circ\text{C}$ to $+85^\circ\text{C}$ Worst-Case $\Delta$ , $+V_{CC} = 5\text{V} \pm 5\%$	12	$\pm 1$ $\pm 2$ $\pm 12$ $\pm 12$ $\pm 12$ 200 0.3	$\pm 2$ $\pm 10$ $\pm 20$ $\pm 20$ $\pm 35$	*	$\pm 0.5$ $\pm 0.5$ $\pm 1$ $\pm 7$ $\pm 7$ *	$\pm 1$ $\pm 1$ $\pm 5$ $\pm 12$ $\pm 12$ $\pm 12$ *	Bits LSB <sup>(2)</sup> LSB LSB LSB LSB $\mu\text{V}_{\text{rms}}$ LSB
<b>SAMPLING DYNAMICS</b> Conversion Time Acquisition Time Throughput Rate Aperture Delay Aperture Jitter Step Response		1.625 0.350		500	*	*	*	$\mu\text{s}$ $\mu\text{s}$ kHz ns ps ns
<b>DYNAMIC CHARACTERISTICS</b> Signal-to-Noise Ratio Total Harmonic Distortion <sup>(4)</sup> Signal-to-(Noise+Distortion) Spurious Free Dynamic Range	$V_{\text{IN}} = 5\text{Vp-p}$ at $10\text{kHz}$ $V_{\text{IN}} = 5\text{Vp-p}$ at $10\text{kHz}$ $V_{\text{IN}} = 5\text{Vp-p}$ at $10\text{kHz}$ $V_{\text{IN}} = 5\text{Vp-p}$ at $10\text{kHz}$		72 $-78$ 68 72	$-72$		*	$-82$ 70 72 75	$-75$ dB dB dB dB
<b>REFERENCE OUTPUT</b> Voltage Source Current <sup>(5)</sup> Line Regulation	$I_{\text{OUT}} = 0$ Static Load $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$	2.475	2.50 0.2	2.525 50	2.48	*	2.52 *	V $\mu\text{A}$ mV
<b>REFERENCE INPUT</b> Range Resistance <sup>(6)</sup>	To Internal Reference Voltage	2.3		2.9	*		*	V k $\Omega$
<b>DIGITAL INPUT/OUTPUT</b> Logic Family Logic Levels: $V_{\text{IH}}$ $V_{\text{IL}}$ $V_{\text{OH}}$ $V_{\text{OL}}$ Data Format	$I_{\text{IH}} \leq +5\mu\text{A}$ $I_{\text{IL}} \leq +5\mu\text{A}$ $I_{\text{OH}} = -500\mu\text{A}$ $I_{\text{OL}} = 500\mu\text{A}$ Binary Two's Complement		CMOS	$+V_{CC} + 0.3$ 0.8 0.4		*	*	V V V V
<b>POWER SUPPLY REQUIREMENT</b> $+V_{CC}$ Quiescent Current Power Dissipation Power-Down	Specified Performance $f_{\text{SAMPLE}} = 500\text{kHz}$ Power-Down	4.75	3.5 0.5 17.5 2.5	5.25 30	*	*	*	V mA mA mW mW
<b>TEMPERATURE RANGE</b> Specified Performance		$-40$		$+85$	*		*	$^\circ\text{C}$

\* Specifications same as ADS7835E.

NOTES: (1) Ideal input span, does not include gain or offset error. (2) LSB means Least Significant Bit, with  $V_{\text{REF}}$  equal to  $+2.5\text{V}$ , one LSB is  $1.22\text{mV}$ . (3) Measured relative to an ideal positive full scale of  $2.499\text{V}$  for positive full-scale error. Measured relative to an ideal negative full scale of  $-2.499\text{V}$  for negative full-scale error. (4) Calculated on the first nine harmonics of the input frequency. (5) If the internal reference is required to source current to an external load, the reference voltage will change due to the internal  $10\text{k}\Omega$  resistor. (6) Can vary  $\pm 30\%$ .

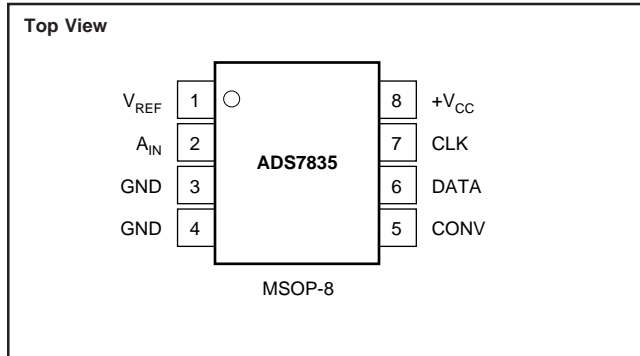
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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

+V <sub>CC</sub> to GND .....	-0.3V to 6V
Analog Inputs to GND .....	-5.3 to +5.3
Digital Inputs to GND .....	-0.3V to (V <sub>CC</sub> + 0.3V)
Power Dissipation .....	325mW
Maximum Junction Temperature .....	+150°C
Operating Temperature Range .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V <sub>REF</sub>	Reference Output. Decouple to ground with a 0.1μF ceramic capacitor and a 2.2μF tantalum capacitor.
2	A <sub>IN</sub>	±2.5V Input
3	GND	Ground
4	GND	Ground
5	CONV	Convert Input. Controls the sample/hold mode, start of conversion, start of serial data transfer, type of serial transfer, and power-down mode. See the Digital Interface section for more information.
6	DATA	Serial Data Output. The 12-bit conversion result is serially transmitted most significant bit first with each bit valid on the rising edge of CLK. By properly controlling the CONV input, it is possible to have the data transmitted least significant bit first. See the Digital Interface section for more information.
7	CLK	Clock Input. Synchronizes the serial data transfer and determines conversion speed.
8	+V <sub>CC</sub>	Power Supply. Decouple to ground with a 0.1μF ceramic capacitor and a 10μF tantalum capacitor.

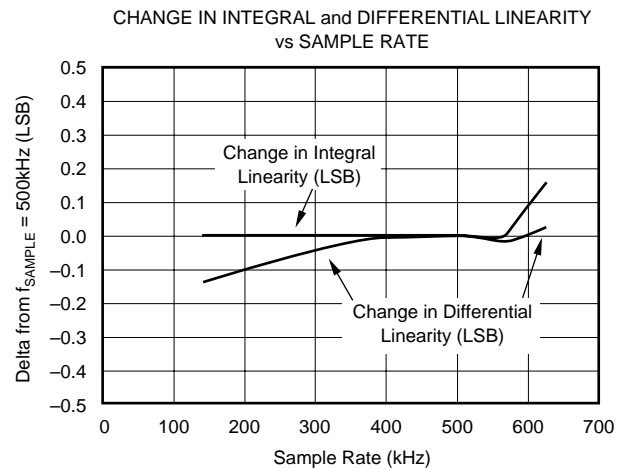
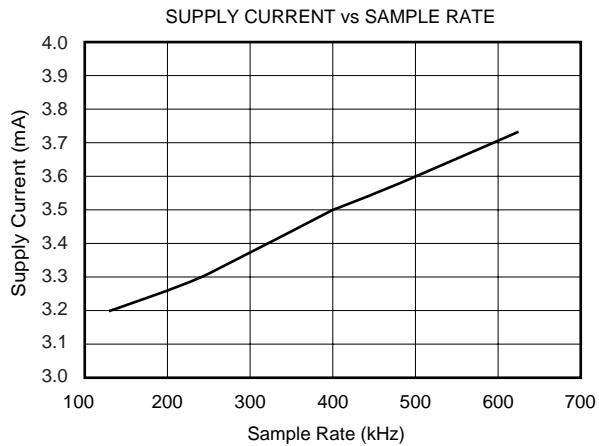
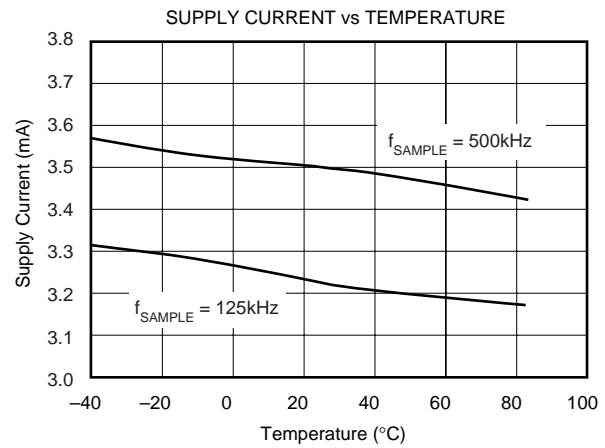
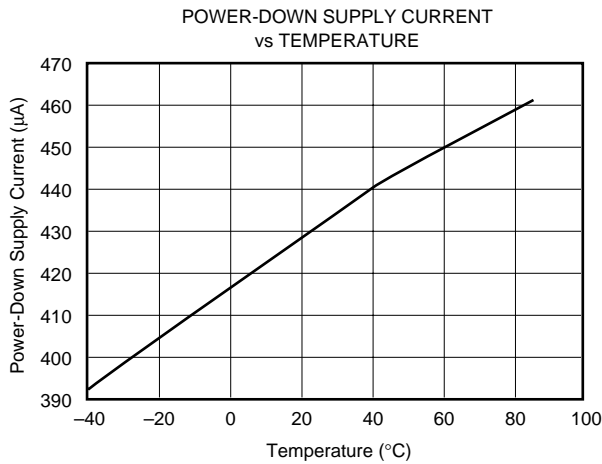
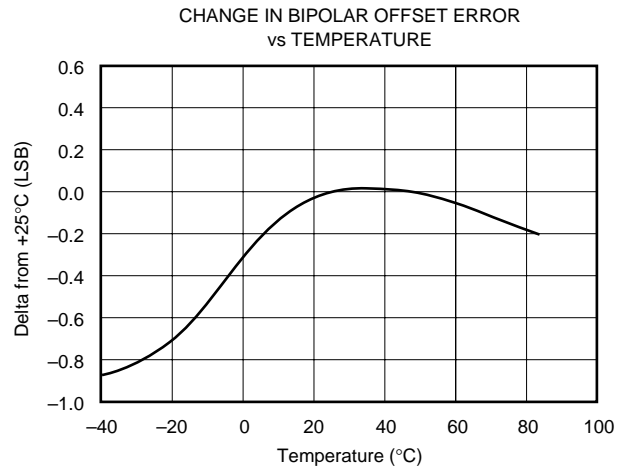
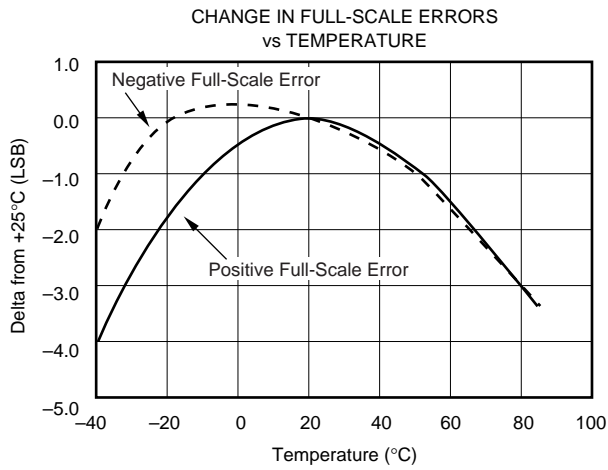
## PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING <sup>(2)</sup>	ORDERING NUMBER <sup>(3)</sup>	TRANSPORT MEDIA
ADS7835E	±2	N/S <sup>(4)</sup>	MSOP-8	337	-40°C to +85°C	B35	ADS7835E/250	Tape and Reel
"	"	"	"	"	"	"	ADS7835E/2K5	Tape and Reel
ADS7835EB	±1	±1	MSOP-8	337	-40°C to +85°C	B35	ADS7835EB/250	Tape and Reel
"	"	"	"	"	"	"	ADS7835EB/2K5	Tape and Reel
ADS7835P	±2	N/S <sup>(4)</sup>	Plastic DIP-8	006	-40°C to +85°C	ADS7835P	ADS7835P	Rails
ADS7835PB	±1	±1	"	"	"	ADS7835PB	ADS7835PB	Rails

NOTE: (1) For detail drawing and dimension table, please see end of data sheet or Package Drawing File on Web. (2) Performance Grade information is marked on the reel. (3) Models with a slash(/) are available only in Tape and reel in quantities indicated (e.g. /250 indicates 250 units per reel, /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS7835E/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to the [www.burr-brown.com](http://www.burr-brown.com) web site under Applications and Tape and Reel Orientation and Dimensions. (4) N/S = Not Specified, typical only. However, 12-Bits no missing codes is guaranteed over temperature.

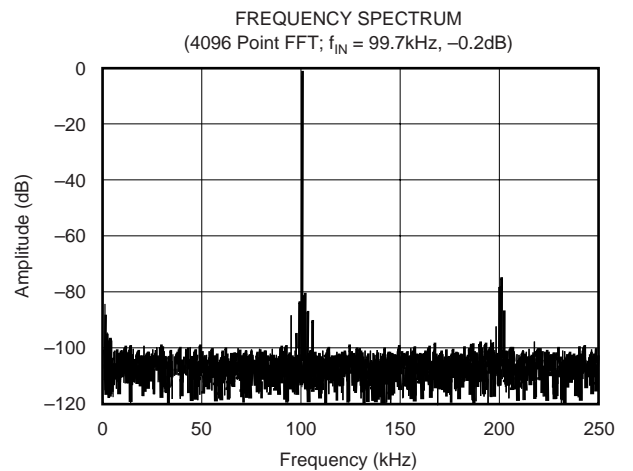
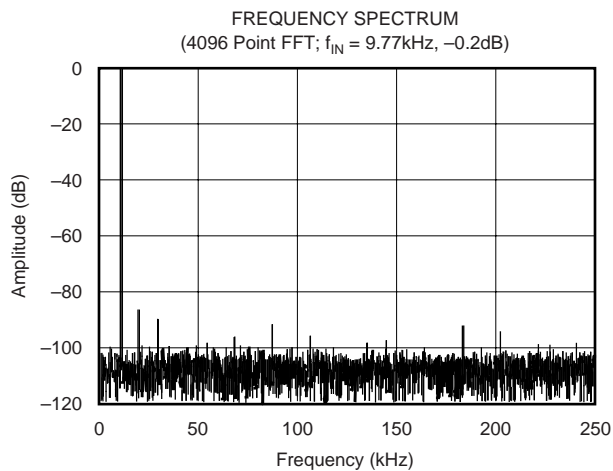
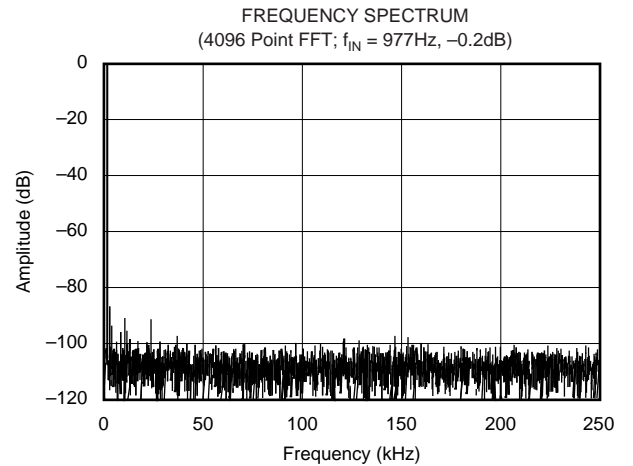
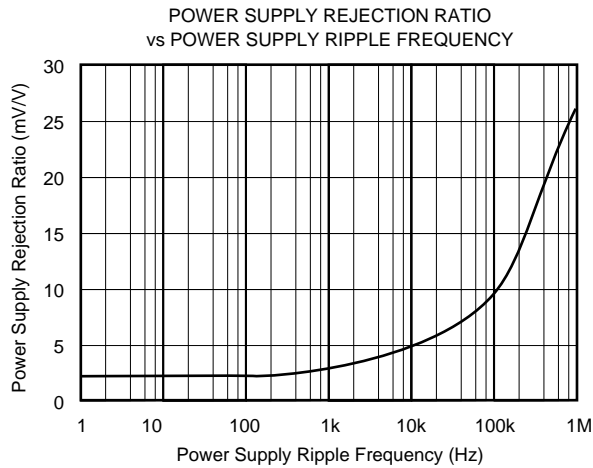
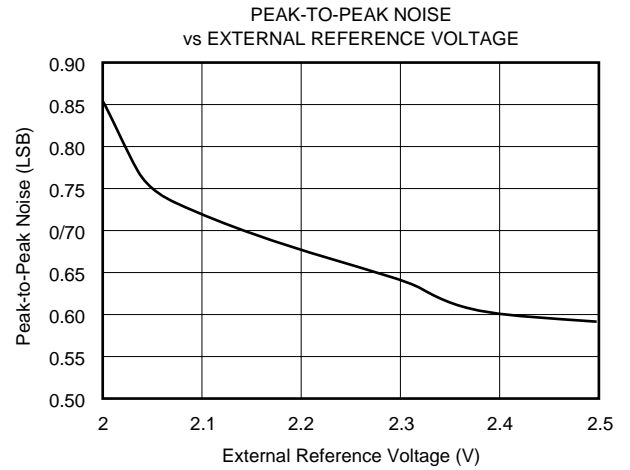
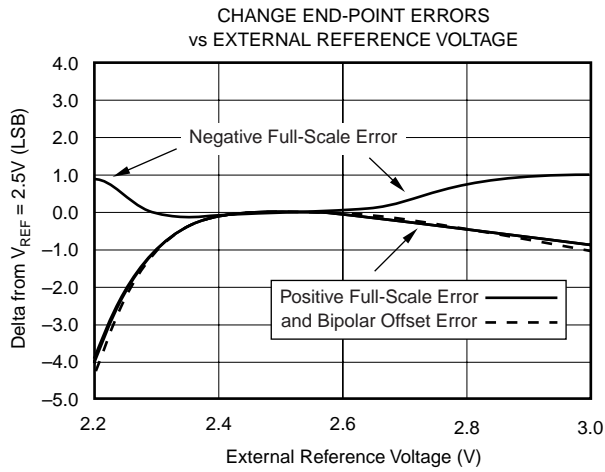
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +5\text{V}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ ,  $f_{\text{CLK}} = 16 \cdot f_{\text{SAMPLE}}$ , and internal  $+2.5\text{V}$  reference, unless otherwise specified.



# TYPICAL PERFORMANCE CURVES (Cont.)

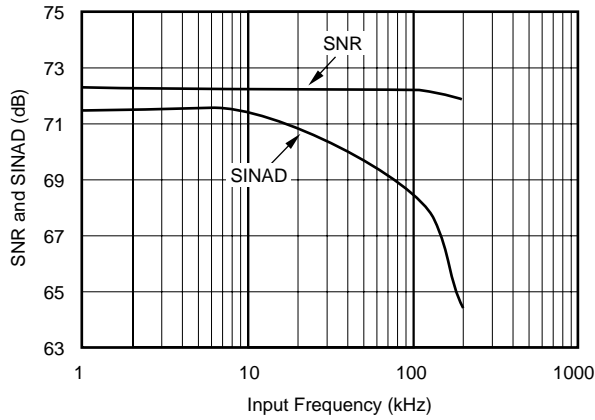
At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +5\text{V}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ ,  $f_{\text{CLK}} = 16 \cdot f_{\text{SAMPLE}}$ , and internal  $+2.5\text{V}$  reference, unless otherwise specified.



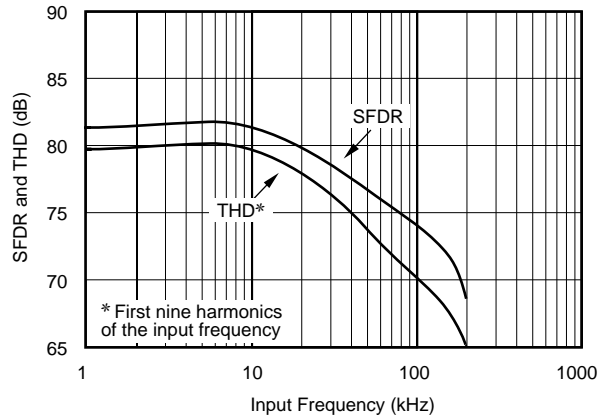
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +5\text{V}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ ,  $f_{\text{CLK}} = 16 \cdot f_{\text{SAMPLE}}$ , and internal  $+2.5\text{V}$  reference, unless otherwise specified.

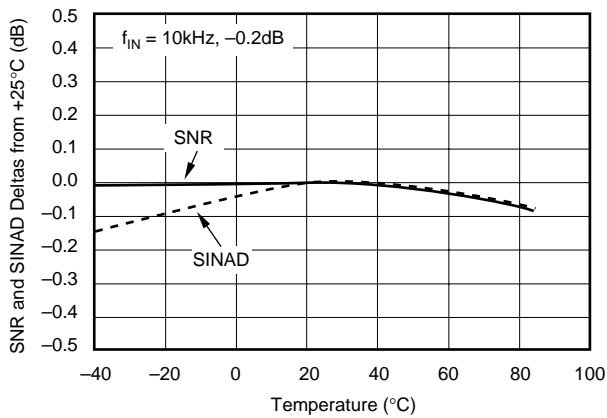
SIGNAL-TO-NOISE and  
SIGNAL-TO-(NOISE + DISTORTION)  
vs INPUT FREQUENCY



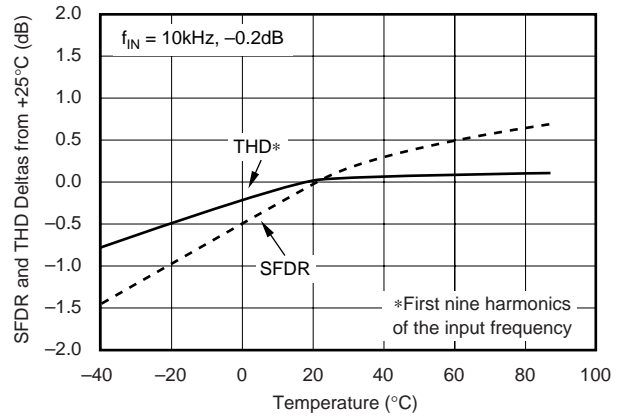
SPURIOUS FREE DYNAMIC RANGE and  
TOTAL HARMONIC DISTORTION  
vs INPUT FREQUENCY



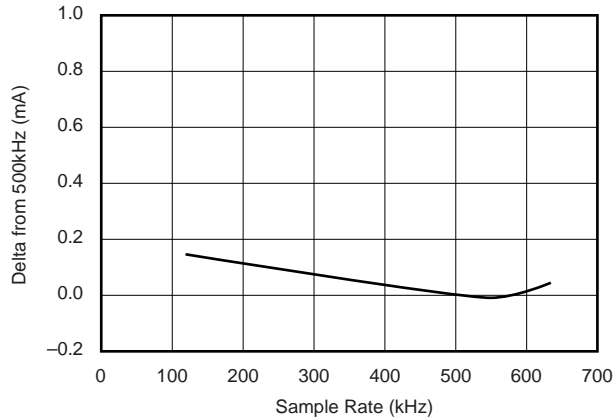
CHANGE IN SIGNAL-TO-NOISE and  
SIGNAL-TO-(NOISE+DISTORTION)  
vs TEMPERATURE



CHANGE IN SPURIOUS FREE DYNAMIC RANGE  
and TOTAL HARMONIC DISTORTION  
vs TEMPERATURE



CHANGE IN BIPOLAR OFFSET ERROR  
vs SAMPLE RATE



# THEORY OF OPERATION

The ADS7835 is a high speed Successive Approximation Register (SAR) analog-to-digital converter (A/D) with an internal 2.5V bandgap reference. The architecture is based on capacitive redistribution which inherently includes a S/H function. The converter is fabricated on a 0.6μ CMOS process. See Figure 1 for the basic operating circuit for the ADS7835.

The ADS7835 requires an external clock to run the conversion process. This clock can vary between 200kHz (12.5kHz throughput) and 8MHz (500kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 50ns and the clock period is at least 125ns. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7835.

The analog input to the ADS7835 is single-ended. The ADS7835 provides a true bipolar input where the input will swing below ground. When using the internal 2.5V reference the input range is ±2.5V (within ±20mV for the low grade and ±12mV for the high grade). When using an external reference the input range is  $-V_{REF}$  to  $+V_{REF}$ . The ADS7835 will accept an external reference with a range of 2.3V to 2.9V.

The digital result of the conversion is provided in a serial manner, synchronous to the CLK input. The provided result is Most Significant Bit (MSB) first and represents the result of the conversion currently in progress—there is no pipeline delay. By properly controlling the CONV and CLK inputs, it is possible to obtain the digital result Least Significant Bit (LSB) first.

## ANALOG INPUT

The analog input (pin 2) of the ADS7835 is connected to a 2kΩ x 2kΩ voltage divider. This divider allows the ADS7835 to accept bipolar inputs while operating from a single 5V supply. The divider is connected to the output buffer of the internal +2.5V supply. When the input is at +full-scale (+2.5V), the voltage at the input to the CDAC (Capacitive Digital-to-Analog Converter) is also +2.5V resulting in negligible input current. When the input is at -full-scale (-2.5V), the voltage at the input of the CDAC is 0V resulting in 1.25mA of current being sourced out of the input pin. It is recommended that a buffer be placed between the analog input signal and the input of the ADS7835.

The input impedance of the ADS7835 depends on whether

the device is in the sample or hold mode. When sampling, the input has a 4kΩ input impedance to the reference. The source of the analog input voltage must be able to charge the input impedance (typically 25pF || 1kΩ) to a 12-bit settling level within the same period. This can be as little as 350ns in some operating modes. When the converter is in the hold mode, the input impedance switches to approximately 2kΩ to ground.

Care must be taken regarding the input voltage on the  $A_{IN}$  pin. The input signal should remain within -5.3V and +5.3V (with a 5V supply) to avoid damaging the converter.

## REFERENCE

The reference voltage on the  $V_{REF}$  pin directly sets the full-scale range of the analog input. The ADS7835 can operate with a reference in the range of 2.3V to 2.9V, for a full-scale range of ±2.3V to ±2.9V.

The voltage at the  $V_{REF}$  pin is internally buffered and this buffer drives the CDAC portion of the converter. This is important because the buffer greatly reduces the dynamic load placed on the reference source. However, the voltage at  $V_{REF}$  will still contain some noise and glitches from the SAR conversion process. These can be reduced by carefully bypassing the  $V_{REF}$  pin to ground as outlined in the sections that follow.

## INTERNAL REFERENCE

The ADS7835 contains an on-board 2.5V reference, resulting in a -2.5V to +2.5V input range on the analog input. The Specification table gives the various specifications for the internal reference. This reference can be used to supply a small amount of source current to an external load, but the load should be static. Due to the internal 10kΩ resistor, a dynamic load will cause variations in the reference voltage, and will dramatically affect the conversion result. Note that even a static load will reduce the internal reference voltage seen at the buffer input. The amount of reduction depends on the load and the actual value of the internal “10kΩ” resistor. The value of this resistor can vary by ±30%.

The  $V_{REF}$  pin should be bypassed with a 0.1μF capacitor placed as close as possible to the ADS7835 package. In addition, a 2.2μF tantalum capacitor should be used in parallel with the ceramic capacitor. Placement of this capacitor, while not critical to performance, should be placed as close to the package as possible.

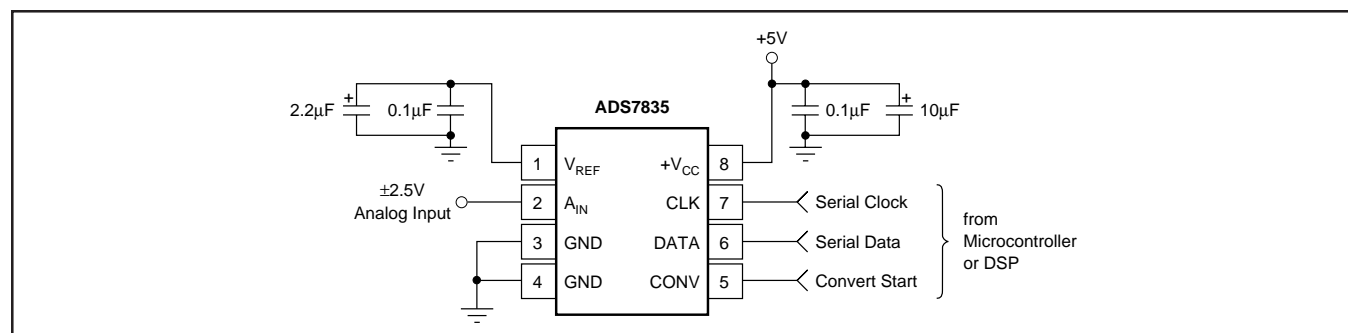


FIGURE 1. Basic Operation of the ADS7835.

## EXTERNAL REFERENCE

The internal reference is connected to the  $V_{REF}$  pin and to the internal buffer via a 10k $\Omega$  series resistor. Thus, the reference voltage can easily be overdriven by an external reference voltage. The voltage range for the external voltage is 2.3V to 2.9V, corresponding to an analog input range of 2.3V to 2.9V in both cases.

While the external reference will not source significant current into the  $V_{REF}$  pin, it does have to drive the 10k $\Omega$  series resistor that is terminated into the 2.5V internal reference (the exact value of the resistor will vary up to  $\pm 30\%$  from part to part). In addition, the  $V_{REF}$  pin should still be bypassed to ground with at least a 0.1 $\mu$ F ceramic capacitor (placed as close to the ADS7835 as possible). The reference will have to be stable with this capacitive load. Depending on the particular reference and A/D conversion speed, additional bypass capacitance may be required, such as the 2.2 $\mu$ F tantalum capacitor shown in Figure 1.

Reasons for choosing an external reference over the internal reference vary, but there are two main reasons. One is to achieve a given input range. The other is to provide greater stability over temperature. (The internal reference is typically 20ppm/ $^{\circ}$ C which translates into a full-scale drift of roughly one output code for every 12 $^{\circ}$ C. This does not take into account other sources of full-scale drift.) If greater stability over temperature is needed, then an external reference with lower temperature drift will be required.

## DIGITAL INTERFACE

Figure 2 shows the serial data timing and Figure 3 shows the basic conversion timing for the ADS7835. The specific timing numbers are listed in Table I. There are several important items in Figure 3 which give the converter additional capabilities over typical 8-pin converters. First, the transition from sample mode to hold mode is synchronous to the falling edge of CONV and is not dependent on CLK. Second, the CLK input is not required to be continuous during the sample mode. After the conversion is complete,

the CLK may be kept LOW or HIGH.

The asynchronous nature of CONV to CLK raises some interesting possibilities, but also some design considerations. Figure 3 shows that CONV has timing restraints in relation to CLK ( $t_{CKCH}$  and  $t_{CKCS}$ ). However, if these times are violated (which could happen if CONV is completely asynchronous to CLK), the converter will perform a conversion correctly, but the exact timing of the conversion is indeterminate. Since the setup and hold time between CONV and CLK has been violated in this example, the start of conversion could vary by one clock cycle. (Note that the start of conversion can be detected by using a pull-up resistor on DATA. When DATA drops out of high impedance and goes LOW, the conversion has started and that

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{ACQ}$	Acquisition Time	350			ns
$t_{CONV}$	Conversion Time	1.625			$\mu$ s
$t_{CKP}$	Clock Period	125		5000	ns
$t_{CKL}$	Clock LOW	50			ns
$t_{CKH}$	Clock HIGH	50			ns
$t_{CKDH}$	Clock Falling to Current Data Bit No Longer Valid	5	15		ns
$t_{CKDS}$	Clock Falling to Next Data Valid		30	50	ns
$t_{CVL}$	CONV LOW	40			ns
$t_{CVH}$	CONV HIGH	40			ns
$t_{CKCH}$	CONV Hold after Clock Falls <sup>(1)</sup>	10			ns
$t_{CKCS}$	CONV Setup to Clock Falling <sup>(1)</sup>	10			ns
$t_{CKDE}$	Clock Falling to DATA Enabled		20	50	ns
$t_{CKDD}$	Clock Falling to DATA High Impedance		70	100	ns
$t_{CKSP}$	Clock Falling to Sample Mode		5		ns
$t_{CKPD}$	Clock Falling to Power-Down Mode		50		ns
$t_{CVHD}$	CONV Falling to Hold Mode (Aperture Delay)		5		ns
$t_{CVSP}$	CONV Rising to Sample Mode		5		ns
$t_{CVPU}$	CONV Rising to Full Power-up		50		ns
$t_{CVDD}$	CONV Changing State to DATA High Impedance		70	100	ns
$t_{CVPD}$	CONV Changing State to Power-Down Mode		50		ns
$t_{DRP}$	CONV Falling to Start of CLK (for hold droop < 0.1 LSB)			5	$\mu$ s

Note: (1) This timing is not required under some situations. See text for more information.

TABLE I. Timing Specifications ( $T_A = -40^{\circ}$ C to  $+85^{\circ}$ C,  $C_{LOAD} = 30$ pF).

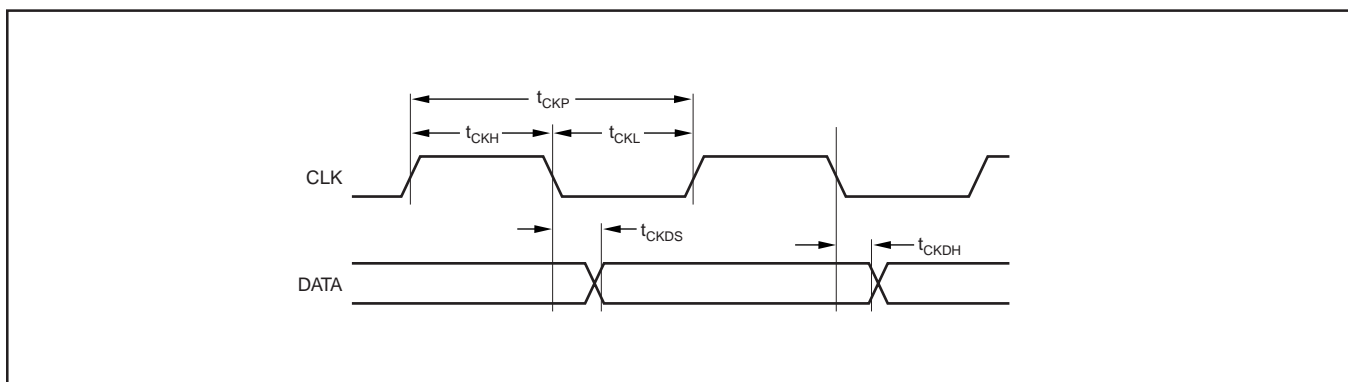


FIGURE 2. Serial Data and Clock Timing.

clock cycle is the first of the conversion.)

In addition, if CONV is completely asynchronous to CLK and CLK is continuous, there is the possibility that CLK will transition just prior to CONV going LOW. If this occurs faster than the 10ns indicated by  $t_{CKCH}$ , there is a chance that some digital feedthrough may be coupled onto the hold capacitor. This could cause a small offset error for that particular conversion.

Thus, there are two basic ways to operate the ADS7835. CONV can be synchronous to CLK and CLK can be continuous. This would be the typical situation when interfacing the converter to a digital signal processor. The second method involves having CONV asynchronous to CLK and gating the operation of CLK (a non-continuous clock). This method would be more typical of an SPI-like interface on a microcontroller. This method would also allow CONV to be generated by a trigger circuit and to initiate (after some delay) the start of CLK. These two methods are covered under the DSP Interfacing and SPI Interfacing sections of this data sheet.

### POWER-DOWN TIMING

The conversion timing shown in Figure 3 does not result in the ADS7835 going into the power-down mode. If the conversion rate of the device is high (approaching 500kHz), there is very little power that can be saved by using the power-down mode. However, since the power-down mode incurs no conversion penalty (the very first conversion is valid) at lower sample rates, significant power can be saved by allowing the device to go into power-down mode be-

tween conversions.

Figure 4 shows the typical method for placing the A/D into the power-down mode. If CONV is kept LOW during the conversion and is LOW at the start of the 13th clock cycle, the device enters the power-down mode. It remains in this mode until the rising edge of CONV. Note that CONV must be HIGH for at least  $t_{ACQ}$  in order to sample the signal properly as well as to power-up the internal nodes.

There are two different methods for clocking the ADS7835. The first involves scaling the CLK input in relation to the conversion rate. For example, an 8MHz input clock and the timing shown in Figure 3 results in a 500kHz conversion rate. Likewise, a 1.6MHz clock would result in a 100kHz conversion rate. The second method involves keeping the clock input as close to the maximum clock rate as possible and starting conversions as needed. This timing is similar to that shown in Figure 4. As an example, a 50kHz conversion rate would require 160 clock periods per conversion instead of the 16 clock periods used at 500kHz.

The main distinction between the two is the amount of time that the ADS7835 remains in power-down. In the first mode, the converter only remains in power-down for a small number of clock periods (depending on how many clock periods there are per each conversion). As the conversion rate scales, the converter always spends the same percentage of time in power-down. Since less power is drawn by the digital logic, there is a small decrease in power consumption, but it is very slight. This effect can be seen in the

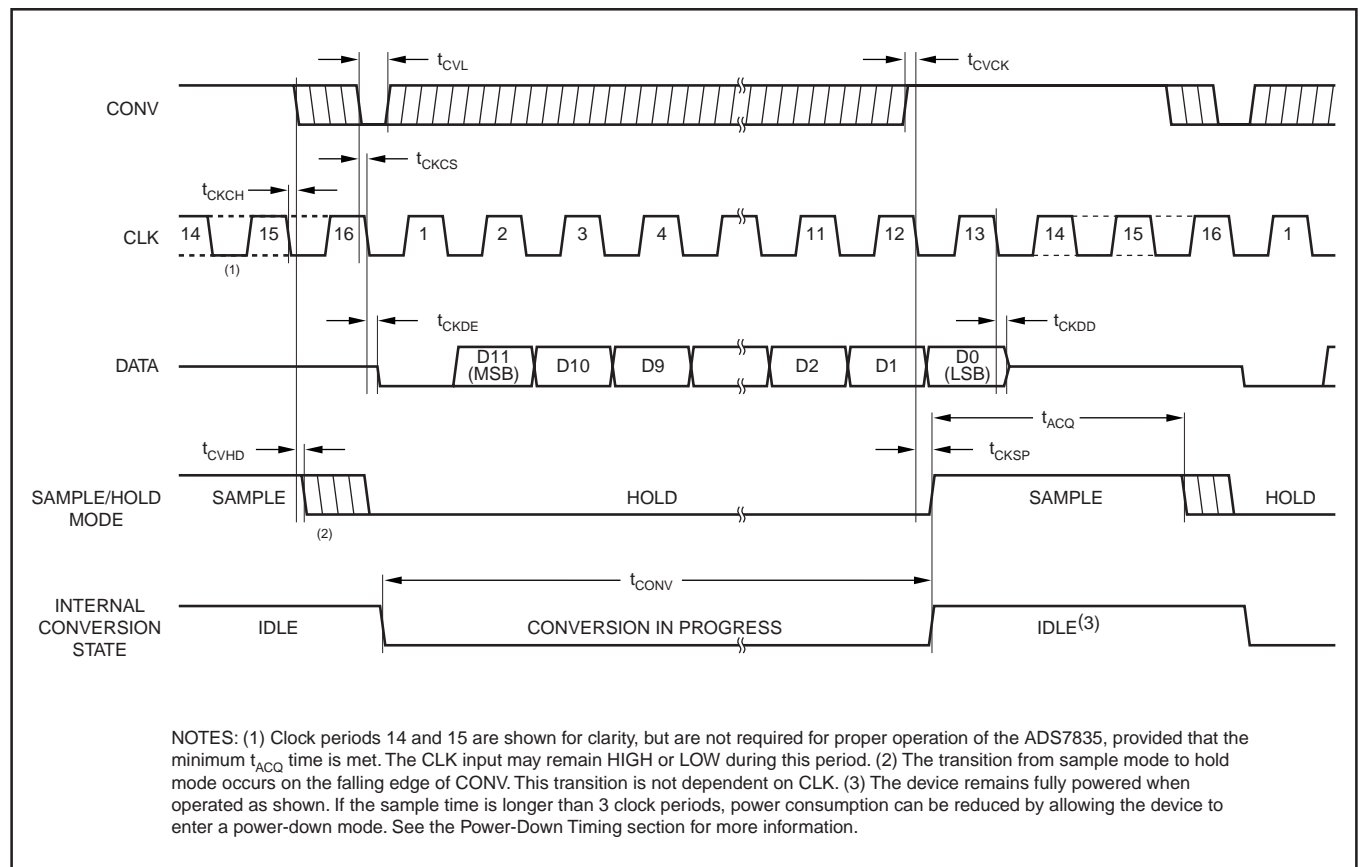


FIGURE 3. Basic Conversion Timing.

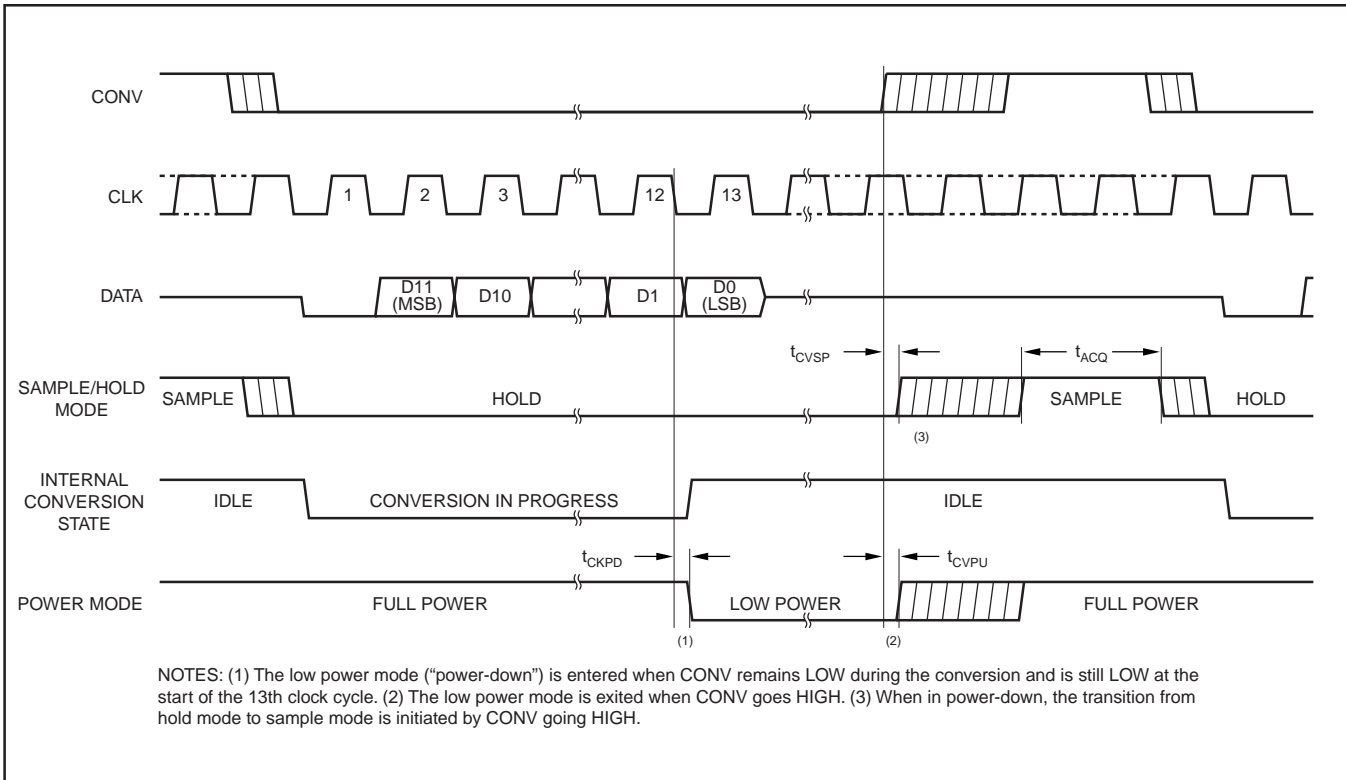


FIGURE 4. Power-Down Timing.

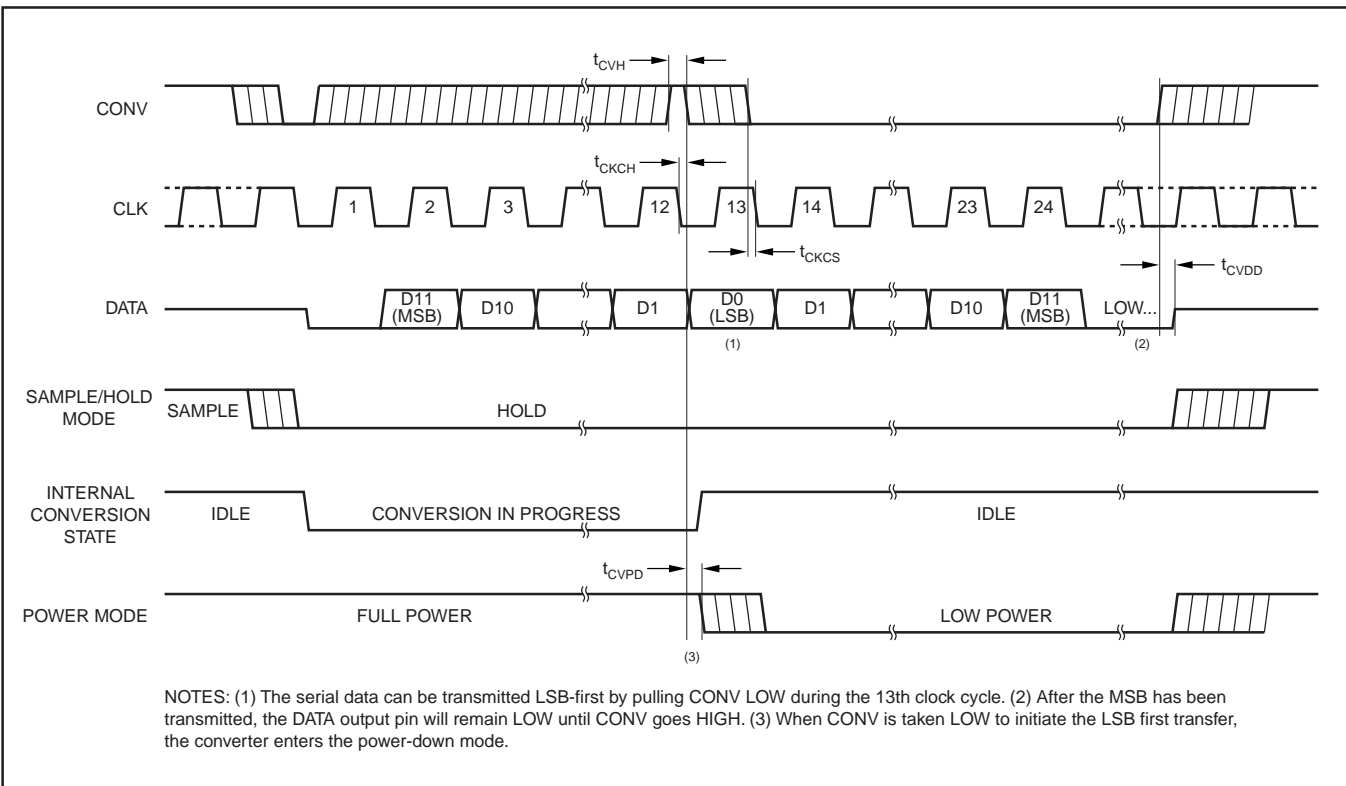


FIGURE 5. Serial Data "LSB-First" Timing.

typical performance curve "Supply Current vs Sample Rate."

In contrast, the second method (clocking at a fixed rate) means that each conversion takes X clock cycles. As the time between conversions get longer, the converter remains

in power-down an increasing percentage of time. This reduces total power consumption by a considerable amount. For example, a 50kHz conversion rate results in roughly 1/10 of the power (minus the reference) that is used at a

500kHz conversion rate.

$f_{\text{SAMPLE}}$	POWER WITH CLK = 16 • $f_{\text{SAMPLE}}$	POWER WITH CLK = 8MHz
500kHz	17.5mW	17.5mW
250kHz	16.5mW	13.5mW
100kHz	15.5mW	10.5mW

TABLE II. Power Consumption versus CLK Input.

Table II offers a look at the two different modes of operation and the difference in power consumption.

### LSB-FIRST DATA TIMING

Figure 5 shows a method to transmit the digital result in a LSB format. This mode is entered when CONV is pulled HIGH during the conversion (before the end of the 12th clock) and then pulled LOW during the 13th clock (when D0, the LSB, is being transmitted). The next 11 clocks then repeat the serial data, but in an LSB-first format. The converter enters the power-down mode during the 13th clock and resumes normal operation when CONV goes

HIGH.

### SHORT-CYCLE TIMING

The conversion currently in progress can be “short-cycled” with the technique shown in Figure 6. This term means that the conversion will terminate immediately, before all 12 bits have been decided. This can be a very useful feature when a resolution of 12 bits is not needed. An example would be when the converter is being used to monitor an input voltage until some condition is met. At that time, the full resolution of the converter would then be used. Short-cycling the conversion can result in a faster conversion rate or lower power dissipation.

There are several very important items shown in Figure 6. The conversion currently in progress is terminated when CONV is taken HIGH during the conversion and then taken LOW prior to  $t_{\text{CKCH}}$  before the start of the 13th clock cycle. Note that if CONV goes LOW during the 13th clock cycle, the LSB-first mode will be entered (Figure 5). Additionally, when CONV goes LOW, the DATA output immediately transitions to high impedance. If the output bit that is present during that clock period is needed, CONV must not go LOW until the bit has been properly latched into the receiving

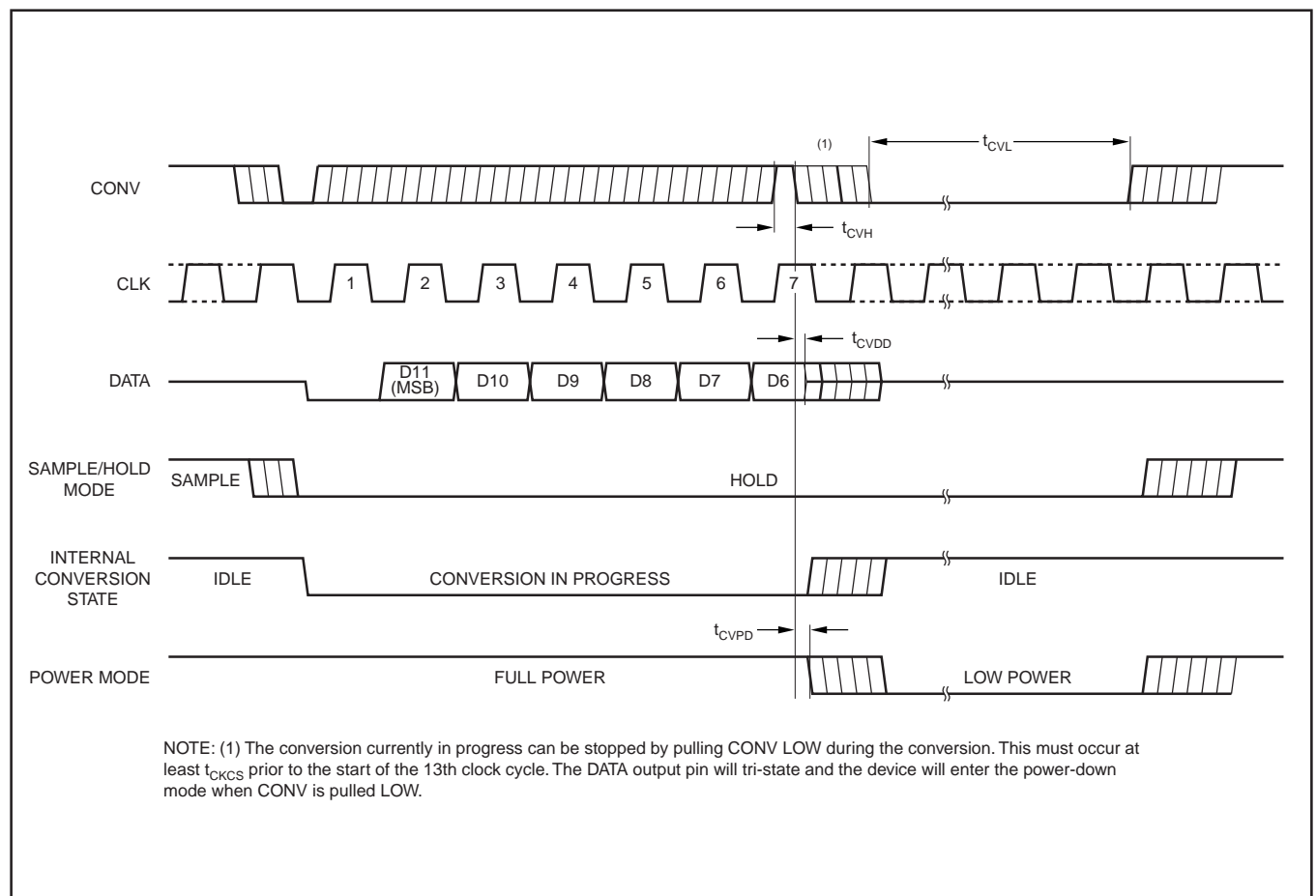


FIGURE 6. Short-Cycle Timing.

logic.

## DATA FORMAT

The ADS7835 output data is in Binary Two's Complement format as shown in Table III. This table shows the ideal output code for the given input voltage and does not include

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT	
Full-Scale Input Range Least Significant Bit (LSB) <sup>(2)</sup>	$-V_{REF}$ to $+V_{REF}$ <sup>(1)</sup>	<b>BINARY TWO'S COMPLEMENT</b>	
	$(-V_{REF}$ to $+V_{REF})/4096$	<b>BINARY CODE</b>	<b>HEX CODE</b>
+Full Scale	2.49878V	0111 1111 1111	7FF
Mid-Scale	0V	0000 0000 0000	000
Mid-Scale -1LSB	-0.00122V	1111 1111 1111	FFF
-Full Scale	-2.49878V	1000 0000 0000	800

NOTES: (1) -2.5V to +2.5V when the internal reference is used. (2) 1.22mV with a 2.5V reference.

TABLE III. Ideal Input Voltages and Output Codes.

the effects of offset, gain, or noise.

## DSP INTERFACING

Figure 7 shows a timing diagram that might be used with a typical digital signal processor such as a TI DSP. For the Buffered Serial Port (BSP) on the TMS320C54X family, CONV would be tied to BFSX, CLK would be tied to BCLKX, and DATA would be tied to BDR.

## SPI/QSPI INTERFACING

Figure 8 shows the timing diagram for a typical Serial Peripheral Interface (SPI) or Queued Serial Peripheral Interface (QSPI). Such interfaces are found on a number of microcontrollers from various manufacturers. CONV would be tied to a general purpose I/O pin (SPI) or to a PCX pin (QSPI), CLK would be tied to the serial clock, and DATA would be tied to the serial input data pin such as MISO (Master In Slave Out).

Note the time  $t_{DRP}$  shown in Figure 8. This represents the maximum amount of time between CONV going LOW and the start of the conversion clock. Since CONV going LOW places the S/H in the hold mode and because the hold capacitor loses charge over time, there is a requirement that time  $t_{DRP}$  be met as well as the maximum clock period

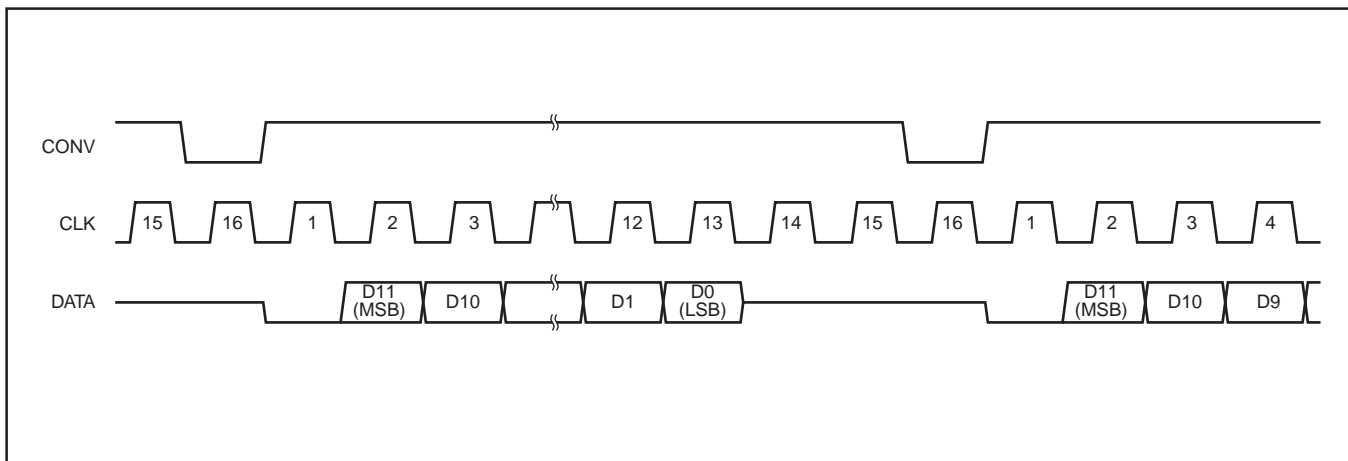


FIGURE 7. Typical DSP Interface Timing.

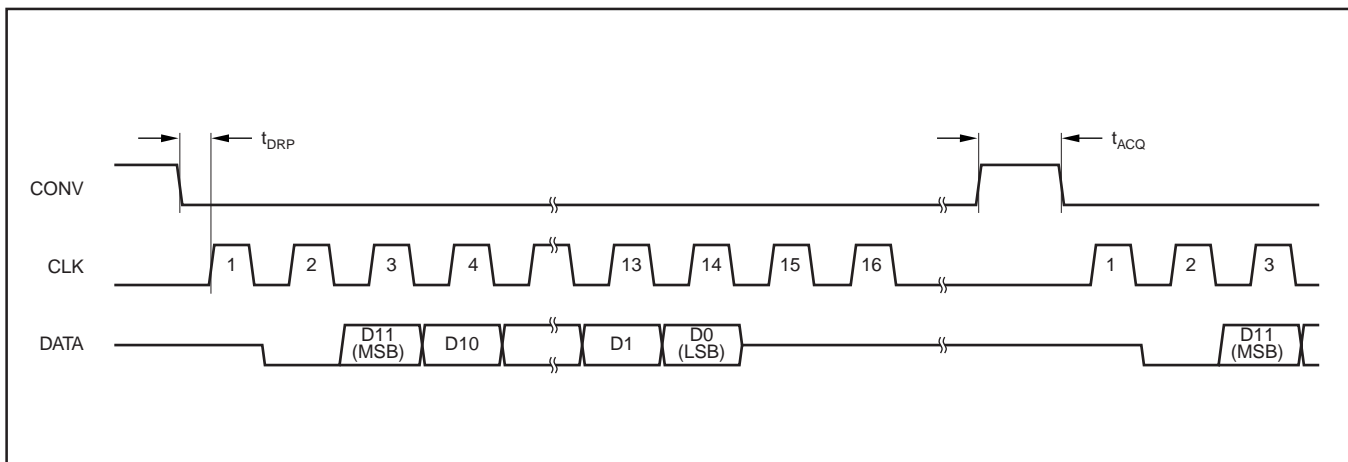


FIGURE 8. Typical SPI/QSPI Interface Timing.

( $t_{CKP}$ ).

## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7835 circuitry. This is particularly true if the CLK input is approaching the maximum input rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the CLK input.

With this in mind, power to the ADS7835 should be clean and well bypassed. A 0.1 $\mu$ F ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1 $\mu$ F to 10 $\mu$ F capacitor is recommended. If needed, an even

larger capacitor and a 5 $\Omega$  or 10 $\Omega$  series resistor may be used to lowpass filter a noisy supply.

The ADS7835 draws very little current from an external reference on average as the reference voltage is internally buffered. However, glitches from the conversion process appear at the  $V_{REF}$  input and the reference source must be able to handle this. Whether the reference is internal or external, the  $V_{REF}$  pin should be bypassed with a 0.1 $\mu$ F capacitor. An additional larger capacitor may also be used, if desired. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7835E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B35	<a href="#">Samples</a>
ADS7835E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B35	<a href="#">Samples</a>
ADS7835E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B35	<a href="#">Samples</a>
ADS7835E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B35	<a href="#">Samples</a>
ADS7835EB/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B35	<a href="#">Samples</a>
ADS7835EB/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		B35	<a href="#">Samples</a>

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7835E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7835E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7835EB/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7835E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7835E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
ADS7835EB/250	VSSOP	DGK	8	250	210.0	185.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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