



**THE DATASHEET OF
ADC161S626CIMME/NOPB**



ADC161S626 16-Bit, 50 to 250 kSPS, Differential Input, MicroPower ADC

1 Features

- 16-bit Resolution With No Missing Codes
- Ensured Performance from 50 to 250 kSPS
- $\pm 0.003\%$ Signal Span Accuracy
- Separate Digital Input/Output Supply
- True Differential Input
- External Voltage Reference Range of 0.5 V to V_A
- Zero-Power Track Mode with 0- μ sec Wake-up Delay
- Wide Input Common-mode Voltage Range of 0 V to V_A
- SPI/QSPI™/MICROWIRE™ Compatible Serial Interface
- Operating Temperature Range of -40°C to $+85^\circ\text{C}$
- Small VSSOP-10 Package
- Key Specifications
 - Conversion Rate 50 to 250 kSPS
 - DNL $+0.8 / -0.5$ LSB
 - INL ± 0.8 LSB
 - Offset Error Temp Drift $2.5 \mu\text{V}/^\circ\text{C}$
 - Gain Error Temp Drift $0.3 \text{ ppm}/^\circ\text{C}$
 - SNR 93.2 dBc
 - THD – 104 dBc
 - Power Consumption
 - 10 kSPS, 5 V 0.24 mW
 - 200 kSPS, 5 V 5.3 mW
 - 250 kSPS, 5 V 5.8 mW
 - Power-Down, 5 V 10 μW

2 Applications

- Direct Sensor Interface
- I/O Modules
- Data Acquisition
- Portable Systems
- Motor Control
- Medical Instruments
- Instrumentation and Control Systems

3 Description

The ADC161S626 is a 16-bit successive-approximation register (SAR) Analog-to-Digital converter (ADC) with a maximum sampling rate of 250 kSPS. The ADC161S626 has a minimum signal span accuracy of $\pm 0.003\%$ over the temperature range of -40°C to $+85^\circ\text{C}$. The converter features a differential analog input with an excellent common-mode signal rejection ratio of 85 dB, making the ADC161S626 suitable for noisy environments.

The ADC161S626 operates with a single analog supply (V_A) and a separate digital input/output (V_{IO}) supply. V_A can range from 4.5 V to 5.5 V and V_{IO} can range from 2.7 V to 5.5 V. This allows a system designer to maximize performance and minimize power consumption by operating the analog portion of the ADC at a V_A of 5 V while interfacing with a 3.3-V controller. The serial data output is binary 2's complement and is SPI compatible.

The performance of the ADC161S626 is ensured over temperature at clock rates of 1 MHz to 5 MHz and reference voltages of 2.5 V to 5.5 V. The ADC161S626 is available in a small 10-lead VSSOP package. The high accuracy, differential input, low power consumption, and small size make the ADC161S626 ideal for direct connection to bridge sensors and transducers in battery operated systems or remote data acquisition applications.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| ADC161S626 | VSSOP (10) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic

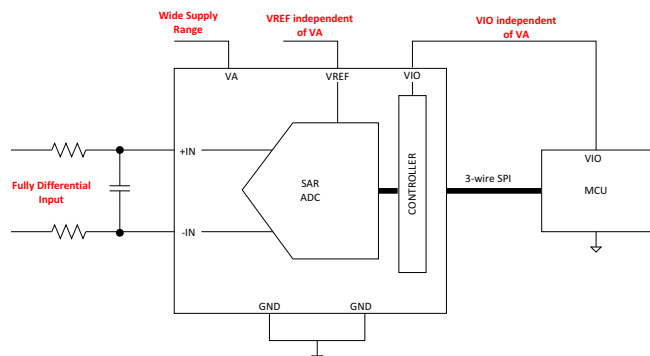


Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 7.4 Device Functional Modes..... | 18 |
| 2 Applications | 1 | 8 Application and Implementation | 22 |
| 3 Description | 1 | 8.1 Application Information..... | 22 |
| 4 Revision History | 2 | 8.2 Typical Application | 22 |
| 5 Pin Configuration and Functions | 3 | 9 Power Supply Recommendations | 24 |
| 6 Specifications | 3 | 9.1 Analog and Digital Power Supplies..... | 24 |
| 6.1 Absolute Maximum Ratings | 3 | 9.2 Voltage Reference | 24 |
| 6.2 ESD Ratings..... | 4 | 10 Layout | 24 |
| 6.3 Recommended Operating Conditions..... | 4 | 10.1 Layout Guidelines | 24 |
| 6.4 Thermal Information | 4 | 10.2 Layout Example | 25 |
| 6.5 Converter Electrical Characteristics..... | 5 | 11 Device and Documentation Support | 26 |
| 6.6 Timing Requirements..... | 7 | 11.1 Device Support..... | 26 |
| 6.7 Typical Characteristics..... | 9 | 11.2 Trademarks | 27 |
| 7 Detailed Description | 15 | 11.3 Electrostatic Discharge Caution..... | 27 |
| 7.1 Overview | 15 | 11.4 Glossary | 27 |
| 7.2 Functional Block Diagram | 15 | 12 Mechanical, Packaging, and Orderable Information | 27 |
| 7.3 Feature Description..... | 15 | | |

4 Revision History

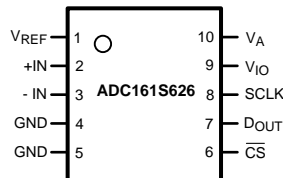
Changes from Revision C (March 2013) to Revision D

Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**

5 Pin Configuration and Functions

10 Pins
VSSOP Package
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-------|---|
| NO. | NAME | | |
| 1 | V_{REF} | I | Voltage Reference $0.5\text{ V} < V_{REF} < V_A$ |
| 2 | +IN | I | Non-Inverting Input |
| 3 | -IN | I | Inverting Input |
| 4 | GND | Power | Ground |
| 5 | GND | Power | Ground |
| 6 | \overline{CS} | I | Chip Select Bar |
| 7 | D_{OUT} | O | Serial Data Output |
| 8 | SCLK | I | Serial Clock |
| 9 | V_{IO} | Power | Digital Input/Output Power $2.7\text{ V} < V_{REF} < 5.5\text{ V}$ |
| 10 | V_A | Power | Analog Power $4.5\text{ V} < V_{REF} < 5.5\text{ V}$ |

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

| | MIN | MAX | UNIT |
|---|------|--------------------|------------------|
| Analog Supply Voltage V_A | -0.3 | 6.5 | V |
| Digital I/O Supply Voltage V_{IO} | -0.3 | 6.5 | V |
| Voltage on Any Analog Input Pin to GND | -0.3 | $(V_A + 0.3)$ | V |
| Voltage on Any Digital Input Pin to GND | -0.3 | $(V_{IO} + 0.3)$ | V |
| Input Current at Any Pin ⁽⁴⁾ | -10 | 10 | mA |
| Package Input Current ⁽⁴⁾ | -50 | 50 | mA |
| Power Consumption at $T_A = 25^\circ\text{C}$ | | See ⁽⁵⁾ | |
| Junction Temperature | | 150 | $^\circ\text{C}$ |
| Storage temperature, T_{stg} | -65 | 150 | $^\circ\text{C}$ |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (4) When the input voltage at any pin exceeds the power supplies (that is, $V_{IN} < \text{GND}$ or $V_{IN} > V_A$), the current at that pin should be limited to 10 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.
- (5) The absolute maximum junction temperature (T_{Jmax}) for this device is 150°C . The maximum allowable power dissipation is dictated by T_{Jmax} , the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{Jmax} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC161S626 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2500 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1250 | |
| | Machine model (MM) | 250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|-------------------------------------|-------------------------------|------------|------|
| Operating Temperature Range | -40 | 85 | °C |
| Supply Voltage, V_A | 4.5 | 5.5 | V |
| Supply Voltage, V_{IO} | 2.7 | 5.5 | V |
| Reference Voltage, V_{REF} | 0.5 | V_A | V |
| Analog Input Pins Voltage Range | 0 | V_A | V |
| Differential Analog Input Voltage | $-V_{REF}$ | $+V_{REF}$ | V |
| Input Common-Mode Voltage, V_{CM} | See Figure 44 | | |
| Digital Input Pins Voltage Range | 0 | V_{IO} | V |
| Clock Frequency | 1 | 5 | MHz |

(1) All voltages are measured with respect to GND = 0V, unless otherwise specified.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | ADC161S626 | UNIT |
|-------------------------------|--|------------|------|
| | | DGS | |
| | | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 163 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 57 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 82 | |
| Ψ_{JT} | Junction-to-top characterization parameter | 6 | |
| Ψ_{JB} | Junction-to-board characterization parameter | 81 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Converter Electrical Characteristics

The following specifications apply for $V_A = 4.5\text{ V}$ to 5.5 V , $V_{IO} = 2.7\text{ V}$ to 5.5 V , and $V_{REF} = 2.5\text{ V}$ to 5.5 V for $f_{SCLK} = 1\text{ MHz}$ to 4 MHz or $V_{REF} = 4.5\text{ V}$ to 5.5 V for $f_{SCLK} = 1\text{ MHz}$ to 5 MHz ; $f_{IN} = 20\text{ kHz}$, and $C_L = 25\text{ pF}$, unless otherwise noted. Maximum and minimum values apply for $T_A = T_{MIN}$ to T_{MAX} ; the typical values are tested at $T_A = 25^\circ\text{C}$.⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---------------------------------------|--|---------------------|-----------|---------------------|--------|
| STATIC CONVERTER CHARACTERISTICS | | | | | | |
| | Resolution with No Missing Codes | | | | 16 | Bits |
| DNL | Differential Non-Linearity | | -1 | -0.5/+0.8 | +2 | LSB |
| INL | Integral Non-Linearity | | -2 | ±0.8 | +2 | LSB |
| OE | Offset Error | $V_{REF} = 2.5\text{ V}$ | -1 | -0.1 | +1 | mV |
| | | $V_{REF} = 5\text{ V}$ | | -0.4 | | mV |
| OE _{DRIFT} | Offset Error Temperature Drift | $V_{REF} = 2.5\text{ V}$ | | 3.7 | | µV/°C |
| | | $V_{REF} = 5\text{ V}$ | | 2.5 | | µV/°C |
| FSE | Positive Full-Scale Error | | -0.03 | -0.003 | 0.03 | %FS |
| | Negative Full-Scale Error | | -0.03 | -0.002 | 0.03 | %FS |
| GE | Positive Gain Error | | -0.02 | -0.002 | 0.02 | %FS |
| | Negative Gain Error | | -0.02 | -0.0001 | 0.02 | %FS |
| GE _{DRIFT} | Gain Error Temperature Drift | | | 0.3 | | ppm/°C |
| DYNAMIC CONVERTER CHARACTERISTICS | | | | | | |
| SINAD | Signal-to-Noise Plus Distortion Ratio | $V_{REF} = 2.5\text{ V}$ | 85 | 88 | | dBc |
| | | $V_{REF} = 4.5\text{ V}$ to 5.5 V | 89 | 93.0 | | dBc |
| SNR | Signal-to-Noise Ratio | $V_{REF} = 2.5\text{ V}$ | 85 | 88 | | dBc |
| | | $V_{REF} = 4.5\text{ V}$ to 5.5 V | 89 | 93.2 | | dBc |
| THD | Total Harmonic Distortion | $V_{REF} = 2.5\text{ V}$ | | -104 | | dBc |
| | | $V_{REF} = 4.5\text{ V}$ to 5.5 V | | -106 | | dBc |
| SFDR | Spurious-Free Dynamic Range | $V_{REF} = 2.5\text{ V}$ | | 108 | | dBc |
| | | $V_{REF} = 4.5\text{ V}$ to 5.5 V | | 111 | | dBc |
| ENOB | Effective Number of Bits | $V_{REF} = 2.5\text{ V}$ | 13.8 | 14.3 | | bits |
| | | $V_{REF} = 4.5\text{ V}$ to 5.5 V | 14.5 | 15.2 | | bits |
| FPBW | -3 dB Full Power Bandwidth | Output at 70.7%FS with FS Differential Input | | 26 | | MHz |
| ANALOG INPUT CHARACTERISTICS | | | | | | |
| V _{IN} | Differential Input Range | | -V _{REF} | | +V _{REF} | V |
| I _{INA} | Analog Input Current | \overline{CS} high | -1 | | 1 | µA |
| | | $V_{REF} = 5\text{ V}$, $V_{IN} = 0\text{ V}$, $f_S = 50\text{ kSPS}$ | | 3.2 | | nA |
| | | $V_{REF} = 5\text{ V}$, $V_{IN} = 0\text{ V}$, $f_S = 200\text{ kSPS}$ | | 10.3 | | nA |
| C _{INA} | Input Capacitance (+IN or -IN) | In Acquisition Mode | | 20 | | pF |
| | | In Conversion Mode | | 4 | | pF |
| CMRR | Common Mode Rejection Ratio | See the Specification Definitions for the test condition | | 85 | | dB |
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| V _{IH} | Input High Voltage | $f_{IN} = 0\text{ Hz}$ | $0.7 \times V_{IO}$ | 1.9 | | V |
| V _{IL} | Input Low Voltage | $f_{IN} = 0\text{ Hz}$ | | 1.7 | $0.3 \times V_{IO}$ | V |
| I _{IND} | Digital Input Current | | -1 | | 1 | µA |
| C _{IND} | Input Capacitance | | | | 4 | pF |

(1) Typical values are at $T_J = 25^\circ\text{C}$ and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).

Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = 4.5\text{ V}$ to 5.5 V , $V_{IO} = 2.7\text{ V}$ to 5.5 V , and $V_{REF} = 2.5\text{ V}$ to 5.5 V for $f_{SCLK} = 1\text{ MHz}$ to 4 MHz or $V_{REF} = 4.5\text{ V}$ to 5.5 V for $f_{SCLK} = 1\text{ MHz}$ to 5 MHz ; $f_{IN} = 20\text{ kHz}$, and $C_L = 25\text{ pF}$, unless otherwise noted. Maximum and minimum values apply for $T_A = T_{MIN}$ to T_{MAX} ; the typical values are tested at $T_A = 25^\circ\text{C}$.⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|---|---|----------------|-----------------------|-------|---------------|
| DIGITAL OUTPUT CHARACTERISTICS | | | | | | |
| V_{OH} | Output High Voltage | $I_{SOURCE} = 200\ \mu\text{A}$ | $V_{IO} - 0.2$ | $V_{IO} - 0.03$ | | V |
| | | $I_{SOURCE} = 1\text{ mA}$ | | $V_{IO} - 0.09$ | | V |
| V_{OL} | Output Low Voltage | $I_{SOURCE} = 200\ \mu\text{A}$ | | 0.01 | 0.4 | V |
| | | $I_{SOURCE} = 1\text{ mA}$ | | 0.07 | | V |
| I_{OZH}, I_{OZL} | TRI-STATE Leakage Current | Force 0V or V_A | -1 | | 1 | μA |
| C_{OUT} | TRI-STATE Output Capacitance | Force 0V or V_A | | 4 | | pF |
| | Output Coding | | | Binary 2's Complement | | |
| POWER SUPPLY CHARACTERISTICS | | | | | | |
| V_A | Analog Supply Voltage Range | | 4.5 | 5 | 5.5 | V |
| V_{IO} | Digital Input/Output Supply Voltage Range | (2) | 2.7 | 3 | 5.5 | V |
| V_{REF} | Reference Voltage Range | | 0.5 | 5 | V_A | V |
| I_{VA} (Conv) | Analog Supply Current, Conversion Mode | $V_A = 5\text{ V}$, $f_{SCLK} = 4\text{ MHz}$, $f_S = 200\text{ kSPS}$ | | 1060 | | μA |
| | | $V_A = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_S = 250\text{ kSPS}$ | | 1160 | 1340 | μA |
| I_{VIO} (Conv) | Digital I/O Supply Current, Conversion Mode | $V_{IO} = 3\text{ V}$, $f_{SCLK} = 4\text{ MHz}$, $f_S = 200\text{ kSPS}$ | | 80 | | μA |
| | | $V_{IO} = 3\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_S = 250\text{ kSPS}$ | | 100 | | μA |
| I_{VREF} (Conv) | Reference Current, Conversion Mode | $V_A = 5\text{ V}$, $f_{SCLK} = 4\text{ MHz}$, $f_S = 200\text{ kSPS}$ | | 80 | | μA |
| | | $V_A = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_S = 250\text{ kSPS}$ | | 100 | 170 | μA |
| I_{VA} (PD) | Analog Supply Current, Power Down Mode (\overline{CS} high) | $f_{SCLK} = 5\text{ MHz}$, $V_A = 5\text{ V}$ | | 7 | | μA |
| | | $f_{SCLK} = 0\text{ Hz}$, $V_A = 5\text{ V}$ ⁽³⁾ | | 2 | 3 | μA |
| I_{VIO} (PD) | Digital I/O Supply Current, Power Down Mode (\overline{CS} high) | $f_{SCLK} = 5\text{ MHz}$, $V_{IO} = 3\text{ V}$ | | 1 | | μA |
| | | $f_{SCLK} = 0\text{ Hz}$, $V_{IO} = 3\text{ V}$ ⁽³⁾ | | 0.3 | 0.5 | μA |
| I_{VREF} (PD) | Reference Current, Power Down Mode (\overline{CS} high) | $f_{SCLK} = 5\text{ MHz}$, $V_{REF} = 5\text{ V}$ | | 0.5 | | μA |
| | | $f_{SCLK} = 0\text{ Hz}$, $V_{REF} = 5\text{ V}$ ⁽³⁾ | | 0.5 | 0.7 | μA |
| PWR (Conv) | Power Consumption, Conversion Mode | $V_A = 5\text{ V}$, $f_{SCLK} = 4\text{ MHz}$, $f_S = 200\text{ kSPS}$, and $f_{IN} = 20\text{ kHz}$, | | 5.3 | | mW |
| | | $V_A = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_S = 250\text{ kSPS}$, and $f_{IN} = 20$ | | 5.8 | 6.7 | mW |
| PWR (PD) | Power Consumption, Power Down Mode (\overline{CS} high) | $f_{SCLK} = 5\text{ MHz}$, $V_A = 5.0\text{ V}$ ⁽³⁾ | | 35 | | μW |
| | | $f_{SCLK} = 0\text{ Hz}$, $V_A = 5.0\text{ V}$ ⁽³⁾ | | 10 | 15 | μW |
| PSRR | Power Supply Rejection Ratio | See the Specification Definitions for the test condition | | -78 | | dB |
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| f_{SCLK} | Maximum Clock Frequency | | 1 | | 5 | MHz |
| f_S | Maximum Sample Rate | | (4)50 | | 250 | kSPS |
| t_{ACQ} | Acquisition/Track Time | | 600 | | | ns |
| t_{CONV} | Conversion/Hold Time | | | | 17 | SCLK cycles |
| t_{AD} | Aperture Delay | See the Specification Definitions | | 6 | | ns |

(2) The value of V_{IO} is independent of the value of V_A . For example, V_{IO} could be operating at 5.5 V while V_A is operating at 4.5 V or V_{IO} could be operating at 2.7 V while V_A is operating at 5.5 V .

(3) This parameter is ensured by design and/or characterization and is not tested in production.

(4) While the maximum sample rate is $f_{SCLK} / 20$, the actual sample rate may be lower than this by having the \overline{CS} rate slower than $f_{SCLK} / 20$.

6.6 Timing Requirements

The following specifications apply for $V_A = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.5\text{ V to }5.5\text{ V}$, $f_{SCLK} = 1\text{ Mz to }5\text{ MHz}$, and $C_L = 25\text{ pF}$, unless otherwise noted. Maximum and minimum values apply for $T_A = T_{MIN}$ to T_{MAX} ; the typical values are tested at $T_A = 25^\circ\text{C}$.⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|-----------|--|-----|-----|-----|------|
| t_{CSS} | \overline{CS} Setup Time prior to an SCLK rising edge | 8 | 3 | | ns |
| t_{CSH} | \overline{CS} Hold Time after an SCLK rising edge | 8 | 3 | | |
| t_{DH} | D_{OUT} Hold Time after an SCLK falling edge | 6 | 11 | | ns |
| t_{DA} | D_{OUT} Access Time after an SCLK falling edge | | 18 | 41 | ns |
| t_{DIS} | D_{OUT} Disable Time after the rising edge of \overline{CS} ⁽²⁾ | | 20 | 30 | ns |
| t_{CS} | Minimum \overline{CS} Pulse Width | 20 | | | ns |
| t_{EN} | D_{OUT} Enable Time after the 2nd falling edge of SCLK | | 20 | 70 | ns |
| t_{CH} | SCLK High Time | 20 | | | ns |
| t_{CL} | SCLK Low Time | 20 | | | ns |
| t_r | D_{OUT} Rise Time | | 7 | | ns |
| t_f | D_{OUT} Fall Time | | 7 | | ns |

- (1) Typical values are at $T_J = 25^\circ\text{C}$ and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
- (2) t_{DIS} is the time for D_{OUT} to change 10% while being loaded by the Timing Test Circuit.

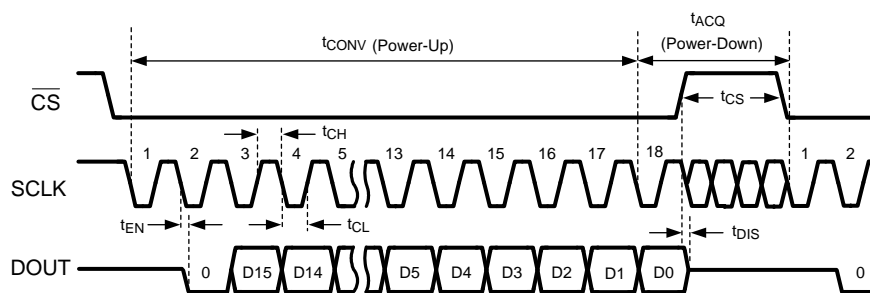


Figure 1. ADC161S626 Single Conversion Timing Diagram

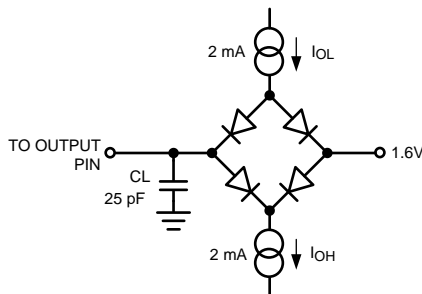


Figure 2. Timing Test Circuit

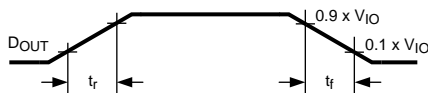
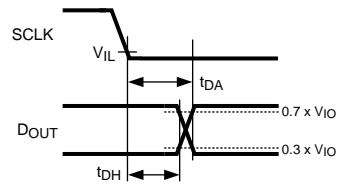
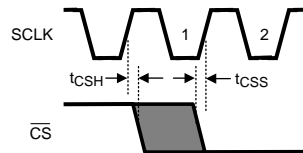
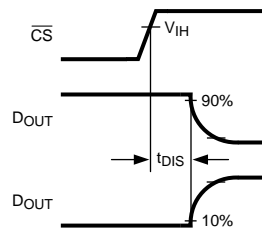


Figure 3. D_{OUT} Rise and Fall Times


Figure 4. D_{OUT} Hold and Access Times

Figure 5. Valid \overline{CS} Assertion Times

Figure 6. Voltage Waveform for t_{DIS}

6.7 Typical Characteristics

$V_A = V_{IO} = V_{REF} = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_{SAMPLE} = 250\text{ kSPS}$, $T_A = +25^\circ\text{C}$, and $f_{IN} = 20\text{ kHz}$ unless otherwise stated.

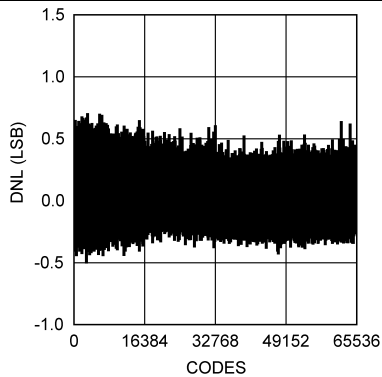


Figure 7. DNL - 250 kSPS

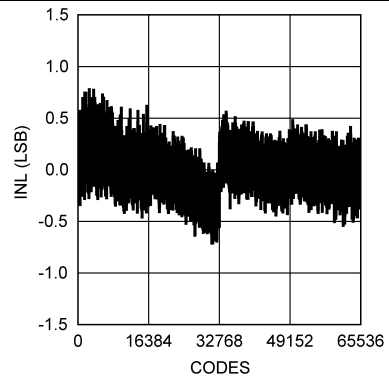


Figure 8. INL - 250 kSPS

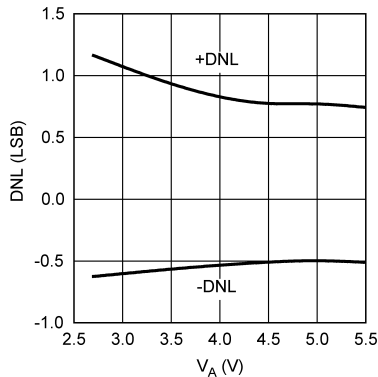


Figure 9. DNL vs. V_A

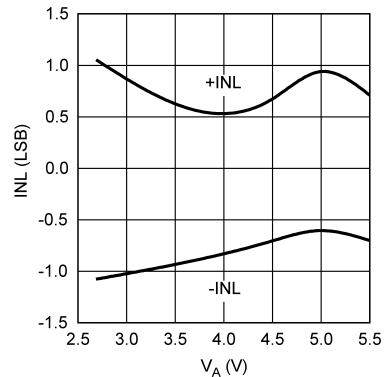


Figure 10. INL vs. V_A

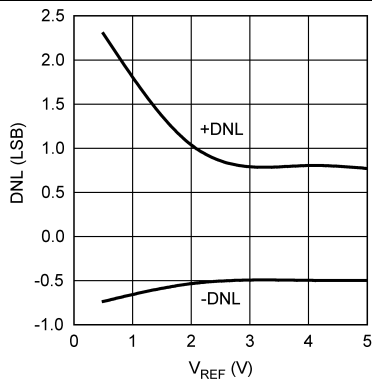


Figure 11. DNL vs. V_{REF}

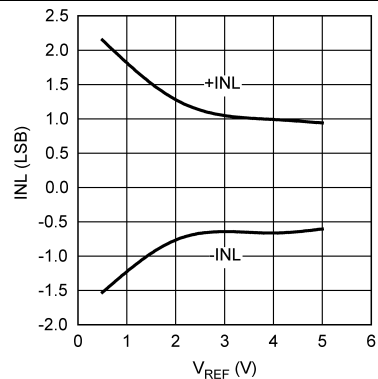


Figure 12. INL vs. V_{REF}

Typical Characteristics (continued)

$V_A = V_{IO} = V_{REF} = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_{SAMPLE} = 250\text{ kSPS}$, $T_A = +25^\circ\text{C}$, and $f_{IN} = 20\text{ kHz}$ unless otherwise stated.

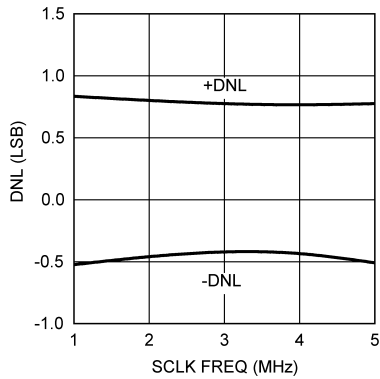


Figure 13. DNL vs. SCLK Frequency

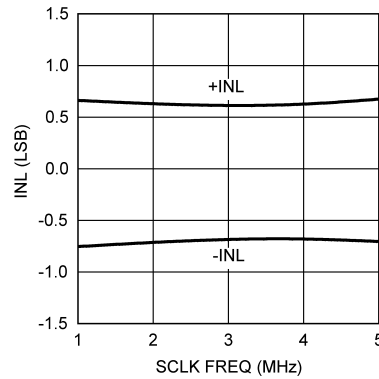


Figure 14. INL vs. SCLK Frequency

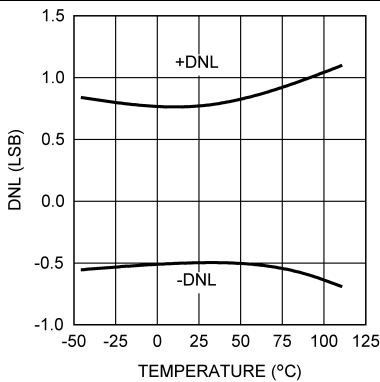


Figure 15. DNL vs. Temperature

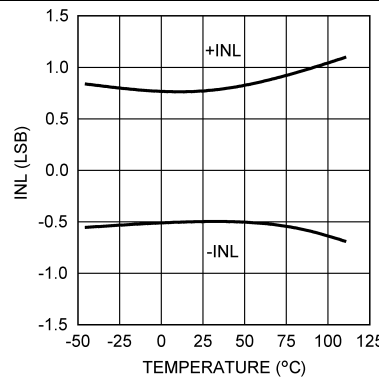


Figure 16. INL vs. Temperature

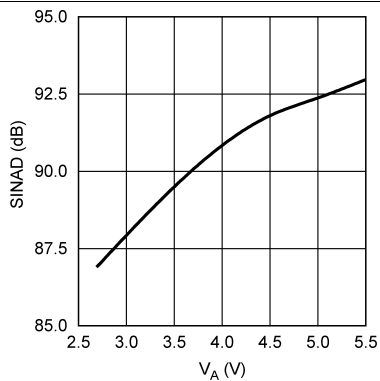


Figure 17. SINAD vs. V_A

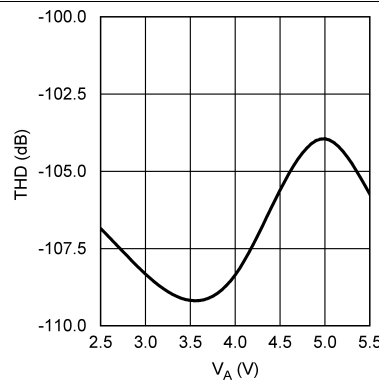


Figure 18. THD vs. V_A

Typical Characteristics (continued)

$V_A = V_{IO} = V_{REF} = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_{SAMPLE} = 250\text{ kSPS}$, $T_A = +25^\circ\text{C}$, and $f_{IN} = 20\text{ kHz}$ unless otherwise stated.

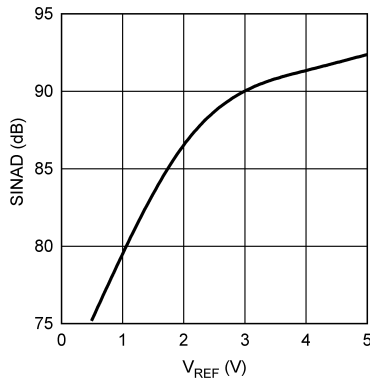


Figure 19. SINAD vs. VREF

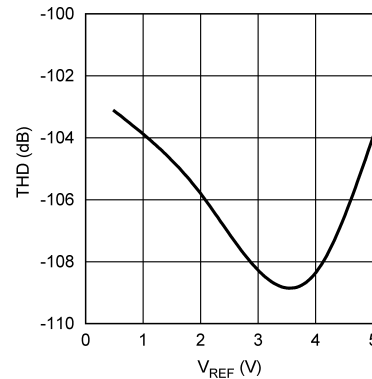


Figure 20. THD vs. VREF

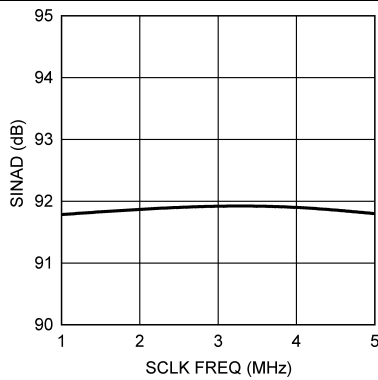


Figure 21. SINAD vs. SCLK Frequency

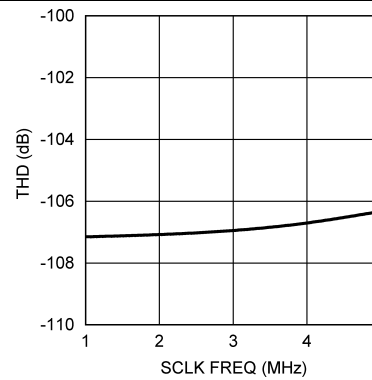


Figure 22. THD vs. SCLK Frequency

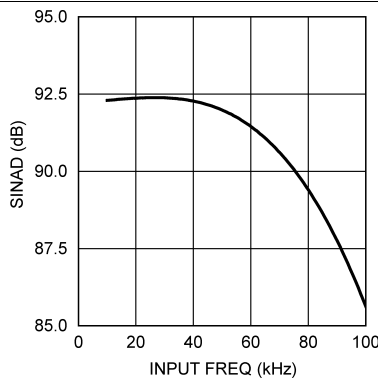


Figure 23. SINAD vs. INPUT Frequency

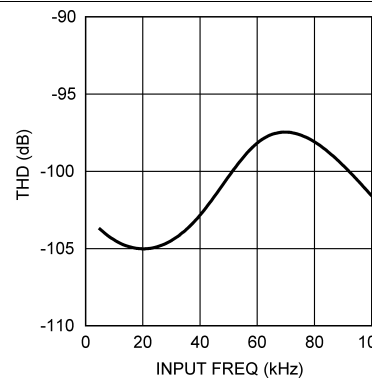
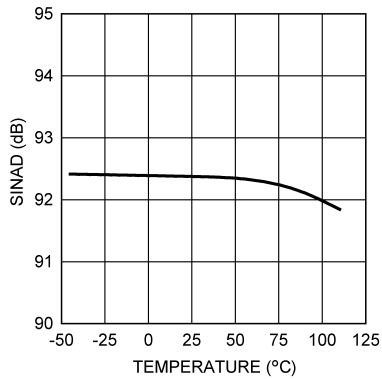
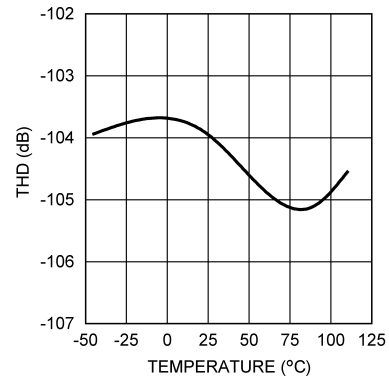
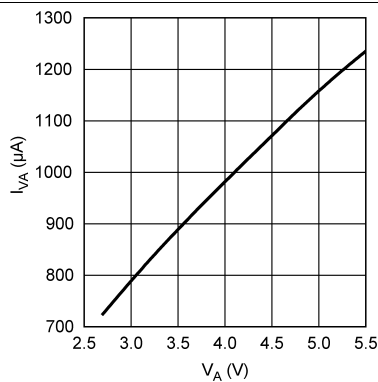
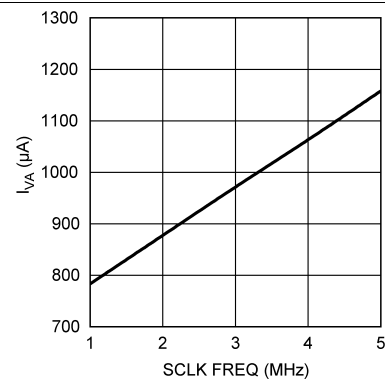
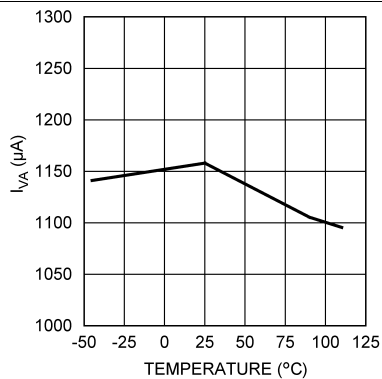
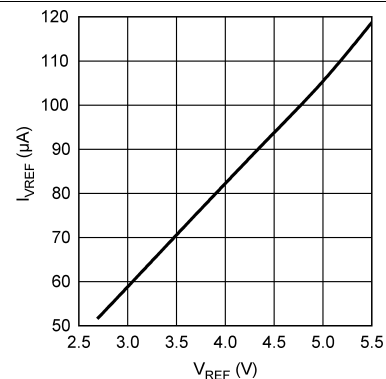


Figure 24. THD vs. INPUT Frequency

Typical Characteristics (continued)
 $V_A = V_{IO} = V_{REF} = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_{SAMPLE} = 250\text{ kSPS}$, $T_A = +25^\circ\text{C}$, and $f_{IN} = 20\text{ kHz}$ unless otherwise stated.

Figure 25. SINAD vs. Temperature

Figure 26. THD vs. Temperature

Figure 27. V_A Current vs. V_A

Figure 28. V_A Current vs. SCLK Frequency

Figure 29. V_A Current vs. Temperature

Figure 30. V_{REF} Current vs. V_{REF}

Typical Characteristics (continued)

$V_A = V_{IO} = V_{REF} = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_{SAMPLE} = 250\text{ kSPS}$, $T_A = +25^\circ\text{C}$, and $f_{IN} = 20\text{ kHz}$ unless otherwise stated.

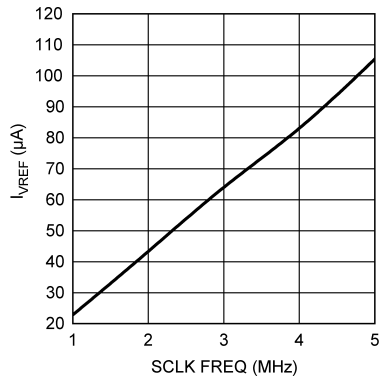


Figure 31. V_{REF} Current vs. SCLK Frequency

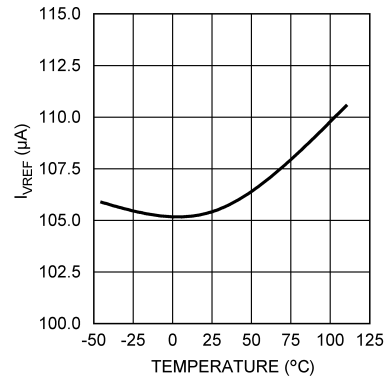


Figure 32. V_{REF} Current vs. Temperature

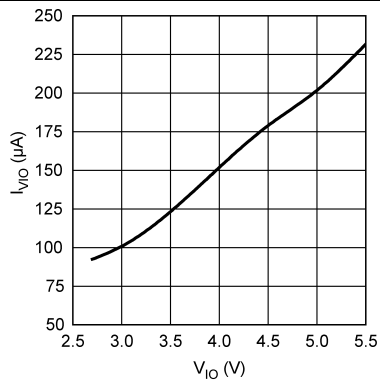


Figure 33. V_{IO} Current vs. V_{IO}

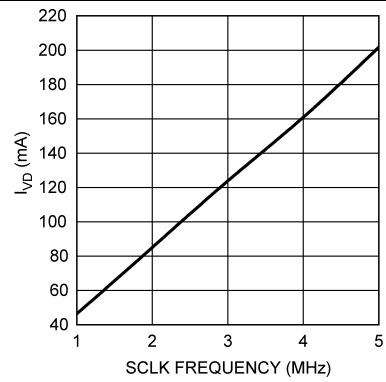


Figure 34. V_{IO} Current vs. SCLK Frequency

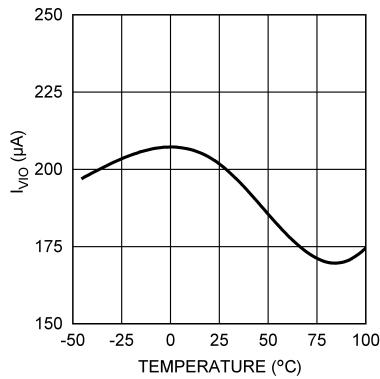


Figure 35. V_{IO} Current vs. Temperature

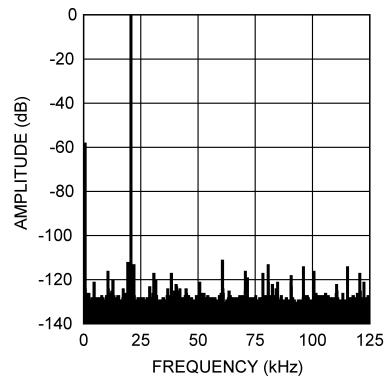


Figure 36. Spectral Response - 250 kSPS

ADC161S626

SNAS468D – SEPTEMBER 2008 – REVISED DECEMBER 2014

www.ti.com

Typical Characteristics (continued)

$V_A = V_{IO} = V_{REF} = 5\text{ V}$, $f_{SCLK} = 5\text{ MHz}$, $f_{SAMPLE} = 250\text{ kSPS}$, $T_A = +25^\circ\text{C}$, and $f_{IN} = 20\text{ kHz}$ unless otherwise stated.

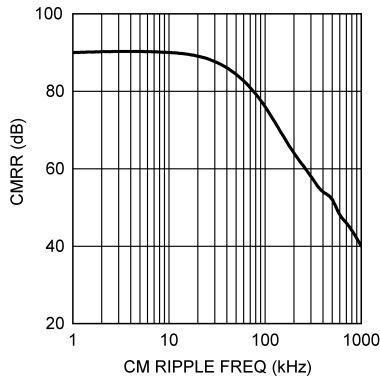


Figure 37. Analog Input CMRR vs. Frequency

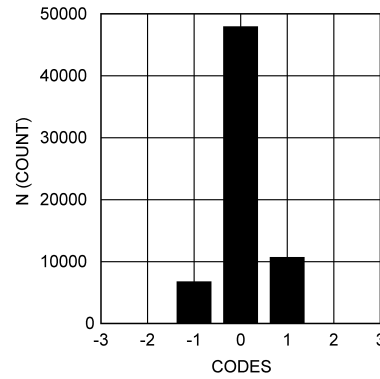


Figure 38. Noise Histogram at Code Center

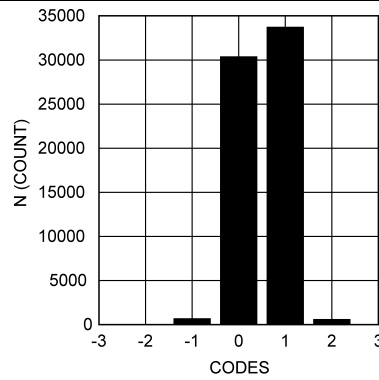


Figure 39. Noise Histogram at Code Transition

Feature Description (continued)

Reducing V_{REF} also reduces the size of the least significant bit (LSB). For example, the size of one LSB is equal to $[(2 \times V_{REF}) / 2^n]$, which is $152.6 \mu\text{V}$ where n is 16 bits and V_{REF} is 5V. When the LSB size goes below the noise floor of the ADC161S626, the noise will span an increasing number of codes and overall performance will suffer. Dynamic signals will have their SNR degrade; while, D.C. measurements will have their code uncertainty increase. Since the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

V_{REF} and analog inputs (+IN and -IN) are connected to the capacitor array through a switch matrix when the input is sampled. Hence, I_{REF} , I_{+IN} , and I_{-IN} are a series of transient spikes that occur at a frequency dependent on the operating sample rate of the ADC161S626.

I_{REF} changes only slightly with temperature. See the curves, “Reference Current vs. SCLK Frequency” and “Reference Current vs. Temperature” in the [Typical Characteristics](#) section for additional details.

7.3.2 Sample and Hold

The ADC161S626 has a differential input where the effective input voltage that is digitized is (+IN) – (–IN).

7.3.2.1 Input Settling

When the ADC161S626 enters acquisition (t_{ACQ}) mode at the end of the conversion window, the internal sampling capacitor (C_{SAMPLE}) is connected to the ADC input via an internal switch and a series resistor (R_{SAMPLE}), as shown in [Figure 40](#). Typical values for C_{SAMPLE} and R_{SAMPLE} are 20 pF and 200 ohms respectively. If there is not a large external capacitor (C_{EXT}) at the analog input of the ADC, a voltage spike will be observed at the input pins. This is a result of C_{SAMPLE} and C_{EXT} being at different voltage potentials. The magnitude and direction of the voltage spike depend on the difference between the voltage of C_{SAMPLE} and C_{EXT} . If the voltage at C_{SAMPLE} is greater than the voltage at C_{EXT} , a positive voltage spike will occur. If the opposite is true, a negative voltage spike will occur. It is not critical for the performance of the ADC161S626 to filter out the voltage spike. Rather, ensure that the transient of the spike settles out within t_{ACQ} .

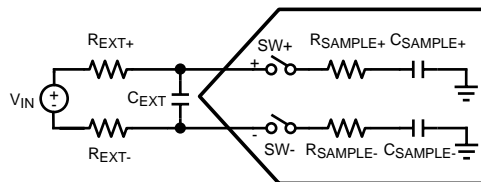


Figure 40. ADC Input Capacitors

7.3.3 Serial Digital Interface

The ADC161S626 communicates via a synchronous 3-wire serial interface as shown in [Figure 1](#) or re-shown in [Figure 41](#) for convenience. \overline{CS} , chip select bar, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of the serial data. D_{OUT} is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first.

A serial frame is initiated on the falling edge of \overline{CS} and ends on the rising edge of \overline{CS} . The ADC161S626's D_{OUT} pin is in a high impedance state when \overline{CS} is high and for the first clock period after \overline{CS} is asserted; D_{OUT} is active for the remainder of time when \overline{CS} is asserted.

The ADC161S626 samples the differential input upon the assertion of \overline{CS} . Assertion is defined as bringing the \overline{CS} pin to a logic low state. For the first 17 periods of the SCLK following the assertion of \overline{CS} , the ADC161S626 is converting the analog input voltage. On the 18th falling edge of SCLK, the ADC161S626 enters acquisition (t_{ACQ}) mode. For the next three periods of SCLK, the ADC161S626 is operating in acquisition mode where the ADC input is tracking the analog input signal applied across +IN and -IN. During acquisition mode, the ADC161S626 is consuming a minimal amount of power.

Feature Description (continued)

The ADC161S626 can enter conversion mode (t_{CONV}) under three different conditions. The first condition involves \overline{CS} going low (asserted) with SCLK high. In this case, the ADC161S626 enters conversion mode on the first falling edge of SCLK after \overline{CS} is asserted. In the second condition, \overline{CS} goes low with SCLK low. Under this condition, the ADC161S626 automatically enters conversion mode and the falling edge of \overline{CS} is seen as the first falling edge of SCLK. In the third condition, \overline{CS} and SCLK go low simultaneously and the ADC161S626 enters conversion mode. While there is no timing restriction with respect to the falling edges of \overline{CS} and SCLK, there are minimum setup and hold time requirements for the falling edge of \overline{CS} with respect to the rising edge of SCLK. See [Figure 5](#) in the *Timing Requirements* section for more information.

7.3.3.1 \overline{CS} Input

The \overline{CS} (chip select bar) input is active low and is CMOS compatible. The ADC161S626 enters conversion mode when \overline{CS} is asserted and the SCLK pin is in a logic low state. When \overline{CS} is high, the ADC161S626 is always in acquisition mode and thus consuming the minimum amount of power. Since \overline{CS} must be asserted to begin a conversion, the sample rate of the ADC161S626 is equal to the assertion rate of \overline{CS} .

Proper operation requires that the fall of \overline{CS} not occur simultaneously with a rising edge of SCLK. If the fall of \overline{CS} occurs during the rising edge of SCLK, the data might be clocked out one bit early. Whether or not the data is clocked out early depends upon how close the \overline{CS} transition is to the SCLK transition, the device temperature, and the characteristics of the individual device. To ensure that the MSB is always clocked out at a given time (the 3rd falling edge of SCLK), it is essential that the fall of \overline{CS} always meet the timing requirement specified in the *Timing Requirements* table.

7.3.3.2 SCLK Input

The SCLK (serial clock) is used as the conversion clock to shift out the conversion result. SCLK is CMOS compatible. Internal settling time requirements limit the maximum clock frequency while internal capacitor leakage limits the minimum clock frequency. The ADC161S626 offers ensured performance with the clock rates indicated in the electrical table.

The ADC161S626 enters acquisition mode on the 18th falling edge of SCLK during a conversion frame. Assuming that the LSB is clocked into a controller on the 18th rising edge of SCLK, there is a minimum acquisition time period that must be met before a new conversion frame can begin. Other than the 18th rising edge of SCLK that was used to latch the LSB into a controller, there is no requirement for the SCLK to transition during acquisition mode. Therefore, it is acceptable to idle SCLK after the LSB has been latched into the controller.

7.3.3.3 Data Output

The data output format of the ADC161S626 is two's complement as shown in [Figure 42](#). This figure indicates the ideal output code for a given input voltage and does not include the effects of offset, gain error, linearity errors, or noise. Each data output bit is output on the falling edges of SCLK. D_{OUT} is in a high impedance state for the 1st falling edge of SCLK while the 2nd SCLK falling edge clocks out a leading zero. The 3rd to 18th SCLK falling edges clock out the conversion result, MSB first.

While most receiving systems will capture the digital output bits on the rising edges of SCLK, the falling edges of SCLK may be used to capture the conversion result if the minimum hold time for D_{OUT} is acceptable. See [Figure 4](#) for D_{OUT} hold (t_{DH}) and access (t_{DA}) times.

D_{OUT} is enabled on the second falling edge of SCLK after the assertion of \overline{CS} and is disabled on the rising edge of \overline{CS} . If \overline{CS} is raised prior to the 18th falling edge of SCLK, the current conversion is aborted and D_{OUT} will go into its high impedance state. A new conversion will begin when \overline{CS} is driven LOW.

Feature Description (continued)

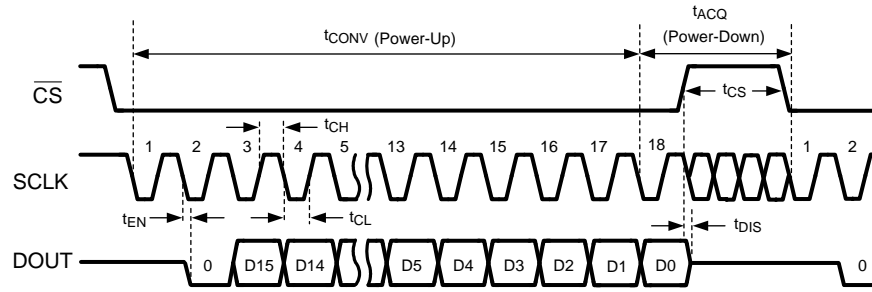


Figure 41. ADC161S626 Single Conversion Timing Diagram

7.4 Device Functional Modes

7.4.1 Differential Input Operation

The transfer curve of the ADC161S626 for a fully differential input signal is shown in Figure 42. A positive full scale output code (0111 1111 1111 1111b or 7FFFh or 32,767d) will be obtained when (+IN) – (-IN) is greater than or equal to (V_{REF} – 1 LSB). A negative full scale code (1000 0000 0000 0000b or 8000h or -32,768d) will be obtained when [(+IN) – (-IN)] is less than or equal to (-V_{REF} + 1 LSB). This ignores gain, offset and linearity errors, which will affect the exact differential input voltage that will determine any given output code.

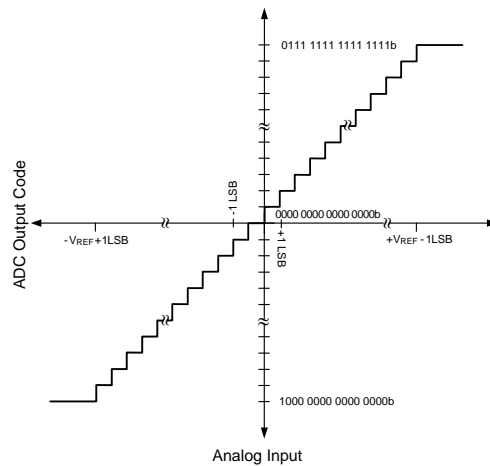


Figure 42. ADC Transfer Curve

Both inputs should be biased at a common mode voltage (V_{CM}), which will be thoroughly discussed in Figure 43 shows the ADC161S626 being driven by a full-scale differential source.

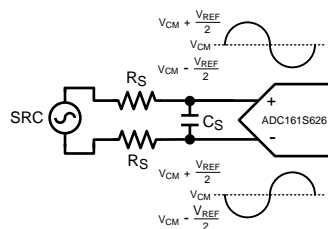


Figure 43. Differential Input

Device Functional Modes (continued)

The allowable input common mode voltage (V_{CM}) range depends upon V_A and V_{REF} used for the ADC161S626. The ranges of V_{CM} are depicted in Figure 44 and Figure 46. Note that these figures only apply to a V_A of 5V. Equations for calculating the minimum and maximum V_{CM} for differential and single-ended operations are shown in Figure 44.

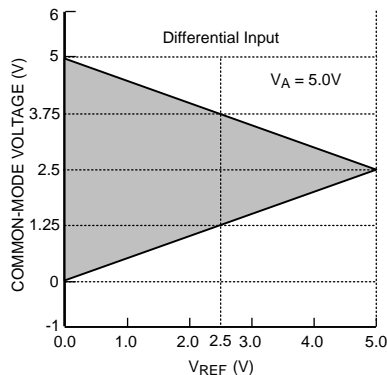


Figure 44. V_{CM} range for Differential Input operation

7.4.2 Single-Ended Input Operation

For single-ended operation, the non-inverting input (+IN) of the ADC161S626 can be driven with a signal that has a peak-to-peak range that is equal to or less than $(2 \times V_{REF})$. The inverting input (-IN) should be biased at a stable V_{CM} that is halfway between these maximum and minimum values. In order to utilize the entire dynamic range of the ADC161S626, V_{REF} is limited to $(V_A / 2)$. This allows +IN a maximum swing range of ground to V_A . Figure 45 shows the ADC161S626 being driven by a full-scale single-ended source.

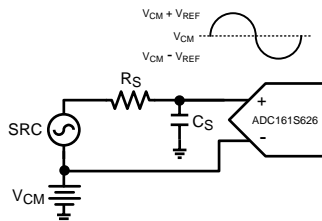


Figure 45. Single-Ended Input

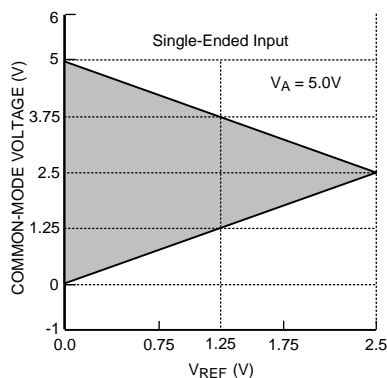


Figure 46. V_{CM} Range for single-Ended Operation

Device Functional Modes (continued)

Since the design of the ADC161S626 is optimized for a differential input, the performance degrades slightly when driven with a single-ended input. Linearity characteristics such as INL and DNL typically degrade by 0.1 LSB and dynamic characteristics such as SINAD typically degrade by 2 dB. Note that single-ended operation should only be used if the performance degradation (compared with differential operation) is acceptable.

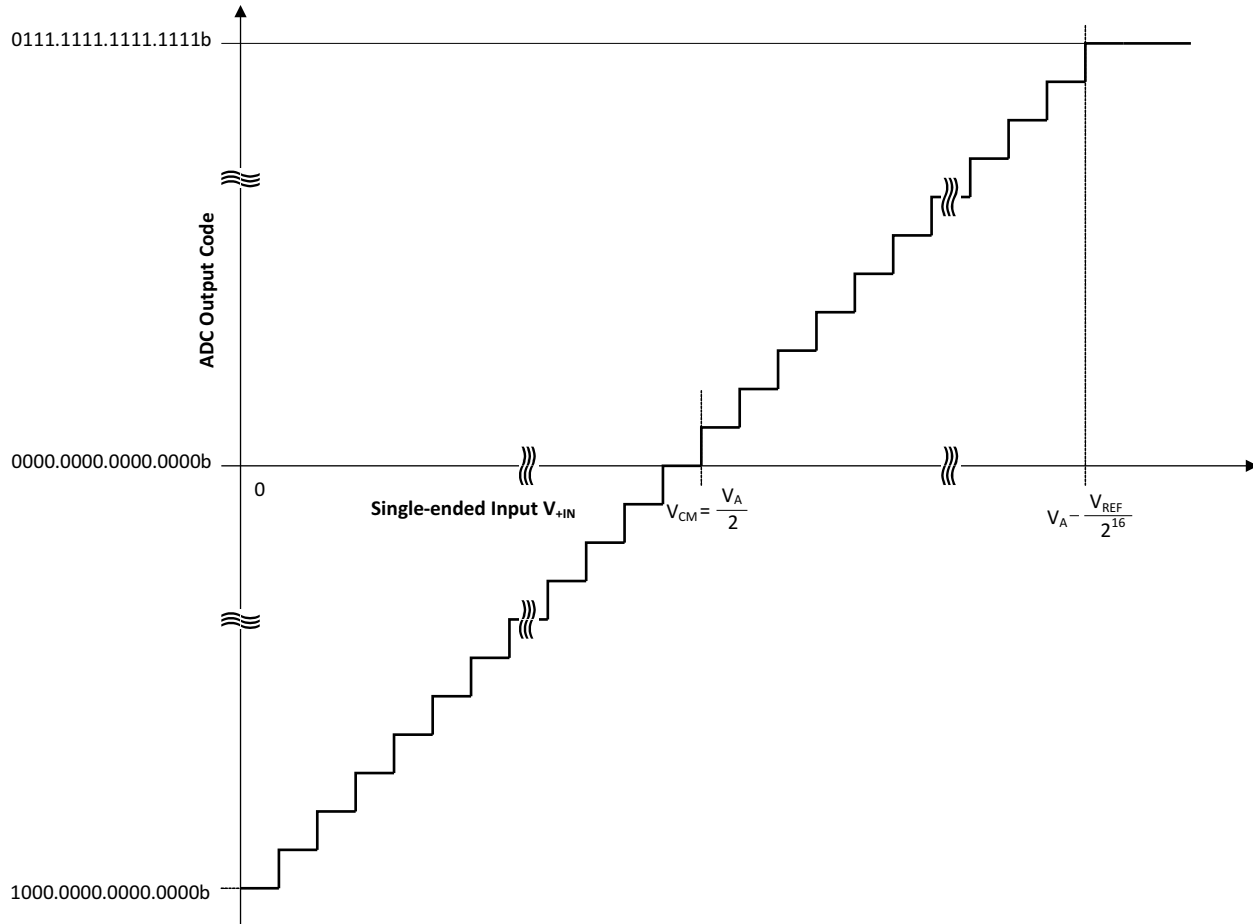


Figure 47. Single-Ended Transfer Characteristic

7.4.3 Short Cycling

Short cycling refers to the process of halting a conversion after the last needed bit is outputted. Short cycling can be used to lower the power consumption in those applications that do not need a full 16-bit resolution, or where an analog signal is being monitored until some condition occurs. In some circumstances, the conversion could be terminated after the first few bits. This will lower power consumption in the converter since the ADC161S626 spends more time in acquisition mode and less time in conversion mode.

Short cycling is accomplished by pulling \overline{CS} high after the last required bit is received from the ADC161S626 output. This is possible because the ADC161S626 places the latest converted data bit on D_{OUT} as it is generated. If only 10-bits of the conversion result are needed, for example, the conversion can be terminated by pulling \overline{CS} high after the 10th bit has been clocked out.

Device Functional Modes (continued)

7.4.4 Burst Mode Operation

Normal operation of the ADC161S626 requires the SCLK frequency to be 20 times the sample rate and the \overline{CS} rate to be the same as the sample rate. However, in order to minimize power consumption in applications requiring sample rates below 250 kSPS, the ADC161S626 should be run with an SCLK frequency of 5 MHz and a \overline{CS} rate as slow as the system requires. When this is accomplished, the ADC161S626 is operating in burst mode. The ADC161S626 enters into acquisition mode at the end of each conversion, minimizing power consumption. This causes the converter to spend the longest possible time in acquisition mode. Since power consumption scales directly with conversion rate, minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following sections outline the design principles of data acquisition system based on the ADC161S626.

8.2 Typical Application

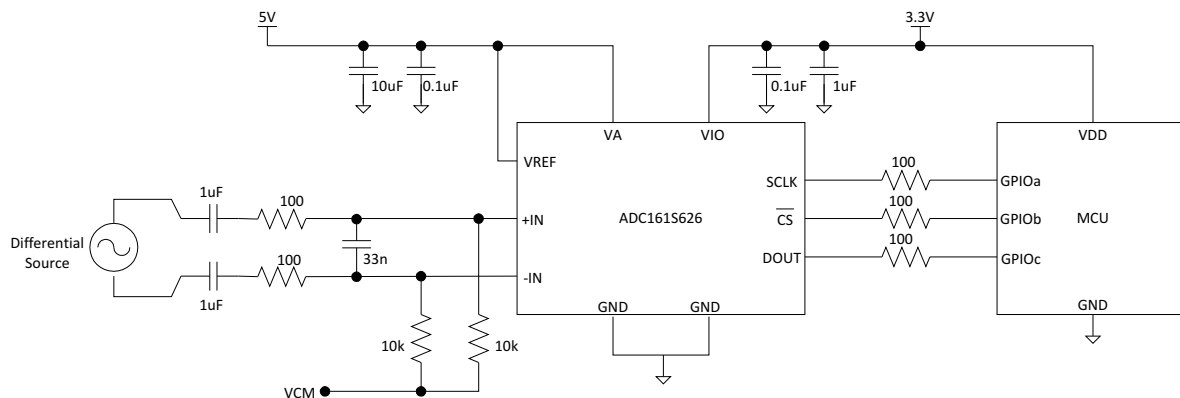


Figure 48. Low Cost, Low Power Data Acquisition System

Figure 48 shows a typical connection diagram for the ADC161S626 operating at V_A of 5 V. V_{REF} is connected to a 2.5-V shunt reference, the LM4020-2.5, to define the analog input range of the ADC161S626 independent of supply variation on the 5-V supply line. The V_{REF} pin should be de-coupled to the ground plane by a 0.1- μ F ceramic capacitor and a tantalum capacitor of 10 μ F. It is important that the 0.1- μ F capacitor be placed as close as possible to the V_{REF} pin while the placement of the tantalum capacitor is less critical. It is also recommended that the V_A and V_{IO} pins of the ADC161S626 be de-coupled to ground by a 0.1- μ F ceramic capacitor in parallel with a 10- μ F tantalum capacitor.

8.2.1 Design Requirements

A positive supply only data acquisition system capable of digitizing differential signals ranging from -5 V to 5 V ($V_{+IN} - V_{-IN}$), $BW = 10$ kHz, and a throughput of 250 kSPS (F_s).

The ADC161S626 has to interface to an MCU whose supply is set at 3.3 V.

8.2.2 Detailed Design Procedure

The signal range requirement forces the design to use 5 V as V_{REF} potential. This, in turn, forces the V_A to be no less than 5 V as well.

The requirement of interfacing to the MCU which is powered by 3.3-V supply, forces the choice of 3.3 V as a V_D supply.

Sampling is in fact a modulation process which may result in aliasing of the input signal, if the input signal is not adequately band limited. In order to avoid the aliasing the Nyquist criterion has to be met:

$$BW_{\text{signal}} \leq \frac{F_s}{2} = 125\text{kHz} \quad (1)$$

Therefore it is necessary to place an anti-aliasing filter at the input of the ADC. The filter may be single pole low pass filter whose pole location has to satisfy:

Typical Application (continued)

$$\frac{1}{2\pi \times R \times C} \leq \frac{F_s}{2} \tag{2}$$

$$R \times C \geq \frac{1}{\pi \times F_s} \tag{3}$$

With $F_s = 250$ kHz, a good choice for the single pole filter is:

$$R = 100$$

$$C = 33 \text{ nF}$$

This reduces the input $BW_{\text{signal}} = 48$ kHz.

The capacitor at the inputs of the device provides not only the filtering of the input signal, but it also absorbs the charge kick-back from the ADC. The kick-back is the result of the internal switches opening at the end of the acquisition period.

The common mode level of the ADC inputs has to be set by the external bias source. The VCM bias has to be isolated from the inputs by a large resistance in order to avoid input signal attenuation.

The VA and VIO sources are already separated in this example, due to the design requirements. This also benefits the overall performance of the ADC, as the potentially noisy VIO supply does not contaminate the VA. In the same vein, further consideration could be given to the SPI interface, especially when the master MCU is capable of producing fast rising edges on the digital bus signals. Inserting small resistances in the digital signal path may help in reducing the ground bounce, and thus improve the overall noise performance of the system.

8.2.3 Application Curve

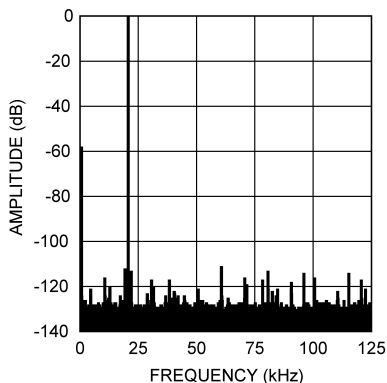


Figure 49. Spectral Response

9 Power Supply Recommendations

9.1 Analog and Digital Power Supplies

Any ADC architecture is sensitive to spikes on the power supply, reference, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. Power to the ADC161S626 should be clean and well bypassed. A 0.1 μF ceramic bypass capacitor and a 1 μF to 10 μF capacitor should be used to bypass the ADC161S626 supply, with the 0.1 μF capacitor placed as close to the ADC161S626 package as possible.

Since the ADC161S626 has both the V_A and V_{IO} pins, the user has three options on how to connect these pins. The first option is to tie V_A and V_{IO} together and power them with the same power supply. This is the most cost effective way of powering the ADC161S626 but is also the least ideal. As stated previously, noise from V_{IO} can couple into V_A and adversely affect performance. The other two options involve the user powering V_A and V_{IO} with separate supply voltages. These supply voltages can have the same amplitude or they can be different. V_A can be set to any value between +4.5V and +5.5V; while V_{IO} can be set to any value between +2.7V and +5.5V.

Best performance will typically be achieved with V_A operating at 5V and V_{IO} at 3V. Operating V_A at 5V offers the best linearity and dynamic performance when V_{REF} is also set to 5V; while operating V_{IO} at 3V reduces the power consumption of the digital logic. Operating the digital interface at 3V also has the added benefit of decreasing the noise created by charging and discharging the capacitance of the digital interface pins.

9.2 Voltage Reference

The reference source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 μF . A larger capacitor value of 1 μF to 10 μF placed in parallel with the 0.1 μF is preferred. While the ADC161S626 draws very little current from the reference on average, there are higher instantaneous current spikes at the reference.

V_{REF} of the ADC161S626, like all A/D converters, does not reject noise or voltage variations. Keep this in mind if V_{REF} is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of an active reference source is recommended. The LM4040 and LM4050 shunt reference families and the LM4120 and LM4140 series reference families are excellent choices for a reference source.

10 Layout

10.1 Layout Guidelines

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible. Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC161S626 due to supply noise, avoid using the same supply for the V_A and V_{REF} of the ADC161S626 that is used for digital circuitry on the board.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated. The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

A single, uniform ground plane and the use of split power planes are recommended. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry should be placed over the digital power plane. Furthermore, the GND pins on the ADC161S626 and all the components in the reference circuitry and input signal chain that are connected to ground should be connected to the ground plane at a quiet point. Avoid connecting these points too close to the ground point of a microprocessor, microcontroller, digital signal processor, or other high power digital device.

Layout Guidelines (continued)

For best performance, care should be taken with the physical layout of the printed circuit board. This is especially true with a low V_{REF} or when the conversion rate is high. At high clock rates there is less time for settling, so it is important that any noise settles out before the conversion begins.

10.2 Layout Example

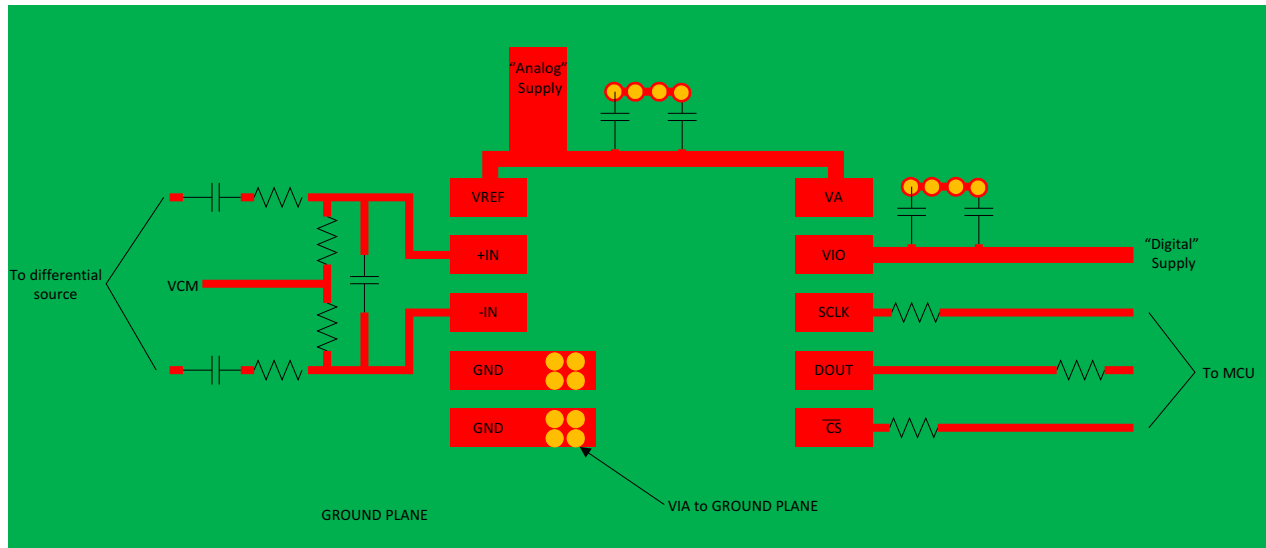


Figure 50. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Specification Definitions

APERTURE DELAY is the time between the first falling edge of SCLK and the time when the input signal is sampled for conversion.

COMMON MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed from 2V to 3V.

$$\text{CMRR} = 20 \text{ LOG} (\Delta \text{ Common Input} / \Delta \text{ Output Offset}) \quad (4)$$

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as $(\text{SINAD} - 1.76) / 6.02$ and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It is the difference between Positive Full-Scale Error and Negative Full-Scale Error and can be calculated as:

$$\text{Gain Error} = \text{Positive Full-Scale Error} - \text{Negative Full-Scale Error} \quad (5)$$

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from $\frac{1}{2}$ LSB below the first code transition through $\frac{1}{2}$ LSB above the last code transition. The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC161S626 is ensured not to have any missing codes.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from code 0x8001h to 0x8000h and $-V_{\text{REF}} + 1 \text{ LSB}$.

NEGATIVE GAIN ERROR is the difference between the negative full-scale error and the offset error.

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 0x0000h to 0x0001h and 1 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from code 0xFFFFh to 0xFFFEh and $V_{\text{REF}} - 1 \text{ LSB}$.

POSITIVE GAIN ERROR is the difference between the positive full-scale error and the offset error.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in the analog supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB. For the ADC161S626, V_A is changed from 4.5V to 5.5V.

$$\text{PSRR} = 20 \text{ LOG} (\Delta \text{Output Offset} / \Delta V_A) \quad (6)$$

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below one-half the sampling frequency, including harmonics but excluding d.c.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not

Device Support (continued)

including harmonics or d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component below one-half the sampling frequency, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output, expressed in dB. THD is calculated as

$$\text{THD} = 20 \times \log_{10} \sqrt{\frac{A_{f_2}^2 + \dots + A_{f_6}^2}{A_{f_1}^2}}$$

where

- A_{f_1} is the RMS power of the input frequency at the output
- A_{f_2} through A_{f_6} are the RMS power in the first 5 harmonic frequencies. (7)

11.2 Trademarks

QSPI is a trademark of Motorola.

MICROWIRE is a trademark of National Semiconductor Corp.

All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|----------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ADC161S626CIMM/NOPB | ACTIVE | VSSOP | DGS | 10 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | X98C | Samples |
| ADC161S626CIMME/NOPB | ACTIVE | VSSOP | DGS | 10 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | X98C | Samples |
| ADC161S626CIMMX/NOPB | ACTIVE | VSSOP | DGS | 10 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | X98C | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADC161S626CIMM/NOPB | VSSOP | DGS | 10 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| ADC161S626CIMME/NOPB | VSSOP | DGS | 10 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| ADC161S626CIMMX/NOPB | VSSOP | DGS | 10 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADC161S626CIMM/NOPB | VSSOP | DGS | 10 | 1000 | 210.0 | 185.0 | 35.0 |
| ADC161S626CIMME/NOPB | VSSOP | DGS | 10 | 250 | 210.0 | 185.0 | 35.0 |
| ADC161S626CIMMX/NOPB | VSSOP | DGS | 10 | 3500 | 367.0 | 367.0 | 35.0 |

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View ADC161S626CIMME/NOPB on WIN SOURCE](#)
- ⊖ [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management