THE DATASHEET OF

CYDMX064B16-65BVXI

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Spec No: 001-08090

Spec Title: CYDMX256A16/CYDMX256B16/CYDMX128A16/ CYDMX128B16/CYDMX064A16/CYDMX064B16, 16K/8K/4K X 16 MOBL(R) ADM ASYNCHRONOUS DUAL-PORT STATIC RAM.

Replaced by: None

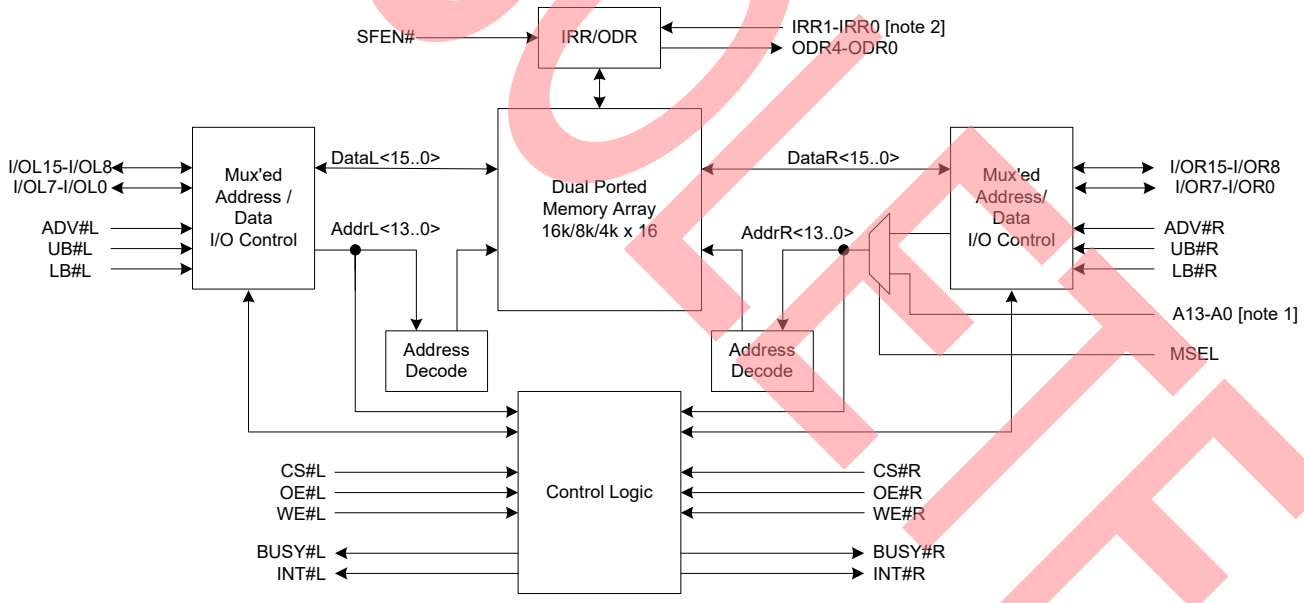
CYDMX256A16/CYDMX256B16
CYDMX128A16/CYDMX128B16
CYDMX064A16/CYDMX064B16

16K/8K/4K × 16 MoBL® ADM Asynchronous Dual-Port Static RAM

Features

- True dual-ported memory block that allow simultaneous independent access
  - One port with dedicated time multiplexed address and data (ADM) interface
  - One port configurable to standard SRAM or time multiplexed address and data interface
- 16 K/8 K/4 K × 16 memory configuration
- High speed access
  - 65 ns or 90 ns ADM interface
  - 40 ns or 60 ns standard SRAM interface
- Fully asynchronous operation
- Port independent 1.8 V, 2.5 V, and 3.0 V IOs
- Ultra low operating power
  - Active: I_{CC} = 15 mA (typical) at 90 ns
  - Active: I_{CC} = 25 mA (typical) at 65 ns
  - Standby: I_{SB3} = 2 µA (typical)
- Port independent power-down
- On-chip arbitration logic
- Mailbox interrupt for port to port communication
- Input Read and Output Drive registers
- Upper byte and lower byte control
- Small package: 6 × 6 mm, 100-ball Pb-free BGA
- Industrial temperature range

Block Diagram



Notes
1. A13-A0 for CYDMX256A16 and CYDMX256B16; A12-A0 for CYDMX128A16 and CYDMX128B16; and A11-A0 for CYDMX064A16 and CYDMX064B16.
2. IRR1 and IRR2 not available for CYDMX256A16 and CYDMX256B16.

Contents

Pin Configurations

Figure 1. 100-ball BGA pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	
A	A5	A8	A11	UB#R	VSS	ADV#R	I/OR15	I/OR12	I/OR10	VSS	A
B	A3	A4	A7	A9	CE#R	WE#R	OE#R	VDDIOR	I/OR9	I/OR6	B
C	A0	A1	A2	A6	LB#R	IRR1[3]	I/OR14	I/OR11	I/OR7	VSS	C
D	ODR4	ODR2	BUSY#R	INT#R	A10	A12[4]	I/OR13	I/OR8	I/OR5	I/O2R	D
E	VSS	DNU	ODR3	INT#L	VSS	VSS	I/OR4	VDDIOR	I/OR1	VSS	E
F	SFEN#	ODR1	BUSY#L	DNU	VCC	VSS	I/OR3	I/OR0	I/OL15	VDDIOL	F
G	ODR0	DNU	DNU	DNU	OE#L	I/OL3	I/OL11	I/OL12	I/OL14	I/OL13	G
H	DNU	DNU	DNU	LB#L	CE#L	I/OL1	VDDIOL	MSEL	DNU	I/OL10	H
J	DNU	DNU	DNU	IRR0[5]	VCC	VSS	I/OL4	I/OL6	I/OL8	I/OL9	J
K	DNU	DNU	DNU	UB#L	ADV#L	WE#L	I/OL0	I/OL2	I/OL5	I/OL7	K
	1	2	3	4	5	6	7	8	9	10	

Notes
3. This pin is A13 for CYDMX256A16 and CYDMX256B16.
4. This pin is DNU for CYDMX064A16 and CYDMX064B16.
5. This pin is DNU for CYDMX256A16 and CYDMX256B16.
6. DNU pins are “do not use” pins. No trace or power component can be connected to these pins.

Pin Definitions

Left Port	Right Port	Description
CS#L	CS#R	Chip select
WE#L	WE#R	Read/Write Enable
OE#L	OE#R	Output Enable
	A0–A13	Address (A0–A11 for 4K device; A0–A12 for 8K device; A0–A13 for 16K device)
	MSEL	Right port interface mode select (0: Standard SRAM; 1: Address/Data Mux)
IOL0–IOL15	IOR0–IOR15	Address/Data Bus Input/Output
ADV#L	ADV#R	Address Latch Enable; ADV#R only use when R-port is in ADM mode
UB#L	UB#R	Upper byte select (IO8–IO15)
LB#L	LB#R	Lower byte select (IO0–IO7)
INT#L	INT#R	Interrupt Flag
BUSY#L	BUSY#R	Busy Flag
SFEN#		Special Function Enable Signal
IRR0-IRR1		Input signals for input read registers for CYDMX128A16, CYDMX128B16, CYDMX064A16 and CYDMX064B16; IRR0 is DNU and IRR1 is A13 for CYDMX256A16 and CYDMX256B16.
ODR0-ODR4		Output signals for output drive registers; These are open drained outputs.
V_{CC}		Core power supply
GND		Ground
VDDIOL		Left port IO power supply
VDDIOR		Right port IO power supply
DNU		No Connect; Do not connect trace or power component to these pins.

Functional Overview

The CYDMX256A16, CYDMX128A16, CYDMX064A16, CYDMX256B16, CYDMX128B16, and CYDMX064B16 are low power CMOS 16K/8K/4K × 16 dual-port static RAMs. The two ports are: one dedicated time multiplexed address and data (ADM) interface and one configurable standard SRAM or ADM interface. The two ports permit independent, asynchronous read and write access to any memory locations. Each port has independent control pins: Chip Select (CS#), Write Enable (WE#), and Output Enable (OE#). Two output flags are provided on each port (BUSY# and INT#). BUSY# flag is triggered when the port is trying to access the same memory location currently being accessed by the other port. The Interrupt flag (INT#) permits communication between ports or systems by means of a mailbox. Power-down feature is controlled independently on each port by a Chip Select (CS#) pin.

The CYDMX256A16, CYDMX128A16, CYDMX064A16, CYDMX256B16, CYDMX128B16, and CYDMX064B16 are available in 100-ball 0.5-mm pitch Ball Grid Array (BGA) packages. Application areas include interprocessor and multiprocessor designs, communications status buffering, and dual-port video and graphics memory.

Power Supply

The core voltage (V_{CC}) can be 1.8 V, 2.5 V, or 3.0 V, as long as it is lower than or equal to the IO voltage. Each port operates on independent IO voltages. This is determined by what is connected to the V_{DDIOL} and V_{DDIOR} pins. The supported IO standards are 1.8 V and 2.5 V LVCMOS and 3.0 V LVTTL.

ADM Interface Read or Write Operation

This description is applicable to both the left ADM port and right port configured as an ADM port.

Three control signals, ADV#, WE#, and CS# are used to perform the read and write operations. Address signals are first applied to the IO bus along with CS# LOW. The addresses are loaded from the IO bus in response to the rising edge of the Address Latch Enable (ADV#) signal. It is necessary to meet the setup (t_{AVDS}) and hold (t_{AVDH}) times given in the AC specifications with valid address information to properly latch the addresses.

After the address signals are latched in, a read operation is issued when WE# stays HIGH. The IO bus becomes High Z when the address signals meet t_{AVDH}. The read data is driven on the IO bus t_{OE} after the OE# is asserted LOW, and held until t_{HZOE} or t_{HZCS} after the rising edge of OE# or CS#, whichever comes first.

A write operation is issued when WE# is asserted LOW. The write data is applied to the IO bus right after address meets the hold time (t_{AVDH}). And write data is written with the rising edge of either WE# or CS#, whichever comes first, and meets data setup (t_{SD}) and hold (t_{HD}) times.

Standard SRAM Interface Read or Write Operation

This description is applicable to the right access port configured as standard SRAM port. Read and write operations with standard SRAM interface configuration is the same as the ADM port except addresses are presented on the A bus. Operation is controlled by CS#, OE#, and WE#. A read operation is issued when WE# is asserted HIGH. A write operation is issued when WE# is asserted LOW. The IO bus is the destination for read data and the source for write data when the read operation is issued. However, write data must be driven to IO when the write operation is issued.

Byte Select Operation

The fundamental word size is 16 bits. Each word is broken up into two 8-bit bytes. Each port has two active LOW byte enables: UB# and LB#. Activating or deactivating the byte enables alters the result of read and write operations to the port. During a write, byte enable asserted HIGH inhibits the corresponding byte to be updated in the addressed memory location. During a read, both byte enables are inputs to the asynchronous output enable control logic. When a byte enable is asserted HIGH, the corresponding data byte is tristated. Subsequently, when the byte enable is asserted LOW, the corresponding data byte is driven with the read data.

Chip Select Operation

Each port has one active LOW chip select signal, CS#. CS# must be asserted LOW for the port to be considered active. To issue a valid read or write operation, the chip select input must be asserted LOW throughout the read or write cycle. When CS# is deasserted HIGH during a write, if t_{WRL}, t_{SD}, and t_{HD} are not met, the contents of the addressed location is not altered.

An automatic power-down feature controlled by deactivating the chip select (CS# HIGH) permits the on-chip circuitry of each port to enter a very low standby power mode.

Output Enable Operation

Each port has one output enable signal, OE#. When OE# is asserted HIGH, IO bus is tri-stated after t_{HZOE}. When OE# is asserted LOW, control of the IO bus is assumed by the asynchronous output enable logic (the logic is controlled by inputs WE#, CS#, UB#, and LB#).

Mailbox Interrupts

The upper two memory locations are used for message passing. The highest memory location (0xFFF for CYDMX064A16 and CYDMX064B16, 0x1FFF for CYDMX128A16 and CYDMX128B16, and 0x3FFF for CYDMX256A16 and CYDMX256B16) is the mailbox for the right port. The second highest memory location (0xFFE for CYDMX064A16 and CYDMX064B16, 0x1FFE for CYDMX128A16 and CYDMX128B16, and 0x3FFE for CYDMX256A16 and CYDMX256B16) is the mailbox for the left port. When one port writes to the opposite port's mailbox, an interrupt signal is generated to the opposite port. The interrupt resets when the owner reads the contents of its own mailbox. The message written to the mailbox is user defined.

Each port reads the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and resetting the interrupt to it.

On power-up, both interrupts are set by default. An initialization program must be run to reset the interrupts.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

Arbitration Logic

The CYDMX256A16, CYDMX128A16, CYDMX064A16, CYDMX256B16, CYDMX128B16, and CYDMX064B16 provide on-chip arbitration to resolve simultaneous memory location access (collision). If both ports' CS# signals are asserted and an address match occurs within each other, the busy logic determines which port has access. If t_{PS} is violated, one of the two ports gains permission to the location, but it is not predictable which port gets the permission. BUSY# is asserted t_{BLA} after an address match or t_{BLC} after CS# is taken LOW.

Input Read Register

The Input Read Register (IRR) feature is available only for CYDMX128A16, CYDMX128B16, CYDMX064A16, and CYDMX064B16 devices. When SFEN# = V_{IL}, the IRR captures the status of two external devices connected to the Input Read pins (IRR0 and IRR1) to address location 0x0000. Address 0x0000 is not available for standard memory accesses when SFEN# = V_{IL}. When SFEN# = V_{IH}, address 0x0000 is available for normal memory accesses. Either port accesses the contents of IRR with normal read operation from address 0x0000. During reads from the IRR, IO<1:0> are valid bits and IO<15:2> are don't care. The IRR inputs are 1.8 V and 2.5 V LVCMOS or 3.0 V LVTTL, depending on the core voltage supply (V_{CC}).

Output Drive Register

The Output Drive Register (ODR) determines the state of up to five external binary state devices by providing a path to V_{SS} for the external circuit. These outputs are open drain. The five external devices operates at different voltages (1.5 V ≤ V_{DDIO} ≤ 3.5 V) but the combined current cannot exceed 40 mA (8 mA maximum for each external device). The status of the ODR bits are set using standard write accesses from either port to address 0x0001 with a '1' corresponding to on and '0' corresponding to off. The status of the ODR bits are read with a normal read access to address 0x0001. When SFEN# = V_{IL}, the ODR is active and address 0x0001 is not available for memory accesses. When SFEN# = V_{IH}, the ODR is inactive and address 0x0001 is used for standard accesses. During reads and writes to ODR, IO<4:0> are valid and IO<15:5> are don't care.

Architecture

The CYDMX256A16, CYDMX128A16, CYDMX064A16, CYDMX256B16, CYDMX128B16, and CYDMX064B16 consist of an array of 16K, 8K, and 4K words of 16 dual-ported SRAM cells, IO, address lines, and control signals (CS#, ADV#, OE#, and WE#). Between the two access ports, one is a dedicated time multiplexed address and data interface; the other is a pin selectable port to either standard SRAM or time multiplexed address and data interface. Independent control signals for each port permit simultaneous access to any location in memory. To handle the situation of writing and reading to the same location, a BUSY# pin is provided on each port. For port to port communication, an Interrupt (INT#) pin is also available on each port.

Table 1. ADM Interface Read/Write with Byte Select Operations

ADV#	CS#	WE#	OE#	UB#	LB#	IO0–IO15	Mode
X	H	X	X	X	X	High Z	Deselected or power-down
X	X	X	H	X	X	High Z	Output disable
X	X	X	X	H	H	High Z	Upper and lower byte deselected
Pulse	L	H	L	L	L	Data Out (IO0–IO15)	Read upper and lower bytes
Pulse	L	H	L	H	L	Data Out (IO0–IO7) High Z (IO8–IO15)	Read lower byte only
Pulse	L	H	L	L	H	High Z (IO0–IO7) Data Out (IO8–IO15)	Read upper byte only
Pulse	L	L	X	L	L	Data In (IO0–IO15)	Write upper and lower bytes
Pulse	L	L	X	H	L	Data In (IO0–IO7) High Z (IO8–IO15)	Write lower byte only
Pulse	L	L	X	L	H	High Z (IO0–IO7) Data In (IO8–IO15)	Write upper byte only

Table 2. Standard SRAM Interface Read/Write with Byte Select Operations

CS#	WE#	OE#	UB#	LB#	IO0-IO15	Mode
H	X	X	X	X	High Z	Deselected or power-down
X	X	H	X	X	High Z	Output disable
X	X	X	H	H	High Z	Upper and lower byte deselected
L	H	L	L	L	Data Out (IO0–IO15)	Read upper and lower bytes
L	H	L	H	L	Data Out (IO0–IO7) High Z (IO8–IO15)	Read lower byte only
L	H	L	L	H	High Z (IO0–IO7) Data Out (IO8–IO15)	Read upper byte only
L	L	X	L	L	Data In (IO0–IO15)	Write upper and lower bytes
L	L	X	H	L	Data In (IO0–IO7) High Z (IO8–IO15)	Write lower byte only
L	L	X	L	H	High Z (IO0–IO7) Data In (IO8–IO15)	Write upper byte only

Table 3. Interrupt Operation Example (Assumes BUSY#L = BUSY#R = HIGH)

Function	Left Port					Right Port				
	WE#L	CS#L	OE#L	AddressL	INT#L	WE#R	CS#R	OE#R	AddressR	INT#R
Set Right INT#R Flag	L	L	X	0x3FFF[7]	X	X	X	X	X	L
Reset Right INT#R Flag	X	X	X	X	X	X	L	L	0x3FFF[7]	H
Set Left INT#L Flag	X	X	X	X	L	L	L	X	0x3FFE[8]	X
Reset Left INT#L Flag	X	L	L	0x3FFE[8]	H	X	X	X	X	X

Table 4. Arbitration Winning Port

CS#L	CS#R	Address Match Left/Right Port	BUSY#L	BUSY#R	Function
X	X	No Match	H	H	Normal
H	X	Match	H	H	Normal
X	H	Match	H	H	Normal
L	L	Match	See Note[9]	See Note[9]	Write Inhibit[10]

Table 5. Input Read Register Operation[11]

SFEN#	CS#	WE#	OE#	UB#	LB#	ADDR	IO_0–IO_1	IO_2–IO_{15}	Mode
H	L	H	L	L	L	x0000-Max	VALID[12]	VALID[12]	Standard Memory Access
L	L	H	L	X	L	x0000	VALID[13]	X	IRR Read

Table 6. Output Drive Register[15]

SFEN#	CS#	WE#	OE#	UB#	LB#	ADDR	IO_0–IO_4	IO_5–IO_{15}	Mode
H	L	H	X[16]	L[12]	L[12]	x0000-Max	VALID[12]	VALID[12]	Standard Memory Access
L	L	L	X	X	L	x0001	VALID[13]	X	ODR Write[17]
L	L	H	L	X	L	x0001	VALID[13]	X	ODR Read

Notes
7. 0x3FFF for CYDMX256A16 and CYDMX256B16, 0x1FFF for CYDMX128A16 and CYDMX128B16, 0xFFF for CYDMX064A16 and CYDMX064B16.
8. 0x3FFE for CYDMX256A16 and CYDMX256B16, 0x1FFE for CYDMX128A16 and CYDMX128B16, 0xFFE for CYDMX064A16 and CYDMX064B16.
9. If it meets tPS, "L" if the CS# and address of the opposite port become stable BEFORE the current port; "H" if the CS# and address of the opposite port become stable AFTER the current port. If tPS is not met, either BUSY#L or BUSY#R results “L”. BUSY#L and BUSY#R cannot be “L” simultaneously.
10. Write operations to the left port are internally ignored when BUSY#L is driving LOW regardless of actual logic level on the pin; Write operations to the right port are internally ignored when BUSY#R is driving LOW regardless of actual logic level on the pin.
11. SFEN# = V_{IL} for IRR reads.
12. UB# or LB# = V_{IL}. If LB# = V_{IL}, then IO<7:0> are valid. If UB# = V_{IL} then IO<15:8> are valid.
13. LB# must be active (LB# = V_{IL}) for these bits to be valid.
14. SFEN# active when either CS#L = V_{IL} or CS#R = V_{IL}. It is inactive when CS#L = CS#R = V_{IH}.
15. SFEN# = V_{IL} for ODR reads and writes.
16. Output enable must be low (OE# = V_{IL}) during reads for valid data to be output.
17. During ODR writes data is also written to the memory.

Maximum Ratings

Exceeding maximum ratings[18] may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential .....–0.5 V to +3.3 V

DC Voltage Applied to Outputs in High Z State ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage[19] ..... –0.5 V to V_{CC} + 0.5 V

Output Current into Outputs (LOW) ..... 90 mA

Static Discharge Voltage ..... > 2000 V

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.8 V ± 100 mV 2.5 V ± 100 mV 3.0 V ± 300 mV

Electrical Characteristics for V_{CC} = 1.8 V

Over the Operating Range

Parameter	Description	P1 IO Voltage	P2 IO Voltage	CYDMX256A16 CYDMX128A16 –65 Min	CYDMX256A16 CYDMX128A16 –65 Typ	CYDMX256A16 CYDMX128A16 –65 Max	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Min	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Typ	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Max	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Typ	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Max	Unit
V_{OH}	Output HIGH voltage (I_{OH} = –100 µA)	1.8 V (any port)		V_{DDIO} – 0.2	–	–	V_{DDIO} – 0.2	–	–	V_{DDIO} – 0.2	–	–	V
	Output HIGH voltage (I_{OH} = –2 mA)	2.5 V (any port)		2.0	–	–	2.0	–	–	2.0	–	–	V
	Output HIGH voltage (I_{OH} = –2 mA)	3.0 V (any port)		2.1	–	–	2.1	–	–	2.1	–	–	V
V_{OL}	Output LOW voltage (I_{OL} = 100 µA)	1.8 V (any port)		–	–	0.2	–	–	0.2	–	–	0.2	V
	Output HIGH voltage (I_{OH} = 2 mA)	2.5 V (any port)		–	–	0.4	–	–	0.4	–	–	0.4	V
	Output HIGH voltage (I_{OH} = 2 mA)	3.0 V (any port)		–	–	0.4	–	–	0.4	–	–	0.4	V
V_{OL} ODR	ODR output LOW voltage (I_{OL} = 8 mA)	1.8 V (any port)		–	–	0.2	–	–	0.2	–	–	0.2	V
		2.5 V (any port)		–	–	0.2	–	–	0.2	–	–	0.2	V
		3.0 V (any port)		–	–	0.2	–	–	0.2	–	–	0.2	V
V_{IH}	Input HIGH voltage	1.8 V (any port)		1.2	–	V_{DDIO} + 0.2	1.2	–	V_{DDIO} + 0.2	1.2	–	V_{DDIO} + 0.2	V
		2.5 V (any port)		1.7	–	V_{DDIO} + 0.3	1.7	–	V_{DDIO} + 0.3	1.7	–	V_{DDIO} + 0.3	V
		3.0 V (any port)		2.0	–	V_{DDIO} + 0.2	2.0	–	V_{DDIO} + 0.2	2.0	–	V_{DDIO} + 0.2	V
V_{IL}	Input LOW voltage	1.8 V (any port)		–0.2	–	0.4	–0.2	–	0.4	–0.2	–	0.4	V
		2.5 V (any port)		–0.3	–	0.6	–0.3	–	0.6	–0.3	–	0.6	V
		3.0 V (any port)		–0.2	–	0.7	–0.2	–	0.7	–0.2	–	0.7	V
I_{OZ}	Output leakage current	1.8 V	1.8 V	–1	–	1	–1	–	1	–1	–	1	µA
		2.5 V	2.5 V	–1	–	1	–1	–	1	–1	–	1	µA
		3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{CEX} ODR	ODR output leakage current. V_{OUT} = V_{DDIO}	1.8 V	1.8 V	–1	–	1	–1	–	1	–1	–	1	µA
		2.5 V	2.5 V	–1	–	1	–1	–	1	–1	–	1	µA
		3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA

Notes
18. The voltage on any input or IO pin cannot exceed the power pin during power-up.
19. Pulse width < 20 ns.

Electrical Characteristics for V_{CC} = 1.8 V (continued)

Over the Operating Range (continued)

Parameter	Description		P1 IO Voltage	P2 IO Voltage	CYDMX256A16 CYDMX128A16 –65 Min	CYDMX256A16 CYDMX128A16 –65 Typ	CYDMX256A16 CYDMX128A16 –65 Max	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Min	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Typ	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Max	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Typ	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Max	Unit
I_{IX}	Input leakage current		1.8 V	1.8 V	–1	–	1	–1	–	1	–1	–	1	µA
			2.5 V	2.5 V	–1	–	1	–1	–	1	–1	–	1	µA
			3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{CC}	Operating current (V_{CC} = Max, I_{OUT} = 0 mA) outputs disabled	Ind.	1.8 V	1.8 V	–	25	40	–	25	40	–	15	25	mA
I_{SB1}	Standby current (both ports TTL level) CE#L and CE#R ≥ V_{CC} – 0.2, f = f_{MAX}	Ind.	1.8 V	1.8 V	–	2	6	–	2	6	–	2	6	µA
I_{SB2}	Standby current (One Port TTL level) CE#L or CE#R ≥ V_{IH}, f = f_{MAX}	Ind.	1.8 V	1.8 V	–	8.5	18	–	8.5	18	–	8.5	14	mA
I_{SB3}	Standby current (both ports CMOS level) CE#L and CE#R ≥ V_{CC} – 0.2 V, f = 0	Ind.	1.8 V	1.8 V	–	2	6	–	2	6	–	2	6	µA
I_{SB4}	Standby current (one port CMOS level) CE#L or CE#R ≥ V_{IH}, f = f_{MAX}[20]	Ind.	1.8 V	1.8 V	–	8.5	18	–	8.5	18	–	8.5	14	mA

Note
20. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Electrical Characteristics for V_{CC} = 2.5 V

Over the Operating Range

Parameter	Description		P1 IO Voltage	P2 IO Voltage	CYDMX256A16 CYDMX128A16 –65 Min	CYDMX256A16 CYDMX128A16 –65 Typ	CYDMX256A16 CYDMX128A16 –65 Max	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Min	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Typ	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Max	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Typ	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Max	Unit
V_{OH}	Output HIGH voltage (I_{OH} = –2 mA)		2.5 V (any port)		2.0	–	–	2.0	–	–	2.0	–	–	V
			3.0 V (any port)		2.1	–	–	2.1	–	–	2.1	–	–	V
V_{OL}	Output LOW voltage (I_{OL} = 2 mA)		2.5 V (any port)		–	–	0.4	–	–	0.4	–	–	0.4	V
			3.0 V (any port)		–	–	0.4	–	–	0.4	–	–	0.4	V
V_{OL} ODR	ODR Output LOW voltage (I_{OL} = 8 mA)		2.5 V (any port)		–	–	0.2	–	–	0.2	–	–	0.2	V
			3.0 V (any port)		–	–	0.2	–	–	0.2	–	–	0.2	V
V_{IH}	Input HIGH voltage		2.5 V (any port)		1.7	–	V_{DDIO} + 0.3	1.7	–	V_{DDIO} + 0.3	1.7	–	V_{DDIO} + 0.3	V
			3.0 V (any port)		2.0	–	V_{DDIO} + 0.2	2.0	–	V_{DDIO} + 0.2	2.0	–	V_{DDIO} + 0.2	V
V_{IL}	Input LOW voltage		2.5 V (any port)		–0.3	–	0.6	–0.3	–	0.6	–0.3	–	0.6	V
			3.0 V (any port)		–0.2	–	0.7	–0.2	–	0.7	–0.2	–	0.7	V
I_{OZ}	Output leakage current		2.5 V	2.5 V	–1	–	1	–1	–	1	–1	–	1	µA
			3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{CEX} ODR	ODR output leakage current. V_{OUT} = V_{CC}		2.5 V	2.5 V	–1	–	1	–1	–	1	–1	–	1	µA
			3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{IX}	Input leakage current		2.5 V	2.5 V	–1	–	1	–1	–	1	–1	–	1	µA
			3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{CC}	Operating current (V_{CC} = Max, I_{OUT} = 0 mA) outputs disabled	Ind.	2.5 V	2.5 V	–	39	55	–	39	55	–	28	40	mA
I_{SB1}	Standby current (both ports TTL level) CE#L and CE#R ≥ V_{CC} – 0.2, f = f_{MAX}	Ind.	2.5 V	2.5 V	–	6	8	–	6	8	–	6	8	µA
I_{SB2}	Standby current (one port TTL level) CE#L or CE#R ≥ V_{IH}, f = f_{MAX}	Ind.	2.5 V	2.5 V	–	21	30	–	21	30	–	18	25	mA
I_{SB3}	Standby current (both ports CMOS level) CE#L and CE#R ≥ V_{CC} – 0.2 V, f = 0	Ind.	2.5 V	2.5 V	–	4	6	–	4	6	–	4	6	µA
I_{SB4}	Standby current (one port CMOS level) CE#L or CE#R ≥ V_{IH}, f = f_{MAX}[21]	Ind.	2.5 V	2.5 V	–	21	30	–	21	30	–	18	25	mA

Note
21. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Electrical Characteristics for 3.0 V

Over the Operating Range

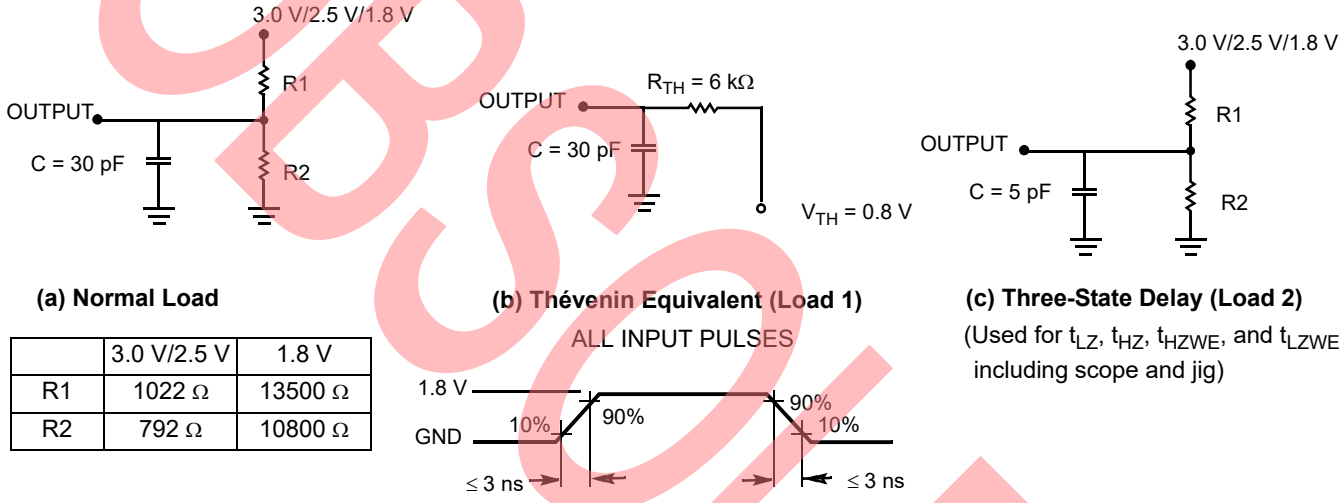
Parameter	Description		P1 IO Voltage	P2 IO Voltage	CYDMX256A16 CYDMX128A16 –65 Min	CYDMX256A16 CYDMX128A16 –65 Typ	CYDMX256A16 CYDMX128A16 –65 Max	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Min	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Typ	CYDMX256B16 CYDMX128B16 CYDMX064B16 –65 Max	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Typ	CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Max	Unit
V_{OH}	Output HIGH voltage (I_{OH} = –2 mA)		3.0 V (any port)		2.1	–	–	2.1	–	–	2.1	–	–	V
V_{OL}	Output LOW voltage (I_{OL} = 2 mA)		3.0 V (any port)		–	–	0.4	–	–	0.4	–	–	0.4	V
V_{OL} ODR	ODR output LOW voltage (I_{OL} = 8 mA)		3.0 V (any port)		–	–	0.2	–	–	0.2	–	–	0.2	V
V_{IH}	Input HIGH voltage		3.0 V (any port)		2.0	–	V_{DDIO} + 0.2	2.0	–	V_{DDIO} + 0.2	2.0	–	V_{DDIO} + 0.2	V
V_{IL}	Input LOW voltage		3.0 V (any port)		–0.2	–	0.7	–0.2	–	0.7	–0.2	–	0.7	V
I_{OZ}	Output leakage current		3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{CEX} ODR	ODR output leakage current. $V_{OUT} = V_{CC}$		3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{IX}	Input leakage current		3.0 V	3.0 V	–1	–	1	–1	–	1	–1	–	1	µA
I_{CC}	Operating current (V_{CC} = Max, I_{OUT} = 0 mA) outputs disabled	Ind.	3.0 V	3.0 V	–	49	70	–	49	70	–	42	60	mA
I_{SB1}	Standby current (both ports TTL level) CE#L and CE#R ≥ V_{CC} – 0.2, f = f_{MAX}	Ind.	3.0 V	3.0 V		7	10		7	10		7	10	µA
I_{SB2}		Ind.	3.0 V	3.0 V		28	40		28	40		25	35	mA
I_{SB3}	Standby current (one port TTL level) CE#L or CE#R ≥ V_{IH}, f = f_{MAX}	Ind.	3.0 V	3.0 V		6	8		6	8		6	8	µA
I_{SB4}		Ind.	3.0 V	3.0 V		28	40		28	40		25	35	mA

Capacitance

Parameter [22]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.0 V	9	pF
C_{OUT}	Output capacitance		10	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



(a) Normal Load

	3.0 V/2.5 V	1.8 V
R1	1022 Ω	13500 Ω
R2	792 Ω	10800 Ω

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 2)

(Used for t_{LZ}, t_{HZ}, t_{HZWE}, and t_{LZWE} including scope and jig)

Note
22. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics for V_{CC} = 1.8 V

Over the Operating Range [23]

Parameter	Description	CYDMX256A16 CYDMX128A16		CYDMX256B16 CYDMX128B16 CYDMX064B16		CYDMX256A16 CYDMX128A16 CYDMX064A16		Unit
		–65		–65		–90		
		Min	Max	Min	Max	Min	Max	
AD Mux Port Read Cycle [24]								
t_{RC}	Read cycle time	65	–	65	–	90	–	ns
t_{ACC1}	Random access ADV# Low to data valid	–	65	–	65	–	90	ns
t_{ACC2}	Random access Address to data valid	–	65	–	65	–	90	ns
t_{ACC3}	Random access CS# to data valid	–	65	–	65	–	90	ns
t_{AVDA}	Random access ADV# High to data valid	–	35	–	35	–	50	ns
t_{AVD}	ADV# low pulse	15	–	15	–	20	–	ns
t_{AVDS}	Address setup to ADV# rising edge	15	–	15	–	20	–	ns
t_{AVDH}	Address hold from ADV# rising edge	3	–	3	–	5	–	ns
t_{CSS}	CS# setup to ADV# rising edge	7	–	7	–	10	–	ns
t_{OE}	OE# Low to data valid	–	35	–	35	–	50	ns
t_{LZOE} [25]	OE# Low to IO Low Z	3	–	3	–	5	–	ns
t_{HZOE}	OE# High to IO High Z	–	15	–	15	–	25	ns
t_{HZCS}	CS# High to IO High Z	–	15	–	15	–	25	ns
t_{DBE}	UB#/LB# Low to IO Valid	–	35	–	35	–	50	ns
t_{LZBE}	UB#/LB# Low to IO Low Z	3	–	3	–	5	–	ns
t_{HZBE}	UB#/LB# High to IO High Z	–	15	–	15	–	25	ns
t_{AVOE}	ADV# High to OE# Low	0	–	0	–	0	–	ns

Notes
23. All timing parameters are measured with Load 2 specified in Figure 2 on page 12.
24. AD Mux port timing applies to left AD Mux port and right port configured to AD Mux port.
25. This parameter is guaranteed by not tested.

Switching Characteristics for V_{CC} = 1.8 V (continued)

Over the Operating Range [23] (continued)

Parameter	Description	CYDMX256A16 CYDMX128A16		CYDMX256B16 CYDMX128B16 CYDMX064B16		CYDMX256A16 CYDMX128A16 CYDMX064A16		Unit
		–65		–65		–90		
		Min	Max	Min	Max	Min	Max	
AD Mux Port Write Cycle[26]								
t_{WC}	Write cycle time	65	–	65	–	90	–	ns
t_{SCS}	CS# Low to write end	65	–	65	–	90	–	ns
t_{AVD}	ADV# Low pulse	15	–	15	–	20	–	ns
t_{AVDS}	Address setup to ADV# rising edge	15	–	15	–	20	–	ns
t_{AVDH}	Address hold from ADV# rising edge	3	–	3	–	5	–	ns
t_{CSS}	CS# setup to ADV# rising edge	7	–	7	–	10	–	ns
t_{WRL}	WE# pulse width	28	–	28	–	45	–	ns
t_{BW}	UB#/LB# Low to write end	28	–	28	–	45	–	ns
t_{SD}	Data setup to write end	20	–	20	–	30	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{LZWE}	WE# High to IO Low Z	0	–	0	–	0	–	ns
t_{AVWE}	ADV# High to WE# Low	0	–	0	–	0	–	ns
Standard Port Read Cycle[27]								
t_{RC}	Read cycle time	40	–	60	–	60	–	ns
t_{AA}	Address to data valid	–	40	–	60	–	60	ns
t_{OHA}	Output hold from address change	5	–	5	–	5	–	ns
t_{ACS}	CS# to data valid	–	40	–	60	–	60	ns
t_{DOE}	OE# Low to data valid	–	25	–	35	–	35	ns
t_{LZOE}[28]	OE# Low to data Low Z	5	–	5	–	5	–	ns
t_{HZOE}	OE# High to data High Z	–	10	–	30	–	30	ns
t_{LZCS}	CS# Low to data Low Z	5	–	5	–	5	–	ns
t_{HZCS}	CS# High to data High Z	–	10	–	30	–	30	ns
t_{LZBE}	UB#/LB# Low to data Low Z	5	–	5	–	5	–	ns
t_{HZBE}	UB#/LB# High to data High Z	–	10	–	30	–	30	ns
t_{ABE}	UB#/LB# access time	–	40	–	60	–	60	ns

Notes
26. AD Mux port timing applies to left AD Mux port and right port configured to AD Mux port.
27. Standard SRAM port timing applies to right port configured to standard SRAM port.
28. This parameter is guaranteed by not tested.

Switching Characteristics for V_{CC} = 1.8 V (continued)

Over the Operating Range [23] (continued)

Parameter	Description	CYDMX256A16 CYDMX128A16		CYDMX256B16 CYDMX128B16 CYDMX064B16		CYDMX256A16 CYDMX128A16 CYDMX064A16		Unit
		–65		–65		–90		
		Min	Max	Min	Max	Min	Max	
Standard SRAM Port Write Cycle								
t_{WC}	Write cycle time	40	–	60	–	60	–	ns
t_{SCS}	CS# Low to Write End	30	–	50	–	50	–	ns
t_{AW}	Address valid to write end	30	–	50	–	50	–	ns
t_{HA}	Address hold from write end	0	–	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	0	–	ns
t_{WRL}	Write pulse width	25	–	45	–	45	–	ns
t_{SD}	Data setup to write end	20	–	30	–	30	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{HZWE}	WE# Low to data High Z	–	15	–	25	–	25	ns
t_{LZWE}	WE# High to data Low Z	0	–	0	–	0	–	ns
Arbitration Timing								
t_{BLA}	BUSY# Low from address match	–	30	–	50	–	50	ns
t_{BHA}	BUSY# High from address mismatch	–	30	–	50	–	50	ns
t_{BLC}	BUSY# Low from CS# Low	–	30	–	50	–	50	ns
t_{BHC}	BUSY# High from CS# High	–	30	–	50	–	50	ns
t_{PS}[29]	Port setup from priority	5	–	5	–	5	–	ns
t_{BDD}	BUSY# High to data valid	–	30	–	50	–	50	ns
t_{WDD}	Write pulse to data delay	–	55	–	85	–	85	ns
t_{DDD}	Write data valid to read data valid	–	45	–	70	–	70	ns
Interrupt Timing								
t_{INS}	INT# set time	–	35	–	55	–	55	ns
t_{INR}	INT# reset time	–	35	–	55	–	55	ns

Note
29. Add 2 ns to this parameter if VCC and VDDIOR are < 1.8 V, and VDDIOL is > 2.5 V at temperature < 0 °C.

Switching Waveforms

Figure 3. ADM Port Read Cycle (Either Port Access, WE# High)

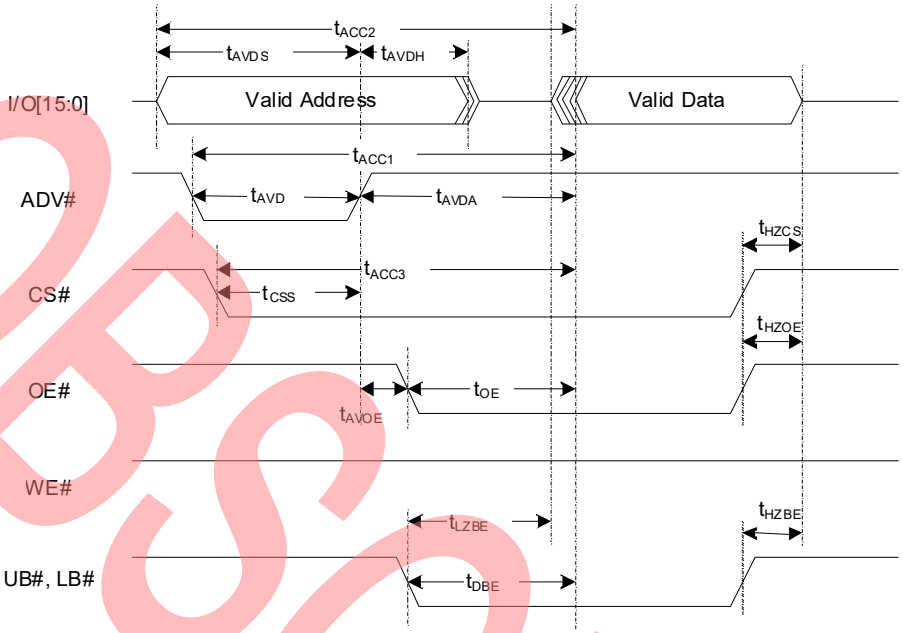


Figure 4. ADM Port Write Cycle (Either Port Access, WE# Controlled, OE# High)

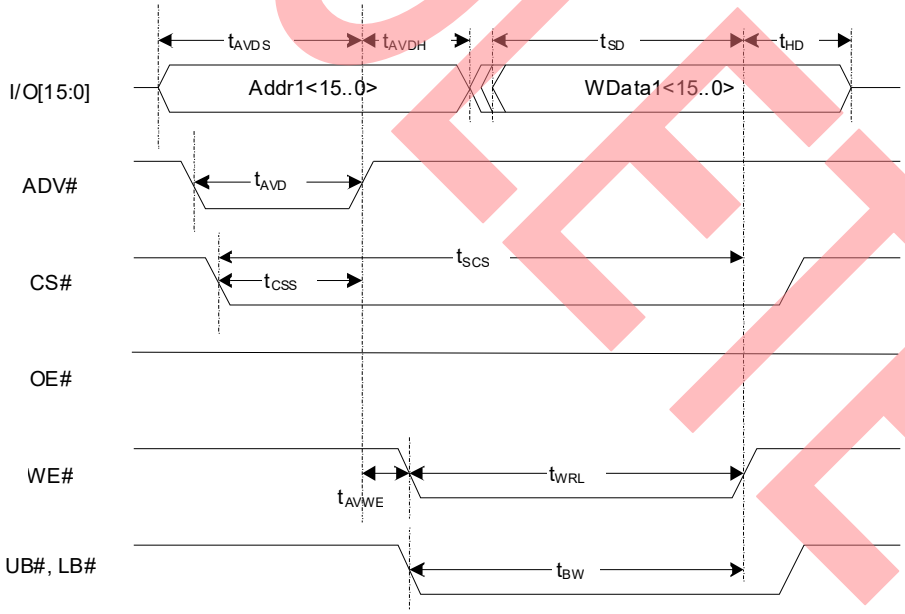


Figure 5. ADM Port Write Cycle (Either Port Access, CS# Controlled, OE# High)

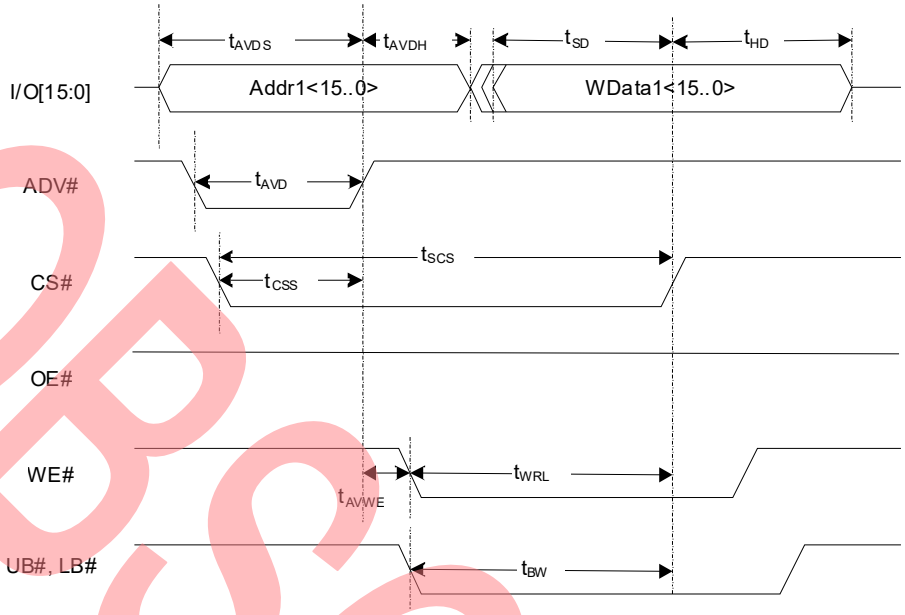


Figure 6. Standard Port Read Cycle (Right Port Access, WE# High)

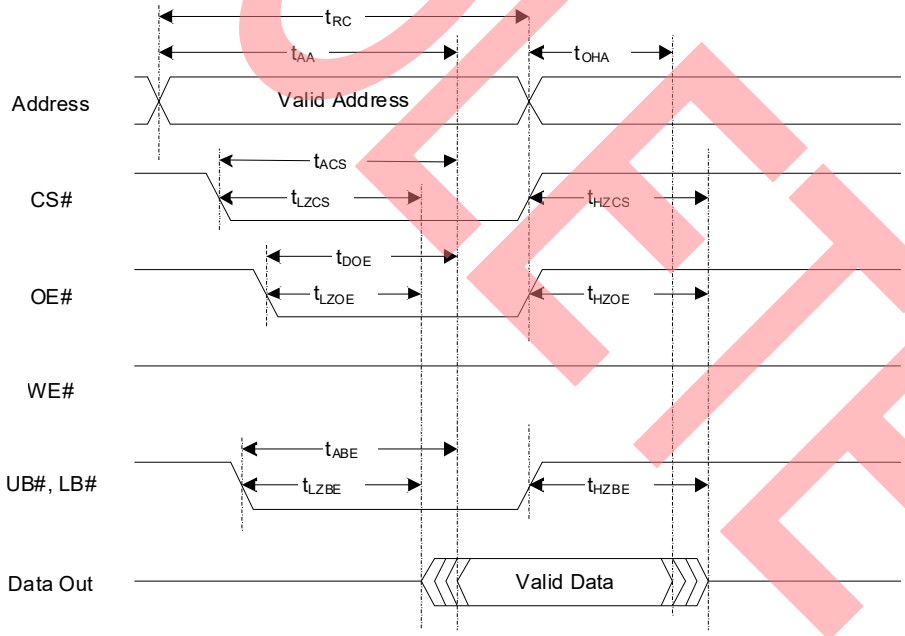


Figure 7. Standard Port Write Cycle (Right Port Access, WE# Controlled)

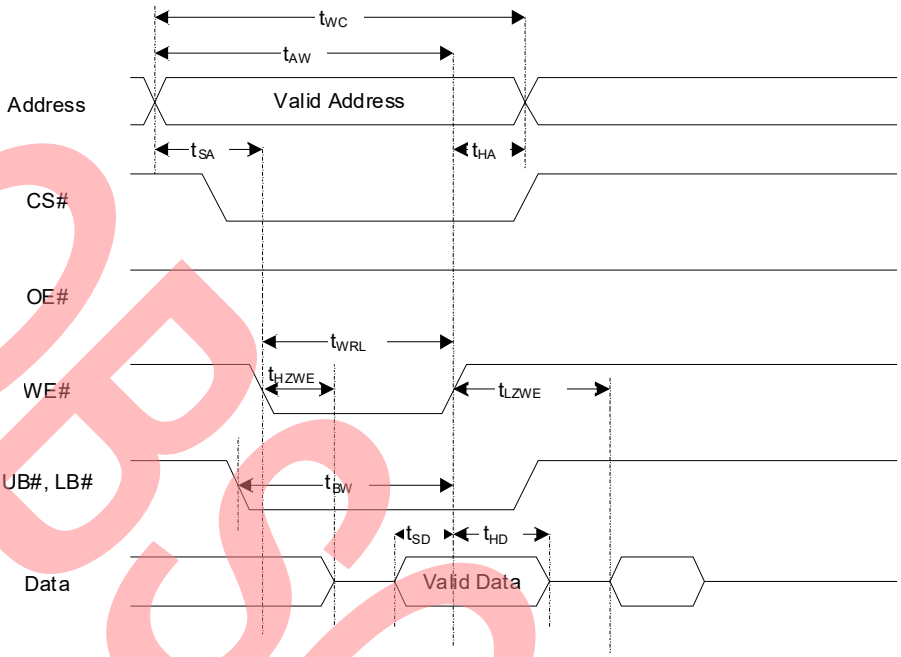


Figure 8. Standard Port Write Cycle (Right Port Access, CS# Controlled)

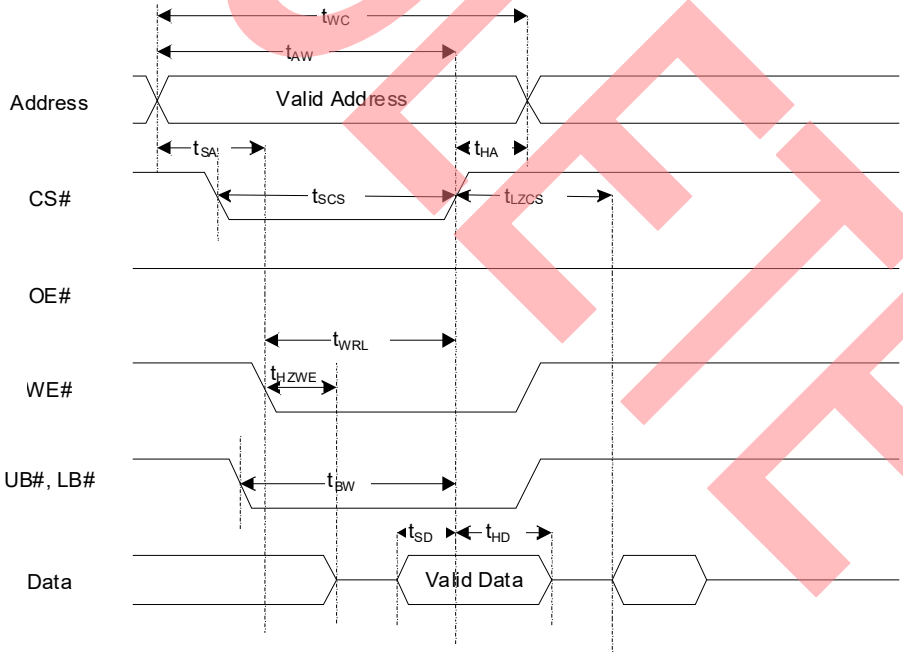


Figure 9. Arbitration Timing

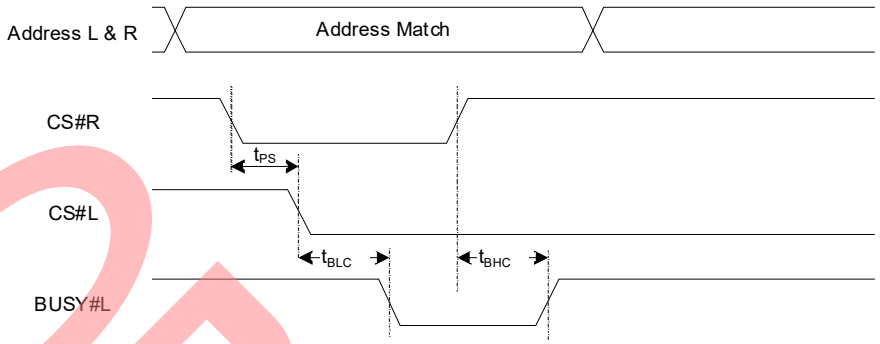


Figure 10. Arbitration Timing (Address Controlled with Left ADM and Right Standard Configuration

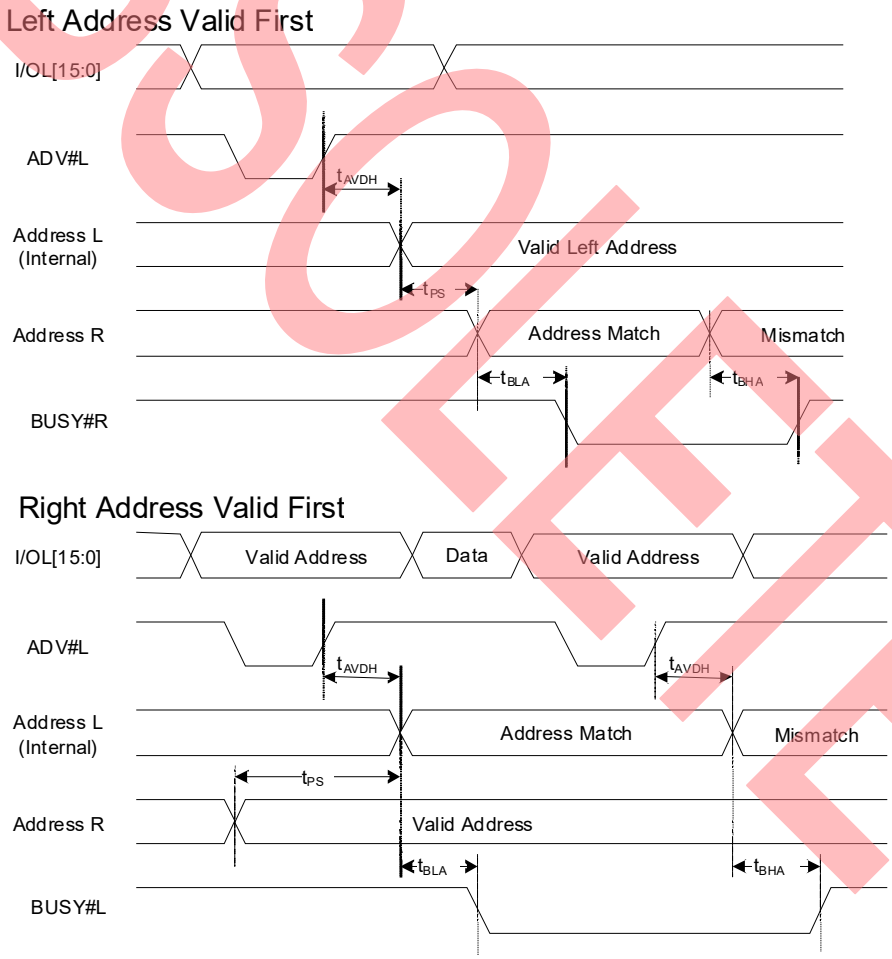


Figure 11. Arbitration Timing (Address Controlled with Left ADM and Right ADM Configuration)

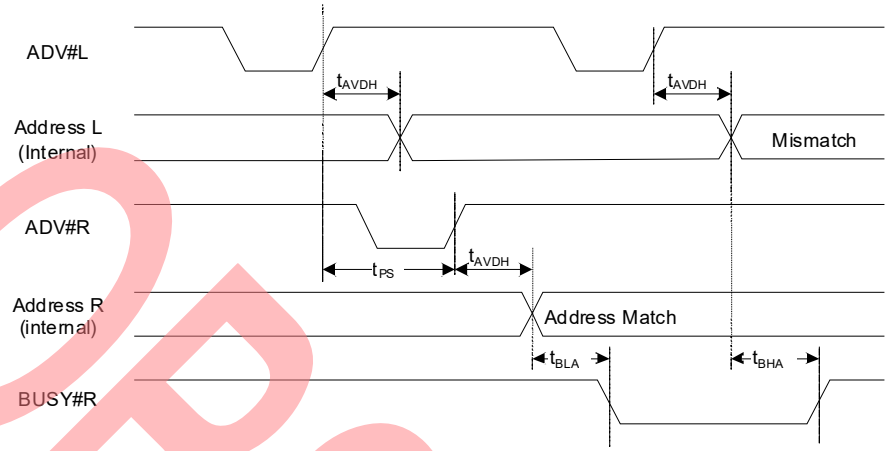


Figure 12. Read with BUSY# Timing

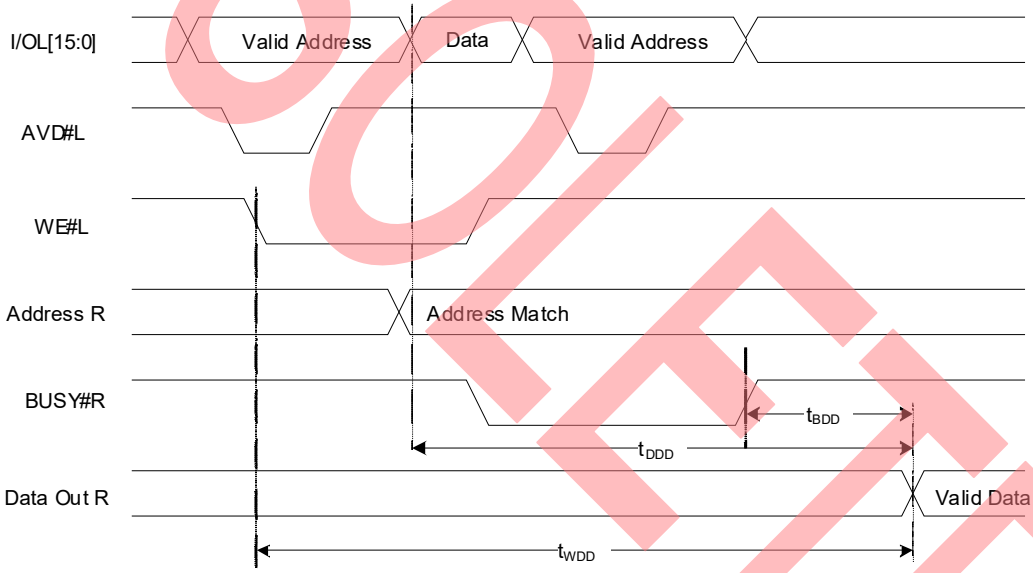
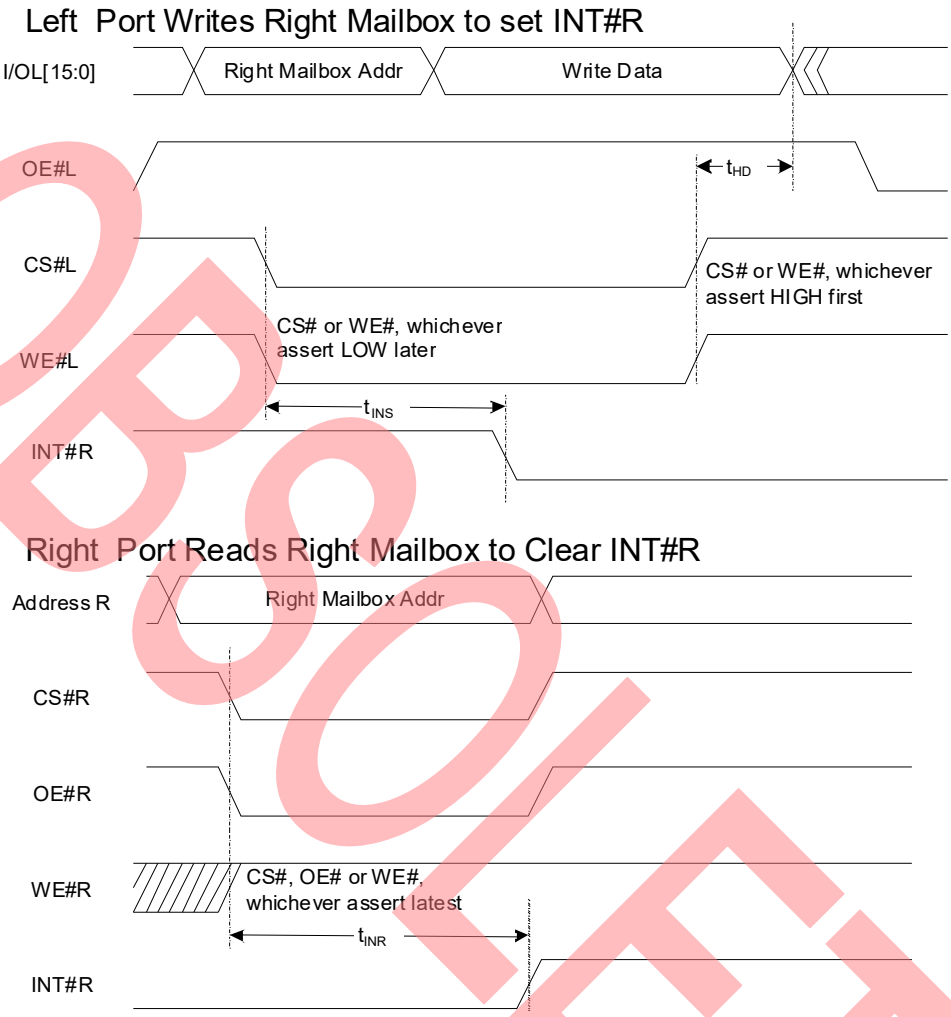


Figure 13. Interrupt Timing



Ordering Information

16K × 16 MoBL ADM Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
65	CYDMX256A16-65BVXI	BZ100	100-ball Pb-free 0.5 mm pitch BGA	Industrial
65	CYDMX256B16-65BVXI	BZ100	100-ball Pb-free 0.5 mm pitch BGA	Industrial
90	CYDMX256A16-90BVXI	BZ100	100-ball Pb-free 0.5 mm pitch BGA	Industrial

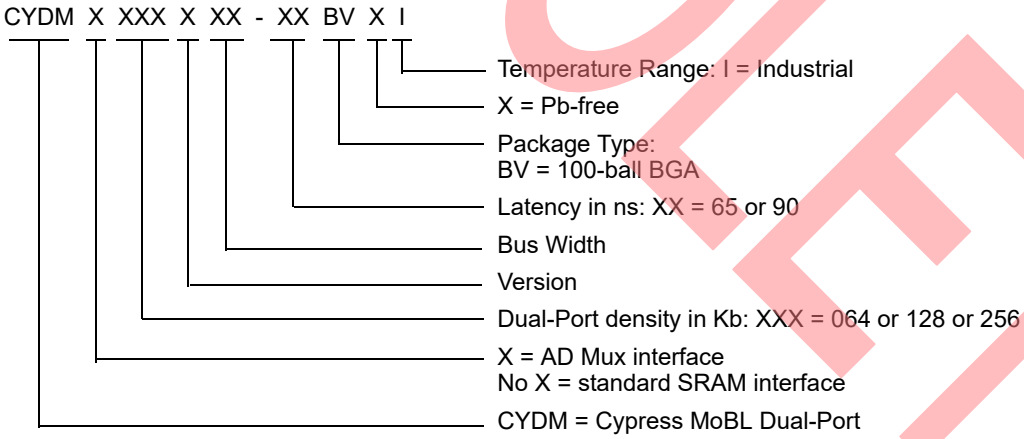
8K × 16 MoBL ADM Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
65	CYDMX128A16-65BVXI	BZ100	100-ball BGA Pb-free	Industrial
65	CYDMX128B16-65BVXI	BZ100	100-ball BGA Pb-free	Industrial

4K × 16 MoBL ADM Asynchronous Dual-Port SRAM

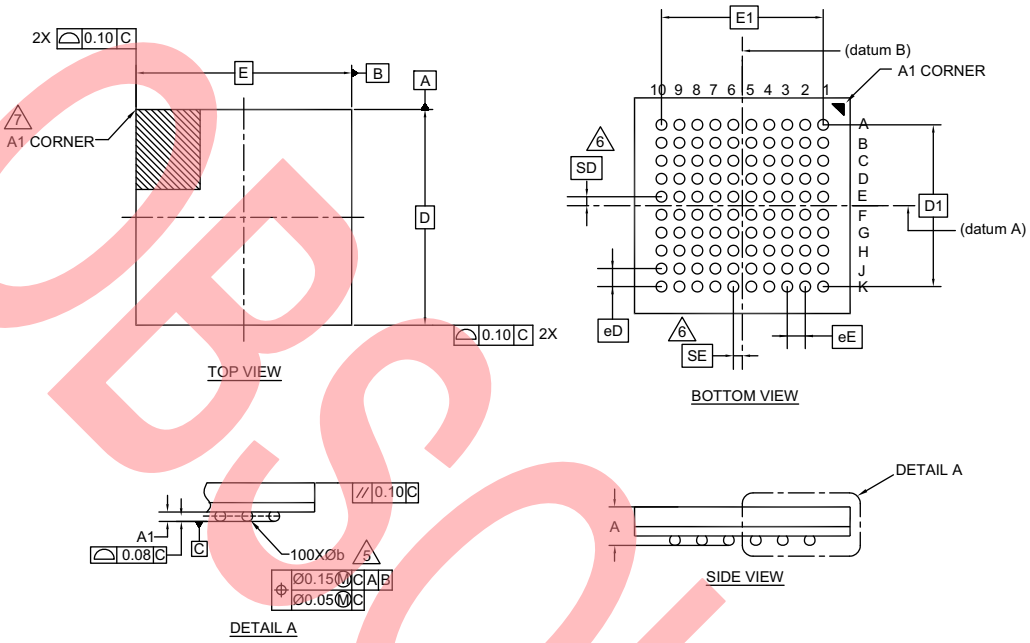
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
90	CYDMX064A16-90BVXI	BZ100	100-ball BGA Pb-free	Industrial

Ordering Code Definitions



Package Diagram

Figure 14. 100-ball VFBGA (6 × 6 × 1.0 mm) BZ100 Package Outline, 51-85209



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	4.50 BSC		
E1	4.50 BSC		
MD	10		
ME	10		
N	100		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

Acronyms

Acronym	Description
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CS}$	Chip Select
I/O	Input/Output
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor-Transistor Logic
ODR	Output Drive Register
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CYDMX256A16/CYDMX256B16/CYDMX128A16/CYDMX128B16/CYDMX064A16/CYDMX064B16, 16K/8K/4K × 16 MoBL® ADM Asynchronous Dual-Port Static RAM Document Number: 001-08090				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	462234	HKH	05/22/2006	New data sheet.
*A	491702	HKH	08/23/2006	Updated Switching Characteristics for VCC = 1.8 V: Removed tBW parameter and its corresponding details under “Standard SRAM Port Write Cycle”. Updated values corresponding to tWC, tSCS, tAW, tWRL parameters. Fixed typo.
*B	500425	HKH	09/07/2006	Changed status from Preliminary to Final. Removed “Cypress Confidential” from header across the document. Updated Electrical Characteristics for VCC = 1.8 V: Replaced TBD with corresponding values. Updated Electrical Characteristics for VCC = 2.5 V: Replaced TBD with corresponding values. Updated Switching Characteristics for VCC = 1.8 V: Added Note 25 and referred the same note in tLZOE parameter under “AD Mux Port Read Cycle”. Updated values of tWC, tSCS parameters under “AD Mux Port Write Cycle” (to reflect bin spec). Added Note 29 and referred the same note in tPS parameter.
*C	2147866	YDT / HKH / AESA	02/27/2008	Updated Switching Characteristics for VCC = 1.8 V: Added a column “CYDMX256B16/CYDMX128B16/CYDMX064B16” and added details of all parameters corresponding to 65 ns speed bin. Updated Ordering Information: Updated part numbers.
*D	3031102	VED	09/15/2010	No technical updates. Post to external web.
*E	3053582	HKH	10/08/2010	Updated Ordering Information: Updated part numbers. Added Ordering Code Definitions. Updated to new template.
*F	3209987	HKH	03/30/2011	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85209 – Changed revision from *C to *D. Updated to new template.
*G	3246085	HKH	05/02/2011	Added Acronyms and Units of Measure. Completing Sunset Review.
*H	3401875	HKH	10/11/2011	Updated Ordering Information: Updated part numbers.
*I	4418141	HBM	06/24/2014	Updated to new template. Completing Sunset Review.
*J	5836836	RAJV	07/28/2017	Updated Package Diagram: spec 51-85209 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*K	6498283	RAJV	03/01/2019	Obsolete document.

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