



**THE DATASHEET OF
CYBLE-022001-00**



AIROC™ Bluetooth® LE module

General description

The Infineon AIROC™ CYBLE-022001-00 is a fully certified and qualified module supporting Bluetooth® Low Energy wireless communication. The CYBLE-022001-00 is a turnkey solution and includes on-board crystal oscillators, chip antenna, passive components, and Infineon PSoC™ 4 Bluetooth® LE. Refer to the PSoC™ 4 Bluetooth® LE [datasheet](#) for additional details on the capabilities of the PSoC™ 4 Bluetooth® LE device used on this module.

The CYBLE-022001-00 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols (I²C, UART, SPI) through its programmable architecture. The CYBLE-022001-00 includes a royalty-free Bluetooth® LE stack compatible with Bluetooth® 5.1 and provides up to 16 GPIOs in a small 10 × 10 × 1.80 mm package.

The CYBLE-022001-00 is a complete solution and an ideal fit for applications requiring Bluetooth® LE wireless connectivity.

Module description

- Module size: 10.0 mm × 10.0 mm × 1.80 mm (with shield)
- Bluetooth® 5.1 single-mode module
- Industrial temperature range: -40°C to +85°C
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- 128-KB flash memory, 16-KB SRAM memory
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Two-pin SWD for programming
- Up to 16 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z analog, HI-Z digital, or strong output
- Certified to FCC, ISED, MIC, KC, and CE regulations
 - FCC ID: WAP2001
 - IC ID: 7922A-2001
 - MIC ID: 005-101007
 - KC ID: MSIP-CRM-Cyp-2001
- Bluetooth® SIG 5.1 qualified
 - QDID: **141250**
 - Declaration ID: **U048555**

Power consumption

- TX output power: -18 dbm to +3 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption of 15.6 mA (radio only, 0 dbm)
- RX current consumption of 16.4 mA (radio only)
- Low power mode support
 - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
 - Hibernate: 150 nA with SRAM retention
 - Stop: 60 nA with XRES wakeup

Functional capabilities

Functional capabilities

- Up to 15 capacitive sensors for buttons or sliders with best-in-class signal-to-noise ratio (SNR) and liquid tolerance
- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two Serial Communication Blocks (SCBs) supporting I²C (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM blocks (TCPWMs)
- Programmable low voltage detect (LVD) from 1.8 V to 4.5 V
- I²S master interface
- Bluetooth® Low Energy protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard Bluetooth® Low Energy profiles and services for interoperability
- Custom profile and service for specific use cases

Benefits

The CYBLE-022001-00 module is provided as a turnkey solution, including all necessary hardware required to use Bluetooth® LE communication standards.

- Proven, qualified, and certified hardware design ready to use
- Small footprint (10 × 10 mm × 1.80 mm), perfect for space constrained applications
- Reprogrammable architecture
- Fully certified module eliminates the time needed for design, development and certification processes
- Bluetooth® SIG qualified with QDID and Declaration ID
- Flexible communication protocol support
- PSoC™ Creator provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a Bluetooth® LE application

More information

Infineon provides a wealth of data at www.infineon.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: [AIROC™ Bluetooth® & Multiprotocol](#)
- PSoC™ 4 BLE silicon datasheet
- Application notes: Infineon offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with AIROC™ Bluetooth® LE modules are:
 - [AN96841](#) - Getting Started with EZ-BLE Module
 - [AN91267](#) - Getting started with PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE
 - [AN97060](#) - PSoC™ 4 BLE and PRoC™ BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) guide
 - [AN91162](#) - Creating a BLE Custom Profile
 - [AN91184](#) - PSoC™ 4 BLE - Designing BLE Applications
 - [AN92584](#) - Designing for Low Power and Estimating Battery Life for BLE Applications
 - [AN85951](#) - PSoC™ 4 and PSoC™ 6 MCU CAPSENSE™ design guide
 - [AN95089](#) - PSoC™ 4/PRoC™ BLE Crystal Oscillator Selection and Tuning Techniques
 - [AN91445](#) - Antenna Design and RF Layout Guidelines

Two easy-to-use design environments to get you started quickly

- Technical reference manual (TRM):
 - PSoC™ BLE [Technical reference manual](#)
- Knowledge base articles
 - [KBA97279](#) - Pin Mapping Differences Between the EZ-BLE™ Creator Evaluation Board (CYBLE-022001-EVAL) and the BLE Pioneer Kit (CY8CKIT-042-BLE)
 - [KBA97094](#) - RF Regulatory Certifications for EZ-BLE™ Creator Module
 - [KBA97095](#) - EZ-BLE™ Module Placement
 - [KBA213976](#) - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
 - [KBA210802](#) - Queries on BLE Qualification and Declaration Processes
 - [KBA218122](#) - 3D Model Files for EZ-BLE/EZ-BT Modules
- Development kits:
 - [CYBLE-022001-EVAL](#), CYBLE-022001-00 Evaluation Board
 - [CY8CKIT-042-BLE](#), Bluetooth® Low Energy Pioneer Kit
 - [CY8CKIT-002](#), PSoC™ MiniProg3 Program and Debug Kit
- Test and debug tools:
 - [CYSmart](#), AIROC™ Bluetooth® Connect App — Bluetooth® LE Test and Debug Tool
 - [CYSmart Mobile](#), AIROC™ Bluetooth® Connect App— Mobile App

Two easy-to-use design environments to get you started quickly

1. PSoC™ Creator Integrated Design Environment (IDE)

PSoC™ Creator is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling and debugging of PSoC™ 3, PSoC™ 4, PSoC™ 5LP, PSoC™ 4 Bluetooth® LE, and AIROC™ Bluetooth® LE module systems with no code size limitations. PSoC™ peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC™ Components.

PSoC™ Components are analog and digital “virtual chips,” represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

2. PSoC™ Creator Component Datasheet - Bluetooth Low Energy (BLE)

The **PSoC™ Creator Component Datasheet - Bluetooth Low Energy (BLE)** provides a comprehensive GUI-based configuration window that lets you quickly design Bluetooth® LE applications. The Component incorporates a Bluetooth® Core Specification v5.1 compliant Bluetooth® LE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth® Low Energy Sub-System (BLESS) hardware via the stack.

AIROC™ Bluetooth® & Bluetooth® LE module firmware platform

The **AIROC™ Bluetooth® & Bluetooth® LE module firmware platform** provides a simple way to access the most common hardware and communication features needed in Bluetooth® LE applications. AIROC™ Bluetooth® & Bluetooth® LE module firmware implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module’s GPIOs, making it easy to add Bluetooth® LE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE. Refer to the AIROC™ Bluetooth® & Bluetooth® LE module firmware webpage for User Manuals and instructions for getting started as well as detailed reference materials.

AIROC™ Bluetooth® LE modules are pre-flashed with the AIROC™ Bluetooth® & Bluetooth® LE module firmware platform. If you do not have AIROC™ Bluetooth® & Bluetooth® LE module firmware pre-loaded on your module, you can download each AIROC™ Bluetooth® LE module’s firmware images on the [AIROC™ Bluetooth® & Bluetooth® LE module firmware webpage](#).

Technical support

Technical support

- **Frequently asked questions (FAQs)**: Learn more about our Bluetooth® LE ECO System.
- **Forum**: See if your question is already answered by fellow developers on the PSoC™ 4 Bluetooth® LE forum.
- Visit our **support** page and create a **technical support case** or contact a **local sales representatives**. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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1 Overview

1.1 Module description

The CYBLE-022001-00 module is a complete module designed to be soldered to the applications main board.

Module dimensions and drawing:

Infineon reserves the right to select components (including the appropriate Bluetooth® LE device) from various vendors to achieve the Bluetooth® LE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in [Figure 1](#). All dimensions are in millimeters (mm).

Table 1 Module design dimensions

| Dimension item | | Specification |
|--|------------|--------------------------------|
| Module dimensions | Length (X) | 10.00 ± 0.15 mm |
| | Width (Y) | 10.00 ± 0.15 mm |
| Antenna location dimensions | Length (X) | 7.00 ± 0.15 mm |
| | Width (Y) | 5.00 ± 0.15 mm |
| PCB thickness | Height (H) | 0.50 ± 0.10 mm |
| Shield height | Height (H) | 1.10 ± 0.10 mm |
| Maximum component height | Height (H) | 1.30-mm typical (chip antenna) |
| Total module thickness (bottom of module to highest component) | Height (H) | 1.80-mm typical |

See [Figure 1](#) for the mechanical reference drawing for CYBLE-022001-00.

Overview

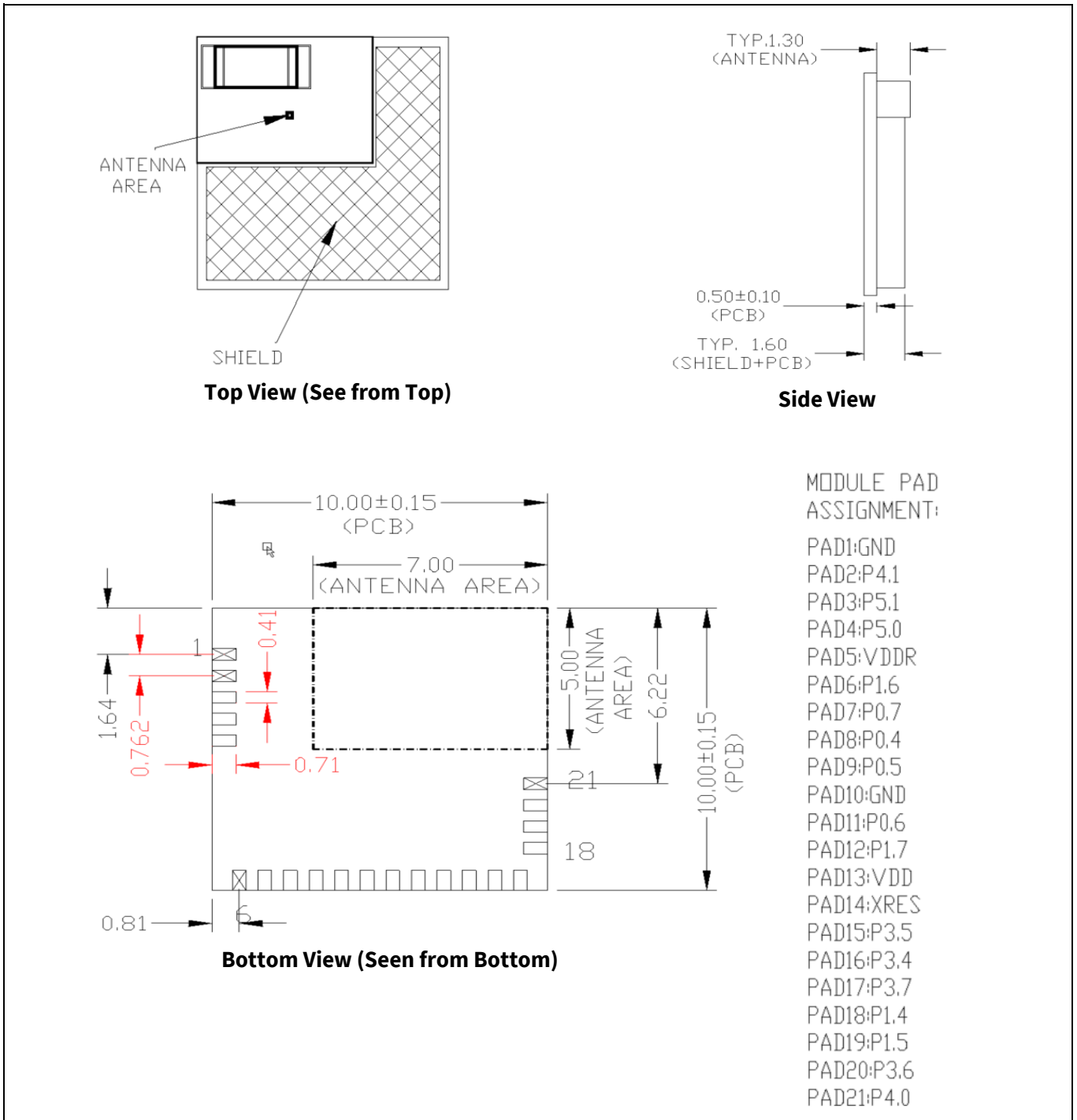


Figure 1 Module mechanical drawing

Note

1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see **“Recommended host PCB layout”** on page 10.

Pad connection interface

2 Pad connection interface

As shown in the bottom view of **Figure 1**, the CYBLE-022001-00 connects to the host board via solder pads on the back of the module. **Table 2** and **Figure 2** detail the solder pad length, width, and pitch dimensions of the CYBLE-022001-00 module.

Table 2 Solder pad connection description

| Name | Connections | Connection type | Pad length dimension | Pad width dimension | Pad pitch |
|------|-------------|-----------------|----------------------|---------------------|-----------|
| SP | 21 | Solder Pads | 0.71 mm | 0.41 mm | 0.76 mm |

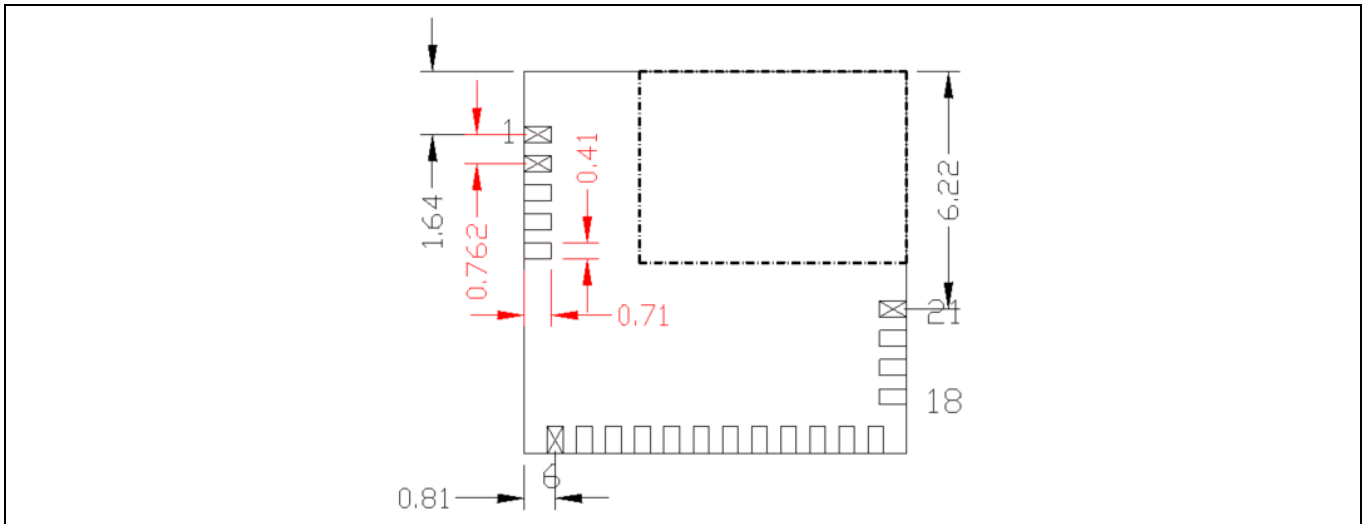


Figure 2 Solder pad dimensions (seen from bottom)

To maximize RF performance, the host layout should follow these recommendations:

- The ideal placement of the Infineon Bluetooth® LE module is in a corner of the host board with the chip antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Refer to **AN96841** for module placement best practices.
- To maximize RF performance, the area immediately around the Infineon Bluetooth® LE module chip antenna should contain an additional keep out area, where no grounding or signal traces are contained. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in **Figure 4** (dimensions are in mm).

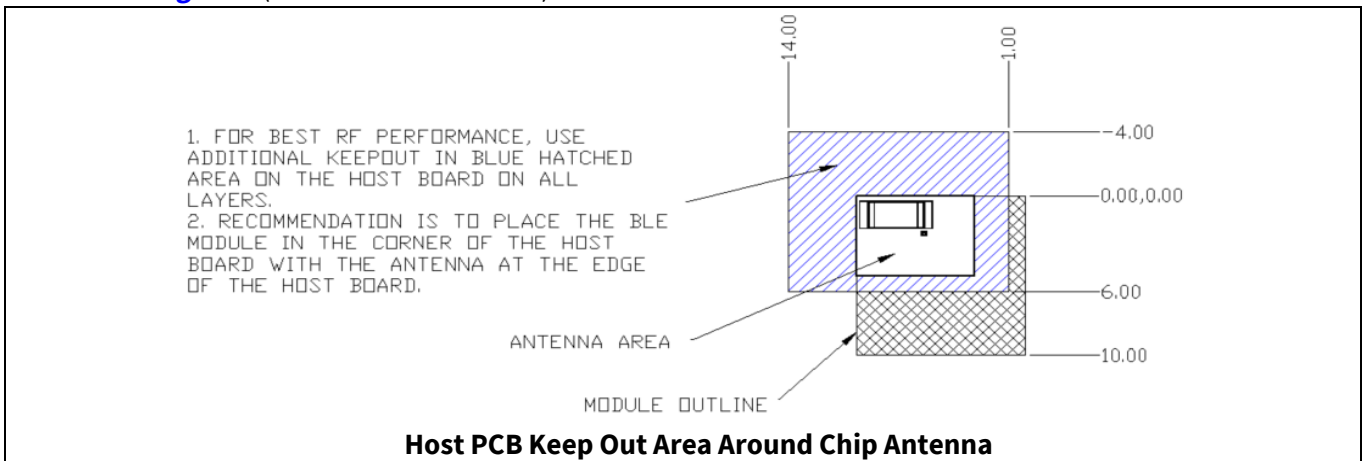


Figure 3 Recommended host PCB keep out area around the CYBLE-022001-00 chip antenna

Recommended host PCB layout

Table 3 provides the center location for each solder pad on the CYBLE-022001-00. All dimensions are referenced to the center of the solder pad. Refer to **Figure 6** for the location of each module solder pad.

Table 3 Module solder pad location

| Solder pad (Center of pad) | Location (X,Y) from origin (mm) | Dimension from origin (mils) |
|---------------------------------------|--|-------------------------------------|
| 1 | (0.26, 1.64) | (10.24, 64.57) |
| 2 | (0.26, 2.41) | (10.24, 94.88) |
| 3 | (0.26, 3.17) | (10.24, 124.80) |
| 4 | (0.26, 3.93) | (10.24, 154.72) |
| 5 | (0.26, 4.69) | (10.24, 184.65) |
| 6 | (0.81, 9.74) | (31.89, 383.46) |
| 7 | (1.57, 9.74) | (61.81, 383.46) |
| 8 | (2.34, 9.74) | (92.13, 383.46) |
| 9 | (3.10, 9.74) | (122.05, 383.46) |
| 10 | (3.86, 9.74) | (151.97, 383.46) |
| 11 | (4.62, 9.74) | (181.89, 383.46) |
| 12 | (5.38, 9.74) | (211.81, 383.46) |
| 13 | (6.15, 9.74) | (242.13, 383.46) |
| 14 | (6.91, 9.74) | (272.05, 383.46) |
| 15 | (7.67, 9.74) | (301.97, 383.46) |
| 16 | (8.43, 9.74) | (331.89, 383.46) |
| 17 | (9.19, 9.74) | (361.81, 383.46) |
| 18 | (9.75, 8.50) | (383.86, 334.65) |
| 19 | (9.75, 7.74) | (383.86, 304.72) |
| 20 | (9.75, 6.98) | (383.86, 274.80) |
| 21 | (9.75, 6.22) | (383.86, 244.88) |

Recommended host PCB layout

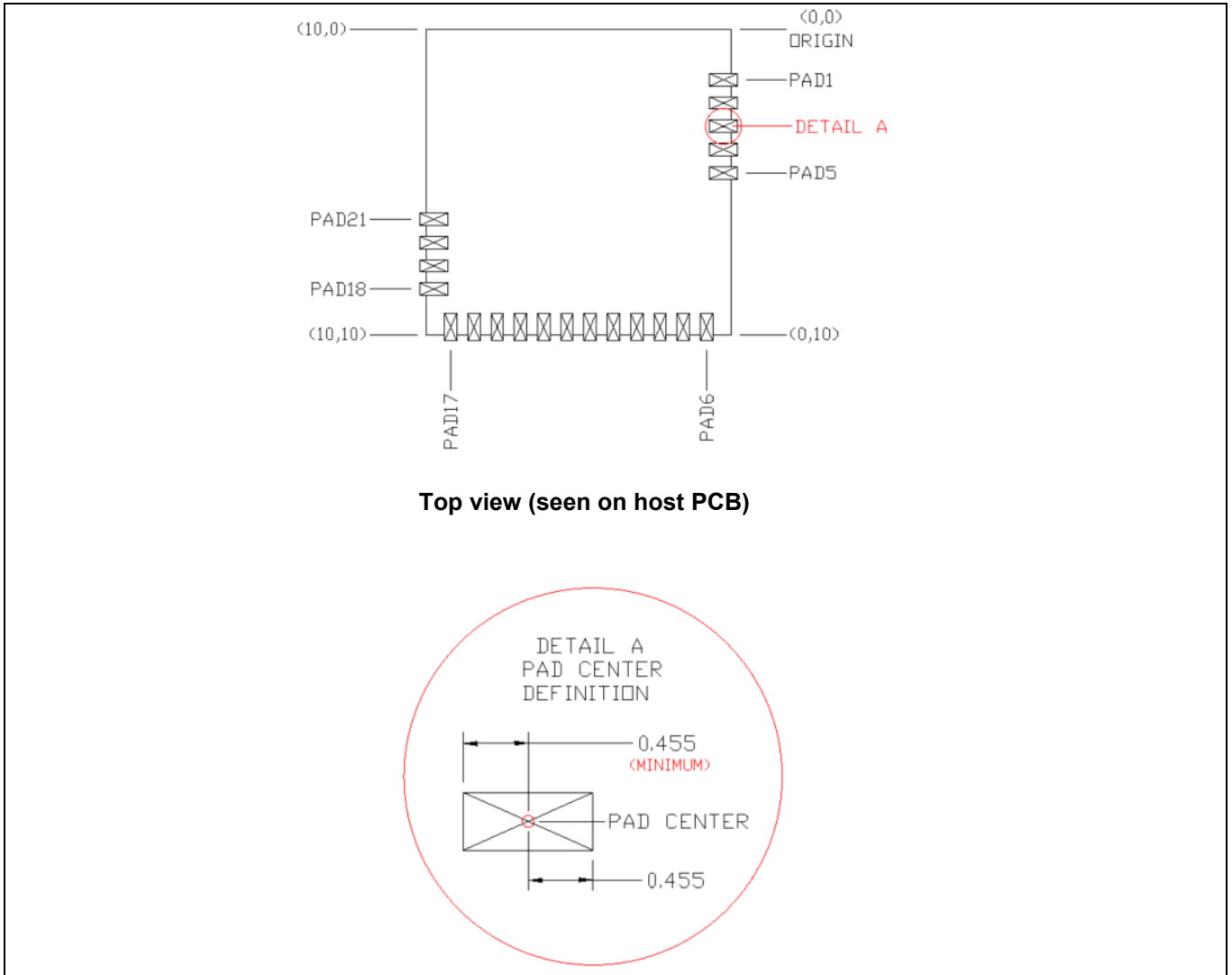


Figure 6 Solder pad reference location

Digital and analog capabilities and connections

4 Digital and analog capabilities and connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. **Table 4** lists the solder pads on CYBLE-022001-00, the Bluetooth® LE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

Table 4 Solder pad connection definitions

| Solder pad number | Device port pin | UART | SPI | I ² C | TCPWM ^[2,3] | CapSense | WCO Out | ECO Out | LCD | SWD | GPIO |
|-------------------|---------------------|---|--------------|------------------|------------------------|----------------------------------|---------|---------|-----|---------------|------|
| 1 | GND ^[4] | Ground Connection | | | | | | | | | |
| 2 | P4.1 ^[5] | ✓(SCB1_CTS) | ✓(SCB1_MISO) | | ✓(TCPWM0_N) | ✓(Sensor/ C _{TANK}) | | | ✓ | | ✓ |
| 3 | P5.1 | ✓(SCB1_TX) | ✓(SCB1_SCLK) | ✓(SCB1_SCL) | ✓(TCPWM3_N) | ✓(Sensor) | | ✓ | ✓ | | ✓ |
| 4 | P5.0 | ✓(SCB1_RX) | ✓(SCB1_SS0) | ✓(SCB1_SDA) | ✓(TCPWM3_P) | ✓(Sensor) | | | ✓ | | ✓ |
| 5 | V _{DDR} | Radio Power Supply (1.9V to 5.5V) | | | | | | | | | |
| 6 | P1.6 | ✓(SCB0_RTS) | ✓(SCB0_SS0) | | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 7 | P0.7 | ✓(SCB0_CTS) | ✓(SCB0_SCLK) | | ✓(TCPWM) | ✓(Sensor) | | | ✓ | ✓ (SWDCLK) | ✓ |
| 8 | P0.4 | ✓(SCB0_RX) | ✓(SCB0_MOSI) | ✓(SCB0_SDA) | ✓(TCPWM) | ✓(Sensor) | | ✓ | ✓ | | ✓ |
| 9 | P0.5 | ✓(SCB0_TX) | ✓(SCB0_MISO) | ✓(SCB0_SCL) | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 10 | GND | Ground Connection | | | | | | | | | |
| 11 | P0.6 | ✓(SCB0_RTS) | ✓(SCB0_SS0) | | ✓(TCPWM) | ✓(Sensor) | | | ✓ | ✓ (SWDIO) | ✓ |
| 12 | P1.7 | ✓(SCB0_CTS) | ✓(SCB0_SCLK) | | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 13 | V _{DD} | Digital Power Supply Input (1.71 to 5.5V) | | | | | | | | | |
| 14 | XRES | External Reset Hardware Connection Input | | | | | | | | | |
| 15 | P3.5 | ✓(SCB1_TX) | | ✓(SCB1_SCL) | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 16 | P3.4 | ✓(SCB1_RX) | | ✓(SCB1_SDA) | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 17 | P3.7 | ✓(SCB1_CTS) | | | ✓(TCPWM) | ✓(Sensor) | ✓ | | ✓ | | ✓ |
| 18 | P1.4 | ✓(SCB0_RX) | ✓(SCB0_MOSI) | ✓(SCB0_SDA) | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 19 | P1.5 | ✓(SCB0_TX) | ✓(SCB0_MISO) | ✓(SCB0_SCL) | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 20 | P3.6 | ✓(SCB1_RTS) | | | ✓(TCPWM) | ✓(Sensor) | | | ✓ | | ✓ |
| 21 | P4.0 ^[6] | ✓(SCB1_RTS) | ✓(SCB1_MOSI) | | ✓(TCPWM0_P) | ✓(C _{MOD}) | | | ✓ | | ✓ |

Notes

- TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
- TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.
- The main board needs to connect both GND connections (Pad 1 and Pad 10) on the module to the common ground of the system.
- When using the capacitive sensing functionality, Pad 2 (P4.1) can be connected to a C_{TANK} capacitor (located off of Infineon Bluetooth® LE Module). C_{Tank} should be used if implementing a shield layer on the capacitive sensor. If used, this capacitor should be placed as close to the module as possible.
- When using the capacitive sensing functionality, Pad 21 (P4.0) must be connected to a C_{MOD} capacitor (located off of Infineon Bluetooth® LE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
- If the I²S feature is used in the design, the I²S pins shall be dynamically routed to the appropriate available GPIO by PSoC™ Creator

Power supply connections and recommended external components

5 Power supply connections and recommended external components

5.1 Power connections

The CYBLE-022001-00 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio. VDD accepts a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 1.9 V to 5.5 V. These specifications can be found in [Table 9](#). The maximum power supply ripple for both power connections on the module is 100 mV, as shown in [Table 7](#).

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

5.2 Connection options

Two connection options are available for any application:

- Single supply: Connect VDD and VDDR to the same supply.
- Independent supply: Power VDD and VDDR separately.

5.3 External component recommendation

In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

[Figure](#) details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-022001-00.

[Figure 8](#) details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω, 100 MHz (Murata BLM21PG331SN1D).

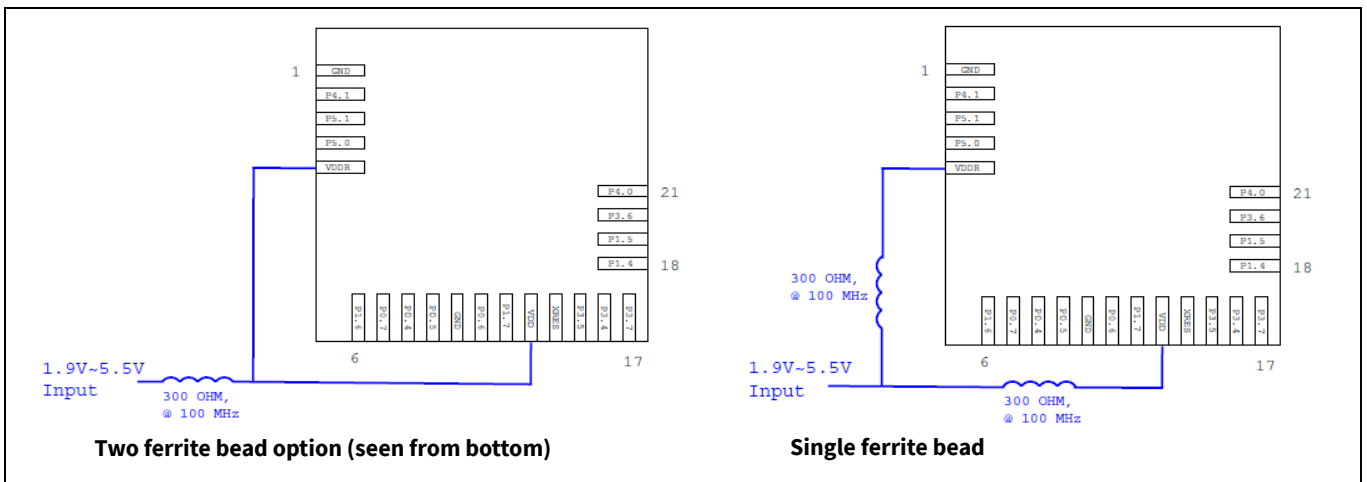


Figure 7 Recommended host schematic options for a Single Supply Option

Power supply connections and recommended external components

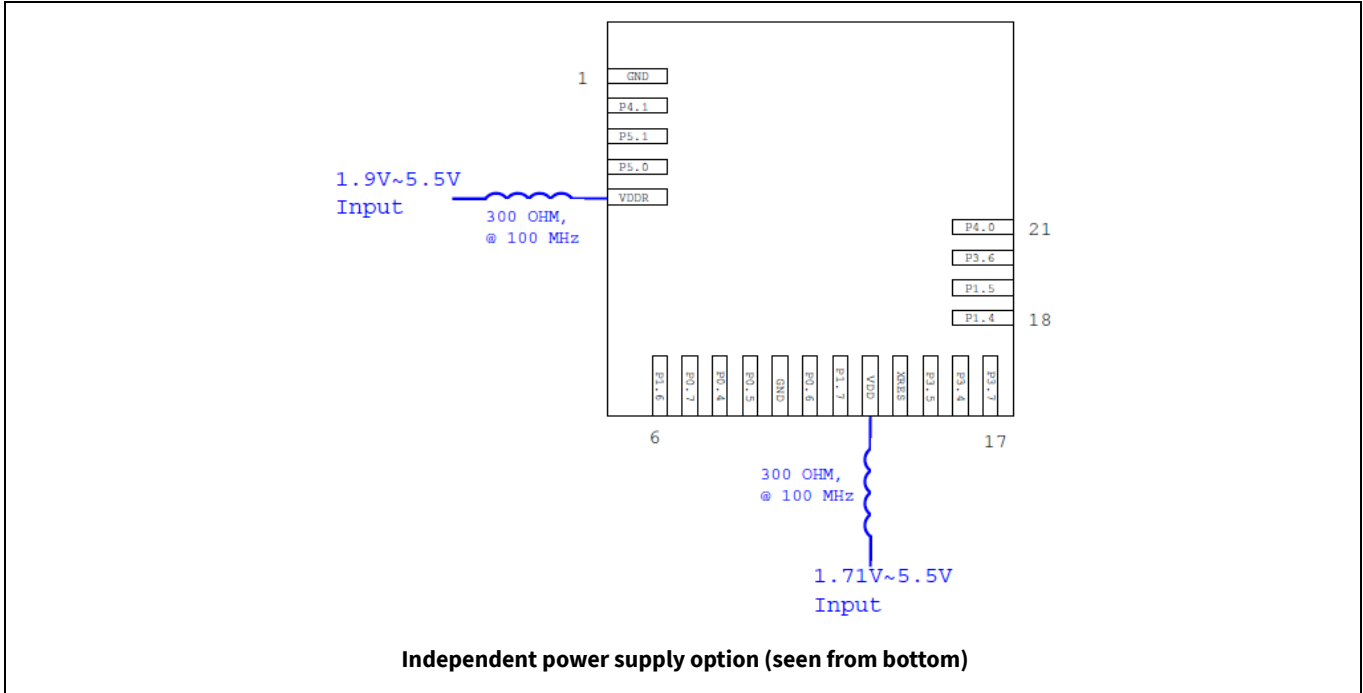


Figure 8 Recommended host schematic for an independent supply option

Power supply connections and recommended external components

The CYBLE-022001-00 schematic is shown in **Figure 9**.

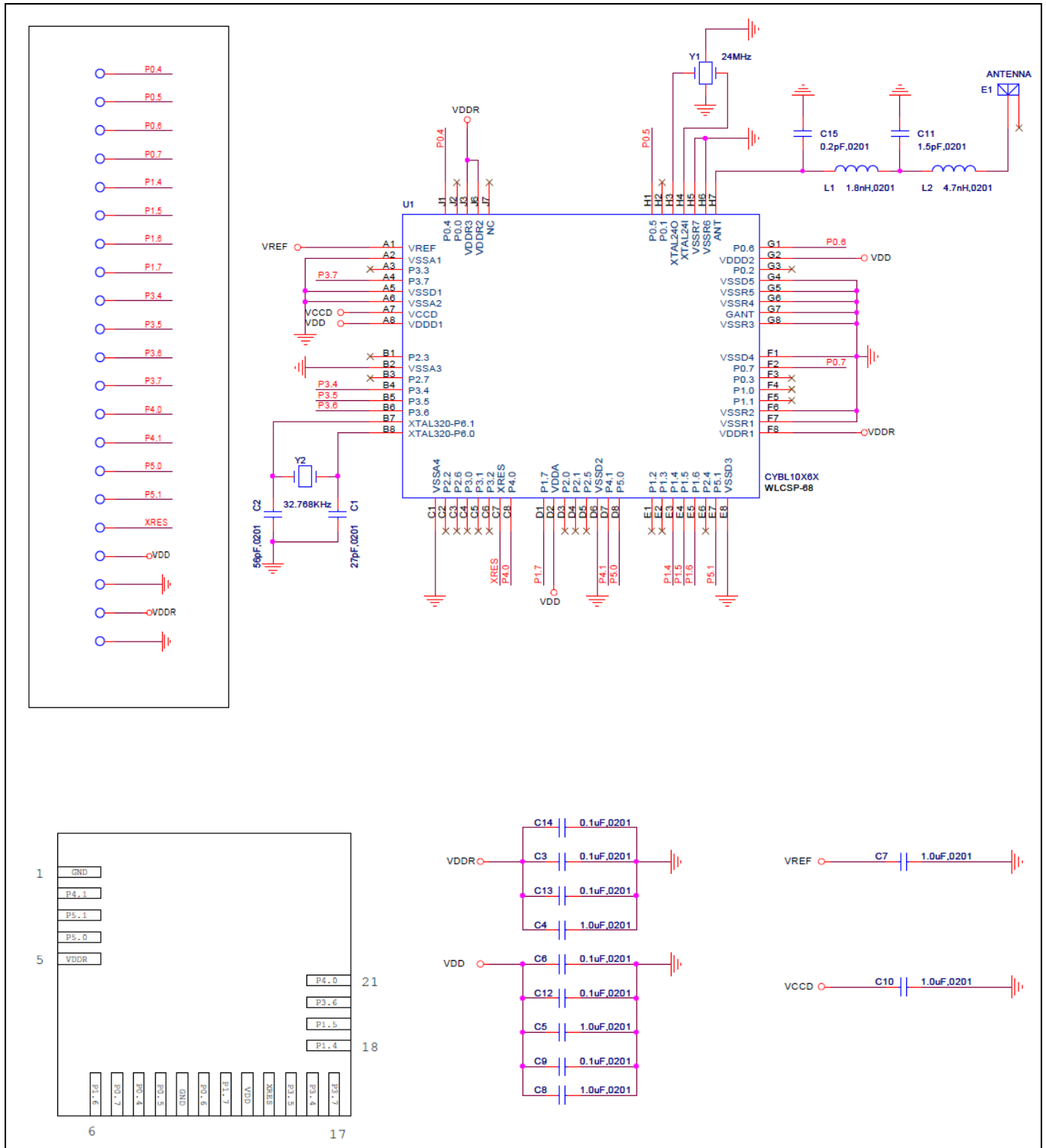


Figure 9 CYBLE-022001-00 schematic diagram

Power supply connections and recommended external components

5.4 Critical components list

Table 5 details the critical components used in the CYBLE-022001-00 module.

Table 5 Critical component list

| Component | Reference designator | Description |
|-----------|----------------------|------------------------------------|
| Silicon | U1 | 68-pin WLCSP PSoC™ 4 Bluetooth® LE |
| Crystal | Y1 | 24.000 MHz, 10PF |
| Crystal | Y2 | 32.768 kHz, 12.5PF |
| Antenna | E1 | 2.4–2.5 GHz chip antenna |

5.5 Antenna design

Table 6 details the chip antenna used in the CYBLE-022001-00 module. The specifications listed are according to the vendor’s datasheet. The Infineon module performance improves many of these characteristics. For more information, see **Table 6**.

Table 6 Chip antenna specifications

| Item | Description |
|---------------------------|--------------------------|
| Chip antenna manufacturer | Johanson Technology Inc. |
| Chip antenna part number | 2450AT18B100 |
| Frequency range | 2400–2500 MHz |
| Peak gain | 0.5-dBi typical |
| Average gain | –0.5-dBi typical |
| Return loss | 9.5-dB minimum |

6 Electrical specification

Table 7 details the absolute maximum electrical characteristics for the Infineon Bluetooth® LE module.

Table 7 CYBLE-022001-00 absolute maximum ratings

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|------------------------|---|------|-----|----------------|------|--|
| V_{DDD_ABS} | Analog, digital, or radio supply relative to V_{SS} ($V_{SSD} = V_{SSA}$) | -0.5 | - | 6 | V | Absolute maximum |
| V_{CCD_ABS} | Direct digital core voltage input relative to V_{SSD} | -0.5 | - | 1.95 | | Absolute maximum |
| V_{DDD_RIPPLE} | Maximum power supply ripple for V_{DD} and V_{DDR} input voltage | - | - | 100 | mV | 3.0-V supply Ripple frequency of 100 kHz to 750 kHz |
| V_{GPIO_ABS} | GPIO voltage | -0.5 | - | $V_{DD} + 0.5$ | v | Absolute maximum |
| I_{GPIO_ABS} | Maximum current per GPIO | -25 | - | 25 | mA | Absolute maximum |
| $I_{GPIO_in-jection}$ | GPIO injection current: Maximum for $V_{IH} > V_{DD}$ and minimum for $V_{IL} < V_{SS}$ | -0.5 | - | 0.5 | | Absolute maximum current injected per pin |
| LU | Pin current for latch up | -200 | | 200 | | - |

Table 8 details the RF characteristics for the Infineon Bluetooth® LE module.

Table 8 CYBLE-022001-00 RF performance characteristics

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------|-------------------------------|------|-------|------|------|------------------------------------|
| RF_O | RF output power on ANT | -18 | 0 | 3 | dBm | Configurable via register settings |
| RX_S | RF receive sensitivity on ANT | - | -87 | - | | Guaranteed by design simulation |
| F_R | Module frequency range | 2400 | - | 2480 | MHz | - |
| G_P | Peak gain | - | 0.5 | - | dBi | - |
| G_{Avg} | Average gain | - | -0.5 | - | | - |
| RL | Return loss | - | -10.5 | - | dB | - |

Electrical specification

Table 9 through **Table 46** list the module-level electrical characteristics for the CYBLE-022001-00. All specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 9 CYBLE-022001-00 DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|--|------|------|------|---------------|--|
| V_{DD1} | Power supply input voltage | 1.8 | – | 5.5 | V | With regulator enabled |
| V_{DD2} | Power supply input voltage unregulated | 1.71 | 1.8 | 1.89 | | Internally unregulated supply |
| V_{DDR1} | Radio supply voltage (radio on) | 1.9 | – | 5.5 | | – |
| V_{DDR2} | Radio supply voltage (radio off) | 1.71 | – | 5.5 | | – |
| Active Mode, $V_{DD} = 1.71\text{ V to }5.5\text{ V}$ | | | | | | |
| I_{DD3} | Execute from flash; CPU at 3 MHz | – | 1.7 | – | mA | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ |
| I_{DD4} | Execute from flash; CPU at 3 MHz | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| I_{DD5} | Execute from flash; CPU at 6 MHz | – | 2.5 | – | | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ |
| I_{DD6} | Execute from flash; CPU at 6 MHz | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| I_{DD7} | Execute from flash; CPU at 12 MHz | – | 4 | – | mA | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ |
| I_{DD8} | Execute from flash; CPU at 12 MHz | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| I_{DD9} | Execute from flash; CPU at 24 MHz | – | 7.1 | – | | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ |
| I_{DD10} | Execute from flash; CPU at 24 MHz | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| I_{DD11} | Execute from flash; CPU at 48 MHz | – | 13.4 | – | | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ |
| I_{DD12} | Execute from flash; CPU at 48 MHz | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| Sleep Mode, $V_{DD} = 1.8\text{ V to }5.5\text{ V}$ | | | | | | |
| I_{DD13} | IMO on | – | – | – | mA | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$, SYSCLK = 3 MHz |
| Sleep Mode, V_{DD} and $V_{DDR} = 1.9\text{ V to }5.5\text{ V}$ | | | | | | |
| I_{DD14} | ECO on | – | – | – | mA | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$, SYSCLK = 3 MHz |
| Deep-Sleep Mode, $V_{DD} = 1.8\text{ V to }3.6\text{ V}$ | | | | | | |
| I_{DD15} | WDT with WCO on | – | 1.5 | – | μA | $T = 25^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ |
| I_{DD16} | WDT with WCO on | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| I_{DD17} | WDT with WCO on | – | – | – | | $T = 25^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$ |
| I_{DD18} | WDT with WCO on | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| Deep-Sleep Mode, $V_{DD} = 1.71\text{ V to }1.89\text{ V}$ (regulator bypassed) | | | | | | |
| I_{DD19} | WDT with WCO on | – | – | – | μA | $T = 25^{\circ}\text{C}$ |
| I_{DD20} | WDT with WCO on | – | – | – | | $T = -40^{\circ}\text{C to }85^{\circ}\text{C}$ |
| Hibernate Mode, $V_{DD} = 1.8\text{ V to }3.6\text{ V}$ | | | | | | |

Electrical specification

Table 9 CYBLE-022001-00 DC specifications (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|--|---------------------------------------|-----|-----|-----|------|---|
| I_{DD27} | GPIO and reset active | - | 150 | - | nA | T = 25°C, V _{DD} = 3.3 V |
| I_{DD28} | GPIO and reset active | - | - | - | | T = -40°C to 85°C |
| Hibernate Mode, V_{DD} = 3.6 V to 5.5 V | | | | | | |
| I_{DD29} | GPIO and reset active | - | - | - | nA | T = 25°C, V _{DD} = 5 V |
| I_{DD30} | GPIO and reset active | - | - | - | | T = -40°C to 85°C |
| Stop Mode, V_{DD} = 1.8 V to 3.6 V | | | | | | |
| I_{DD33} | Stop-mode current (V _{DD}) | - | 20 | - | nA | T = 25°C, V _{DD} = 3.3 V |
| I_{DD34} | Stop-mode current (V _{DDR}) | - | 40 | -- | | T = 25°C, V _{DDR} = 3.3 V |
| I_{DD35} | Stop-mode current (V _{DD}) | - | - | - | | T = -40°C to 85°C |
| I_{DD36} | Stop-mode current (V _{DDR}) | - | - | - | | T = -40°C to 85°C, V _{DDR} = 1.9 V to 3.6 V |
| Stop Mode, V_{DD} = 3.6 V to 5.5 V | | | | | | |
| I_{DD37} | Stop-mode current (V _{DD}) | - | - | - | nA | T = 25°C, V _{DD} = 5 V |
| I_{DD38} | Stop-mode current (V _{DDR}) | - | - | - | | T = 25°C, V _{DDR} = 5 V |
| I_{DD39} | Stop-mode current (V _{DD}) | - | - | - | | T = -40°C to 85°C |
| I_{DD40} | Stop-mode current (V _{DDR}) | - | - | - | | T = -40°C to 85°C |

Table 10 AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------------|-----------------------------|-----|-----|-----|------|--|
| F_{CPU} | CPU frequency | DC | - | 48 | MHz | 1.71 V ≤ V _{DD} ≤ 5.5 V |
| T_{SLEEP} | Wakeup from Sleep mode | - | 0 | - | μs | Guaranteed by characterization |
| $T_{DEEPSLEEP}$ | Wakeup from Deep-Sleep mode | - | - | 25 | | 24-MHz IMO. Guaranteed by characterization |
| $T_{HIBERNATE}$ | Wakeup from Hibernate mode | - | - | 2 | ms | Guaranteed by characterization |
| T_{STOP} | Wakeup from Stop mode | - | - | 2 | | XRES wakeup |

Electrical specification

6.1 GPIO
Table 11 GPIO DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------------|---|----------------------|-----|---------------------|--|--|
| $V_{IH}^{[8]}$ | Input voltage HIGH threshold | $0.7 \times V_{DD}$ | – | – | V | CMOS input |
| | LVTTL input, $V_{DD} < 2.7\text{ V}$ | $0.7 \times V_{DD}$ | – | – | | – |
| | LVTTL input, $V_{DD} \geq 2.7\text{ V}$ | 2.0 | – | – | | – |
| V_{IL} | Input voltage LOW threshold | – | – | $0.3 \times V_{DD}$ | | CMOS input |
| | LVTTL input, $V_{DD} < 2.7\text{ V}$ | – | – | $0.3 \times V_{DD}$ | | – |
| | LVTTL input, $V_{DD} \geq 2.7\text{ V}$ | – | – | 0.8 | | – |
| V_{OH} | Output voltage HIGH level | $V_{DD} - 0.6$ | – | – | | $I_{OH} = 4\text{ mA}$ at $3.3\text{-V } V_{DD}$ |
| | Output voltage HIGH level | $V_{DD} - 0.5$ | – | – | | $I_{OH} = 1\text{ mA}$ at $1.8\text{-V } V_{DD}$ |
| V_{OL} | Output voltage LOW level | – | – | 0.6 | | $I_{OL} = 8\text{ mA}$ at $3.3\text{-V } V_{DD}$ |
| | Output voltage LOW level | – | – | 0.6 | | $I_{OL} = 4\text{ mA}$ at $1.8\text{-V } V_{DD}$ |
| | Output voltage LOW level | – | – | 0.4 | $I_{OL} = 3\text{ mA}$ at $3.3\text{-V } V_{DD}$ | |
| R_{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | k Ω | – |
| $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | | – |
| I_{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DD} = 3.3\text{ V}$ |
| I_{IL_CTBM} | Input leakage on CTBm input pins | – | – | 4 | | – |
| C_{IN} | Input capacitance | – | – | 7 | pF | – |
| V_{HYSTTL} | Input hysteresis LVTTL | 25 | 40 | – | mV | $V_{DD} > 2.7\text{ V}$ |
| $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 \times V_{DD}$ | – | – | 1 | – |
| I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | – | – | 100 | μA | – |
| I_{TOT_GPIO} | Maximum total source or sink chip current | – | – | 200 | mA | – |

Note

 8. V_{IH} must not exceed $V_{DD} + 0.2\text{ V}$.

Electrical specification

Table 12 GPIO AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------------------|---|-----|-----|------|------|---|
| T _{RISEF} | Rise time in Fast-Strong mode | 2 | – | 12 | ns | 3.3-V V _{DD} , C _{LOAD} = 25 pF |
| T _{FALLF} | Fall time in Fast-Strong mode | 2 | – | 12 | | 3.3-V V _{DD} , C _{LOAD} = 25 pF |
| T _{RISES} | Rise time in Slow-Strong mode | 10 | – | 60 | | 3.3-V V _{DD} , C _{LOAD} = 25 pF |
| T _{FALLS} | Fall time in Slow-Strong mode | 10 | – | 60 | | 3.3-V V _{DD} , C _{LOAD} = 25 pF |
| F _{GPIOOUT1} | GPIO F _{OUT} ; 3.3 V ≤ V _{DD} ≤ 5.5 V Fast-Strong mode | – | – | 33 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| F _{GPIOOUT2} | GPIO F _{OUT} ; 1.7 V ≤ V _{DD} ≤ 3.3 V Fast-Strong mode | – | – | 16.7 | | 90/10%, 25-pF load, 60/40 duty cycle |
| F _{GPIOOUT3} | GPIO F _{OUT} ; 3.3 V ≤ V _{DD} ≤ 5.5 V Slow-Strong mode | – | – | 7 | | 90/10%, 25-pF load, 60/40 duty cycle |
| F _{GPIOOUT4} | GPIO F _{OUT} ; 1.7 V ≤ V _{DD} ≤ 3.3 V Slow-Strong mode | – | – | 3.5 | | 90/10%, 25-pF load, 60/40 duty cycle |
| F _{GPIOIN} | GPIO input operating frequency 1.71 V ≤ V _{DD} ≤ 5.5 V | – | – | 48 | | 90/10% V _{IO} |

Table 13 OVT GPIO DC specifications (P5_0 and P5_1 Only)

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------------|--|-----|-----|-----|------|--|
| I _{IL} | Input leakage (absolute value). V _{IH} > V _{DD} | – | – | 10 | μA | 25°C, V _{DD} = 0 V, V _{IH} = 3.0 V |
| V _{OL} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 20 mA, V _{DD} > 2.9 V |

Table 14 OVT GPIO AC specifications (P5_0 and P5_1 Only)

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|------------------------|--|-----|-----|-----|------|---|
| T _{RISE_OVFS} | Output rise time in Fast-Strong mode | 1.5 | – | 12 | ns | 25-pF load, 10%–90%, V _{DD} = 3.3 V |
| T _{FALL_OVFS} | Output fall time in Fast-Strong mode | 1.5 | – | 12 | | 25-pF load, 10%–90%, V _{DD} = 3.3 V |
| T _{RISESS} | Output rise time in Slow-Strong mode | 10 | – | 60 | | 25-pF load, 10%–90%, V _{DD} = 3.3 V |
| T _{FALLSS} | Output fall time in Slow-Strong mode | 10 | – | 60 | | 25-pF load, 10%–90%, V _{DD} = 3.3 V |
| F _{GPIOOUT1} | GPIO F _{OUT} ; 3.3 V ≤ V _{DD} ≤ 5.5 V Fast-Strong mode | – | – | 24 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| F _{GPIOOUT2} | GPIO F _{OUT} ; 1.71 V ≤ V _{DD} ≤ 3.3 V Fast-Strong mode | – | – | 16 | | 90/10%, 25-pF load, 60/40 duty cycle |

Electrical specification

6.2 XRES
Table 15 XRES DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|----------------------|--|------------------------|-----|------------------------|------|--------------------|
| V _{IH} | Input voltage HIGH threshold | 0.7 × V _{DDD} | - | - | V | CMOS input |
| V _{IL} | Input voltage LOW threshold | - | - | 0.3 × V _{DDD} | | |
| R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | - |
| C _{IN} | Input capacitance | - | 3 | - | pF | - |
| V _{HYSXRES} | Input voltage hysteresis | - | 100 | - | mV | - |
| I _{DIODE} | Current through protection diode to V _{DD} /V _{SS} | - | - | 100 | μA | - |

Table 16 XRES AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------------|-------------------|-----|-----|-----|------|--------------------|
| T _{RESETWIDTH} | Reset pulse width | 1 | - | - | μs | - |

6.2.1 Temperature sensor
Table 17 Temperature sensor specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|----------------------|-----------------------------|-----|-----|-----|------|--------------------|
| T _{SENSACC} | Temperature-sensor accuracy | -5 | ±1 | 5 | °C | -40 to +85°C |

6.2.2 SAR ADC
Table 18 SAR ADC DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|------------------------------------|-----------------|-----|------------------|------|--|
| A_RES | Resolution | - | - | 12 | bits | - |
| A_CHNIS_S | Number of channels - single-ended | - | - | 6 | | 6 full-speed ^[9] |
| A-CHNKS_D | Number of channels - differential | - | - | 3 | | Diff inputs use neighboring I/O ^[9] |
| A-MONO | Monotonicity | - | - | - | | Yes |
| A_GAINERR | Gain error | - | - | ±0.1 | % | With external reference |
| A_OFFSET | Input offset voltage | - | - | 2 | mV | Measured with 1-V V _{REF} |
| A_ISAR | Current consumption | - | - | 1 | mA | - |
| A_VINS | Input voltage range - single-ended | V _{SS} | - | V _{DDA} | V | - |
| A_VIND | Input voltage range - differential | V _{SS} | - | V _{DDA} | | - |
| A_INRES | Input resistance | - | - | 2.2 | kΩ | - |
| A_INCAP | Input capacitance | - | - | 10 | pF | - |
| VREFSAR | Trimmed internal reference to SAR | -1 | - | 1 | % | Percentage of V _{bg} (1.024 V) |

Note

9. A maximum of six single-ended ADC Channels can be accomplished only if the AMUX Buses are not being used for other functionality (e.g. CapSense). If the AMUX Buses are being used for other functionality, then the

Electrical specification

Table 19 SAR ADC AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|------------|--|------|-----|-------------|------|--|
| A_PSRR | Power-supply rejection ratio | 70 | – | – | dB | Measured at 1-V reference |
| A_CMRR | Common-mode rejection ratio | 66 | – | – | | – |
| A_SAMP | Sample rate | – | – | 1 | MSPS | 806 KSPS for Part Numbers devices |
| Fsarintref | SAR operating speed without external ref. bypass | – | – | 100 | KSPS | 12-bit resolution |
| A_SNR | Signal-to-noise ratio (SNR) | 65 | – | – | dB | $F_{IN} = 10 \text{ kHz}$ |
| A_BW | Input bandwidth without aliasing | – | – | $A_SAMP/2$ | kHz | – |
| A_INL | Integral nonlinearity. $V_{DD} = 1.71 \text{ V}$ to 5.5 V , 1 MSPS | –1.7 | – | 2 | LSB | $V_{REF} = 1 \text{ V}$ to V_{DD} |
| A_INL | Integral nonlinearity. $V_{DDD} = 1.71 \text{ V}$ to 3.6 V , 1 MSPS | –1.5 | – | 1.7 | | $V_{REF} = 1.71 \text{ V}$ to V_{DD} |
| A_INL | Integral nonlinearity. $V_{DD} = 1.71 \text{ V}$ to 5.5 V , 500 KSPS | –1.5 | – | 1.7 | | $V_{REF} = 1 \text{ V}$ to V_{DD} |
| A_DNL | Differential nonlinearity. $V_{DD} = 1.71 \text{ V}$ to 5.5 V , 1 MSPS | –1 | – | 2.2 | | $V_{REF} = 1 \text{ V}$ to V_{DD} |
| A_DNL | Differential nonlinearity. $V_{DD} = 1.71 \text{ V}$ to 3.6 V , 1 MSPS | –1 | – | 2 | | $V_{REF} = 1.71 \text{ V}$ to V_{DD} |
| A_DNL | Differential nonlinearity. $V_{DD} = 1.71 \text{ V}$ to 5.5 V , 500 KSPS | –1 | – | 2.2 | | $V_{REF} = 1 \text{ V}$ to V_{DD} |
| A_THD | Total harmonic distortion | – | – | –65 | dB | $F_{IN} = 10 \text{ kHz}$ |

Electrical specification

6.2.3 CSD
Table 20 CSD block specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|------------------------|--|------|-----|-----|-------|--|
| V _{CSD} | Voltage range of operation | 1.71 | – | 5.5 | V | – |
| IDAC1 | DNL for 8-bit resolution | –1 | – | 1 | LSB | – |
| IDAC1 | INL for 8-bit resolution | –3 | – | 3 | | – |
| IDAC2 | DNL for 7-bit resolution | –1 | – | 1 | | – |
| IDAC2 | INL for 7-bit resolution | –3 | – | 3 | | – |
| SNR | Ratio of counts of finger to noise | 5 | – | – | Ratio | Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan |
| I _{DAC1_CRT1} | Output current of IDAC1 (8 bits) in High range | – | 612 | – | μA | – |
| I _{DAC1_CRT2} | Output current of IDAC1 (8 bits) in Low range | – | 306 | – | | – |
| I _{DAC2_CRT1} | Output current of IDAC2 (7 bits) in High range | – | 305 | – | | – |
| I _{DAC2_CRT2} | Output current of IDAC2 (7 bits) in Low range | – | 153 | – | | – |

6.3 Digital peripherals
6.3.1 Timer
Table 21 Timer DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|-------------------------------------|-----|-----|-----|------|--------------------|
| I _{TIM1} | Block current consumption at 3 MHz | – | – | 42 | μA | 16-bit timer |
| I _{TIM2} | Block current consumption at 12 MHz | – | – | 130 | | |
| I _{TIM3} | Block current consumption at 48 MHz | – | – | 535 | | |

Table 22 Timer AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------------|--------------------------------|----------------------|-----|-----|------|--------------------|
| T _{TIMFREQ} | Operating frequency | F _{CLK} | – | 48 | MHz | – |
| T _{CAPWINT} | Capture pulse width (internal) | 2 × T _{CLK} | – | – | ns | – |
| T _{CAPWEXT} | Capture pulse width (external) | 2 × T _{CLK} | – | – | | – |
| T _{TIMRES} | Timer resolution | T _{CLK} | – | – | | – |
| T _{TENWIDINT} | Enable pulse width (internal) | 2 × T _{CLK} | – | – | | – |
| T _{TENWIDEXT} | Enable pulse width (external) | 2 × T _{CLK} | – | – | | – |
| T _{TIMRESWINT} | Reset pulse width (internal) | 2 × T _{CLK} | – | – | | – |
| T _{TIMRESEXT} | Reset pulse width (external) | 2 × T _{CLK} | – | – | | – |

Electrical specification

6.3.2 Counter

Table 23 Counter DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|-------------------------------------|-----|-----|-----|------|--------------------|
| I _{CTR1} | Block current consumption at 3 MHz | – | – | 42 | μA | 16-bit counter |
| I _{CTR2} | Block current consumption at 12 MHz | – | – | 130 | | |
| I _{CTR3} | Block current consumption at 48 MHz | – | – | 535 | | |

Table 24 Counter AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------------|--------------------------------|----------------------|-----|-----|------|--------------------|
| T _{CTRFREQ} | Operating frequency | F _{CLK} | – | 48 | MHz | – |
| T _{CTRPWINT} | Capture pulse width (internal) | 2 × T _{CLK} | – | – | ns | – |
| T _{CTRPWEXT} | Capture pulse width (external) | 2 × T _{CLK} | – | – | | – |
| T _{CTRES} | Counter Resolution | T _{CLK} | – | – | | – |
| T _{CENWIDINT} | Enable pulse width (internal) | 2 × T _{CLK} | – | – | | – |
| T _{CENWIDEXT} | Enable pulse width (external) | 2 × T _{CLK} | – | – | | – |
| T _{CTRRESWINT} | Reset pulse width (internal) | 2 × T _{CLK} | – | – | | – |
| T _{CTRRESWEXT} | Reset pulse width (external) | 2 × T _{CLK} | – | – | | – |

Electrical specification

6.3.3 Pulse Width Modulation (PWM)

Table 25 PWM DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|------------|-------------------------------------|-----|-----|-----|------|--------------------|
| I_{PWM1} | Block current consumption at 3 MHz | – | – | 42 | μA | 16-bit PWM |
| I_{PWM2} | Block current consumption at 12 MHz | – | – | 130 | | |
| I_{PWM3} | Block current consumption at 48 MHz | – | – | 535 | | |

Table 26 PWM AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|------------------|-------------------------------|--------------------|-----|-----|------|--------------------|
| $T_{PWMFREQ}$ | Operating frequency | F_{CLK} | – | 48 | MHz | – |
| $T_{PWMPWINT}$ | Pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| T_{PWMEXT} | Pulse width (external) | $2 \times T_{CLK}$ | – | – | | – |
| $T_{PWMKILLINT}$ | Kill pulse width (internal) | $2 \times T_{CLK}$ | – | – | | – |
| $T_{PWMKILLEXT}$ | Kill pulse width (external) | $2 \times T_{CLK}$ | – | – | | – |
| $T_{PWMEINT}$ | Enable pulse width (internal) | $2 \times T_{CLK}$ | – | – | | – |
| $T_{PWMEEXT}$ | Enable pulse width (external) | $2 \times T_{CLK}$ | – | – | | – |
| $T_{PWMRESWINT}$ | Reset pulse width (internal) | $2 \times T_{CLK}$ | – | – | | – |
| $T_{PWMRESWEXT}$ | Reset pulse width (external) | $2 \times T_{CLK}$ | – | – | | – |

6.3.4 LCD direct drive

Table 27 LCD direct drive DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|----------------|---|-----|------|------|------|---------------------------------------|
| I_{LCDLOW} | Operating current in low-power mode | – | 17.5 | – | μA | 16 × 4 small segment display at 50 Hz |
| C_{LCDCAP} | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| LCD_{OFFSET} | Long-term segment offset | – | 20 | – | mV | – |
| I_{LCDOP1} | LCD system operating current $V_{BIAS} = 5\text{ V}$ | – | 2 | – | mA | 32 × 4 segments. 50 Hz at 25°C |
| I_{LCDOP2} | LCD system operating current $V_{BIAS} = 3.3\text{ V}$ | – | 2 | – | | 32 × 4 segments 50 Hz at 25°C |

Table 28 LCD Direct Drive AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------|----------------|-----|-----|-----|------|--------------------|
| F_{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | – |

Electrical specification

6.4 Serial communication
Table 29 Fixed I²C DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|---|-----|-----|-----|------|--------------------|
| I _{I2C1} | Block current consumption at 100 kHz | - | - | 50 | μA | - |
| I _{I2C2} | Block current consumption at 400 kHz | - | - | 155 | | - |
| I _{I2C3} | Block current consumption at 1 Mbps | - | - | 390 | | - |
| I _{I2C4} | I ² C enabled in Deep-Sleep mode | - | - | 1.4 | | - |

Table 30 Fixed I²C AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|-------------|-----|-----|-----|------|--------------------|
| F _{I2C1} | Bit rate | - | - | 400 | kHz | - |

Table 31 Fixed UART DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|--------------------|--|-----|-----|-----|------|--------------------|
| I _{UART1} | Block current consumption at 100 kbps | - | - | 55 | μA | - |
| I _{UART2} | Block current consumption at 1000 kbps | - | - | 312 | | - |

Table 32 Fixed UART AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|-------------|-----|-----|-----|------|--------------------|
| F _{UART} | Bit rate | - | - | 1 | Mbps | - |

Table 33 Fixed SPI DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|-------------------------------------|-----|-----|-----|------|--------------------|
| I _{SPI1} | Block current consumption at 1 Mbps | - | - | 360 | μA | - |
| I _{SPI2} | Block current consumption at 4 Mbps | - | - | 560 | | - |
| I _{SPI3} | Block current consumption at 8 Mbps | - | - | 600 | | - |

6.5 Memory
Table 34 Flash DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|------------------------------------|------|-----|-----|------|--------------------------|
| V _{PE} | Erase and program voltage | 1.71 | - | 5.5 | V | - |
| T _{WS48} | Number of Wait states at 32–48 MHz | 2 | - | - | | CPU execution from flash |
| T _{WS32} | Number of Wait states at 16–32 MHz | 1 | - | - | | CPU execution from flash |
| T _{WS16} | Number of Wait states for 0–16 MHz | 0 | - | - | | CPU execution from flash |

Electrical specification

Table 35 Flash AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------------|---|-------|-----|-----|---------|-------------------------|
| $T_{ROWWRITE}^{[10]}$ | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| $T_{ROWERASE}^{[10]}$ | Row erase time | – | – | 13 | | – |
| $T_{ROWPROGRAM}^{[10]}$ | Row program time after erase | – | – | 7 | | – |
| $T_{BULKERASE}^{[10]}$ | Bulk erase time (128 KB) | – | – | 35 | | – |
| $T_{DEVPROG}^{[10]}$ | Total device program time | – | – | 25 | seconds | – |
| F_{END} | Flash endurance | 100 K | – | – | cycles | – |
| F_{RET} | Flash retention. $T_A \leq 55^\circ\text{C}$, 100 K P/E cycles | 20 | – | – | years | – |
| F_{RET2} | Flash retention. $T_A \leq 85^\circ\text{C}$, 10 K P/E cycles | 10 | – | – | | – |

6.6 System resources

6.6.1 Power-On-Reset (POR)

Table 36 POR DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|----------------|----------------------|------|-----|------|------|--------------------|
| $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.45 | V | – |
| $V_{FALLIPOR}$ | Falling trip voltage | 0.75 | – | 1.40 | | – |
| $V_{IPORHYST}$ | Hysteresis | 15 | – | 200 | mV | – |

Table 37 POR AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------|---|-----|-----|-----|---------------|--------------------|
| $TPPOR_TR$ | Precision power-on reset (PPOR) response time in Active and Sleep modes | – | – | 1 | μs | – |

Table 38 Brown-out detect

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------------|--|------|-----|-----|------|--------------------|
| $V_{FALLPPOR}$ | BOD trip voltage in Active and Sleep modes | 1.64 | – | – | V | – |
| $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.4 | – | – | | – |

Table 39 Hibernate reset

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---------------|-------------------------------|-----|-----|-----|------|--------------------|
| $V_{HBRTRIP}$ | BOD trip voltage in Hibernate | 1.1 | – | – | V | – |

Note

10. It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watch-dogs. Make certain that these are not inadvertently activated.

Electrical specification

6.6.2 Voltage monitors (LVD)
Table 40 Voltage monitor DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|--------------------|--------------------------|------|------|------|------|--------------------|
| V _{LVI1} | LVI_A/D_SEL[3:0] = 0000b | 1.71 | 1.75 | 1.79 | V | – |
| V _{LVI2} | LVI_A/D_SEL[3:0] = 0001b | 1.76 | 1.80 | 1.85 | | – |
| V _{LVI3} | LVI_A/D_SEL[3:0] = 0010b | 1.85 | 1.90 | 1.95 | | – |
| V _{LVI4} | LVI_A/D_SEL[3:0] = 0011b | 1.95 | 2.00 | 2.05 | | – |
| V _{LVI5} | LVI_A/D_SEL[3:0] = 0100b | 2.05 | 2.10 | 2.15 | | – |
| V _{LVI6} | LVI_A/D_SEL[3:0] = 0101b | 2.15 | 2.20 | 2.26 | | – |
| V _{LVI7} | LVI_A/D_SEL[3:0] = 0110b | 2.24 | 2.30 | 2.36 | | – |
| V _{LVI8} | LVI_A/D_SEL[3:0] = 0111b | 2.34 | 2.40 | 2.46 | | – |
| V _{LVI9} | LVI_A/D_SEL[3:0] = 1000b | 2.44 | 2.50 | 2.56 | | – |
| V _{LVI10} | LVI_A/D_SEL[3:0] = 1001b | 2.54 | 2.60 | 2.67 | | – |
| V _{LVI11} | LVI_A/D_SEL[3:0] = 1010b | 2.63 | 2.70 | 2.77 | | – |
| V _{LVI12} | LVI_A/D_SEL[3:0] = 1011b | 2.73 | 2.80 | 2.87 | | – |
| V _{LVI13} | LVI_A/D_SEL[3:0] = 1100b | 2.83 | 2.90 | 2.97 | | – |
| V _{LVI14} | LVI_A/D_SEL[3:0] = 1101b | 2.93 | 3.00 | 3.08 | | – |
| V _{LVI15} | LVI_A/D_SEL[3:0] = 1110b | 3.12 | 3.20 | 3.28 | | – |
| V _{LVI16} | LVI_A/D_SEL[3:0] = 1111b | 4.39 | 4.50 | 4.61 | | – |
| LVI_IDD | Block current | – | – | 100 | μA | – |

Table 41 Voltage monitor AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|----------------------|---------------------------|-----|-----|-----|------|--------------------|
| T _{MONTRIP} | Voltage monitor trip time | – | – | 1 | μs | – |

6.6.3 SWD interface
Table 42 SWD interface specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------------|---|----------|-----|---------|------|----------------------------------|
| F _{SWDCLK1} | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| F _{SWDCLK2} | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | – | – | 7 | | |
| T _{SWDI_SETUP} | T = 1/f SWDCLK | 0.25 × T | – | – | ns | – |
| T _{SWDI_HOLD} | T = 1/f SWDCLK | 0.25 × T | – | – | | – |
| T _{SWDO_VALID} | T = 1/f SWDCLK | – | – | 0.5 × T | | – |
| T _{SWDO_HOLD} | T = 1/f SWDCLK | 1 | – | – | | – |

Electrical specification

6.6.4 Internal main oscillator
Table 43 IMO DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|---------------------------------|-----|-----|------|------|--------------------|
| I _{IMO1} | IMO operating current at 48 MHz | – | – | 1000 | μA | – |
| I _{IMO2} | IMO operating current at 24 MHz | – | – | 325 | | – |
| I _{IMO3} | IMO operating current at 12 MHz | – | – | 225 | | – |
| I _{IMO4} | IMO operating current at 6 MHz | – | – | 180 | | – |
| I _{IMO5} | IMO operating current at 3 MHz | – | – | 150 | | – |

Table 44 IMO AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|----------------------|--------------------------------------|-----|-----|-----|------|-----------------------------|
| F _{IMOTOL3} | Frequency variation from 3 to 48 MHz | – | – | ±2 | % | With API-called calibration |
| F _{IMOTOL3} | IMO startup time | – | 12 | – | μs | – |

6.6.5 Internal low-speed oscillator
Table 45 ILO DC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------|---------------------------------|-----|-----|------|------|--------------------|
| I _{ILO2} | ILO operating current at 32 kHz | – | 0.3 | 1.05 | μA | – |

Table 46 ILO AC specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|------------------------|--------------------------|-----|-----|-----|------|--------------------|
| T _{STARTILO1} | ILO startup time | – | – | 2 | ms | – |
| F _{ILOTRIM1} | 32-kHz trimmed frequency | 15 | 32 | 50 | kHz | – |

Table 47 Recommended ECO trim value

| Parameter | Description | Value | Details/conditions |
|---------------------|--|------------|---|
| ECO _{TRIM} | 24-MHz trim value (firmware configuration) | 0x00009898 | Recommended trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAP-TRIM_REG |

6.6.6 Bluetooth® LE subsystem
Table 48 Bluetooth® LE subsystem

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|----------------------------------|---|-----|-----|-----|------|---------------------------------------|
| RF Receiver specification | | | | | | |
| RXS, IDLE | RX sensitivity with idle transmitter | – | –89 | – | dBm | – |
| | RX sensitivity with idle transmitter excluding Balun loss | – | –91 | – | | Guaranteed by design simulation |
| RXS, DIRTY | RX sensitivity with dirty transmitter | – | –87 | –70 | | RF-PHY Specification (RCV-LE/CA/01/C) |
| RXS, HIGHGAIN | RX sensitivity in high-gain mode with idle transmitter | – | –91 | – | | – |
| PRXMAX | Maximum input power | –10 | –1 | – | | RF-PHY Specification (RCV-LE/CA/06/C) |

Electrical specification

Table 48 Bluetooth® LE subsystem (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|--------------------------------------|--|-----|-----|-----|------|--|
| CI1 | Cochannel interference, Wanted signal at -67 dBm and Interferer at FRX | - | 9 | 21 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI2 | Adjacent channel interference Wanted signal at -67 dBm and Interferer at FRX ±1 MHz | - | 3 | 15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI3 | Adjacent channel interference Wanted signal at -67 dBm and Interferer at FRX ±2 MHz | - | -29 | - | | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI4 | Adjacent channel interference Wanted signal at -67 dBm and Interferer at ≥FRX ±3 MHz | - | -39 | - | | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI5 | Adjacent channel interference Wanted Signal at -67 dBm and Interferer at Image frequency (F _{IMAGE}) | - | -20 | - | | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI3 | Adjacent channel interference Wanted signal at -67 dBm and Interferer at Image frequency (F _{IMAGE} ± 1 MHz) | - | -30 | - | | RF-PHY Specification (RCV-LE/CA/03/C) |
| OBB1 | Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 30–2000 MHz | -30 | -27 | - | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| OBB2 | Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 2003–2399 MHz | -35 | -27 | - | | RF-PHY Specification (RCV-LE/CA/04/C) |
| OBB3 | Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 2484–2997 MHz | -35 | -27 | - | | RF-PHY Specification (RCV-LE/CA/04/C) |
| OBB4 | Out-of-band blocking, Wanted signal a -67 dBm and Interferer at F = 3000–12750 MHz | -30 | -27 | - | | RF-PHY Specification (RCV-LE/CA/04/C) |
| IMD | Intermodulation performance Wanted signal at -64 dBm and 1-Mbps Bluetooth® LE, third, fourth, and fifth offset channel | -50 | - | - | | RF-PHY Specification (RCV-LE/CA/05/C) |
| RXSE1 | Receiver spurious emission 30 MHz to 1.0 GHz | - | - | -57 | | 100-kHz measurement bandwidth ETSI EN300 328 V1.8.1 |
| RXSE2 | Receiver spurious emission 1.0 GHz to 12.75 GHz | - | - | -47 | | 1-MHz measurement bandwidth ETSI EN300 328 V1.8.1 |
| RF transmitter specifications | | | | | | |
| TXP, ACC | RF power accuracy | - | ±1 | - | dB | - |
| TXP, RANGE | RF power control range | - | 20 | - | | - |

Electrical specification

Table 48 Bluetooth® LE subsystem (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------|--|------|-----|-------|--------------------|---------------------------------------|
| TXP, 0dBm | Output power, 0-dB Gain setting (PA7) | - | 0 | - | dBm | - |
| TXP, MAX | Output power, maximum power setting (PA10) | - | 3 | - | | - |
| TXP, MIN | Output power, minimum power setting (PA1) | - | -18 | - | | - |
| F2AVG | Average frequency deviation for 10101010 pattern | 185 | - | - | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| F1AVG | Average frequency deviation for 11110000 pattern | 225 | 250 | 275 | | RF-PHY Specification (TRM-LE/CA/05/C) |
| EO | Eye opening = $\Delta F2AVG/\Delta F1AVG$ | 0.8 | - | - | | RF-PHY Specification (TRM-LE/CA/05/C) |
| FTX, ACC | Frequency accuracy | -150 | - | 150 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, MAXDR | Maximum frequency drift | -50 | - | 50 | | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, INITDR | Initial frequency drift | -20 | - | 20 | | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, DR | Maximum drift rate | -20 | - | 20 | kHz/ 50 μ s | RF-PHY Specification (TRM-LE/CA/06/C) |
| IBSE1 | In-band spurious emission at 2-MHz offset | - | - | -20 | dBm | RF-PHY Specification (TRM-LE/CA/03/C) |
| IBSE2 | In-band spurious emission at ≥ 3 -MHz offset | - | - | -30 | | RF-PHY Specification (TRM-LE/CA/03/C) |
| TXSE1 | Transmitter spurious emissions (average), <1.0 GHz | - | - | -55.5 | | FCC-15.247 |
| TXSE2 | Transmitter spurious emissions (average), >1.0 GHz | - | - | -41.5 | | FCC-15.247 |

RF current specifications

| | | | | | | |
|---------------|--|---|------|---|----|---------------------------------|
| IRX | Receive current in normal mode | - | 18.7 | - | mA | - |
| IRX_RF | Radio receive current in normal mode | - | 16.4 | - | | Measured at V_{DDR} |
| IRX, HIGHGAIN | Receive current in high-gain mode | - | 21.5 | - | | - |
| ITX, 3dBm | TX current at 3-dBm setting (PA10) | - | 20 | - | | - |
| ITX, 0dBm | TX current at 0-dBm setting (PA7) | - | 16.5 | - | | - |
| ITX_RF, 0dBm | Radio TX current at 0 dBm setting (PA7) | - | 15.6 | - | | Measured at V_{DDR} |
| ITX_RF, 0dBm | Radio TX current at 0 dBm excluding Balun loss | - | 14.2 | - | | Guaranteed by design simulation |
| ITX,-3dBm | TX current at -3-dBm setting (PA4) | - | 15.5 | - | | - |
| ITX,-6dBm | TX current at -6-dBm setting (PA3) | - | 14.5 | - | | - |
| ITX,-12dBm | TX current at -12-dBm setting (PA2) | - | 13.2 | - | | - |
| ITX,-18dBm | TX current at -18-dBm setting (PA1) | - | 12.5 | - | | - |

Electrical specification

Table 48 Bluetooth® LE subsystem (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-----------------|---|-----|------|-----|------|--|
| lavg_1sec, 0dBm | Average current at 1-second Bluetooth® LE connection interval | - | 17.1 | - | μA | TXP: 0 dBm; ±20-ppm master and slave clock accuracy. For empty PDU exchange |
| lavg_4sec, 0dBm | Average current at 4-second Bluetooth® LE connection interval | - | 6.1 | - | | TXP: 0 dBm; ±20-ppm master and slave clock accuracy. For empty PDU exchange |

General RF specifications

| | | | | | | |
|---------|---|------|------|------|-------|---|
| FREQ | RF operating frequency | 2400 | - | 2482 | MHz | - |
| CHBW | Channel spacing | - | 2 | - | | - |
| DR | On-air data rate | - | 1000 | - | kbits | - |
| IDLE2TX | Bluetooth® LE.IDLE to Bluetooth® LE. TX transition time | - | 120 | 140 | μs | - |
| IDLE2RX | Bluetooth® LE.IDLE to Bluetooth® LE. RX transition time | - | 75 | 120 | | - |

RSSI specifications

| | | | | | | |
|-----------|--------------------|---|----|---|----|---|
| RSSI, ACC | RSSI accuracy | - | ±5 | - | dB | - |
| RSSI, RES | RSSI resolution | - | 1 | - | | - |
| RSSI, PER | RSSI sample period | - | 6 | - | μs | - |

7 Environmental specifications

7.1 Environmental compliance

This Infineon Bluetooth® LE module is built in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen Free (HF) directives. The Infineon module and components used to produce this module are RoHS and HF compliant.

7.2 RF certification

The CYBLE-022001-00 module is certified under the following RF certification standards:

- FCC: WAP2001
- CE
- IC: 7922A-2001
- MIC: 005-101007
- KC: MSIP-CRM-Cyp-2001

7.3 Safety certification

The CYBLE-022001-00 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

7.4 Environmental conditions

Table 49 describes the operating and storage conditions for the Infineon Bluetooth® LE module.

Table 49 Environmental conditions for CYBLE-022001-00

| Description | Minimum specification | Maximum specification |
|--|-----------------------|-----------------------------|
| Operating temperature | -40°C | 85°C |
| Operating humidity (relative, non-condensation) | 5% | 85% |
| Thermal ramp rate | - | 3°C/minute |
| Storage temperature | -40°C | 85°C |
| Storage temperature and humidity | - | 85°C at 85% |
| ESD: Module integrated into system Components ^[11] | - | 15 kV Air 2.2 kV Contact |

7.5 ESD and EMI protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note

11. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

8 Regulatory information

8.1 FCC

FCC NOTICE:

The device CYBLE-022001-00, including the antenna 2450AT18B100 from Johanson Technology, complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Infineon Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP2001.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP2001"

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antennas listed below. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in [Table 6](#), to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-022001-00 with the chip antenna mounted (FCC ID: WAP2001) is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-022001-00 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

Regulatory information

8.2 ISED

Innovation, Science and Economic Development Canada (ISED) certification

CYBLE-022001-00 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development Canada (ISED).

License: IC: 7922A-2001

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in [Table 6](#), having a maximum gain of 0.5 dBi. Antennas not included in this list or having a gain greater than 0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYBLE-022001-00 including the antenna 2450AT18B100 from Johanson technology, complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon Semiconductor IC identifier for this product as well as the ISED Notice above. The IC identifier is 7922A-2001. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-2001"

Regulatory information

8.3 European R&TTE declaration of conformity

Hereby, Infineon Semiconductor declares that the Bluetooth® module CYBLE-022001-00 complies with the essential requirements and other relevant provisions of Directive 2014/53/EU. As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labeled as follows:

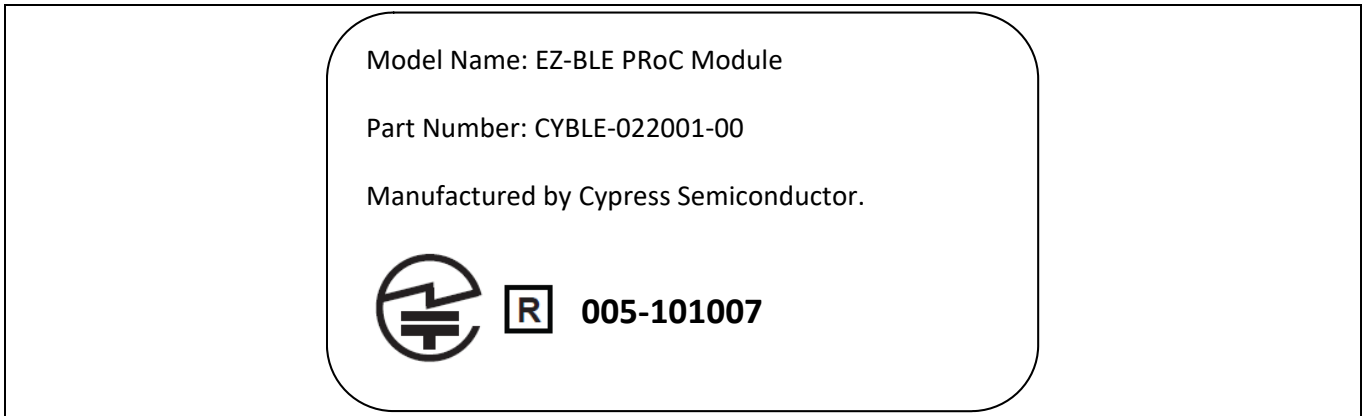


All versions of the CYBLE-022001-00 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

8.4 MIC Japan

CYBLE-022001-00 is certified as a module with type certification number 005-101007. End products that integrate CYBLE-022001-00 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.



8.5 KC Korea

CYBLE-022001-00 is certified for use in Korea with certificate number MSIP-CRM-Cyp-2001.

한국 인증 세부정보:



1. 제품명(모델명): 특정소출력무선기기(무선데이터통신시스템용 무선기기), CYBLE-022001-00
2. 인증번호: MSIP-CRM-Cyp-2001
3. 라이선스 소유자: Cypress Semiconductor Corporation
4. 제조일자: 2015.04
5. 제조업체/국가명: Cypress Semiconductor Corporation/ 중국

해당 무선설비는 전파혼신 가능성이 있으므로 인명안전과 관련된 서비스는 할 수 없습니다.

Packaging

9 Packaging

Table 50 Solder reflow peak temperature

| Module part number | Package | Maximum peak temperature | Maximum time at peak temperature | No. of cycles |
|--------------------|------------|--------------------------|----------------------------------|---------------|
| CYBLE-022001-00 | 21-pad SMT | 260°C | 30 seconds | 2 |

Table 51 Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Module part number | Package | MSL |
|--------------------|------------|-------|
| CYBLE-022001-00 | 21-pad SMT | MSL 3 |

The CYBLE-022001-00 is offered in tape and reel packaging. **Figure 10** details the tape dimensions used for the CYBLE-022001-00.

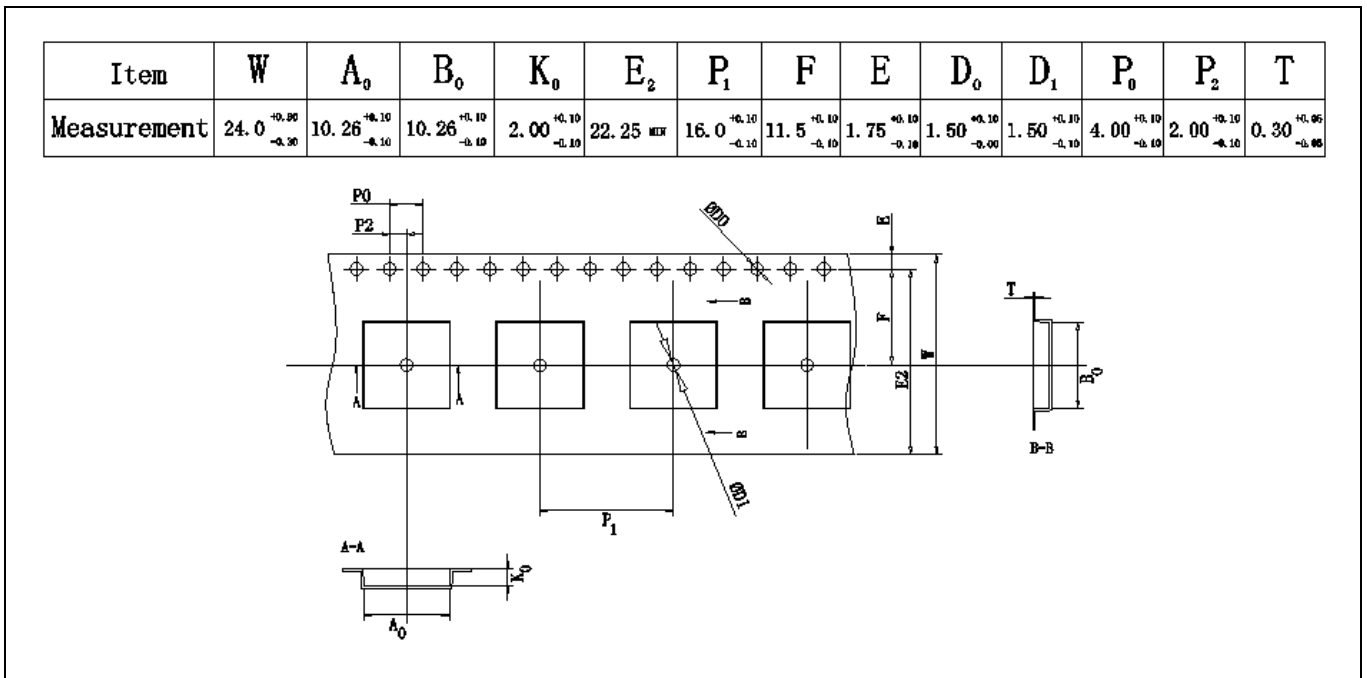


Figure 10 CYBLE-022001-00 tape dimensions

Figure 11 details the orientation of the CYBLE-022001-00 in the tape as well as the direction for unreeling.

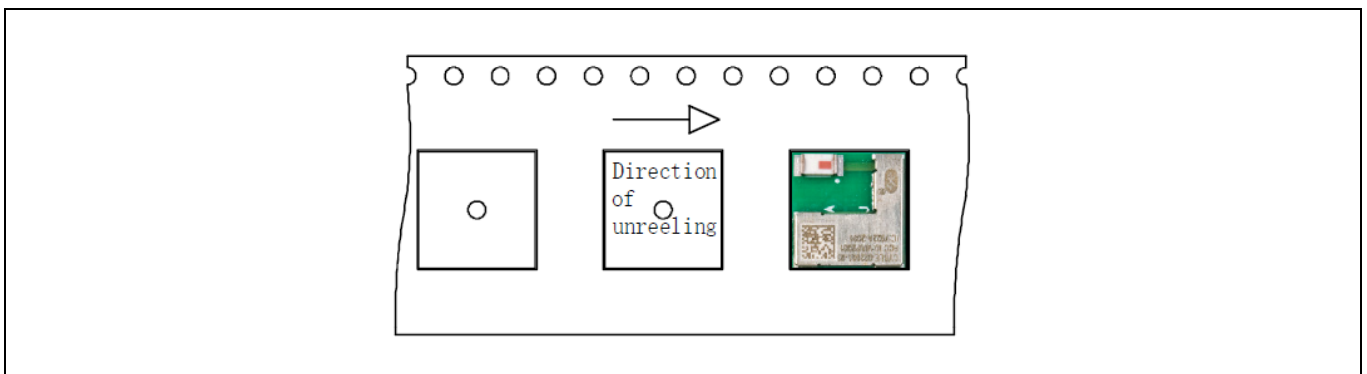


Figure 11 Component orientation in tape and unreeling direction

Packaging

Figure 12 details reel dimensions used for the CYBLE-022001-00.

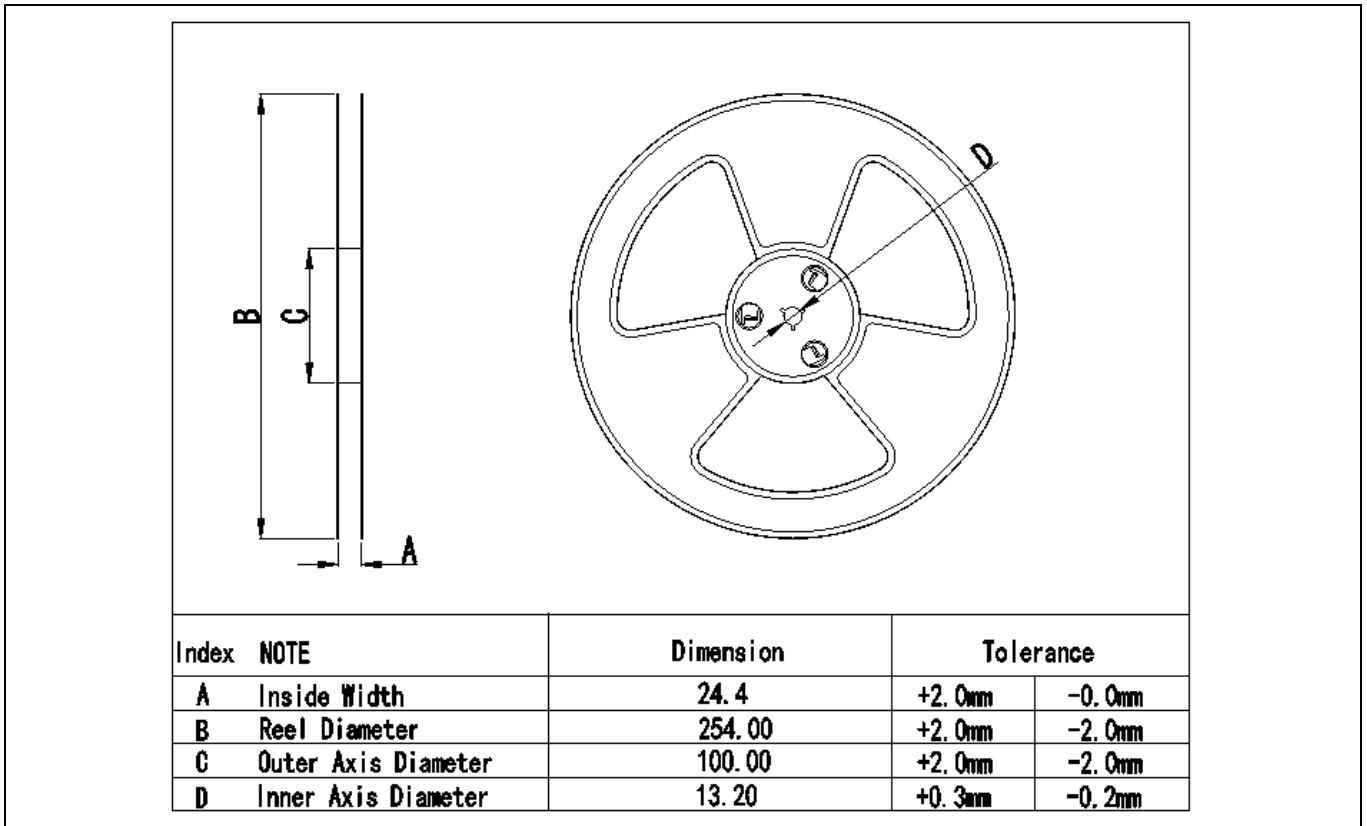


Figure 12 Reel dimensions

The CYBLE-022001-00 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-022001-00 is detailed in [Figure 13](#).

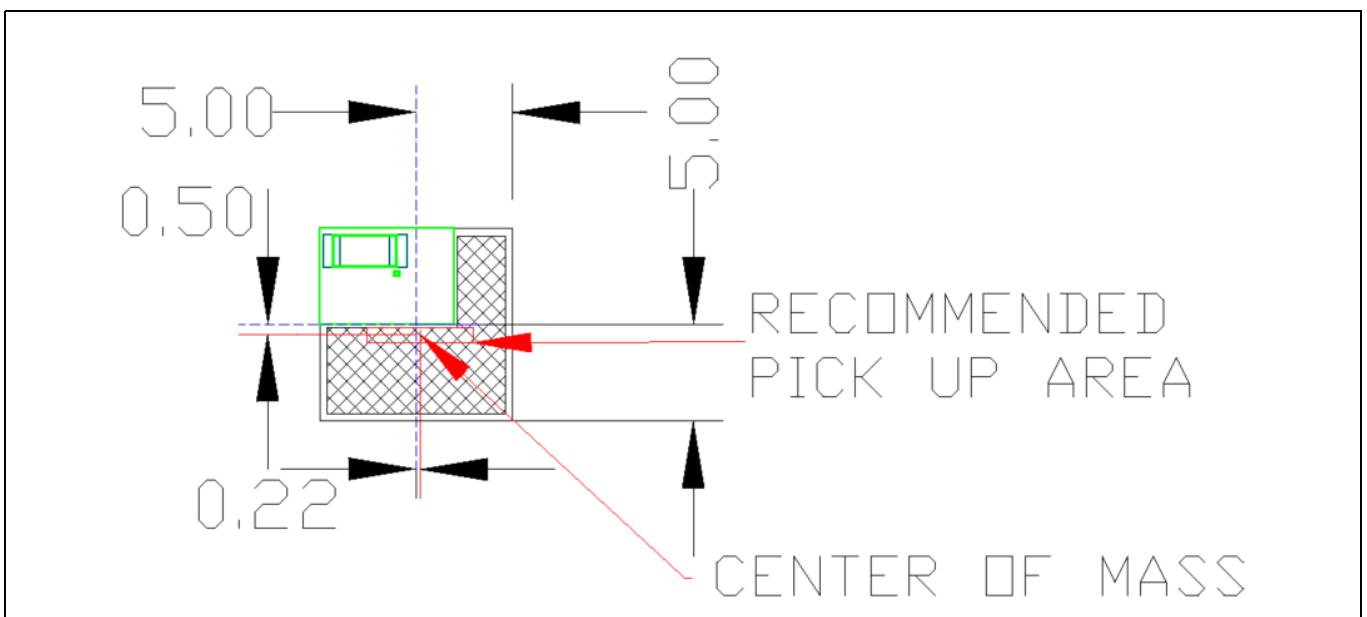


Figure 13 CYBLE-022001-00 center of mass

Ordering information

10 Ordering information

Table 52 lists the CYBLE-022001-00 part number and features. **Table 53** lists the reel shipment quantities for the CYBLE-022001-00.

Table 52 Ordering information

| Part number | CPU Speed (MHz) | Flash Size (KB) | CapSense™ | SCB | TCPWM | 12-bit SAR ADC | I ² S | LCD | Package | Packing |
|-----------------|-----------------|-----------------|-----------|-----|-------|----------------|------------------|-----|---------|---------------|
| CYBLE-022001-00 | 48 | 128 | Yes | 2 | 4 | 1 Msps | Yes | Yes | 21-SMT | Tape and Reel |

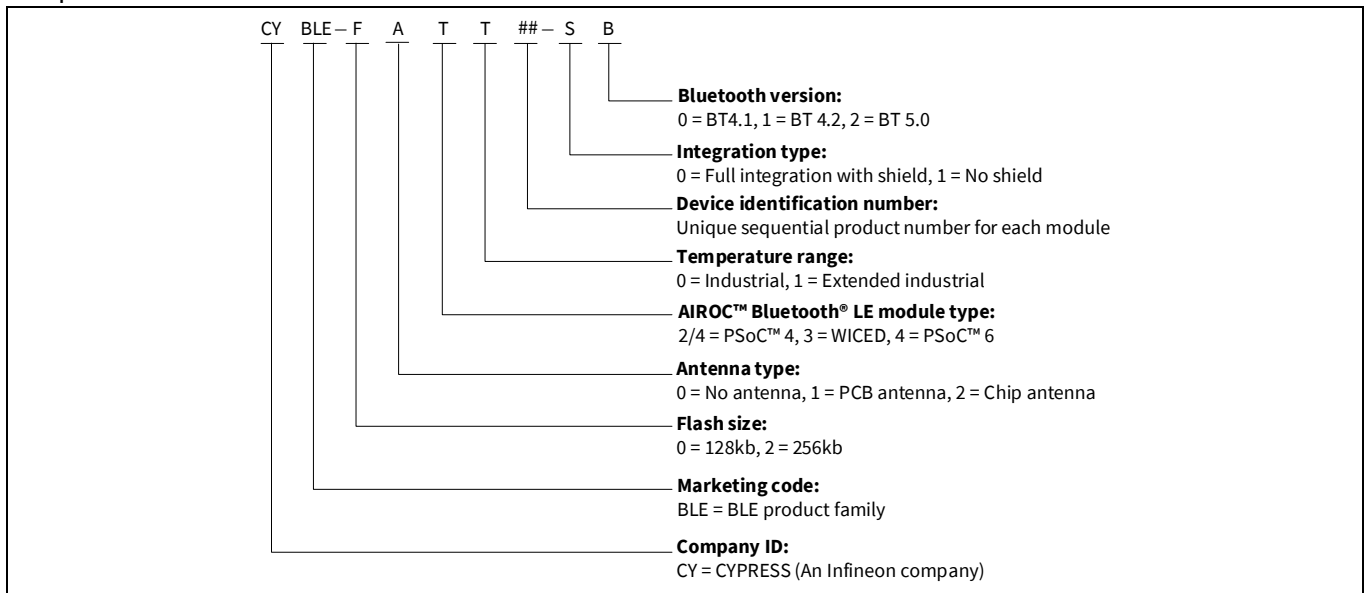
Table 53 Tape and reel package quantity and minimum order amount

| Description | Minimum reel quantity | Maximum reel quantity | Comments |
|------------------------------|-----------------------|-----------------------|------------------------------------|
| Reel Quantity | 500 | 500 | Ships in 500 unit reel quantities. |
| Minimum Order Quantity (MOQ) | 500 | – | – |
| Order Increment (OI) | 500 | – | – |

The CYBLE-022001-00 is offered in tape and reel packaging. The CYBLE-022001-00 ships with a maximum of 500 units/reel.

10.1 Part numbering convention

The part numbers are of the form CYBLE-FATT##-SB where the fields are defined as follows.



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| | |
|--|---|
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| U.S. Infineon Headquarter Contact Info | (408) 943-2600 |
| Infineon website address | http://www.infineon.com |

11 Acronyms

Table 54 Acronyms used in this document

| Acronym | Description |
|----------------|--|
| BLE | Bluetooth® Low-energy |
| Bluetooth® SIG | Bluetooth® Special Interest Group |
| CE | European Conformity |
| CSA | Canadian Standards Association |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FCC | Federal Communications Commission |
| GPIO | general-purpose input/output |
| IC | Industry Canada |
| IDE | integrated design environment |
| KC | Korea Certification |
| MIC | Ministry of Internal Affairs and Communications (Japan) |
| PCB | Printed circuit board |
| RX | receive |
| QDID | qualification design ID |
| SMT | surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs |
| TCPWM | timer, counter, pulse-width modulation |
| TUV | Germany: Technischer Überwachungs-Verein (Technical Inspection Association) |
| TX | transmit |

12 Document conventions

12.1 Units of measure

Table 55 Unit of measures

| Symbol | Unit of measure |
|--------|-----------------|
| °C | degree Celsius |
| kV | kilovolt |
| mA | milliamperes |
| mm | millimeters |
| mV | millivolt |
| µA | microamperes |
| µm | micrometers |
| MHz | megahertz |
| GHz | gigahertz |
| V | volt |
| dB | decibel |
| ms | millisecond |
| µs | microsecond |
| ns | nanosecond |
| pF | picofarad |
| kΩ | kiloohm |

Revision history

Revision history

| Document revision | Date | Description of changes |
|-------------------|------------|---|
| ** | 2015-02-18 | Preliminary data sheet for CYBLE-022001-00 module. |
| *A | 2015-03-09 | <p>Updated Overview:</p> <p>Updated Module description:</p> <p>Updated Module dimensions and drawing:</p> <p>Updated Figure (Updated Module Pad Assignment).</p> <p>Updated Recommended host PCB layout:</p> <p>Updated Table 3:</p> <p>Updated table caption to read as “Module Solder Pad Connection Dimensions”.</p> <p>Updated Table 4:</p> <p>Changed Pad 10 from NC to GND.</p> <p>Updated Power supply connections and recommended external components:</p> <p>Updated External component recommendation:</p> <p>Updated Figure (Changed Pad 10 from NC to GND).</p> <p>Updated Figure 8 (Changed Pad 10 from NC to GND).</p> <p>Updated Figure 9 (Changed Pad 10 from NC to GND).</p> |
| *B | 2015-04-01 | <p>Updated Document Title to read as “CYBLE-022001-00, EZ-BLE™ Creator Module”.</p> <p>Replaced terms “pre-certified” with “certified” and “pre-qualified” with “qualified” respectively in all instances across the document.</p> <p>Updated General description:</p> <p>Updated Module description:</p> <p>Updated description.</p> <p>Added hyperlinks in required places.</p> <p>Updated Power consumption:</p> <p>Updated description.</p> <p>Updated Functional capabilities:</p> <p>Updated description.</p> <p>Updated Electrical specification:</p> <p>Updated Table 10:</p> <p>Updated details in “Details/Conditions” column of T_{STOP} parameter to “XRES wakeup”.</p> <p>Updated Acronyms:</p> <p>Added “QDID”.</p> |
| *C | 2015-06-23 | <p>Changed status from Preliminary to Final.</p> <p>Updated General description:</p> <p>Updated Module description:</p> <p>Updated description.</p> <p>Updated Functional capabilities:</p> <p>Change number of capacitive sensors supported from 13 to 15.</p> <p>Updated Power supply connections and recommended external components:</p> <p>Updated Power connections:</p> <p>Updated description.</p> <p>Updated Figure 9 (To final design schematic).</p> <p>Updated Electrical specification:</p> <p>Update Table 9:</p> <p>Changed typical value of I_{DD15} from 1.3 μA to 1.5 μA.</p> <p>Updated Ordering information:</p> <p>No change in part numbers.</p> <p>Added Part numbering convention.</p> <p>Added Packaging.</p> <p>Updated Acronyms:</p> <p>Added “SMT”.</p> |

Revision history

| Document revision | Date | Description of changes |
|-------------------|------------|--|
| *D | 2015-12-14 | <p>Updated General description: Updated description. Added hyperlinks in required places. Added More information. Updated Overview: Updated Module description: Updated Module dimensions and drawing: Updated Figure (to improve clarity and viewing). Updated Pad connection interface: Updated description. Updated Figure (to improve clarity and viewing). Updated Figure 4 (to improve clarity and viewing). Updated Recommended host PCB layout: Updated Figure (to improve clarity and viewing). Added Figure (to show solder pad location from module origin). Updated Table 3(to provide the location to the center of each solder pad from the origin (in mm and mils)). Added Figure (to provide the location to the center of each solder pad from the origin (in mm and mils)). Updated Electrical specification: Updated XRES: Added Temperature sensor. Added SAR ADC. Added CSD. Updated Digital peripherals: Added Timer. Added Counter. Added Pulse Width Modulation (PWM). Added LCD direct drive. Updated System resources: Added Bluetooth® LE subsystem. Updated ISED: Updated description (Added French translation for IC Radiation Exposure Statement for Canada in accordance with IC requirements). Updated Packaging: Added Table 50. Added Table 51. Completing Sunset Review.</p> |

Revision history

| Document revision | Date | Description of changes |
|-------------------|------------|---|
| *E | 2016-02-22 | <p>Updated General description: Updated Module description: Re-ordered descriptions. No change to content. Updated Overview: Updated Module description: Updated Module dimensions and drawing: Updated Figure 1 (changed orientation to match PSoC™ Creator). Updated Pad connection interface: Updated Figure 2 (changed orientation to match PSoC™ Creator). Updated Figure 3 (changed orientation to match PSoC™ Creator). Updated Recommended host PCB layout: Updated Figure 4 (changed orientation to match PSoC™ Creator). Updated Figure 5 (changed orientation to match PSoC™ Creator). Updated Figure 6 (changed orientation to match PSoC™ Creator). Updated Table 4 (Added additional information with respect to the functional capabilities for each solder pad). Updated Power supply connections and recommended external components: Updated External component recommendation: Updated Figure (changed orientation to match PSoC™ Creator). Updated Figure 8 (changed orientation to match PSoC™ Creator). Updated Figure 9 (changed orientation to match PSoC™ Creator). Updated Packaging: Updated Figure 13 (changed orientation to match PSoC™ Creator).</p> |
| *F | 2016-09-02 | <p>Updated More information: Updated description. Updated hyperlinks. Updated Electrical specification: Updated System resources: Updated Internal low-speed oscillator: Updated Table 6: Updated details in “Value” column corresponding to ECO_{TRIM} parameter. Updated Environmental specifications: Added Safety certification. Updated Ordering information: No change in part numbers. Added Table 53 (To specify minimum and maximum reel quantities that ship for orders of the CYBLE-022001-00 module). Updated to new template.</p> |
| *G | 2016-11-23 | <p>Updated Two easy-to-use design environments to get you started quickly: Added AIROC™ Bluetooth® & Bluetooth® LE module firmware platform. Updated Recommended host PCB layout: Updated Figure 4. Updated Figure 5. Updated Figure 6. Updated Power supply connections and recommended external components: Updated External component recommendation: Updated Figure. Updated Figure 8. Updated Digital and analog capabilities and connections: Updated Table 4: Updated details under “TCPWM” column (to add TCPWM capability on Port 2 pins). Added Note 3 and referred the same note in “TCPWM” column.</p> |

Revision history

| Document revision | Date | Description of changes |
|-------------------|------------|--|
| *H | 2016-12-14 | Updated Electrical specification : Updated SAR ADC : Updated Table 18 : Added Note 9 and referred the same note in “Details/Conditions” column corresponding to A_CHNIS_S and A-CHNKS_D parameters. Completing Sunset Review. |
| *I | 2017-04-18 | Updated Cypress Logo and Copyright. |
| *J | 2017-12-22 | Updated Packaging : Updated Figure 10 (Updated reel dimensions). Updated Figure 12 (Updated reel dimensions). Completing Sunset Review. |
| *K | 2018-03-08 | Updated Document Title to read as “CYBLE-022001-00, EZ-BLE™ Creator Module”. Replaced “PProC™ Module” and “PProC Module” with “Creator Module” in all instances across the document. Replaced “PProC™ BLE” and “PProC BLE” with “PSoC™ 4 BLE” and “PSoC 4 BLE” in all instances across the document. Updated General description : Updated Module description : Updated description. Updated More information : Updated description. Updated hyperlinks. Updated Environmental specifications : Updated Environmental compliance : Updated description. Updated Regulatory information : Updated ISED : Updated description. Updated Ordering information : No change in part numbers. Updated Part numbering convention . |
| *L | 2019-07-03 | Updated Regulatory information : Updated European R&TTE declaration of conformity : Replaced 1999/5/EC with 2014/53/EU. Updated to new template. |
| *M | 2020-09-02 | Updated General description : Updated hyperlinks. Updated description. Updated Module description : Updated description. Updated hyperlinks. Updated More information : Updated hyperlinks. Updated Two easy-to-use design environments to get you started quickly : Updated PSoC™ Creator Integrated Design Environment (IDE) : Updated PSoC™ Creator Component Datasheet - Bluetooth Low Energy (BLE) : Updated hyperlinks. Updated description. Updated Regulatory information : Added Packaging . Updated to new template. |

Revision history

| Document revision | Date | Description of changes |
|--------------------------|-------------|--|
| *N | 2020-13-23 | Replaced “Bluetooth® Low Energy (BLE)” with “Bluetooth® Low Energy” in all instances across the document. Replaced “BLE” with “Bluetooth® LE” in all instances across the document. |
| *O | 2021-03-29 | No technical updates. Completing Sunset Review. |
| *P | 2023-03-30 | Removed ANATEL section. Migrated to Infineon template. |

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