# THE DATASHEET OF

# CPC7583BC

# CPC7583

## Line Card Access Switch

## Features

- Small 20-pin or 28-pin SOIC or 28-pin DFN
- DFN version provides 65% PCB area reduction over 4th generation EMRs
- Monolithic IC reliability
- Low, matched, $R_{ON}$
- Eliminates the need for zero-cross switching
- Flexible switch timing for transition from ringing mode to talk mode.
- Clean, bounce-free switching
- SLIC tertiary protection via integrated current limiting, voltage clamping and thermal shutdown
- 5 V operation with power consumption < 10.5 mW
- Intelligent battery monitor
- Logic-level inputs, no external drive circuitry required
- SOIC versions pin-compatible with Legerity 7583/8583 family

## Applications

- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

## Description

The CPC7583 is a monolithic 10-pole line card access switch in a 20- or 28-pin SOIC or a 28-pin DFN package. It provides the necessary functions to replace three 2-Form-C electromechanical relays on analog line cards and combined voice and data line cards found in central office, access, and PBX equipment. The device contains solid state switches for tip and ring line break, ringing injection/ringing return, and test access. The CPC7583 requires only a +5 V supply and offers break-before-make or make-before-break switch operation.

## Ordering Information

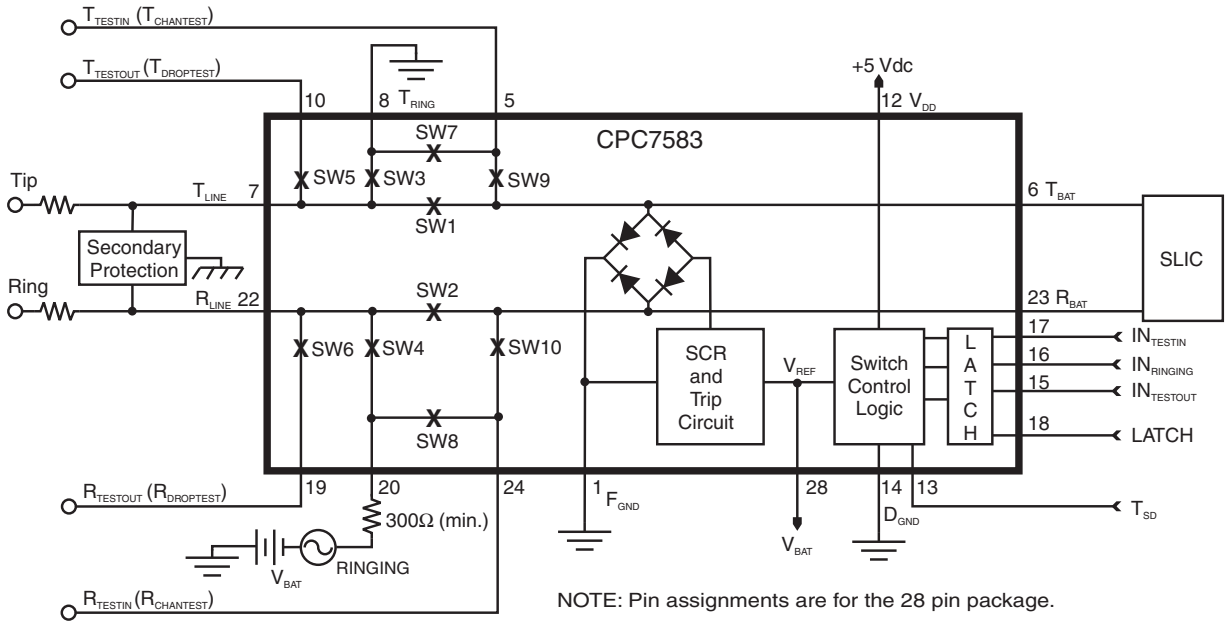
CPC7583 part numbers are specified as shown here:

B - 28-pin SOIC delivered 29/Tube, 1000/Reel
M - 28-pin DFN delivered 33/Tube, 1000/Reel
Z - 20-pin SOIC delivered 40/Tube, 1000/Reel

CPC7583 x x xx

TR - Add for Tape & Reel Version

A - With Protection SCR
B - Without Protection SCR
C - With Extra Logic State and With Protection SCR
D - With Extra Logic State and Without Protection SCR

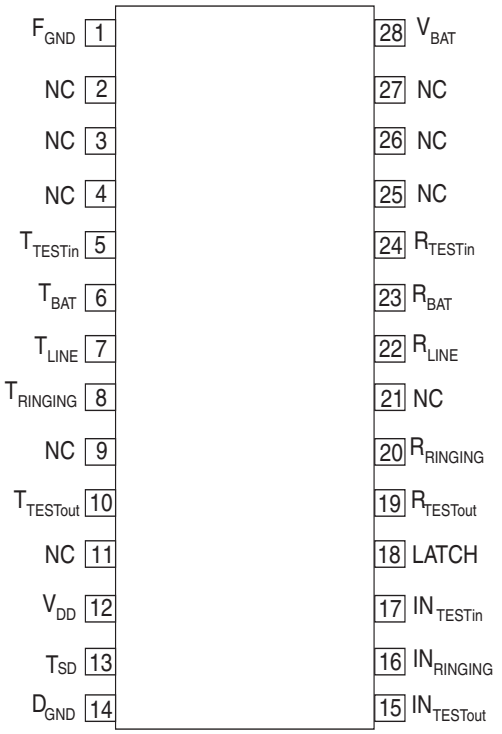



NOTE: Pin assignments are for the 28 pin package.

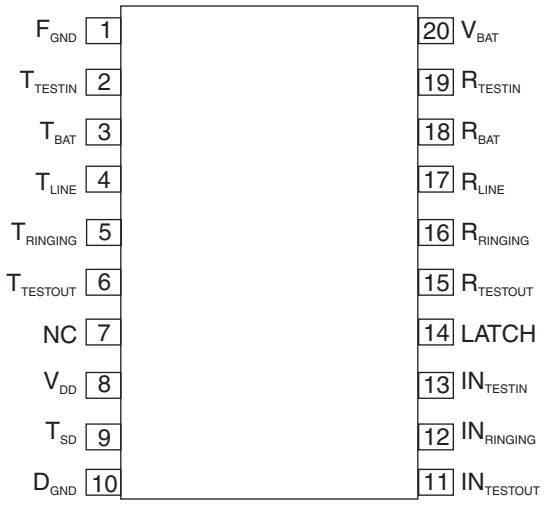
# 1. Specifications

## 1.1 Package Pinout

CPC7583B &
CPC7583M




CPC7583Z




## 1.2 Pinout Description

| 20 Pin | 28 Pin | Name | Description |
|---|---|---|---|
| 1 | 1 | $F_{GND}$ | Fault ground. |
| | 2 | NC | No connection. |
| | 3 | NC | No connection. |
| | 4 | NC | No connection. |
| 2 | 5 | $T_{TESTin}$ | Tip lead of the TESTin bus. |
| 3 | 6 | $T_{BAT}$ | Tip lead of the SLIC. |
| 4 | 7 | $T_{LINE}$ | Tip lead of the line side. |
| 5 | 8 | $T_{RINGING}$ | Ringing generator return. |
| | 9 | NC | Not connected. |
| 6 | 10 | $T_{TESTout}$ | Tip lead of the TESTout bus. |
| 7 | 11 | NC | No connection. |
| 8 | 12 | $V_{DD}$ | +5 V supply. |
| 9 | 13 | $T_{SD}$ | Temperature shutdown pin. |
| 10 | 14 | $D_{GND}$ | Digital ground. |
| 11 | 15 | $IN_{TESTout}$ | Logic control input. |
| 12 | 16 | $IN_{RINGING}$ | Logic control input. |
| 13 | 17 | $IN_{TESTin}$ | Logic control input. |
| 14 | 18 | LATCH | Data latch enable control input. |
| 15 | 19 | $R_{TESTout}$ | Ring lead of the TESTout bus. |
| 16 | 20 | $R_{RINGING}$ | Ringing generator source. |
| | 21 | NC | No connection. |
| 17 | 22 | $R_{LINE}$ | Ring lead of the line side. |
| 18 | 23 | $R_{BAT}$ | Ring lead of the SLIC. |
| 19 | 24 | $R_{TESTin}$ | Ring lead of the TESTin bus. |
| | 25 | NC | No connection. |
| | 26 | NC | No connection. |
| | 27 | NC | No connection. |
| 20 | 28 | $V_{BAT}$ | Battery supply. |

### 1.3 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Operating temperature | -40 | +110 | °C |
| Storage temperature | -40 | +150 | °C |
| Operating relative humidity | 5 | 95 | % |
| +5 V power supply ($V_{DD}$) | -0.3 | 7 | V |
| Battery Supply | - | -85 | V |
| $D_{GND}$ to $F_{GND}$ separation | -5 | +5 | V |
| Logic input voltage | -0.3 | $V_{DD}$ +0.3 | V |
| Logic input to switch output isolation | - | 320 | V |
| Switch open contact isolation (SW1, SW2, SW3, SW5, SW6, SW7, SW9, SW10) | - | 320 | V |
| Switch open contact isolation (SW4) | - | 465 | V |
| Switch open contact isolation (SW8) | - | 235 | V |

Absolute maximum electrical ratings are at 25°C

*Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.*

### 1.4 ESD Rating

| ESD Rating (Human Body Model) |
|---|
| 1000 V |

### 1.5 General Conditions

Unless otherwise specified, minimum and maximum values are production testing requirements.

Typical values are characteristic of the device at 25°C and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

Specifications cover the operating temperature range $T_A$ = -40°C to +85°C. Also, unless otherwise specified all testing is performed with $V_{DD}$ = +5$V_{dc}$, logic low input voltage is 0$V_{dc}$ and logic high input voltage is +5$V_{dc}$.

## 1.6 Switch Specifications

### 1.6.1 Break Switches, SW1 and SW2

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Off-state leakage current** | | | | | | |
| +25° C | $V_{SW}$ (differential) = -320 V to gnd<br>$V_{SW}$ (differential) = +260 V to -60 V | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ (differential) = -330 V to gnd<br>$V_{SW}$ (differential) = +270 V to -60 V | | | 0.3 | | |
| -40° C | $V_{SW}$ (differential) = -310 V to gnd<br>$V_{SW}$ (differential) = +250 V to -60 V | | | 0.1 | | |
| **$R_{ON}$** | | | | | | |
| +25° C | $I_{SW}$(on) = ±10 mA, ±40 mA,<br>$R_{BAT}$ and $T_{BAT}$ = -2 V | $R_{ON}$ | - | 14.5 | - | Ω |
| +85° C | | | | 20.5 | 28 | |
| -40° C | | | | 10.5 | - | |
| $R_{ON}$ match | Per on-resistance test condition of SW1 & SW2 | $\Delta R_{ON}$ | | 0.15 | 0.8 | |
| **DC current limit** | | | | | | |
| +25° C | $V_{SW}$ (on) = ±10 V | $I_{SW}$ | - | 225 | - | mA |
| +85° C | | | 80 | 150 | | |
| -40° C | | | - | 400 | 425 | |
| Dynamic current limit ($t \leq 0.5$ µs) | Break switches on, ringing switches off, apply ±1 kV 10x1000 µs pulse, with appropriate protection in place. | | - | 2.5 | - | A |
| **Logic input to switch output isolation** | | | | | | |
| +25° C | $V_{SW}$ ($T_{LINE}$, $R_{LINE}$) = ±320 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ ($T_{LINE}$, $R_{LINE}$) = ±330 V, logic inputs = gnd | | - | 0.3 | | |
| -40° C | $V_{SW}$ ($T_{LINE}$, $R_{LINE}$) = ±310 V, logic inputs = gnd | | - | 0.1 | | |
| dv/dt sensitivity | - | - | - | 200 | - | V/µs |

1.6.2 Ringing Return Switch, SW3

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Off-state leakage current** | | | | | | |
| +25° C | $V_{SW}$ (differential) = -320 V to gnd<br>$V_{SW}$ (differential) = +260 V to -60 V | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ (differential) = -330 V to gnd<br>$V_{SW}$ (differential) = +270 V to -60 V | | | 0.3 | | |
| -40° C | $V_{SW}$ (differential) = -310 V to gnd<br>$V_{SW}$ (differential) = +250 V to -60 V | | | 0.1 | | |
| **$R_{ON}$** | | | | | | |
| +25° C | $I_{SW}$(on) = ±0 mA, ±10 mA | $R_{ON}$ | - | 60 | - | Ω |
| +85° C | | | | 85 | 110 | |
| -40° C | | | | 45 | - | |
| **DC current limit** | | | | | | |
| +25° C | $V_{SW}$ (on) = ± 10 V | $I_{SW}$ | - | 120 | - | mA |
| +85° C | | | 70 | 85 | | |
| -40° C | | | - | 210 | | |
| Dynamic current limit ($t \leq 0.5$ µs) | Break switches off, ringing switches on, apply ±1 kV 10x1000 µs pulse, with appropriate protection in place. | | | 2.5 | | A |
| **Logic input to switch output isolation** | | | | | | |
| +25° C | $V_{SW}$ ($T_{RING}$, $T_{LINE}$) = ±320 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ ($T_{RING}$, $T_{LINE}$) = ±330 V, logic inputs = gnd | | | 0.3 | | |
| -40° C | $V_{SW}$ ($T_{RING}$, $T_{LINE}$) = ±310 V, logic inputs = gnd | | | 0.1 | | |
| dv/dt sensitivity | - | - | - | 200 | - | V/µs |

1.6.3 Ringing Switch, SW4

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Off-state leakage current** | | | | | | |
| +25° C | $V_{SW}$ (differential) = -255 V to +210 V<br>$V_{SW}$ (differential) = +255 V to -210 V | $I_{SW}$ | - | 0.05 | 1 | µA |
| +85° C | $V_{SW}$ (differential) = -270 V to +210 V<br>$V_{SW}$ (differential) = +270 V to -210 V | | | 0.1 | 1 | |
| -40° C | $V_{SW}$ (differential) = -245 V to +210 V<br>$V_{SW}$ (differential) = +245 V to -210 V | | | 0.05 | 1 | |
| On Voltage | $I_{SW}$ (on) = ± 1 mA | - | | 1.5 | 3 | V |
| Ringing generator current to ground during ringing | Inputs set for ringing mode | $I_{RINGING}$ | | 0.1 | 0.25 | mA |
| On steady-state current* | Inputs set for ringing mode | $I_{SW}$ | | - | 150 | mA |
| Surge current* | - | - | | - | 2 | A |
| Release current | - | $I_{RINGING}$ | | 450 | - | µA |
| $R_{ON}$ | $I_{SW}$ (on) = ±70 mA, ±80 mA | $R_{ON}$ | | 10 | 15 | Ω |
| **Logic input to switch output isolation** | | | | | | |
| +25° C | $V_{SW}$ ($R_{RING}$, $R_{LINE}$) = ±320 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ ($R_{RING}$, $R_{LINE}$) = ±330 V, logic inputs = gnd | | | 0.3 | | |
| -40° C | $V_{SW}$ ($R_{RING}$, $R_{LINE}$) = ±310 V, logic inputs = gnd | | | 0.1 | | |
| dv/dt sensitivity | - | - | | 200 | - | V/µs |

**Secondary protection and ringing source current limiting must prevent exceeding this parameter.*

### 1.6.4 $TEST_{OUT}$ Switches, SW5 and SW6

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Off-state leakage current** | | | | | | |
| +25° C | $V_{SW}$ (differential) = -320 V to gnd<br>$V_{SW}$ (differential) = +260 V to -60 V | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ (differential) = -330 V to gnd<br>$V_{SW}$ (differential) = +260 V to -60 V | | | 0.3 | | |
| -40° C | $V_{SW}$ (differential) = -310 V to gnd<br>$V_{SW}$ (differential) = +250 V to -60 V | | | 0.1 | | |
| **$R_{ON}$** | | | | | | |
| +25° C | $I_{SW}$(on) = ±10 mA, ±40 mA | $R_{ON}$ | - | 35 | - | Ω |
| +85° C | | | | 50 | 70 | |
| -40° C | | | | 26 | - | |
| **DC current limit** | | | | | | |
| +25° C | $V_{SW}$ (on) = ±10 V | $I_{SW}$ | - | 140 | - | mA |
| +85° C | | | 80 | 100 | - | |
| -40° C | | | - | 210 | 250 | |
| Dynamic current limit ($t \leq 0.5$ µs) | Break switches in on state, ringing switches off, apply ±1 kV at 10x1000 µs pulse, with appropriate secondary protection in place. | | - | 2.5 | - | A |
| **Logic input to switch output isolation** | | | | | | |
| +25° C | $V_{SW}$ ($T_{TESTout}$, $T_{LINE}$, $R_{TESTout}$, $R_{LINE}$) = ±320 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ ($T_{TESTout}$, $T_{LINE}$, $R_{TESTout}$, $R_{LINE}$) = ±330 V, logic inputs = gnd | $I_{SW}$ | - | 0.3 | 1 | µA |
| -40° C | $V_{SW}$ ($T_{TESTout}$, $T_{LINE}$, $R_{TESTout}$, $R_{LINE}$) = ±310 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| dv/dt sensitivity | - | - | | 200 | - | V/µs |

1.6.5 Ringing Test Return Switch, SW7

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Off-state leakage current** | | | | | | |
| +25° C | $V_{SW}$ (differential) = -320 V to gnd<br>$V_{SW}$ (differential) = +260 to -60 V | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ (differential) = -330 V to gnd<br>$V_{SW}$ (differential) = +270 V to -60 V | | | 0.3 | | |
| -40° C | $V_{SW}$ (differential) = -310 V to gnd<br>$V_{SW}$ (differential) = +250 V to -60 V | | | 0.1 | | |
| **$R_{ON}$** | | | | | | |
| +25° C | $I_{SW}$(on) = ±10 mA, ±40 mA | $R_{ON}$ | - | 60 | - | Ω |
| +85° C | | | | 85 | 100 | |
| -40° C | | | | 45 | - | |
| **DC current limit** | | | | | | |
| +25° C | $V_{SW}$ (on) = ±10 V | $I_{SW}$ | 70 | 120 | - | mA |
| +85° C | | | | 80 | | |
| -40° C | | | | 210 | | |
| **Logic input to switch output isolation** | | | | | | |
| +25° C | $V_{SW}$ ($T_{RING}$, $T_{TESTin}$) = ±320 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ ($T_{RING}$, $T_{TESTin}$) = ±330 V, logic inputs = gnd | | | 0.3 | | |
| -40° C | $V_{SW}$ ($T_{RING}$, $T_{TESTin}$) = ±310 V, logic inputs = gnd | | | 0.1 | | |
| dv/dt sensitivity | - | - | | 200 | - | V/µs |

### 1.6.6 Ringing Test Switch, SW8

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Off-state leakage current** | | | | | | |
| +25° C | $V_{SW}$ (differential) = -60 V to +175 V | $I_{SW}$ | - | 0.05 | 1 | µA |
| +85° C | | | | 0.1 | | |
| -40° C | | | | 0.05 | | |
| On Voltage | $I_{SW(ON)}$ = ±1 mA | - | | 0.75 | 1.5 | V |
| $R_{ON}$ | $I_{SW(ON)}$ = ±70 mA, ±80 mA | $R_{ON}$ | | 35 | - | Ω |
| Release Current | - | - | | 450 | - | µA |
| **Logic input to switch output isolation** | | | | | | |
| +25° C | $V_{SW}$ ($R_{RING}$, $R_{TESTin}$) = ±320 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ ($R_{RING}$, $R_{TESTin}$) = ±330 V, logic inputs = gnd | | | 0.3 | | |
| -40° C | $V_{SW}$ ($R_{RING}$, $R_{TESTin}$) = ±310 V, logic inputs = gnd | | | 0.1 | | |
| dv/dt sensitivity | - | - | | 200 | - | V/µs |

### 1.6.7 $TEST_{In}$ Switches, SW9 and SW10

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Off-state leakage current** | | | | | | |
| +25° C | $V_{SW}$ (differential) = -320 V to gnd<br>$V_{SW}$ (differential) = -60 V to +260 V | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ (differential) = -330 V to gnd<br>$V_{SW}$ (differential) = -60 V to +270 V | | | 0.3 | | |
| -40° C | $V_{SW}$ (differential) = -310 V to gnd<br>$V_{SW}$ (differential) = -60 V to +250 V | | | 0.1 | | |
| **$R_{ON}$** | | | | | | |
| +25° C | $I_{SW}$(on) = ±10 mA, ±40 mA | $R_{ON}$ | - | 35 | - | Ω |
| +85° C | | | | 50 | 70 | |
| -40° C | | | | 26 | - | |
| **DC current limit** | | | | | | |
| +25° C | $V_{SW}$ (on) = ±10 V | $I_{SW}$ | - | 160 | - | mA |
| +85° C | | | 80 | 110 | - | |
| -40° C | | | - | 210 | 250 | |
| **Logic input to switch output isolation** | | | | | | |
| +25° C | $V_{SW}$ ($T_{TESTin}$, $R_{TESTin}$) = ±320 V, logic inputs = gnd | $I_{SW}$ | - | 0.1 | 1 | µA |
| +85° C | $V_{SW}$ ($T_{TESTin}$, $R_{TESTin}$) = ±330 V, logic inputs = gnd | | | 0.3 | | |
| -40° C | $V_{SW}$ ($T_{TESTin}$, $R_{TESTin}$) = ±310 V, logic inputs = gnd | | | 0.1 | | |
| dv/dt sensitivity | - | - | | 200 | - | V/µs |

## 1.7 Additional Electrical Characteristics

| Parameter | Test Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Digital Inputs** | | | | | | |
| Input low voltage | - | $V_{IL}$ | - | - | 1.5 | V |
| Input high voltage | - | $V_{IH}$ | 3.5 | - | - | |
| Input leakage current (high) | $V_{DD}$ = 5.5 V, $V_{BAT}$ = -75 V, $V_{IH}$ = 5 V | $I_{IH}$ | - | 0.1 | 1 | µA |
| Input leakage current (low) | $V_{DD}$ = 5.5 V, $V_{BAT}$ = -75 V, $V_{IL}$ = 0 V | $I_{IL}$ | - | 0.1 | 1 | |
| **Voltage Requirements** | | | | | | |
| $V_{DD}$ | - | $V_{DD}$ | 4.5 | 5.0 | 5.5 | V |
| $V_{BAT}$[1] | - | $V_{BAT}$ | -19 | - | -72 | V |
| [1] *$V_{BAT}$ is used only for internal protection circuitry. If $V_{BAT}$ goes more positive than -10 V, the device will enter the all-off state and will remain in the all-off state until the battery goes more negative than -15 V* | | | | | | |
| **Power Requirements** | | | | | | |
| Power consumption in talk and all-off states | $V_{DD}$ = 5 V, $V_{BAT}$ = -48 V, measure $I_{DD}$ and $I_{BAT}$ | P | - | 3.5 | 7.5 | mW |
| Power consumption in any other state | $V_{DD}$ = 5 V, $V_{BAT}$ = -48 V, measure $I_{DD}$ and $I_{BAT}$ | P | | 5.0 | 10.5 | |
| $V_{DD}$ current in talk and all-off states | $V_{DD}$ = 5 V, $V_{BAT}$ = -48 V | $I_{DD}$ | - | 0.7 | 1.5 | mA |
| $V_{DD}$ current in any other state | | $I_{DD}$ | - | 1.0 | 1.9 | |
| $V_{BAT}$ current in any state | $V_{DD}$ = 5V, $V_{BAT}$ = -48 V | $I_{BAT}$ | - | 4 | 10 | µA |
| **Temperature Shutdown Requirements (temperature shutdown flag is active low)** | | | | | | |
| Shutdown activation temperature | Not production tested - limits are guaranteed by design and Quality Control sampling audits. | $T_{SD\_on}$ | 110 | 125 | 150 | °C |
| Shutdown circuit hysteresis | | $T_{SD\_off}$ | 10 | - | 25 | °C |

## 1.8 Protection Circuitry Electrical Specifications

| Parameter | Conditions | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| **Parameters Related to the Diodes in the Diode Bridge** | | | | | | |
| Voltage drop at continuous current (50/60 Hz) | Apply ± dc current limit of break switches | Forward Voltage | - | 2.8 | 3.5 | V |
| Voltage drop at surge current | Apply ± dynamic current limit of break switches | Forward Voltage | - | 5 | - | |
| **Parameters Related to the Protection SCR (CPC7583xA and CPC7583xC)** | | | | | | |
| Surge current | | - | - | - | * | A |
| Trigger current | +25° C | $I_{TRIG}$ | - | 200 | - | mA |
| | +85° C | $I_{TRIG}$ | | 120 | - | |
| Hold current | +25° C | $I_{HOLD}$ | | 265 | - | |
| | +85° C | $I_{HOLD}$ | 100 | 170 | - | |
| Gate trigger voltage | $I_{GATE} = I_{TRIGGER}$ § | $V_{TBAT}$ or $V_{RBAT}$ | $V_{BAT}$ -4 | - | $V_{BAT}$ -2 | V |
| Reverse leakage current | $V_{BAT}$ = -48 V | $I_{VBAT}$ | - | - | 1.0 | µA |
| On-state voltage | 0.5 A, t = 0.5 µs | $V_{TBAT}$ or $V_{RBAT}$ | | -3 | - | V |
| | 2.0 A, t = 0.5 µs | | | -5 | - | V |

*Passes GR1089 and ITU-T K.20 with appropriate secondary protection in place.
§$V_{BAT}$ must be capable of sourcing $I_{TRIGGER}$ for the internal SCR to activate.

## 1.9 Truth Tables

### 1.9.1 Truth Table for CPC7583xA and CPC7583xB

| State | $IN_{RINGING}$ | $IN_{TESTIN}$ | $IN_{TESTOUT}$ | Latch | $T_{SD}$ | $TEST_{IN}$ Switches | Break Switches | Ringing Test Switches | Ringing Switches | $TEST_{OUT}$ Switches |
|---|---|---|---|---|---|---|---|---|---|---|
| Talk | 0 | 0 | 0 | 0 | 1 or Floating [1] | Off | On | Off | Off | Off |
| TESTout | 0 | 0 | 1 | | | Off | Off | Off | Off | On |
| TESTin | 0 | 1 | 0 | | | On | Off | Off | Off | Off |
| Simultaneous TESTin and TESTout | 0 | 1 | 1 | | | On | Off | Off | Off | On |
| Ringing | 1 | 0 | 0 | | | Off | Off | Off | On | Off |
| Ringing Generator Test | 1 | 1 | 0 | | | Off | Off | On | Off | Off |
| Latched | X | X | X | 1 | | Unchanged | Unchanged | Unchanged | Unchanged | Unchanged |
| All Off | 1 | 0 | 1 | 0 | | Off | Off | Off | Off | Off |
| | 1 | 1 | 1 | 0 | | Off | Off | Off | Off | Off |
| | X | X | X | X | 0 [2] | Off | Off | Off | Off | Off |

[1] If $T_{SD}$ is tied high, thermal shutdown is disabled. If $T_{SD}$ is left floating, the thermal shutdown mechanism functions normally.
[2] Forcing $T_{SD}$ to ground overrides the logic input pins and forces an all off state.

1.9.2 Truth Table for CPC7583xC and CPC7583xD

| State | $IN_{RINGING}$ | $IN_{TESTIN}$ | $IN_{TESTOUT}$ | Latch | $T_{SD}$ | $TEST_{IN}$ Switches | Break Switches | Ringing Test Switches | Ringing Switches | $TEST_{OUT}$ Switches |
|---|---|---|---|---|---|---|---|---|---|---|
| Talk | 0 | 0 | 0 | 0 | 1 or Floating [1] | Off | On | Off | Off | Off |
| TESTout | 0 | 0 | 1 | | | Off | Off | Off | Off | On |
| TESTin | 0 | 1 | 0 | | | On | Off | Off | Off | Off |
| Simultaneous TESTin and TESTout | 0 | 1 | 1 | | | On | Off | Off | Off | On |
| Ringing | 1 | 0 | 0 | | | Off | Off | Off | On | Off |
| Ringing Generator Test | 1 | 1 | 0 | | | Off | Off | On | Off | Off |
| Simultaneous TESTout and Ringing Generator Test | 1 | 1 | 1 | | | Off | Off | On | Off | On |
| Latched | X | X | X | 1 | | Unchanged | Unchanged | Unchanged | Unchanged | Unchanged |
| All Off | 1 | 0 | 1 | 0 | | Off | Off | Off | Off | Off |
| | X | X | X | X | 0 [2] | Off | Off | Off | Off | Off |

[1] If $T_{SD}$ is tied high, thermal shutdown is disabled. If $T_{SD}$ is left floating, the thermal shutdown mechanism functions normally.

[2] Forcing $T_{SD}$ to ground overrides the logic input pins and forces an all off state.

## 2. Functional Description

### 2.1 Introduction

The CPC7583 has the following states:

- **Talk**. Loop break switches SW1, and SW2 closed, all other switches open.
- **Ringing**. Ringing switches SW3, SW4 closed, all other switches open.
- **TESTout**. Testout switches SW5, SW6 closed, all other switches open.
- **Ringing generator test**. SW7, SW8 closed, all other switches open.
- **TESTin**. Testin switches SW9 and SW10 closed.
- **Simultaneous TESTin and TESTout**. SW9, SW10, SW5, and SW6 closed, all other switches open.
- **Simultaneous test out and ringing generator test**. SW5, SW6, SW7, and SW8 closed, all other switches open (only on the xC and xD versions).
- **All Off**. All switches open.

See "Truth Tables" on page 12 for more information.

The CPC7583 offers break-before-make and make-before-break switching from the ringing state to the talk state with simple logic level input control. Solid-state switch construction means no impulse noise is generated when switching during ringing cadence or ring trip, eliminating the need for external zero-cross switching circuitry. State-control is via logic-level input so no additional driver circuitry is required. The linear line break switches SW1 and SW2 have exceptionally low $R_{ON}$ and excellent matching characteristics. The ringing switch SW4 has a minimum open contact breakdown voltage of 465 V. This is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Integrated into the CPC7583 is an over voltage clamping circuit, active current limiting, and a thermal shutdown mechanism to provide protection to the SLIC device during a fault condition. Positive and negative surges are reduced by the current limiting circuitry and hazardous potentials are diverted to ground via diodes and the integrated SCR. Power-cross potentials are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC7583 from an overvoltage fault condition, the use of a secondary protector is required. The secondary protector must limit the voltage seen at the $T_{LINE}$ and $R_{LINE}$ terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is recommended. With proper selection of the secondary protector, a line card using the CPC7583 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

The CPC7583 operates from a +5 V supply only. This gives the device extremely low idle and active power consumption and allows use with virtually any range of battery voltage. The battery voltage is also used by the CPC7583 as a reference for the integrated protection circuit. In the event of a loss of battery voltage, the CPC7583 enters the all-off state.

### 2.2 Switch Logic

The CPC7583 provides, when switching from the ringing state to the talk state, the ability to control the release timing of the ringing switches SW3 and SW4 relative to the state of the loop break switches SW1 and SW2 using simple logic-level input. This is referred to as a make-before-break or break-before-make operation. When the line break switch contacts (SW1 and SW2) are closed (or made) before the ringing access switch contacts (SW3 and SW4) are opened (broken), this is referred to as make-before-break operation. Break-before-make operation occurs when the ringing access contacts (SW3 and SW4) are opened (broken) before the line break switch contacts (SW1 and SW2) are closed (made). With the CPC7583, the make-before-break and break-before-make operations can easily be selected by applying the proper sequence of logic inputs to $IN_{TESTout}$, $IN_{RINGING}$, and $IN_{TESTin}$.

The logic sequences for either mode of operation are given in "Make-Before-Break Operation (Ringing to Talk Transition)" on page 15 and "Break-Before-Make Operation (Ringing to Talk Transition)" on page 15. Logic states and explanations are given in "Truth Tables" on page 12.

Break-before-make operation can also be achieved using the $T_{SD}$ pin as an input. In "Break-Before-Make Operation (Ringing to Talk Transition)" on page 15, lines 2 and 3, it is possible to induce the switches to the all-off state by grounding $T_{SD}$ instead of applying input to the logic pins. This has the effect of overriding the logic inputs and forcing the device to the all-off state. For

20 Hz ringing hold this input state for 25 ms. During this hold period, toggle the inputs from the ringing state to the talk state. After the 25 ms, release $T_{SD}$ to return switch control to the input pins $IN_{TESTout}$, $IN_{RINGING}$, $IN_{TESTin}$ and the latch control pin.

2.2.1 Make-Before-Break Operation (Ringing to Talk Transition)

| State | $IN_{RINGING}$ | $IN_{TESTIN}$ | $IN_{TESTOUT}$ | Latch | $T_{SD}$ | Timing | Break Switches 1 and 2 | Ring Return Switch 3 | Ring Access Switch 4 | All Other Test Switches |
|---|---|---|---|---|---|---|---|---|---|---|
| Ringing | 1 | 0 | 0 | 0 | Floating | - | Off | On | On | Off |
| Make-before-break | 0 | 0 | 0 | | Floating | SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of ringing. In this transition state, current that is limited to the dc break switch current limit value will be sourced from the ring node of the SLIC. | On | Off | On | Off |
| Talk | 0 | 0 | 0 | | Floating | Zero-cross current has occurred | On | Off | Off | Off |

2.2.2 Break-Before-Make Operation (Ringing to Talk Transition)

| State | $IN_{RINGING}$ | $IN_{TESTIN}$ | $IN_{TESTOUT}$ | Latch | $T_{SD}$ | Timing | Break Switches 1 and 2 | Ring Return Switch 3 | Ring Access Switch 4 | All Other Test Switches |
|---|---|---|---|---|---|---|---|---|---|---|
| Ringing | 1 | 0 | 0 | 0 | Floating | - | Off | On | On | Off |
| All off | 1 | 0 | 1 | | Floating | Hold this state for one-half of ringing cycle. SW4 waiting for zero current to turn off. | Off | Off | On | Off |
| All off | 1 | 0 | 1 | | Floating | Zero current has occurred. SW4 has opened | Off | Off | Off | Off |
| Talk | 0 | 0 | 0 | | Floating | Close break switches | On | Off | Off | Off |

## 2.3 Alternate Break-Before-Make Operation

Note that break-before-make operation can also be achieved using $T_{SD}$ as an input. In lines 2 and 3 of the table **"Break-Before-Make Operation (Ringing to Talk Transition)" on page 15**, instead of using the logic input pins to force the all-off state, force $T_{SD}$ to ground. This overrides the logic inputs and also forces the all off state. Hold this state for one-half of the ringing cycle. During this $T_{SD}$ forced all-off state, change the inputs from the power ringing state ($IN_{RING}$ = 1, $IN_{TESTIN}$ = 0, $IN_{TESTOUT}$ = 0) to the talk state ($IN_{RING}$ = 0, $IN_{TESTIN}$ = 0, $IN_{TESTOUT}$ = 0). After the hold period, release $T_{SD}$ to return switch control to the input pins which will set the talk state.

## 2.4 Data Latch

The CPC7583 has an integrated data latch. The latch operation is controlled by logic-level input at the LATCH pin. The data input of the latch are the input pins, while the output of the data latch is an internal node used for state control. When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly through to state control. A change in input will be reflected by a change in switch state. When the LATCH control pin is at logic 1, the data latch is active and a change in input control will not affect switch state. The switches will remain in the position they were in when the LATCH changed from

logic 0 to logic 1 and will not respond to changes in input as long as the latch is at logic 1. The $T_{SD}$ input is not tied to the data latch. Therefore, $T_{SD}$ is not affected by the LATCH input and the $T_{SD}$ input will override state control.

### 2.5 $T_{SD}$ Behavior

Setting $T_{SD}$ to +5V allows switch control using the logic inputs. This setting, however, also disables the thermal shutdown circuit and is therefore not recommended. When using logic control via the input pins, $T_{SD}$ should be allowed to float. As a result, the two recommended states when using $T_{SD}$ as a control are 0, which forces the device to an all-off state, or float, which allows logic inputs to remain active. This requires the use of an open-collector type buffer.

### 2.6 Ringing Switch Zero-Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ringing switch is designed to delay the change in state until the next zero-crossing. Once on, the switch requires a zero-current cross to turn off, and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter the logic input until the next zero crossing. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing switches. See Clare application note **AN-144, Impulse Noise Benefits of Line Card Access Switches** for more information. The attributes of ringing switch SW4 may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300 Ω in series with the ringing generator is recommended.

### 2.7 Power Supplies

Both a +5 V supply and battery voltage are connected to the CPC7583. Switch state control is powered exclusively by the +5 V supply. As a result, the CPC7583 exhibits extremely low power consumption during both active and idle states.

The battery voltage is not used for switch control but rather as a supply for the integrated secondary protection circuitry. The integrated SCR is designed to trigger when the voltage at $T_{BAT}$ or $R_{BAT}$ drops 2 to 4 V below the applied voltage on the $V_{BAT}$ pin. This trigger prevents a fault induced overvoltage event at the $T_{BAT}$ or $R_{BAT}$ nodes.

### 2.8 Battery Voltage Monitor

The CPC7583 also uses the $V_{BAT}$ voltage to monitor battery voltage. If battery voltage is lost, the CPC7583 immediately enters the all-off state. It remains in this state until the battery voltage is restored. The device also enters the all-off state if the system battery voltage goes more positive than –10 V, and remains in the all-off state until the battery voltage goes more negative than –15 V. This battery monitor feature draws a small current from the battery (less than 1 μA typical) and will add slightly to the device's overall power dissipation.

### 2.9 Protection

#### 2.9.1 Diode Bridge/SCR

The CPC7583 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground via $F_{GND}$. Voltage is clamped to a diode drop above ground. During a negative transient of 2V to 4V more negative than the voltage source at $V_{BAT}$, the SCR conducts and faults are shunted to $F_{GND}$ via the SCR or the diode bridge.

In order for the SCR to crowbar or foldback, the on voltage (see **"Protection Circuitry Electrical Specifications" on page 12**) of the SCR must be less negative than the $V_{BAT}$ voltage. If the $V_{BAT}$ voltage is less negative than the SCR on voltage, or if the $V_{BAT}$ supply is unable to source the trigger current, the SCR will not crowbar.

For power induction or power-cross fault conditions, the positive cycle of the transient is clamped to a diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the $V_{BAT}$ reference voltage by two to four volts, steering the fault current to ground.

#### 2.9.2 Current Limiting function

If a lightning strike transient occurs when the device is in the talk state, the current is passed along the line to the integrated protection circuitry and restricted by the dynamic current limit response of the active switches. During the talk state when a 1000V 10x1000 μS pulse (GR-1089-CORE lightning) is applied to the line though a properly clamped external protector, the current into $T_{LINE}$ or $R_{LINE}$ will be a pulse with a typical magnitude of 2.5 A and a duration of less than 0.5 μs.

If a power-cross fault occurs with the device in the talk state, the current is passed though break switches SW1 and SW2 on to the integrated protection circuit and is limited by the dynamic DC current limit response of the two break switches. The DC current limit, specified over temperature, is between 80 mA and 425 mA, and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to power cross fault, the measured current at $T_{LINE}$ or $R_{LINE}$ will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will enter the all-off state.

### 2.10 Temperature Shutdown

The thermal shutdown mechanism will activate when the device temperature reaches a minimum of 110° C, placing the device in the all-off state regardless of logic input. During thermal shutdown mode, the voltage out of the $T_{SD}$ pin will read 0 V. Normal output of $T_{SD}$ is $V_{DD}$.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross transient, the device temperature will rise and the thermal shutdown will activate forcing the switches to the all-off state. At this point the current measured into $T_{LINE}$ or $R_{LINE}$ will drop to zero. Once the device enters thermal shutdown it will remain in the all-off state until the temperature of the device drops below the deactivation level of the thermal shutdown circuit. This will permit the device to return to normal operation. If the transient has not passed, current will flow up to the value allowed by the dynamic DC current limiting of the switches and heating will begin again, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector could activate and shunt all current to ground.

### 2.11 External Protection Elements

The CPC7583 requires only over-voltage secondary protection on the loop side of the device. The integrated protection feature described above negates the need for additional protection on the SLIC side. The secondary protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7583. A foldback or crowbar type protector is recommended to minimize stresses on the CPC7583.

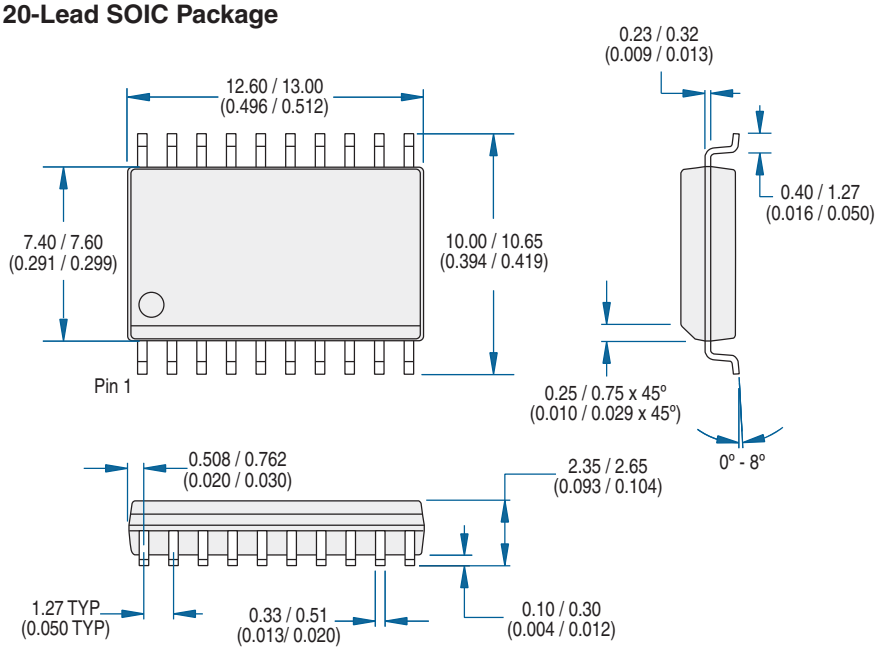
Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors and PTCs.

# 3. Manufacturing Information

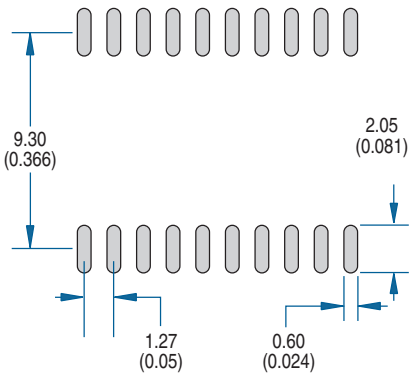
## 3.1 Mechanical Dimensions and PCB Land Patterns

### 3.1.1 CPC7583Z

**20-Lead SOIC Package**



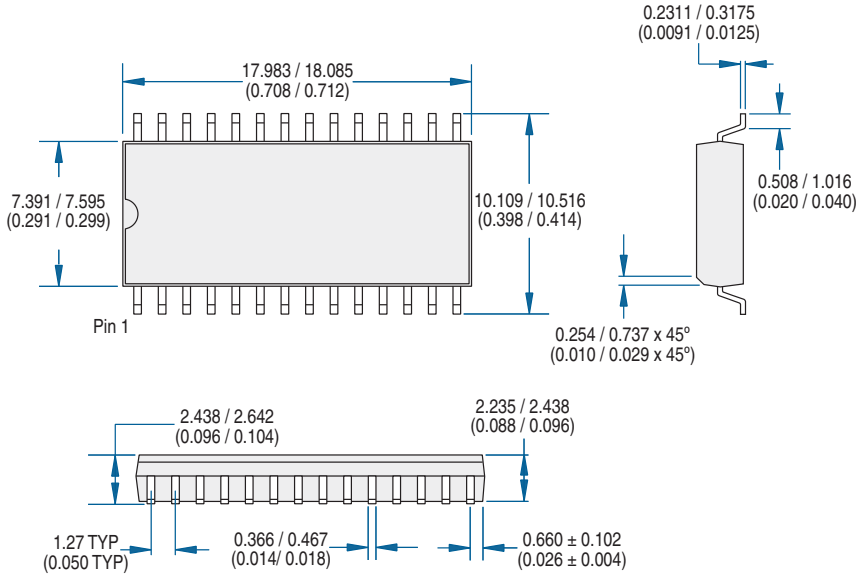

**Recommended PCB Land Pattern**



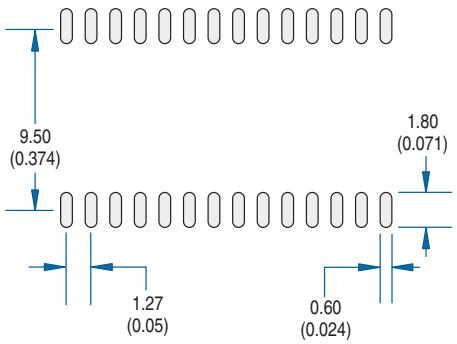

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

### 3.1.2 CPC7583B

**28-Lead SOIC Package**



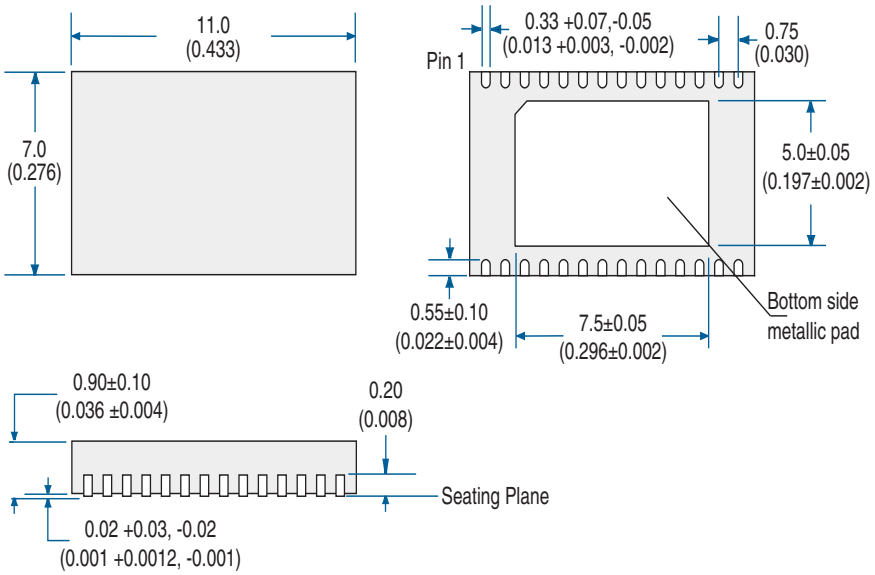

**Recommended PCB Land Pattern**



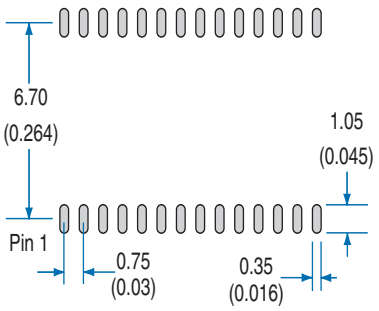

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

3.1.3 CPC7583M

**28-Lead DFN Package**




**Recommended PCB Land Pattern**

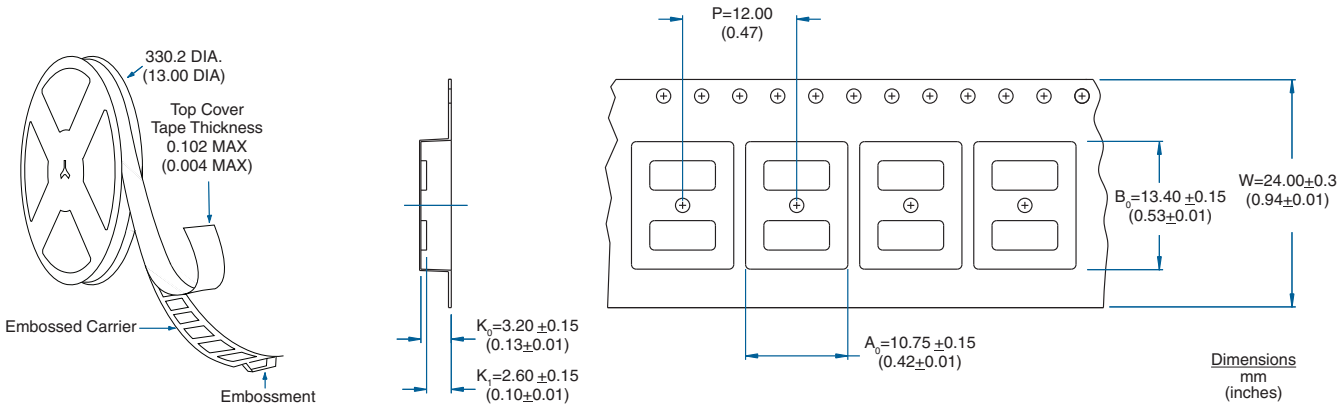



Dimensions
mm
(inches)

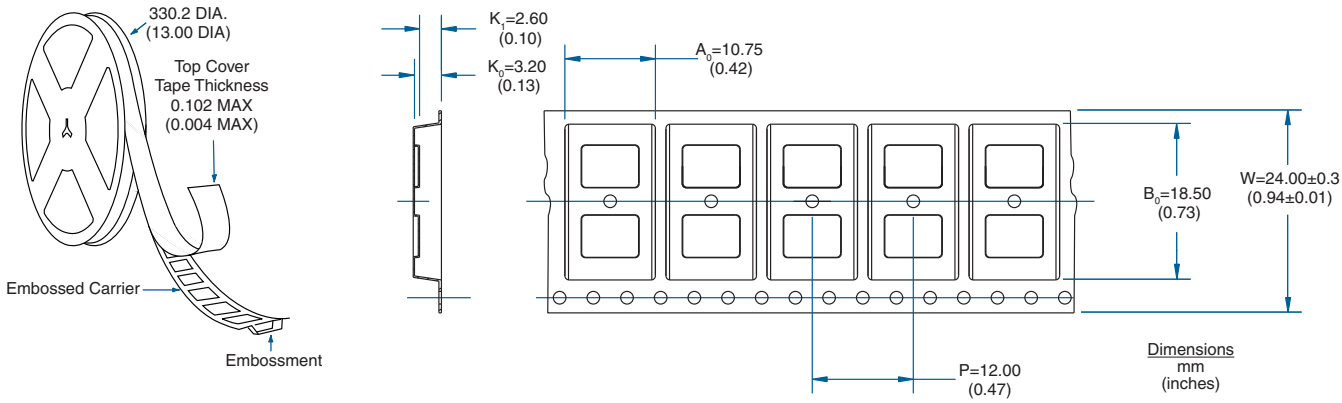
NOTE: Because the metallic pad on the bottom of the DFN package is connected to the substrate of the die, Clare recommends that no printed circuit board traces cross this area to avoid potential shorting issues.

## 3.2 Tape and Reel Specifications

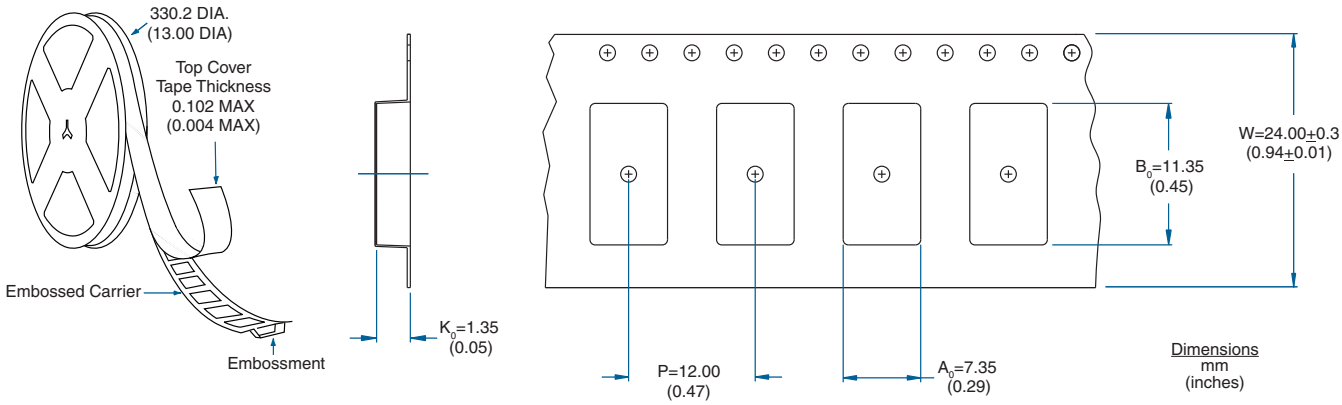
### 3.2.1 CPC7583Z (20-Pin SOIC) - Tape and Reel Dimensions




### 3.2.2 CPC7583B (28-Pin SOIC) - Tape and Reel Dimensions




### 3.2.3 CPC7583M (28-Pin DFN) - Tape and Reel Dimensions



## 3.3 Soldering

### 3.3.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity for this product using IPC/JEDEC standard J-STD-020. Moisture uptake from atmospheric humidity occurs by diffusion. During the solder reflow process, in which the component is attached to the PCB, the whole body of the component is exposed to high process temperatures. The combination of moisture uptake and high reflow soldering temperatures may lead to moisture induced delamination and cracking of the component. To prevent this, this component must be handled in accordance with IPC/JEDEC standard J-STD-033 per the labeled moisture sensitivity level (MSL), level 1 for the SOIC package, and level 3 for the DFN package.

### 3.3.2 Reflow Profile

For proper assembly, this component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

## 3.4 Washing

Clare does not recommend ultrasonic cleaning of this part.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