



**THE DATASHEET OF
SI4731-C40-GU**



TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. Electrical Specifications	4
2. Typical Application Schematic (QFN)	17
3. Typical Application Schematic (SSOP)	18
4. Bill of Materials (QFN/SSOP)	19
5. Functional Description	20
5.1. Overview	20
5.2. Operating Modes	20
5.3. FM Receiver	21
5.4. AM Receiver	21
5.5. Digital Audio Interface (Si4731 Only)	21
5.6. Stereo Audio Processing	22
5.7. De-emphasis	23
5.8. Stereo DAC	23
5.9. Soft Mute	23
5.10. RDS/RBDS Processor (Si4731 Only)	23
5.11. Tuning	23
5.12. Seek	23
5.13. Reference Clock	23
5.14. Control Interface	23
5.15. GPO Outputs	25
5.16. Firmware Upgrades	25
5.17. Reset, Powerup, and Powerdown	25
5.18. Programming with Commands	25
6. Commands and Properties	26
7. Pin Descriptions: Si4730/31-GM	29
8. Pin Descriptions: Si4730/31-GU	30
9. Ordering Guide	31
10. Package Markings (Top Marks)	32
10.1. Si4730/31 Top Mark (QFN)	32
10.2. Top Mark Explanation (QFN)	32
10.3. Si4730/31 Top Mark (SSOP)	33
10.4. Top Mark Explanation (SSOP)	33
11. Package Outline: Si4730/31 QFN	34
12. PCB Land Pattern: Si4730/31 QFN	35
13. Package Outline: Si4730/31 SSOP	37
14. PCB Land Pattern: Si4730/31 SSOP	38
15. Additional Reference Resources	39
Document Change List	40
Contact Information	42

Si4730/31-C40

1. Electrical Specifications

Table 1. Recommended Operating Conditions¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage ²	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.85	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	μ s
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	μ s
Ambient Temperature	T_A		-20	25	85	°C

Note:

1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at $V_{DD} = 3.3$ V and 25 °C unless otherwise stated.
2. SSOP devices operate down to $V_{DD} = 2$ V at 25 °C.

Table 2. Absolute Maximum Ratings^{1,2}

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	-0.5 to 3.9	V
Input Current ³	I_{IN}	10	mA
Input Voltage ³	V_{IN}	-0.3 to ($V_{IO} + 0.3$)	V
Operating Temperature	T_{OP}	-40 to 95	°C
Storage Temperature	T_{STG}	-55 to 150	°C
RF Input Level ⁴		0.4	V_{PK}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4730/31 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. At RF input pins, FMI and AMI.

Table 3. DC Characteristics(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
Supply Current ¹	I _{FM}		—	19.2	22	mA
Supply Current ²	I _{FM}	Low SNR level	—	19.9	23	mA
RDS Supply Current ¹	I _{FM}		—	19.2	23	mA
AM Mode						
Supply Current ¹	I _{AM}	Analog Output Mode	—	15.4	20.5	mA
Supplies and Interface						
Interface Supply Current	I _{IO}		—	320	600	μA
V _{DD} Powerdown Current	I _{DDPD}		—	10	20	μA
V _{IO} Powerdown Current	I _{IOPD}	SCLK, RCLK inactive	—	1	10	μA
High Level Input Voltage ³	V _{IH}		0.7 x V _{IO}	—	V _{IO} + 0.3	V
Low Level Input Voltage ³	V _{IL}		-0.3	—	0.3 x V _{IO}	V
High Level Input Current ³	I _{IH}	V _{IN} = V _{IO} = 3.6 V	-10	—	10	μA
Low Level Input Current ³	I _{IL}	V _{IN} = 0 V, V _{IO} = 3.6 V	-10	—	10	μA
High Level Output Voltage ⁴	V _{OH}	I _{OUT} = 500 μA	0.8 x V _{IO}	—	—	V
Low Level Output Voltage ⁴	V _{OL}	I _{OUT} = -500 μA	—	—	0.2 x V _{IO}	V
Notes:						
1. Specifications are guaranteed by characterization.						
2. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.						
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.						
4. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.						

Si4730/31-C40

Table 4. Reset Timing Characteristics^{1,2,3}

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.85$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
\overline{RST} Pulse Width and GPO1, GPO2/ \overline{INT} Setup to $\overline{RST}\uparrow^4$	t_{SRST}	100	—	—	μs
GPO1, GPO2/ \overline{INT} Hold from $\overline{RST}\uparrow$	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of \overline{RST} .
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of \overline{RST} , and stays high until after the first start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of \overline{RST} .
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 μs , to provide time for on-chip 1 M Ω devices (active while \overline{RST} is low) to pull GPO1 high and GPO2 low.

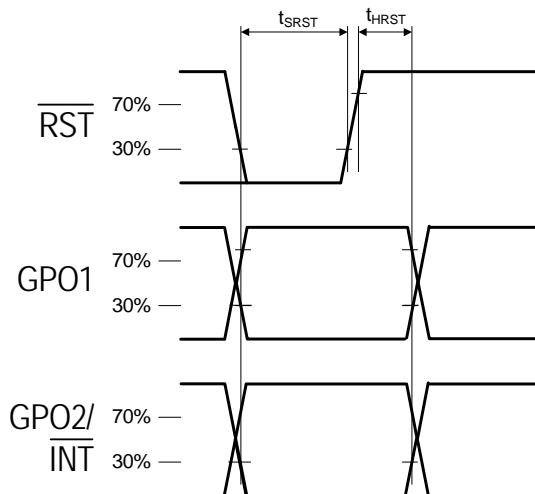


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics^{1,2,3}(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f _{SCL}		0	—	400	kHz
SCLK Low Time	t _{LOW}		1.3	—	—	μs
SCLK High Time	t _{HIGH}		0.6	—	—	μs
SCLK Input to SDIO ↓ Setup (START)	t _{SU:STA}		0.6	—	—	μs
SCLK Input to SDIO ↓ Hold (START)	t _{HD:STA}		0.6	—	—	μs
SDIO Input to SCLK ↑ Setup	t _{SU:DAT}		100	—	—	ns
SDIO Input to SCLK ↓ Hold ^{4,5}	t _{HD:DAT}		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	t _{SU:STO}		0.6	—	—	μs
STOP to START Time	t _{BUF}		1.3	—	—	μs
SDIO Output Fall Time	t _{f:OUT}		$20 + 0.1 \frac{C_b}{1\text{pF}}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	t _{f:IN} t _{r:IN}		$20 + 0.1 \frac{C_b}{1\text{pF}}$	—	300	ns
SCLK, SDIO Capacitive Loading	C _b		—	—	50	pF
Input Filter Pulse Suppression	t _{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$, and stays high until after the first start condition.
4. The Si4730/31 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum t_{HD:DAT} specification.
5. The maximum t_{HD:DAT} has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 kHz, t_{HD:DAT} may be violated as long as all other timing parameters are met.

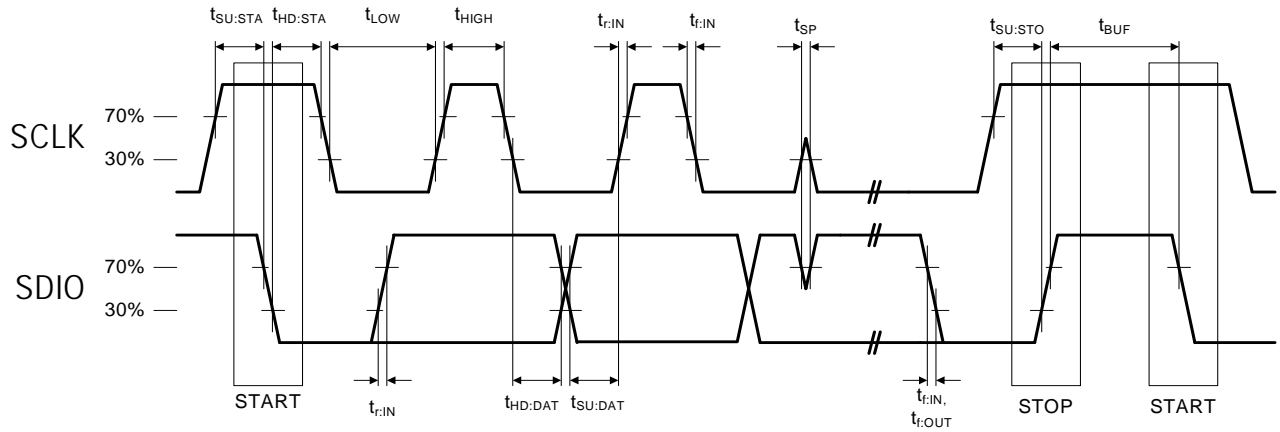


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

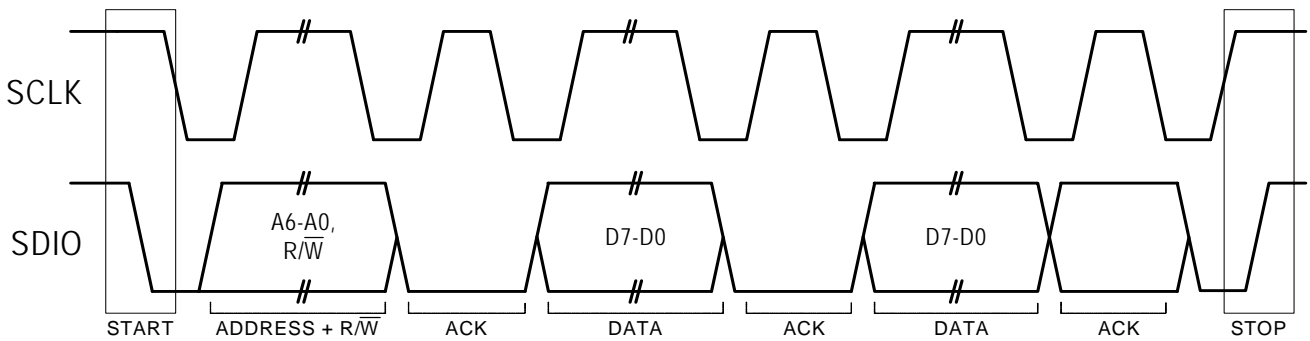
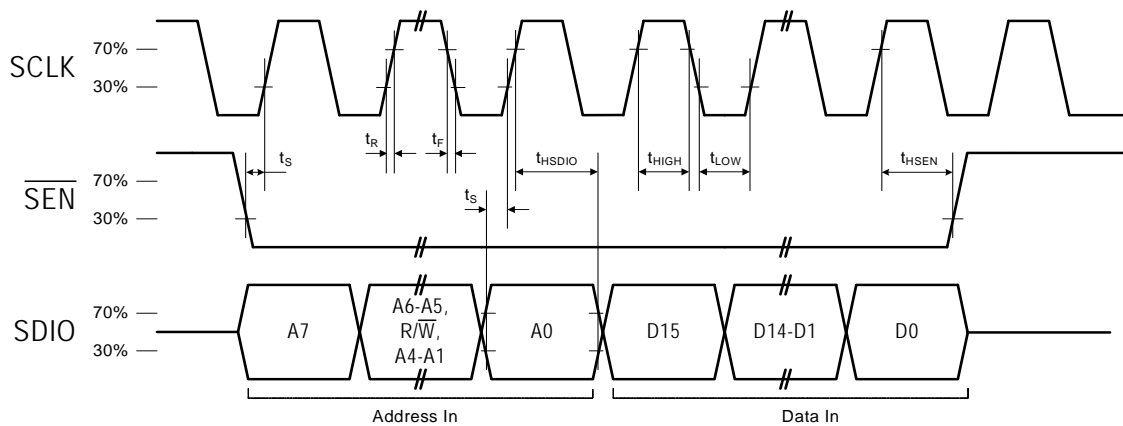
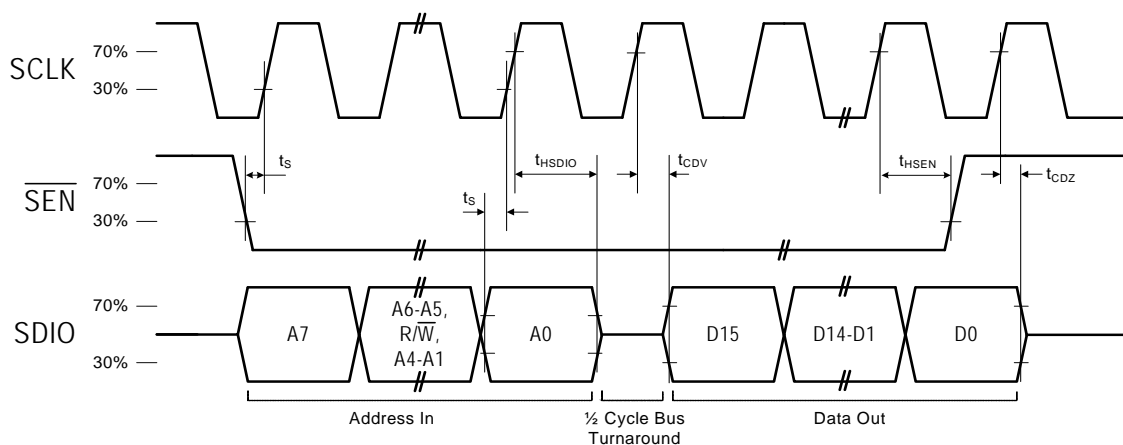


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics $(V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, V_{IO} = 1.85 \text{ to } 3.6 \text{ V}, T_A = -20 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, \overline{SEN} to SCLK \uparrow Setup	t_S		20	—	—	ns
SDIO Input to SCLK \uparrow Hold	t_{HSDIO}		10	—	—	ns
\overline{SEN} Input to SCLK \downarrow Hold	t_{HSEN}		10	—	—	ns
SCLK \uparrow to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK \uparrow to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, \overline{SEN} , SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

**Figure 4. 3-Wire Control Interface Write Timing Parameters****Figure 5. 3-Wire Control Interface Read Timing Parameters**

Si4730/31-C40

Table 7. SPI Control Interface Characteristics

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.85$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, \overline{SEN} to SCLK \uparrow Setup	t_S		15	—	—	ns
SDIO Input to SCLK \uparrow Hold	t_{HSDIO}		10	—	—	ns
\overline{SEN} Input to SCLK \downarrow Hold	t_{HSEN}		5	—	—	ns
SCLK \downarrow to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK \downarrow to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, \overline{SEN} , SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

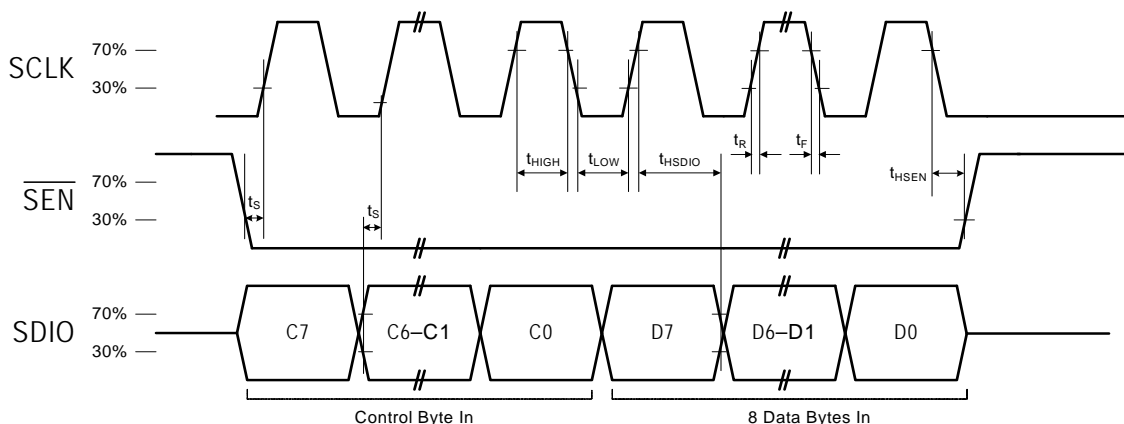


Figure 6. SPI Control Interface Write Timing Parameters

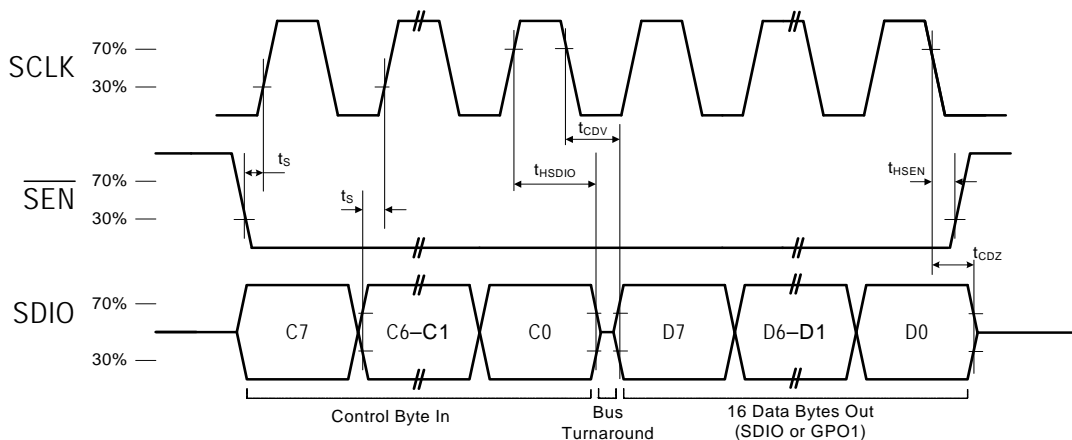
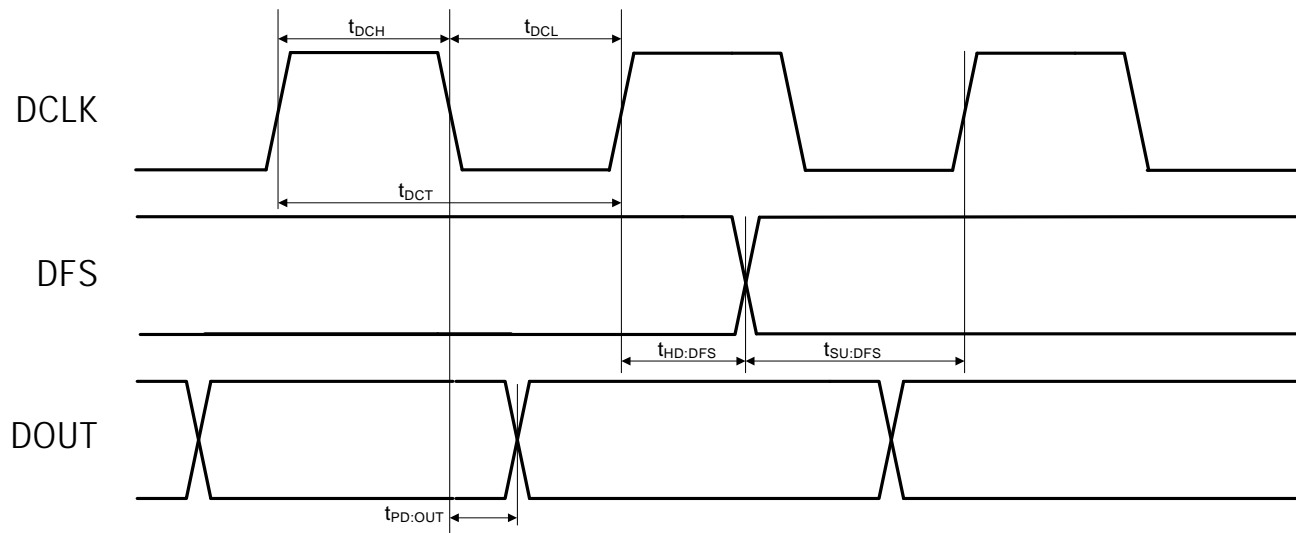


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics $(V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, V_{IO} = 1.85 \text{ to } 3.6 \text{ V}, T_A = -20 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	12	ns

**Figure 8. Digital Audio Interface Timing Parameters, I²S Mode**

Si4730/31-C40

Table 9. FM Receiver Characteristics^{1,2}

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.85$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity with Headphone Network ^{3,4,5}		(S+N)/N = 26 dB	—	2.2	3.5	μ V EMF
Sensitivity with 50 Ω Network ^{3,4,5,6}		(S+N)/N = 26 dB	—	1.1	—	μ V EMF
RDS Sensitivity ⁶		$\Delta f = 2$ kHz, RDS BLER < 5%	—	15	—	μ V EMF
LNA Input Resistance ^{6,7}			3	4	5	k Ω
LNA Input Capacitance ^{6,7}			4	5	6	pF
Input IP3 ^{6,8}			100	105	—	dB μ V EMF
AM Suppression ^{3,4,6,7}		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		± 200 kHz	35	50	—	dB
Alternate Channel Selectivity		± 400 kHz	60	70	—	dB
Spurious Response Rejection ⁶		In-band	35	—	—	dB
Audio Output Voltage ^{3,4,7}			72	80	90	mV _{RMS}
Audio Output L/R Imbalance ^{3,7,9}			—	—	1	dB
Audio Frequency Response Low ⁶		-3 dB	—	—	30	Hz
Audio Frequency Response High ⁶		-3 dB	15	—	—	kHz
Audio Stereo Separation ^{7,9}			32	42	—	dB
Audio Mono S/N ^{3,4,5,7,10}			55	63	—	dB
Audio Stereo S/N ^{4,5,6,7,10,11}			—	58	—	dB
Audio THD ^{3,7,9}			—	0.1	0.5	%
De-emphasis Time Constant ⁶		FM_DEEMPHASIS = 2	70	75	80	μ s
		FM_DEEMPHASIS = 1	45	50	54	μ s

Notes:

1. Additional testing information is available in "AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure." Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. $F_{MOD} = 1$ kHz, 75 μ s de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. $\Delta f = 22.5$ kHz.
5. $B_{AF} = 300$ Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. $V_{EMF} = 1$ mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
9. $\Delta f = 75$ kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. Blocker Amplitude = 100 dB μ V
13. Sensitivity measured at (S+N)/N = 26 dB.
14. At temperature (25°C).

Table 9. FM Receiver Characteristics^{1,2} (Continued)(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking Sensitivity ^{3,4,5,6,12,13}		$\Delta f = \pm 400$ kHz	—	32	—	dB μ V
		$\Delta f = \pm 4$ MHz	—	38	—	dB μ V
Intermode Sensitivity ^{3,4,5,6,12,13}		$\Delta f = \pm 400$ kHz, ± 800 kHz	—	40	—	dB μ V
		$\Delta f = \pm 4$ MHz, ± 8 MHz	—	35	—	dB μ V
Audio Output Load Resistance ^{6,10}	R _L	Single-ended	10	—	—	k Ω
Audio Output Load Capacitance ^{6,10}	C _L	Single-ended	—	—	50	pF
Seek/Tune Time ⁶		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time ⁶		From powerdown	—	—	110	ms
RSSI Offset ¹⁴		Input levels of 8 and 60 dB μ V at RF Input	-3	—	3	dB

Notes:

1. Additional testing information is available in "AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure." Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 μ s de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. $\Delta f = 22.5$ kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
9. $\Delta f = 75$ kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. Blocker Amplitude = 100 dB μ V
13. Sensitivity measured at (S+N)/N = 26 dB.
14. At temperature (25°C).

Si4730/31-C40

Table 10. 64–75.9 MHz Input Frequency FM Receiver Characteristics^{1,2,6}

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.85$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		64	—	75.9	MHz
Sensitivity with Headphone Network ^{3,4,5}		(S+N)/N = 26 dB	—	4.0	—	μ V EMF
LNA Input Resistance ⁷			3	4	5	k Ω
LNA Input Capacitance ⁷			4	5	6	pF
Input IP3 ⁸			100	105	—	dB μ V EMF
AM Suppression ^{3,4,7}		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		\pm 200 kHz	—	50	—	dB
Alternate Channel Selectivity		\pm 400 kHz	—	70	—	dB
Audio Output Voltage ^{3,4,7}			72	80	90	mV _{RMS}
Audio Output L/R Imbalance ^{3,7,9}			—	—	1	dB
Audio Frequency Response Low		–3 dB	—	—	30	Hz
Audio Frequency Response High		–3 dB	15	—	—	kHz
Audio Mono S/N ^{3,4,5,7,10}			55	63	—	dB
Audio THD ^{3,7,9}			—	0.1	0.5	%
De-emphasis Time Constant		FM_DEEMPHASIS = 2	70	75	80	μ s
		FM_DEEMPHASIS = 1	45	50	54	μ s
Audio Output Load Resistance ¹⁰	R_L	Single-ended	10	—	—	k Ω
Audio Output Load Capacitance ¹⁰	C_L	Single-ended	—	—	50	pF
Seek/Tune Time		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time		From powerdown	—	—	110	ms
RSSI Offset ¹¹		Input levels of 8 and 60 dB μ V EMF	–3	—	3	dB

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. $F_{MOD} = 1$ kHz, 75 μ s de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. $\Delta f = 22.5$ kHz.
5. $B_{AF} = 300$ Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. $V_{EMF} = 1$ mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
9. $\Delta f = 75$ kHz.
10. At L_{OUT} and R_{OUT} pins.
11. At temperature (25 °C).

Table 11. AM Receiver Characteristics^{1,2}(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, TA = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f _{RF}		520	—	1710	kHz
Sensitivity ^{3,4,5,6}		(S+N)/N = 26 dB	—	25	35	μV EMF
Large Signal Voltage Handling ^{4,6,7}		THD < 8%	—	300	—	mV _{RMS}
Power Supply Rejection Ratio ⁶		ΔV _{DD} = 100 mV _{RMS} , 100 Hz	—	40	—	dB
Audio Output Voltage ^{3,4,8}			54	60	67	mV _{RMS}
Audio S/N ^{3,4,5,8}			50	56	—	dB
Audio THD ^{3,4,8}			—	0.1	0.5	%
Antenna Inductance ^{6,9}			180	—	450	μH
Powerup Time ⁶		From powerdown	—	—	110	ms

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 520 kHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. FMOD = 1 kHz, 30% modulation, 2 kHz channel filter.
4. Analog audio output mode.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. See “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure” for evaluation method.
8. V_{IN} = 5 mV_{rms}.
9. Stray capacitance on antenna and board must be < 10 pF to achieve full tuning range at higher inductance levels.

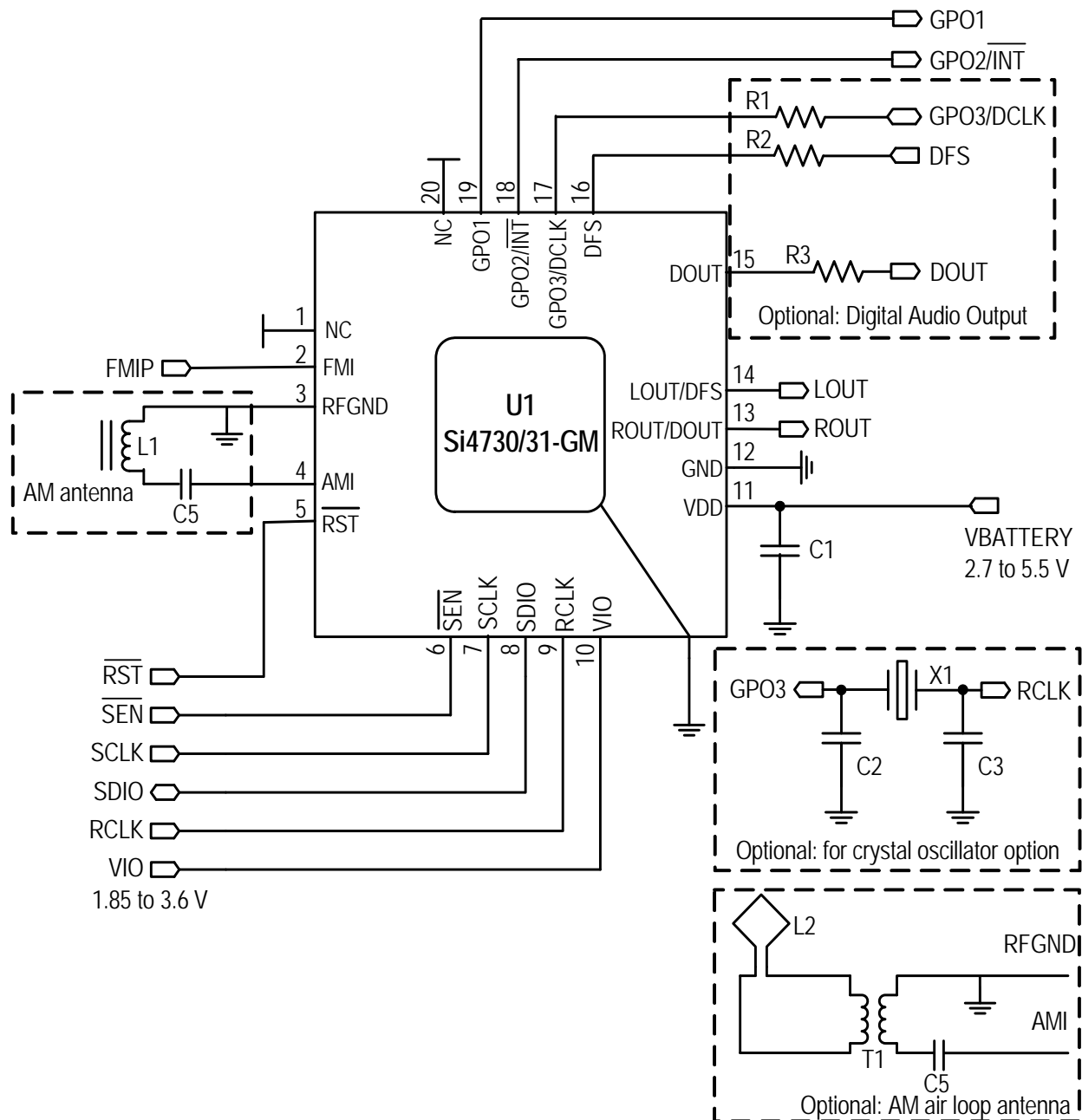
Si4730/31-C40

Table 12. Reference Clock and Crystal Characteristics

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.85$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies ¹			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance ²			-100	—	100	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance ²			-100	—	100	ppm
Board Capacitance			—	—	3.5	pF
Notes:						
1. The Si4730/31 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. For more details, see Table 6 of "AN332: Si47xx Programming Guide".						
2. A frequency tolerance of ± 50 ppm is required for FM seek/tune using 50 kHz channel spacing.						

2. Typical Application Schematic (QFN)

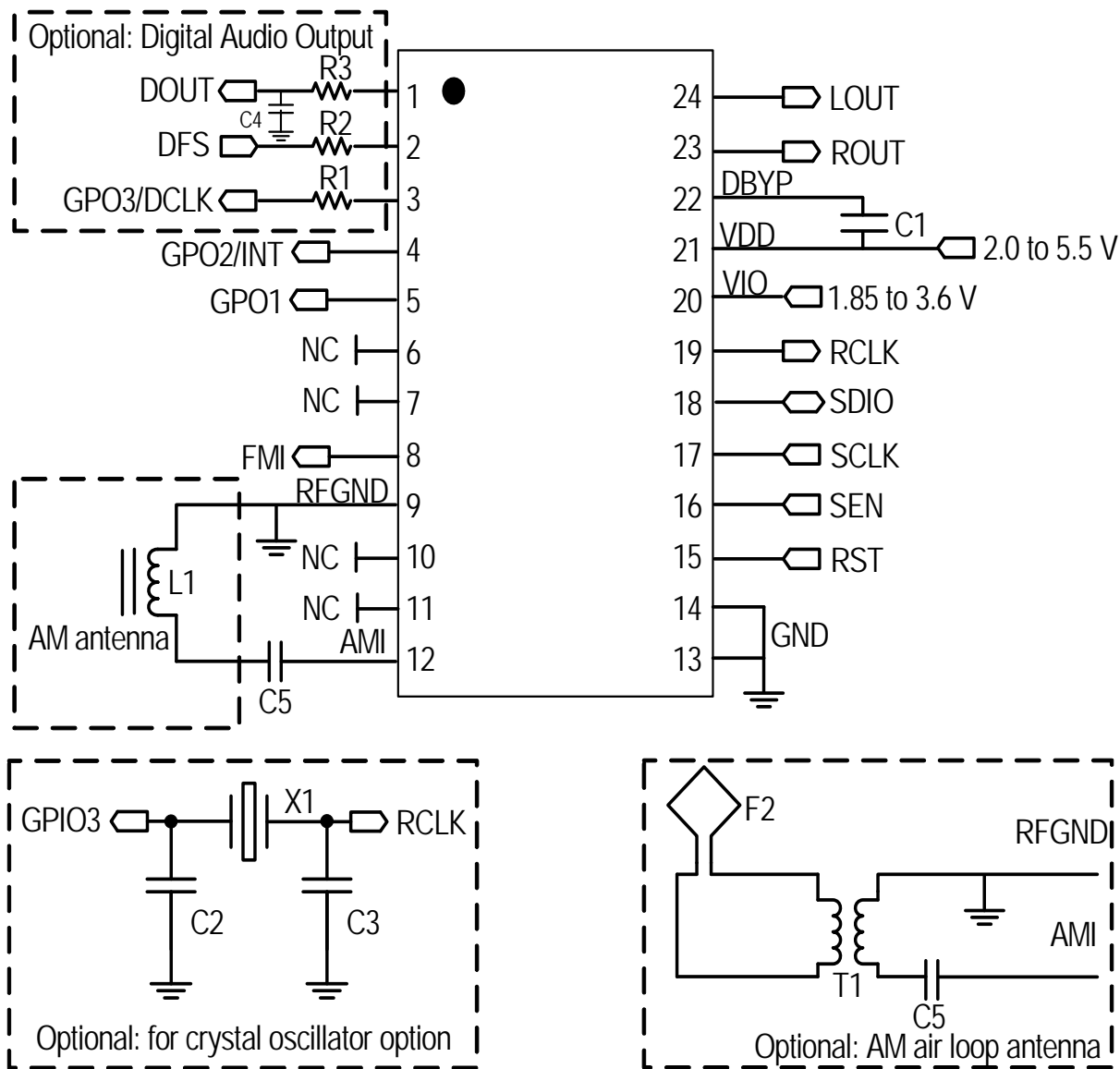


Notes:

1. Place C1 close to V_{DD} pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the FM antenna interface, and pin 4 connects to the AM antenna interface.
6. Place Si4730/31 as close as possible to antenna and keep the FMI and AMI traces as short as possible.

Si4730/31-C40

3. Typical Application Schematic (SSOP)



Notes:

1. Place C1 close to V_{DD} and DBYP pins.
2. All grounds connect directly to GND plane on PCB.
3. Pins 6 and 7 are no connects, leave floating.
4. Pins 10 and 11 are unused. Tie these pins to GND.
5. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
6. Pin 8 connects to the FM antenna interface, and pin 12 connects to the AM antenna interface.
7. Place Si4730/31 as close as possible to antenna and keep the FMI and AMI traces as short as possible.

4. Bill of Materials (QFN/SSOP)

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, $\pm 20\%$, Z5U/X7R	Murata
C5	Coupling capacitor, 0.47 μF , $\pm 20\%$, Z5U/X7R	Murata
L1	Ferrite loop stick, 180–450 μH	Jiaxin
U1	Si4730/31 AM/FM Radio Tuner	Silicon Laboratories
Optional Components		
T1	Transformer, 1–5 turns ratio	Jiaxin, UMEC
L2	Air loop antenna, 10–20 μH	Various
C2, C3	Crystal load capacitors, 22 pF, $\pm 5\%$, COG (Optional for crystal oscillator option)	Venkel
C4	Noise mitigating capacitor, 2~5 pF (Optional for digital audio)	Murata
X1	32.768 kHz crystal (Optional for crystal oscillator option)	Epson
R1	Resistor, 2 k Ω (Optional for digital audio)	Venkel
R2	Resistor, 2 k Ω (Optional for digital audio)	Venkel
R3	Resistor, 600 Ω (Optional for digital audio)	Venkel

In the analog audio output mode, ROUT and LOUT are used for the audio output pins. In the digital audio mode, DOUT, DFS, and DCLK pins are used. Concurrent analog/digital audio output mode is also available requiring all five pins. The receiver mode and the audio output mode are set by the POWER_UP command listed in Table 14, “Selected Si473x Commands,” on page 26.

5.3. FM Receiver

The Si4730/31 FM receiver is based on the proven Si4700/01 FM tuner. The receiver uses a digital low-IF architecture allowing the elimination of external components and factory adjustments. The Si4730/31 integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (64 to 108 MHz). An AGC circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the Si4730/31 to perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

5.4. AM Receiver

The highly-integrated Si4730/31 supports worldwide AM band reception from 520 to 1710 kHz using a digital low-IF architecture with a minimum number of external components and no manual alignment required. This digital low-IF architecture allows for high-precision filtering offering excellent selectivity and SNR with minimum variation across the AM band. The DSP also provides adjustable channel step sizes in 1 kHz increments, AM demodulation, soft mute, seven different channel bandwidth filters, and additional features, such as a programmable automatic volume control (AVC) maximum gain allowing users to adjust the level of background noise. Similar to the FM receiver, the integrated LNA and AGC optimize sensitivity and rejection of strong interferers allowing better reception of weak stations.

The Si4730/31 provides highly-accurate digital AM tuning without factory adjustments. To offer maximum flexibility, the receiver supports a wide range of ferrite loop sticks from 180–450 μ H. An air loop antenna is supported by using a transformer to increase the effective inductance from the air loop. Using a 1:5 turn ratio inductor, the inductance is increased by 25 times and easily supports all typical AM air loop antennas which generally vary between 10 and 20 μ H.

5.5. Digital Audio Interface (Si4731 Only)

The digital audio interface operates in slave mode and supports three different audio data formats:

- I²S
- Left-Justified
- DSP Mode

5.5.1. Audio Data Formats

In I²S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

5.5.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

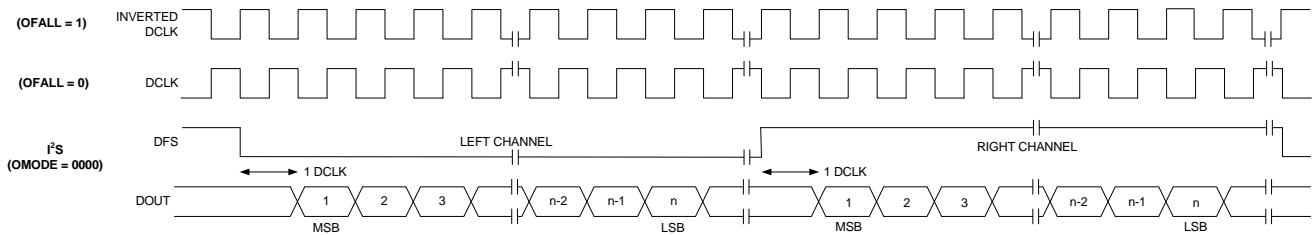


Figure 10. I²S Digital Audio Format

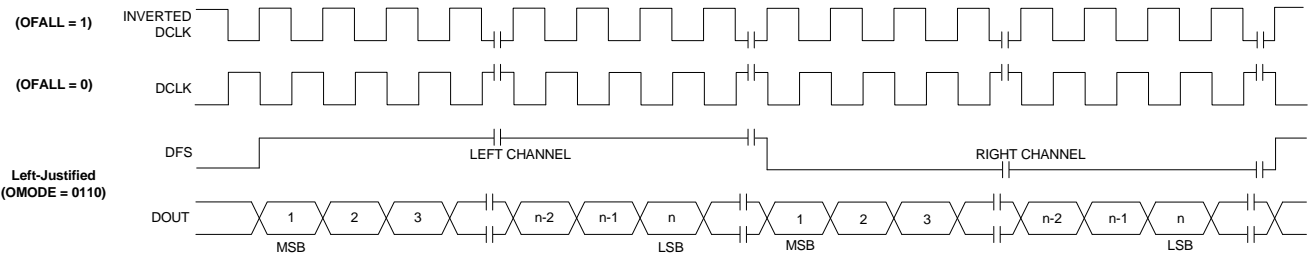


Figure 11. Left-Justified Digital Audio Format

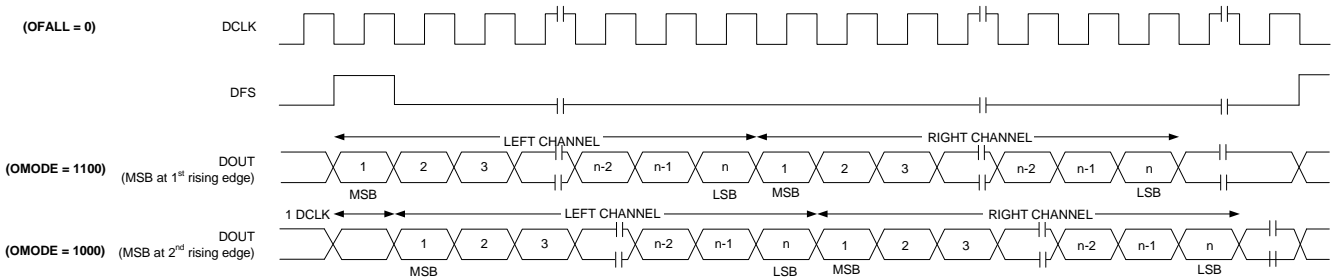


Figure 12. DSP Digital Audio Format

5.6. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 13 below.

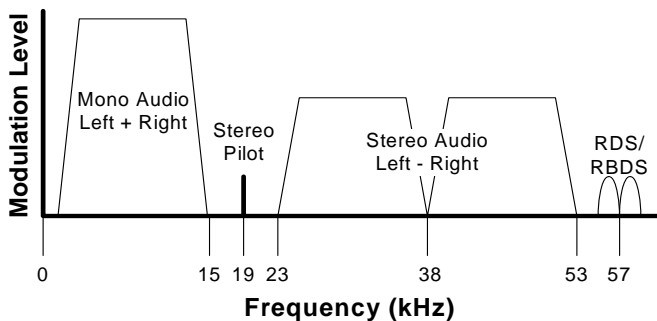


Figure 13. MPX Signal Spectrum

5.6.1. Stereo Decoder

The Si4730/31's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively. The Si4731 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

5.6.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Stereo/mono status can be monitored with the FM_RSQ_STATUS command. Mono operation can be forced with the FM_BLEND_MONO_THRESHOLD property.

5.7. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4730/31 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 μ s and is set by the FM_DEEMPHASIS property.

5.8. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property.

5.9. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The softmute attenuation level is adjustable using the FM_SOFT_MUTE_MAX_ATTENUATION and AM_SOFT_MUTE_MAX_ATTENUATION properties.

5.10. RDS/RBDS Processor (Si4731 Only)

The Si4731 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction.

The Si4731 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The Si4731 reports RDS decoder synchronization status and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors or that the block checksum contains errors.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

5.11. Tuning

The tuning frequency is directly programmed using the FM_TUNE_FREQ and AM_TUNE_FREQ commands. The Si4730/31 supports channel spacing steps of 10 kHz in FM mode and 1 kHz in AM mode.

5.12. Seek

Seek tuning will search up or down for a valid channel. Valid channels are found when the receive signal strength indicator (RSSI) and the signal-to-noise ratio (SNR) values exceed the set threshold. Using the SNR qualifier rather than solely relying on the more traditional RSSI qualifier can reduce false stops and increase the number of valid stations detected. Seek is initiated using the FM_SEEK_START and AM_SEEK_START commands. The RSSI and SNR threshold settings are adjustable using properties (see Table 15).

5.13. Reference Clock

The Si4730/31 reference clock is programmable, supporting RCLK frequencies in Table 12. Refer to Table 3, "DC Characteristics," on page 5 for switching voltage levels and Table 9, "FM Receiver Characteristics," on page 12 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "2. Typical Application Schematic (QFN)" on page 17. This mode is enabled using the POWER_UP command. Refer to Table 14, "Selected Si473x Commands," on page 26.

The Si4730/31 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4730/31 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4730/31 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The seek/tune complete (STC) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

5.14. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4730/31 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The Si4730/31 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of RST. The GPO1 pin includes an internal pull-up resistor, which is connected while

\overline{RST} is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while \overline{RST} is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 13.

Table 13. Bus Mode Select on Rising Edge of \overline{RST}

Bus Mode	GPO1	GPO2
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of \overline{RST} , the pins GPO1 and GPO2 are used as general purpose output (O) pins, as described in Section “5.15. GPO Outputs”. In any bus mode, commands may only be sent after V_{IO} and V_{DD} supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

5.14.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of \overline{RST} , and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of \overline{RST} .

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4730/31 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4730/31 will respond to only a single device address, this address can be changed with the \overline{SEN} pin (note that the \overline{SEN} pin is not used for signaling in 2-wire mode). When $\overline{SEN} = 0$, the 7-bit device address is 0010001b. When $\overline{SEN} = 1$, the address is 1100011b.

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4730/31 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4730/31 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4730/31.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

5.14.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of \overline{RST} .

The 3-wire bus mode uses the SCLK, SDIO, and \overline{SEN} pins. A transaction begins when the user drives \overline{SEN} low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 9-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4730/31 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets \overline{SEN} high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while \overline{SEN} is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

5.14.3. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.

SPI bus mode uses the SCLK, SDIO, and $\overline{\text{SEN}}$ pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. A transaction begins when the system controller drives $\overline{\text{SEN}} = 0$. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

- 0x48 = write a command (controller drives 8 additional bytes on SDIO).
- 0x80 = read a response (device drives 1 additional byte on SDIO).
- 0xC0 = read a response (device drives 16 additional bytes on SDIO).
- 0xA0 = read a response (device drives 1 additional byte on GPO1).
- 0xE0 = read a response (device drives 16 additional bytes on GPO1).

For write operations, the system controller must drive exactly 8 data bytes (a command and seven arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

For read operations, the controller must read exactly 1 byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep $\overline{\text{SEN}}$ low until all bytes have transferred. A transaction may be aborted at any time by setting $\overline{\text{SEN}}$ high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

5.15. GPO Outputs

The Si4730/31 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-impedance. The GPO pins can be reconfigured as specialized functions. GPO2/INT can be configured to provide interrupts and GPO3 can be configured to provide external crystal support or as DCLK in digital audio output mode.

5.16. Firmware Upgrades

The Si4730/31 contains on-chip program RAM to accommodate minor changes to the firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new radio designs and those already deployed in the field.

5.17. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

5.18. Programming with Commands

To ease development time and offer maximum customization, the Si4730/31 provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control an action such as powerup the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command. A partial list of commands is available in Table 14, “Selected Si473x Commands,” on page 26.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold. A partial list of properties is available in Table 15, “Selected Si473x Properties,” on page 27.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a 1-byte status update, indicating interrupt and clear-to-send status information. For a detailed description of the commands and properties for the Si4730/31, see “AN332: Si47xx Programming Guide.”

6. Commands and Properties

Table 14. Selected Si473x Commands

Cmd	Name	Description
0x01	POWER_UP	Powerup device and mode selection. Modes include AM or FM receive, analog or digital output, and reference clock or crystal support.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Powerdown device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x20	FM_TUNE_FREQ	Selects the FM tuning frequency.
0x21	FM_SEEK_START	Begins searching for a valid frequency.
0x23	FM_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel.
0x24	FM_RDS_STATUS	Returns RDS information for current channel and reads an entry from the RDS FIFO (Si4731 only).
0x40	AM_TUNE_FREQ	Selects the AM tuning frequency.
0x41	AM_SEEK_START	Begins searching for a valid frequency.
0x43	AM_RSQ_STATUS	Queries the status of the RSQ of the current channel.

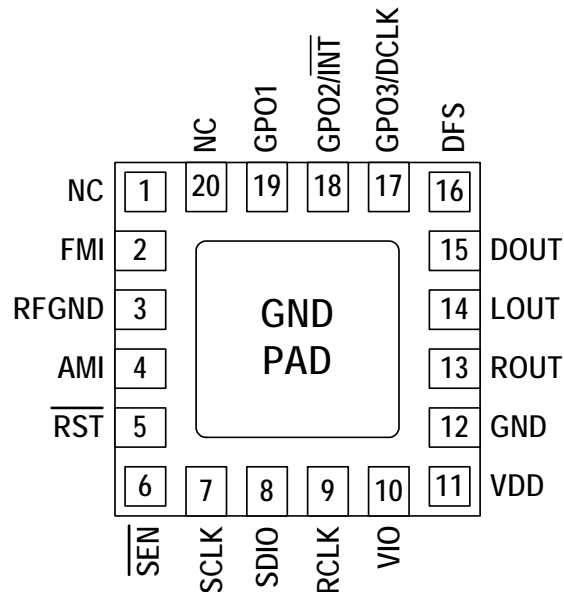
Table 15. Selected Si473x Properties

Prop	Name	Description	Default
0x1100	FM_DEEMPHASIS	Sets de-emphasis time constant. Default is 75 μ s.	0x0002
0x1105	FM_BLEND_STEREO_THRESHOLD	Sets RSSI threshold for stereo blend (full stereo above threshold, blend below threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 49 dB μ V.	0x0031
0x1106	FM_BLEND_MONO_THRESHOLD	Sets RSSI threshold for mono blend (full mono below threshold, blend above threshold). To force stereo, set this to 0. To force mono, set this to 127. Default value is 30 dB μ V.	0x001E
0x1200	FM_RSQ_INT_SOURCE	Configures interrupt related to RSQ metrics.	0x0000
0x1300	FM_SOFT_MUTE_RATE	Sets the attack and decay rates when entering and leaving soft mute.	0x0040
0x1302	FM_SOFT_MUTE_MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 16 dB.	0x0010
0x1303	FM_SOFT_MUTE_SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 4 dB.	0x0004
0x1400	FM_SEEK_BAND_BOTTOM	Sets the bottom of the FM band for seek. Default is 8750.	0x222E
0x1401	FM_SEEK_BAND_TOP	Sets the top of the FM band for seek. Default is 10790.	0x2A26
0x1402	FM_SEEK_FREQ_SPACING	Selects frequency spacing for FM seek.	0x000A
0x1403	FM_SEEK_TUNE_SNR_THRESHOLD	Sets the SNR threshold for a valid FM Seek/Tune. Default value is 3 dB.	0x0003
0x1404	FM_SEEK_TUNE_RSSI_THRESHOLD	Sets the RSSI threshold for a valid FM Seek/Tune. Default value is 20 dB μ V.	0x0014
0x1500	RDS_INT_SOURCE	Configures RDS interrupt behavior.	0x0000
0x1501	RDS_INT_FIFO_COUNT	Sets the minimum number of RDS groups stored in the receive RDS FIFO required before RDS RECV is set.	0x0000
0x1502	RDS_CONFIG	Configures RDS setting.	0x0000
0x3100	AM_DEEMPHASIS	Sets de-emphasis time constant. Can be set to 50 μ s. De-emphasis is disabled by default.	0x0000
0x3102	AM_CHANNEL_FILTER	Selects the bandwidth of the channel filter for AM reception. The choices are 6, 4, 3, 2.5, 2, 1.8, or 1 kHz. In addition, a power line rejection filter can be applied. The default is the 2 kHz bandwidth filter without power line rejection.	0x0003
0x3103	AM_AUTOMATIC_VOLUME_CONTROL_MAX_GAIN	Selects the maximum gain for automatic volume control.	0x1543
0x3200	AM_RSQ_INTERRUPTS	Configures interrupt related to RSQ metrics. All interrupts are disabled by default.	0x0000
0x3300	AM_SOFT_MUTE_RATE	Sets the rate of attack when entering or leaving soft mute. The default is 278 dB/s.	0x0040
0x3302	AM_SOFT_MUTE_MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB).	0x0008
0x3303	AM_SOFT_MUTE_SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 0 dB, which disables soft mute.	0x0008
0x3400	AM_SEEK_BAND_BOTTOM	Sets the bottom of the AM band for seek. Default is 520.	0x0208

Table 15. Selected Si473x Properties (Continued)

Prop	Name	Description	Default
0x3401	AM_SEEK_BAND_TOP	Sets the top of the AM band for seek.	0x06AE
0x3402	AM_SEEK_FREQ_SPACING	Selects frequency spacing for AM seek. Default is 10 kHz spacing.	0x000A
0x3403	AM_SEEK_SNR_THRESHOLD	Sets the SNR threshold for a valid AM Seek/Tune. If the value is zero, then SNR threshold is not considered when doing a seek. Default value is 5 dB.	0x0005
0x3404	AM_SEEK_RSSI_THRESHOLD	Sets the RSSI threshold for a valid AM Seek/Tune. If the value is zero, then RSSI threshold is not considered when doing a seek. Default value is 25 dBuV.	0x0019
0x4000	RX_VOLUME	Sets the output volume.	0x003F
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently in FM mode.	0x0000

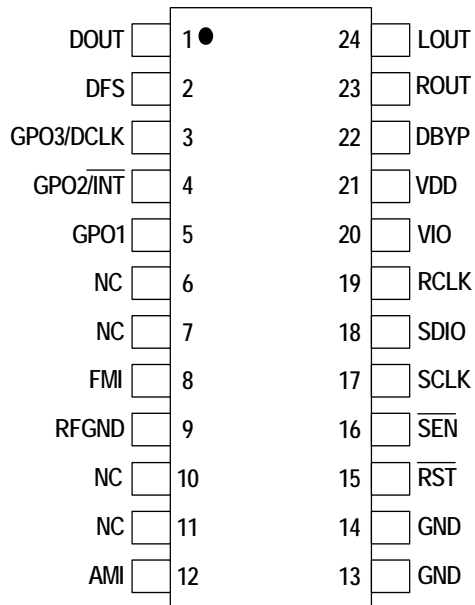
7. Pin Descriptions: Si4730/31-GM



Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM RF inputs. FMI should be connected to the antenna trace.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	AMI	AM RF input. AMI should be connected to the AM antenna.
5	RST	Device reset (active low) input.
6	SEN	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	V _{IO}	I/O supply voltage.
11	V _{DD}	Supply voltage. May be connected directly to battery.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.
13	ROUT	Right audio line output in analog output mode.
14	LOUT	Left audio line output in analog output mode.
15	DOUT	Digital output data in digital output mode.
16	DFS	Digital frame synchronization input in digital output mode.
17	GPO3/DCLK	General purpose output, crystal oscillator, or digital bit synchronous clock input in digital output mode.
18	GPO2/INT	General purpose output or interrupt pin.
19	GPO1	General purpose output.

Si4730/31-C40

8. Pin Descriptions: Si4730/31-GU



Pin Number(s)	Name	Description
1	DOUT	Digital output data in digital output mode.
2	DFS	Digital frame synchronization input in digital output mode.
3	GPO3/DCLK	General purpose output, crystal oscillator, or digital bit synchronous clock input in digital output mode.
4	GPO2/INT	General purpose output or interrupt pin.
5	GPO1	General purpose output.
6,7	NC	No connect. Leave floating.
8	FMI	FM RF inputs. FMI should be connected to the antenna trace.
9	RFGND	RF ground. Connect to ground plane on PCB.
10,11	NC	Unused. Tie these pins to GND.
12	AMI	AM RF input. AMI should be connected to the AM antenna.
13,14	GND	Ground. Connect to ground plane on PCB.
15	RST	Device reset (active low) input.
16	SEN	Serial enable input (active low).
17	SCLK	Serial clock input.
18	SDIO	Serial data input/output.
19	RCLK	External reference oscillator input.
20	V _{IO}	I/O supply voltage.
21	V _{DD}	Supply voltage. May be connected directly to battery.
22	DBYP	Dedicated bypass for V _{DD} and V _{IO} .
23	ROUT	Right audio line output in analog output mode.
24	LOUT	Left audio line output in analog output mode.

9. Ordering Guide

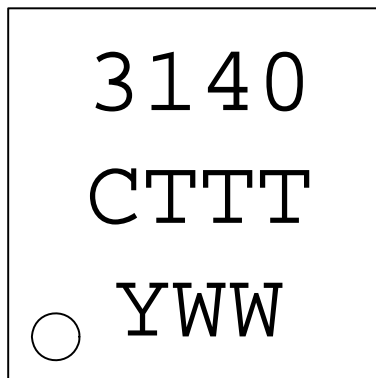
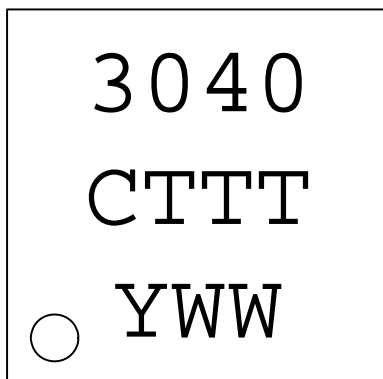
Part Number*	Description	Package Type	Operating Temperature/Voltage
Si4730-C40-GM	AM/FM Broadcast Radio Receiver	QFN Pb-free	-20 to 85 °C 2.7 to 5.5 V
Si4730-C40-GU	AM/FM Broadcast Radio Receiver	SSOP Pb-free	-20 to 85 °C 2.0 to 5.5 V
Si4731-C40-GM	AM/FM Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	-20 to 85 °C 2.7 to 5.5 V
Si4731-C40-GU	AM/FM Broadcast Radio Receiver with RDS/RBDS	SSOP Pb-free	-20 to 85 °C 2.0 to 5.5 V

***Note:** Add an "(R)" at the end of the device part number to denote tape and reel option; 2500 quantity per reel. SSOP devices operate down to $V_{DD} = 2\text{ V}$ at 25 °C.

Si4730/31-C40

10. Package Markings (Top Marks)

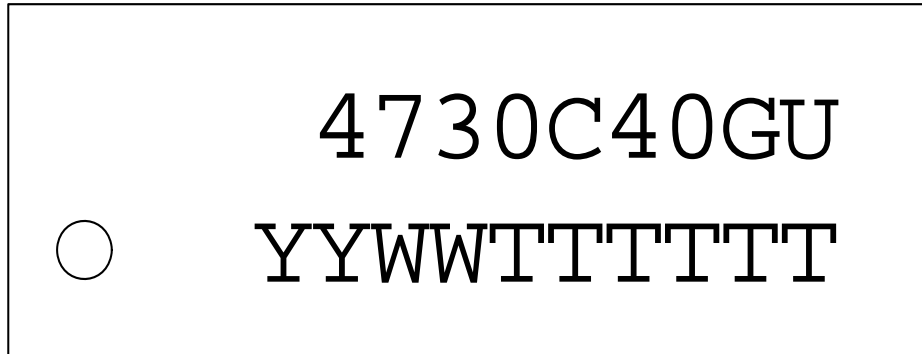
10.1. Si4730/31 Top Mark (QFN)



10.2. Top Mark Explanation (QFN)

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	30 = Si4730, 31 = Si4731.
	Firmware Revision	40 = Firmware Revision 4.0.
Line 2 Marking:	Die Revision	C = Revision C Die.
	TTT = Internal Code	Internal tracking code.
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier.
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and work week of the mold date.

10.3. Si4730/31 Top Mark (SSOP)



10.4. Top Mark Explanation (SSOP)

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	4730 = Si4730; 4731 = Si4731.
	Die Revision	C = Revision C die.
	Firmware Revision	40 = Firmware Revision 4.0.
Line 2 Marking:	YY = Year WW = Work week TTTTTT = Manufacturing code	Assigned by the Assembly House.

Si4730/31-C40

11. Package Outline: Si4730/31 QFN

Figure 14 illustrates the package details for the Si4730/31. Table 16 lists the values for the dimensions shown in the illustration.

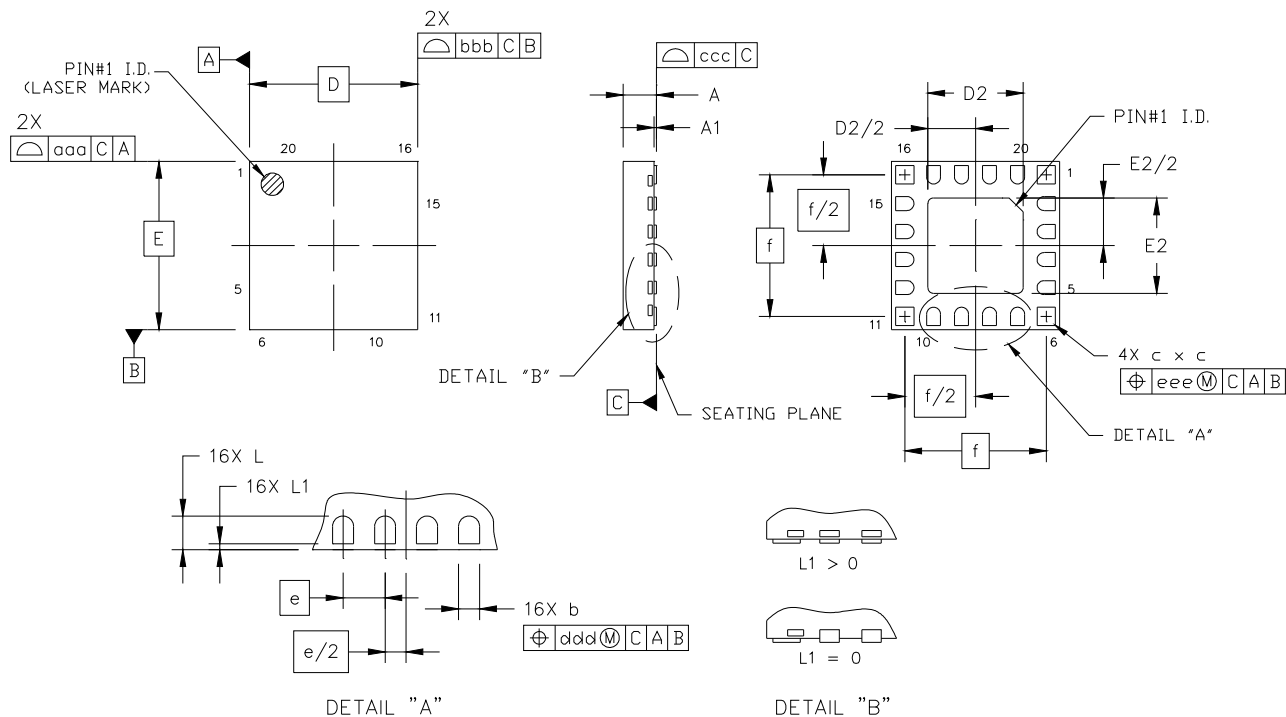


Figure 14. 20-Pin Quad Flat No-Lead (QFN)

Table 16. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D	3.00 BSC		
D2	1.65	1.70	1.75
e	0.50 BSC		
E	3.00 BSC		
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f	2.53 BSC		
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

12. PCB Land Pattern: Si4730/31 QFN

Figure 15 illustrates the PCB land pattern details for the Si4730/31-C40-GM QFN. Table 17 lists the values for the dimensions shown in the illustration.

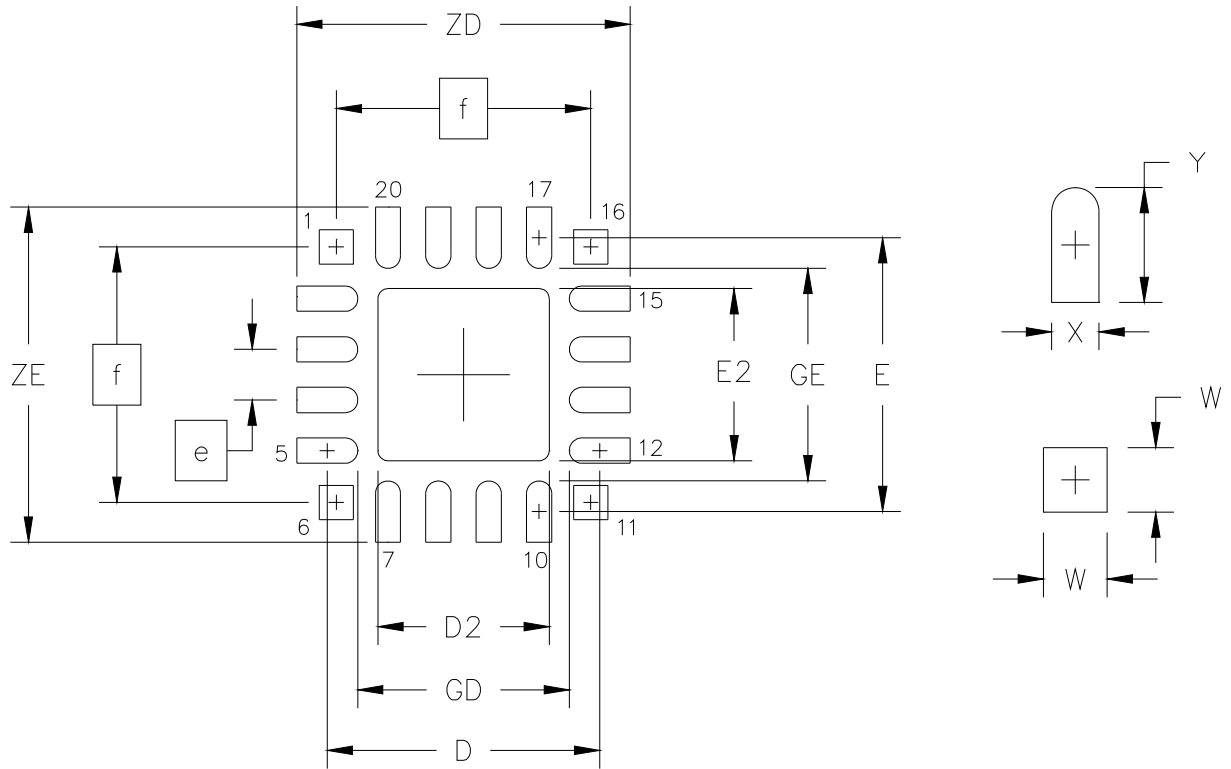


Figure 15. PCB Land Pattern

Table 17. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

13. Package Outline: Si4730/31 SSOP

Figure 16 illustrates the package details for the Si4730/31. Table 18 lists the values for the dimensions shown in the illustration.

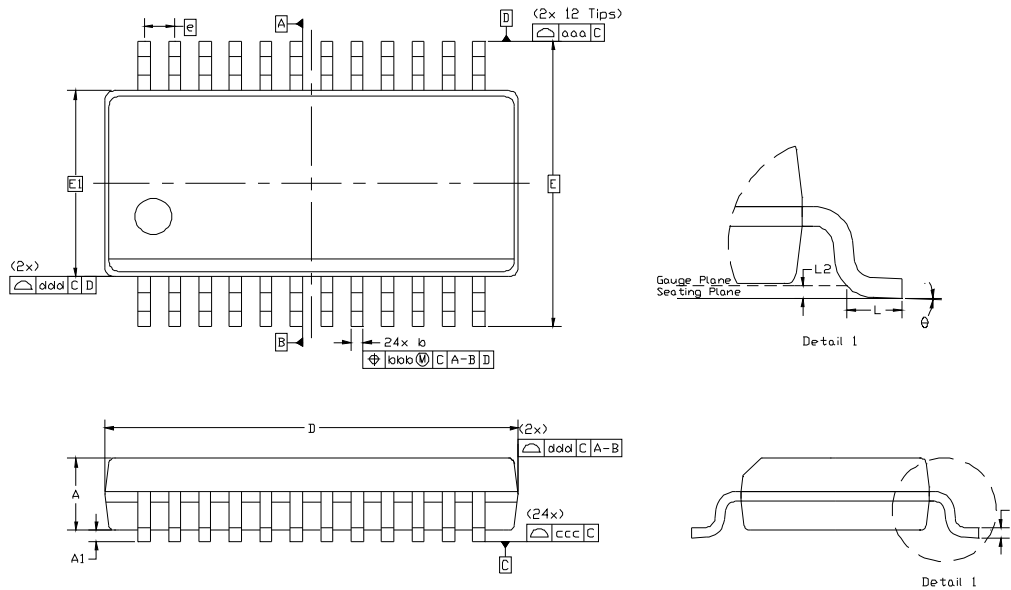


Figure 16. 24-Pin SSOP

Table 18. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.20		
bbb	0.18		
ccc	0.10		
ddd	0.10		
Notes:			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AE.			
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

14. PCB Land Pattern: Si4730/31 SSOP

Figure 17 illustrates the PCB land pattern details for the Si4730/31-C40-GU SSOP. Table 19 lists the values for the dimensions shown in the illustration.

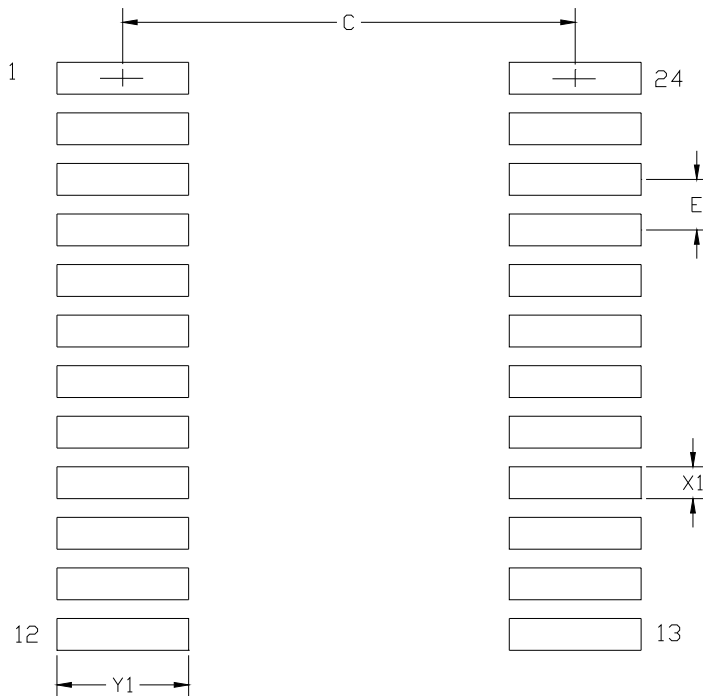


Figure 17. PCB Land Pattern

Table 19. PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.40
E	0.65 BSC	
X1	0.35	0.45
Y1	1.55	1.75
General:		
1. All dimensions shown are in millimeters (mm) unless otherwise noted.		
2. This land pattern design is based on the IPC-7351 guidelines.		
Solder Mask Design:		
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.		
Stencil Design:		
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.		
5. The stencil thickness should be 0.125 mm (5 mils).		
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.		
Card Assembly:		
7. A No-Clean, Type-3 solder paste is recommended.		
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

15. Additional Reference Resources

Contact your local sales representatives for more information or to obtain copies of the following references:

- EN55020 Compliance Test Certificate
- AN332: Si47xx Programming Guide
- AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines
- AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 0.7

- Updated Table 3, “DC Characteristics,” on page 5.
- Updated Table 9, “FM Receiver Characteristics^{1,2},” on page 12.
- Updated Table 15, “Selected Si473x Properties,” on page 27.
- Updated Table 10.4, “Top Mark Explanation (SSOP),” on page 33.

Revision 0.7 to Revision 0.71

- V_{IO} minimum changed from 1.5 V to 1.85 V.

Revision 0.71 to Revision 1.0

- Updated patent information on page 1.
- Pin 22 changed from “GND” to “DBYP.”
- Updated Table 1 on page 4.
- Updated Table 3 on page 5.
- Updated Table 9 on page 12.
- Updated Table 11 on page 15.
- Updated “3. Typical Application Schematic (SSOP)” on page 18.
- Updated “4. Bill of Materials (QFN/SSOP)” on page 19.
- Updated “8. Pin Descriptions: Si4730/31-GU” on page 30.
- Updated “9. Ordering Guide” on page 31.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.



400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: FMinfo@silabs.com
Internet: www.silabs.com

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.
Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View SI4731-C40-GU on WIN SOURCE](#)
-  [Skyworks Solutions Inc. Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management