



**THE DATASHEET OF  
MAX1604EAI**





# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

## General Description

The MAX1601/MAX1604 DC power-switching ICs contain a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two CardBus or PC Card host sockets. Key features include ultra-low-resistance switches, small packaging, soft-switching action, and compliance with PCMCIA specifications for 3V/5V switching. 3.3V-only power switching for fast, 32-bit CardBus applications is supported in two ways: stiff, low-resistance 3.3V switches allow high 3.3V load currents (up to 1A); and completely independent internal charge pumps let the 3.3V switch operate normally, even if the +5V and +12V supplies are disconnected or turned off to conserve power. The internal charge pumps are regulating types that draw reduced input current when the VCC switches are static. Also, power consumption is automatically reduced to 10 $\mu$ A max when the switches are programmed to high-Z or GND states over the serial interface, unlike other solutions that may require a separate shutdown-control input.

Other key features include guaranteed specifications for output current limit level, and guaranteed specifications for output rise/fall times (in compliance with PCMCIA specifications). Reliability is enhanced by thermal-overload protection, accurate current limiting, an overcurrent-fault flag output, undervoltage lockout, and extra ESD protection at the VCC/VPP outputs. The SMBus serial interface is flexible, and can tolerate logic input levels in excess of the positive supply rail.

The MAX1604 and MAX1601 are identical, except for the MAX1604's VY switch, which has roughly three-times the on-resistance (typically 140m $\Omega$ ). The MAX1601/MAX1604 fit two complete CardBus/PCMCIA switches into a space-saving, narrow (0.2in. or 5mm wide) SSOP package.

## Applications

Desktop Computers	Data Loggers
Notebook Computers	Digital Cameras
Docking Stations	Printers
Handy-Terminals	PCMCIA Read/Write Drives

**Pin Configuration appears on last page.**

SMBus is a trademark of Intel Corp.

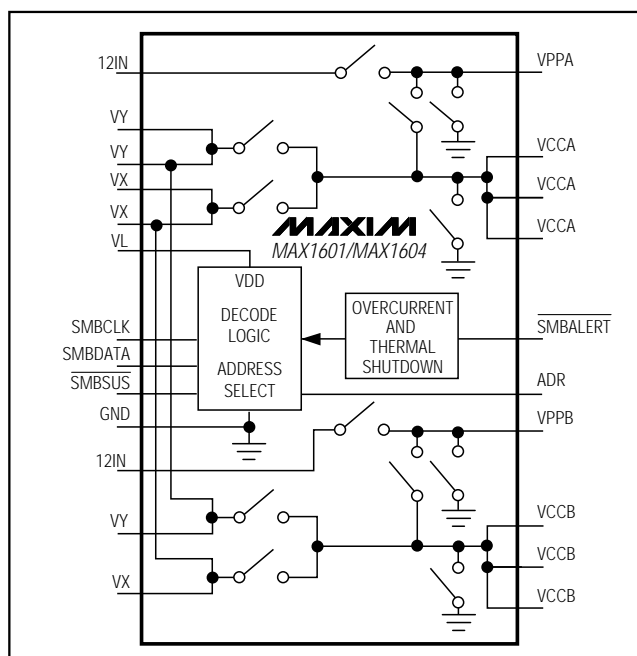
## Features

- ◆ Supports Two CardBus Sockets
- ◆ 1A, 0.08 $\Omega$  Max VY VCC Switch (MAX1601 only)  
1A, 0.14 $\Omega$  Max VX VCC Switch
- ◆ Soft Switching for Low Inrush Surge Current
- ◆ Overcurrent Protection
- ◆ Overcurrent/Thermal-Fault Flag Output
- ◆ Thermal Shutdown at T<sub>j</sub> = +150°C
- ◆ Independent Internal Charge Pumps
- ◆ Break-Before-Make Switching Action
- ◆ 10 $\mu$ A Max Standby Supply Current
- ◆ 5V and 12V Not Required for Low-RDS(ON) 3.3V Switching
- ◆ Complies with PCMCIA 3V/5V Switching Specifications
- ◆ Super-Small, 28-Pin SSOP Package (0.2in. or 5mm wide)
- ◆ System Management Bus (SMBus) Serial Interface

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1601EAI	-40°C to +85°C	28 SSOP
MAX1604EAI	-40°C to +85°C	28 SSOP

## Simplified Block Diagram



# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

## ABSOLUTE MAXIMUM RATINGS

Inputs/Outputs to GND (VL, VX, VY, VCCA, VCCB) (Note 1).....	-0.3V, +6V	VCCA, VCCB Short Circuit to GND.....	Continuous
VPP Inputs/Outputs to GND (12INA, 12INB, VPPA, VPPB) (Note 1) .....	-0.3V, +15V	VPPA, VPPB Short Circuit to GND.....	Continuous
Inputs and Outputs to GND (SMBCLK, SMBDATA, SMBSUS, SMBALERT) (Note 1) .....	-0.3V, +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C) SSOP (derate 9.52mW/°C above +70°C) .....	762mW
ADR Input to GND .....	-0.3V, (VL + 0.3V)	Operating Temperature Range MAX1601EAI/MAX1604EAI .....	-40°C to +85°C
VCCA, VCCB Output Current (Note 2).....	4A	Storage Temperature Range .....	-65°C to +160°C
VPPA, VPPB Output Current (Note 2) .....	250mA	Lead Temperature (soldering, 10sec) .....	+300°C

**Note 1:** There are no parasitic diodes between any of these pins, so there are no power-up sequencing restrictions (for example, logic input signals can be applied even if all of the supply voltage inputs are grounded).

**Note 2:** VCC and VPP outputs are internally current-limited to safe values. See the *Electrical Characteristics* table.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, T<sub>A</sub> = 0°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER-SUPPLY SECTION</b>					
Input Voltage Range	VX, VY or VL	3.0		5.5	V
	12INA, 12INB	11		13	
Undervoltage Lockout Threshold	VL falling edge	2.4	2.5	2.8	V
	12IN falling edge	1.8	3.0		
	12IN rising edge	5	8	10	
	VX, VY falling edge	1.4	2.5	2.8	
Standby Supply Current	VX or VY, all switches 0V or high-Z, control inputs = 0V or VL, T <sub>A</sub> = +25°C			1	μA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VL, no VCC loads		20	100	μA
VX Quiescent Supply Current	Any combination of VX switches on, control inputs = 0V or high-Z, no VCC loads		20	100	μA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL, T <sub>A</sub> = +25°C			1	μA
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads		15	100	μA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL, T <sub>A</sub> = +25°C		4	10	μA
VL Quiescent Supply Current	Any combination of switches on		25	150	μA
VL Fall Rate	When using VL as shutdown pin (Note 3)			0.05	V/μs
<b>VCC SWITCHES</b>					
Operating Output Current Range	VCCA or VCCB, VX = VY = 3V to 5.5V	0		1	A
On-Resistance, VY Switches	12INA = 12INB = 0V to 13V, VY = 3V, VX = 0V to 5.5V, I <sub>SWITCH</sub> = 1A, T <sub>A</sub> = +25°C	MAX1601	0.06	0.08	Ω
		MAX1604	0.14	0.24	
On-Resistance, VX Switches	12INA = 12INB = 0V to 13V, VX = 4.5V, VY = 0V to 5.5V, I <sub>SWITCH</sub> = 1A, T <sub>A</sub> = +25°C		0.10	0.14	Ω

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

MAX1601/MAX1604

## ELECTRICAL CHARACTERISTICS (continued)

(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, TA = 0°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Limit	VCCA or VCCB	1.2		4.0	A
Output Sink Current	VCCA or VCCB < 0.4V, programmed to 0V state	20			mA
Output Leakage Current	VCCA or VCCB forced to 0V, high-Z state, TA = +25°C			10	μA
Output Propagation Delay Plus Rise Time	VCCA or VCCB, 0V to VX or VY, CL = 30μF, RL = 25Ω, 50% of input to 90% of output, TA = +25°C		2	10	ms
Output Rise Time	VCCA or VCCB, 0V to VX or VY, CL = 1μF, RL = open circuit, 10% to 90% points, TA = +25°C	100	1200		μs
Output Propagation Delay Plus Fall Time	VCCA or VCCB, VX or VY to 0V, CL = 30μF, RL = open circuit, 50% of input to 10% of output, TA = +25°C		60	100	ms
Output Fall Time	VCCA or VCCB, VX or VY to 0V, CL = 1μF, RL = 25Ω, 90% to 10% points		6		ms
<b>VPP SWITCHES</b>					
Operating Output Current Range	VPPA or VPPB	0		120	mA
On-Resistance, 12V Switches	12IN = 11.6V, ISWITCH = 100mA, TA = +25°C		0.70	1	Ω
On-Resistance, VPP = VCC Switches	Programmed to VX (5V) or VY (3.3V), TA = +25°C		1	3	Ω
Output Current Limit	VPPA or VPPB, programmed to 12V	130	200	260	mA
Output Sink Current	VPPA or VPPB < 0.4V, programmed to 0V state	10			mA
Output Leakage Current	VPPA or VPPB forced to 0V, high-Z state, TA = +25°C			10	μA
Output Propagation Delay Plus Rise Time	VPPA or VPPB, 0V to 12IN_, CL = 0.1μF, 50% of input to 90% of output, TA = +25°C		1.2	30	ms
Output Rise Time	VPPA or VPPB, 0V to 12IN_, CL = 0.1μF, 10% to 90% points, TA = +25°C	100	800		μs
Output Propagation Delay Plus Fall Time	VPPA or VPPB, 12IN_ to 0V, CL = 0.1μF, 50% of input to 10% of output, TA = +25°C		9	60	ms
Output Fall Time	VPPA or VPPB, 12IN_ to 0V, CL = 0.1μF, 90% to 10% points		1		ms
<b>INTERFACE AND LOGIC SECTION</b>					
SMBALERT Signal Propagation Delay	VCC_ or VPP_, load step to SMBALERT output, 50% point to 50% point (Note 3)		3		μs
SMBALERT Output Low Voltage	ISINK = 1mA, low state			0.4	V
SMBALERT Output Leakage Current	VSMBALERT = 5.5V, high state	-0.1		0.1	μA
Thermal Shutdown Threshold	Hysteresis = +20°C (Note 4)		150		°C
Logic Input Low Voltage	SMBSUS, SMBCLK, SMBDATA			0.8	V
Logic Input High Voltage	SMBSUS, SMBCLK, SMBDATA	2.2			V
Logic Output Low Voltage	SMBDATA, ISINK = 4mA			0.4	V

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

MAX1601/MAX1604

## ELECTRICAL CHARACTERISTICS (continued)

(VL = VY = 3.3V, VX = 5V, I2INA = I2INB = 12V, TA = 0°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMB Input Capacitance	SMBSUS, SMBCLK, SMBDATA		5		pF
SMBCLK Clock Frequency	SMBus spec = 10kHz min	DC		100	kHz
SMBCLK Clock Low Time	tLOW 10% to 10% points	4.7			μs
SMBCLK Clock High Time	tHIGH 90% to 90% points	4			μs
SMB Repeated Start-Condition Setup Time	tSU:STA 90% to 90% points	250			ns
SMB Start-Condition Hold Time	tHD:STA 10% of SMBDATA to 90% of SMBCLK	4			μs
SMB Stop-Condition Setup Time	tSU:STO 90% of SMBCLK to 10% of SMBDATA	4			μs
SMB Data Valid to SMBCLK Rising-Edge Time	tSU:DAT 10% or 90% of SMBDATA to 10% of SMBCLK	500			ns
SMB Data Hold Time	tHD:DAT (Note 5)	0			ns
Bus Free Time	tBUF between start and stop conditions	4.7			μs
ADR Input Low Voltage				0.6	V
ADR Input High Voltage		1.5			V
Logic Input Bias Current	ADR, SMBSUS, SMBCLK, SMBDATA	-1		1	μA
SCL Fall to SDA Valid (Master Clocking-In Data)			100	1000	ns
Start-Condition Setup		4.7			μs

**Note 3:** Not production tested.

**Note 4:** Thermal limit not active in standby state (all switches programmed to GND or high-Z state).

**Note 5:** A transition must internally provide at least a hold time in order to bridge the undefined region (300ns max) of the falling edge of SMBCLK.

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

MAX1601/MAX1604

## ELECTRICAL CHARACTERISTICS

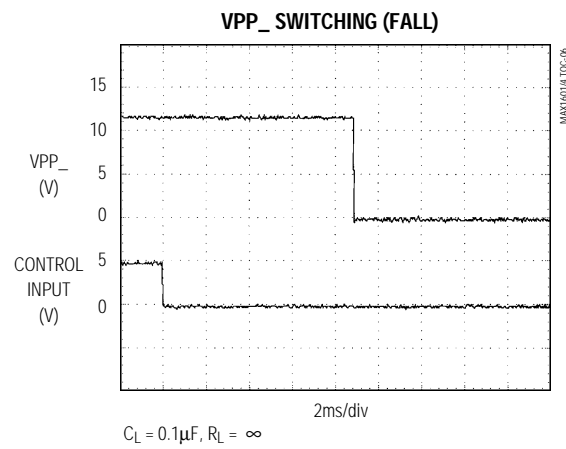
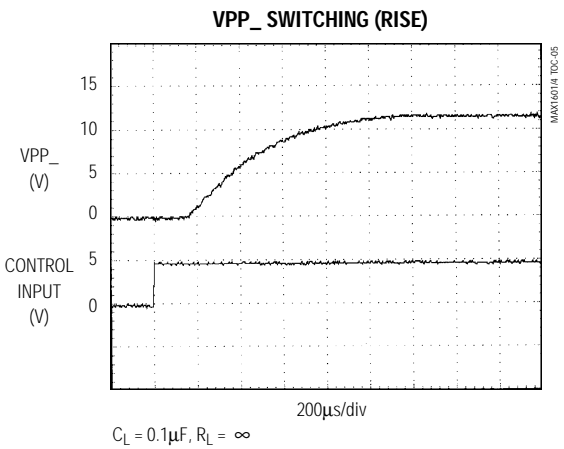
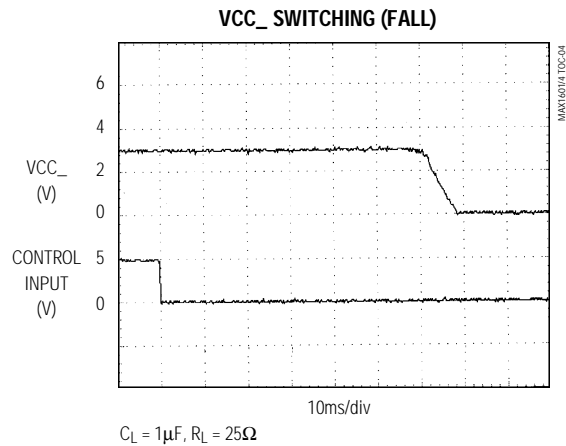
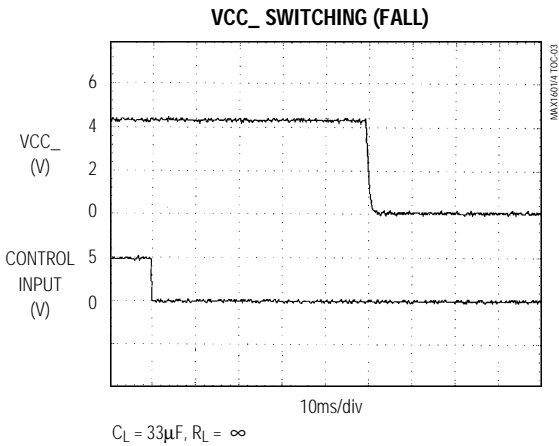
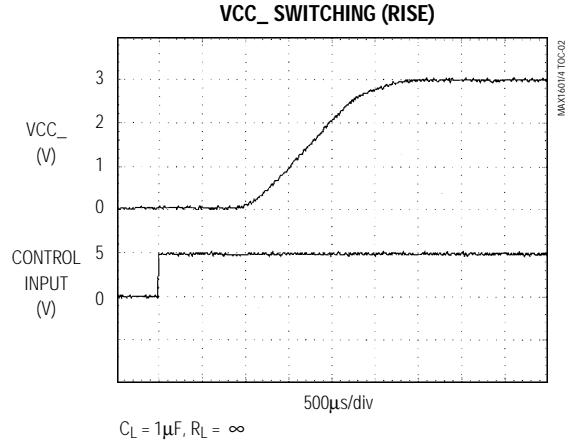
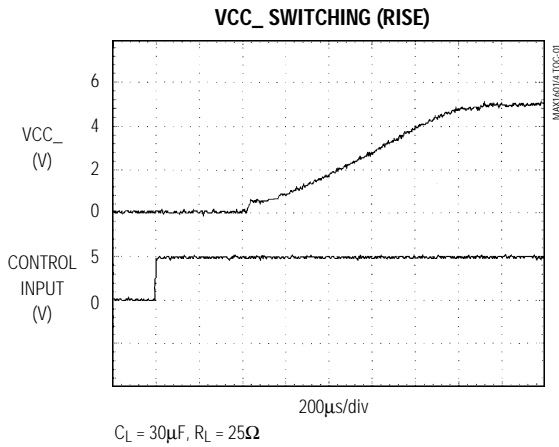
(VL = VY = 3.3V, VX = 5V, 12INA = 12INB = 12V, TA = -40°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER-SUPPLY SECTION</b>					
Input Voltage Range	VX, VY or VL	3.0		5.5	V
	12INA, 12INB	11		13	
Undervoltage Lockout Threshold	VL falling edge, hysteresis = 1%	2.3		2.9	V
	12IN falling edge	1.8			
	12IN rising edge	5		10	
	VX, VY falling edge	1.4		2.9	
Standby Supply Current	VX or VY, all switches 0V or high-Z, control inputs = 0V or VL			15	μA
VY Quiescent Supply Current	Any combination of VY switches on, control inputs = 0V or VL, no VCC loads			100	μA
VX Quiescent Supply Current	Any combination of VX switches on, control inputs = 0V or high-Z, no VCC loads			100	μA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL			15	μA
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads			100	μA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL			15	μA
VL Quiescent Supply Current	Any combination of switches on			150	μA
<b>INTERFACE AND LOGIC SECTION</b>					
$\overline{\text{SMBALERT}}$ Output Low Voltage	ISINK = 1mA, low state			0.4	V
Logic Input Low Voltage	SMBCLK, SMBDATA, $\overline{\text{SMBSUS}}$			0.8	V
Logic Input High Voltage	SMBCLK, SMBDATA, $\overline{\text{SMBSUS}}$	2.2			V
Logic Output Low Voltage	SMBDATA, ISINK = 4mA			0.4	V
ADR Input Low Voltage				0.6	V
ADR Input High Voltage		1.5			V

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

## Typical Operating Characteristics

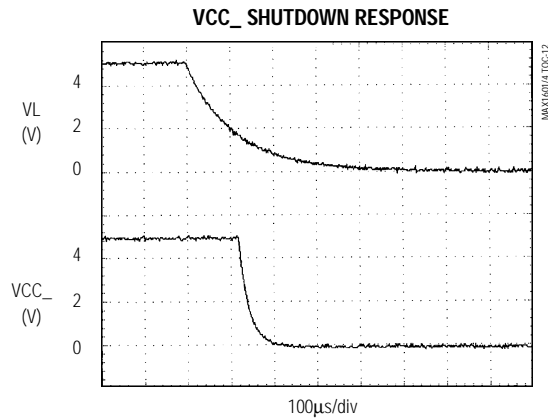
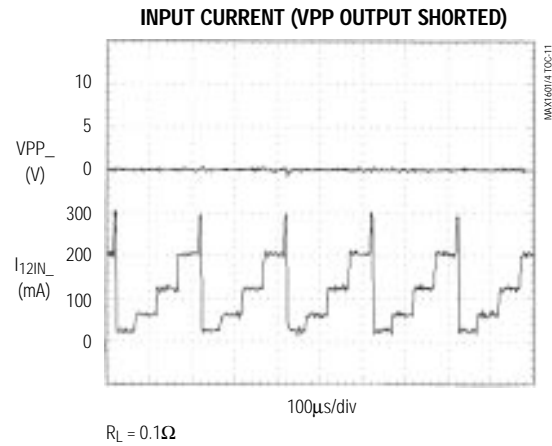
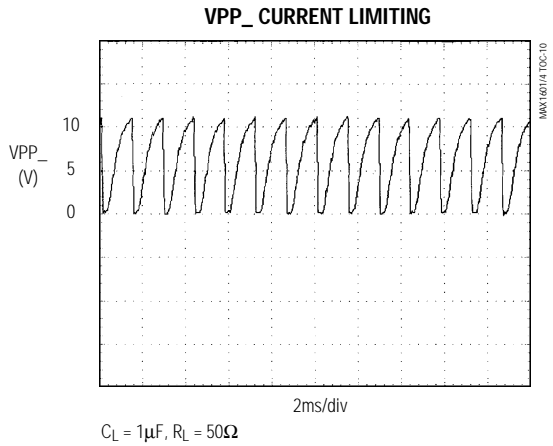
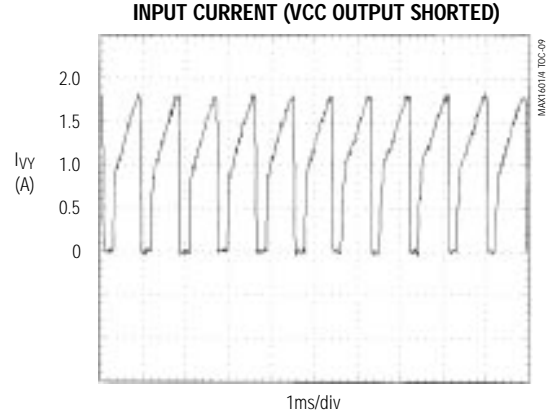
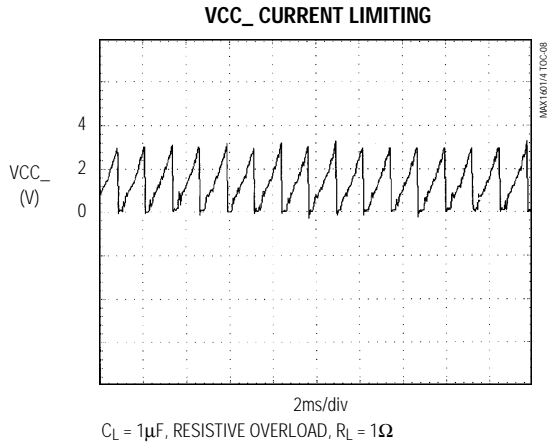
(VL = VY = 3.3V, VX = 5V, 12IN, TA = +25°C, unless otherwise noted.)



# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

MAX1601/MAX1604

Typical Operating Characteristics (continued)  
 (VL = VY = 3.3V, VX = 5V, I2IN, TA = +25°C, unless otherwise noted.)

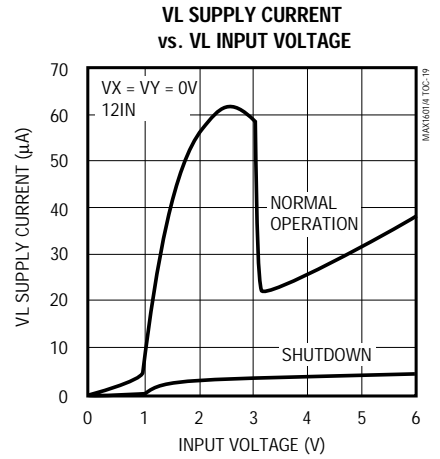
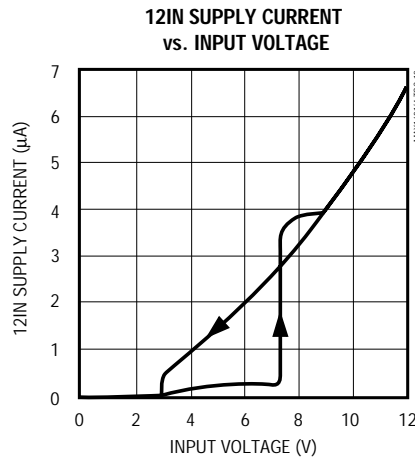
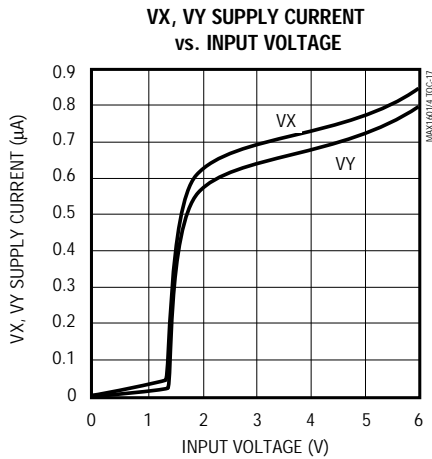
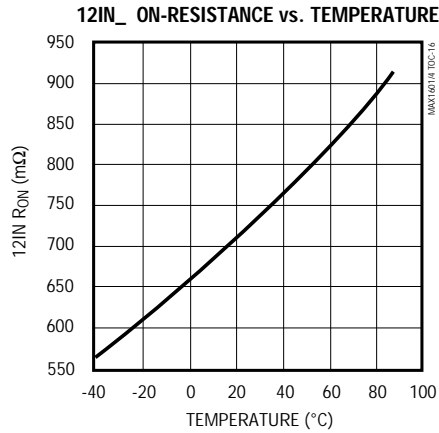
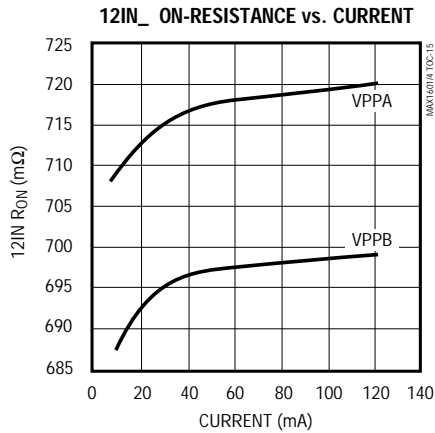
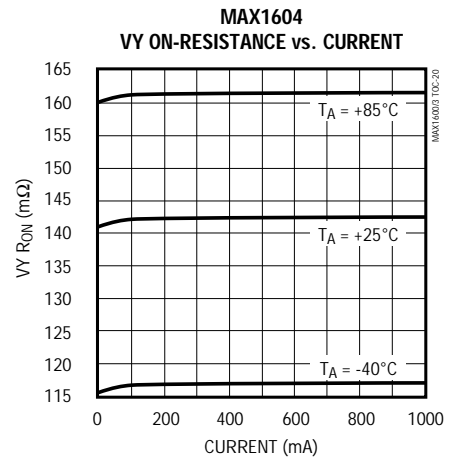
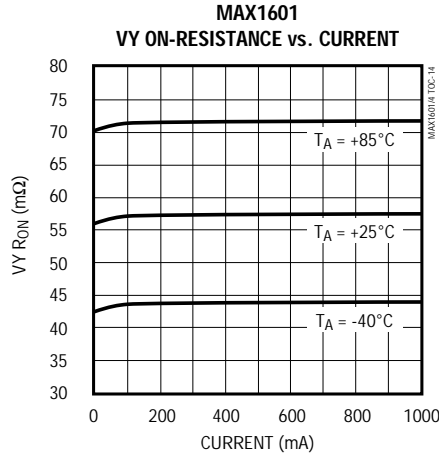
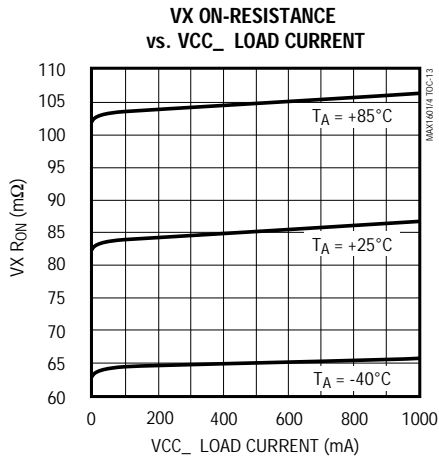


CIRCUIT OF FIGURE 2

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

## Typical Operating Characteristics (continued)

(VL = VY = 3.3V, VX = 5V, 12IN, TA = +25°C, unless otherwise noted.)



# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

## Pin Description

MAX1601/MAX1604

PIN	NAME	FUNCTION
1, 25	GND	Ground
2, 3, 26, 27	N.C.	No internal connection
4	12INA	+12V Supply Voltage Input, internally connects to channel A VPP switch. Tie to VPPA if not used.
5	VPPA	Channel A VPP Output
6, 8, 10	VX	VX Supply-Voltage Inputs. VX pins must be connected together. Input range is 3V to 5.5V. VX is normally connected to 5V.
7, 22, 24	VCCA	Channel A VCC Outputs
9, 18, 20	VCCB	Channel B VCC Outputs
11	VPPB	Channel B VPP Output
12	12INB	+12V Supply Voltage Input, internally connects to channel B VPP switch. Tie to VPPB if not used.
13	ADR	Address Input, sets SMBus address location. See Table 1 for address selection.
14	$\overline{\text{SMBSUS}}$	SMBus Suspend-Mode Control Input. The device will execute commands previously stored in the normal-mode register if $\overline{\text{SMBSUS}}$ is high, or will execute commands previously stored in the suspend-mode register if $\overline{\text{SMBSUS}}$ is low.
15	SMBCLK	SMBus Clock Input
16	SMBDATA	SMBus Data Input/Output, open drain
17	$\overline{\text{SMBALERT}}$	Fault-Detection Interrupt Output. $\overline{\text{SMBALERT}}$ goes low if either channel VCC or VPP switch is current limiting or undervoltage lockout, or if the thermal protection circuit is activated. $\overline{\text{SMBALERT}}$ is an open-drain output that requires an external pull-up resistor.
19, 21, 23	VY	VY Supply-Voltage Inputs. VY pins must be connected together. Input range is 3V to 5.5V. VY is normally connected to 3V.
28	VL	Logic Supply-Voltage Inputs. Connect to the +3.3V or +5V host system supply. VL can be supplied via the output of a CMOS-logic gate to produce an overriding shutdown. When used as a shutdown input, VL should have a 1k $\Omega$ series resistor with a 0.1 $\mu$ F capacitor to ground (Figure 2). Note that VL must be greater than undervoltage lockout for any switches to be turned on.

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

MAX1601/MAX1604

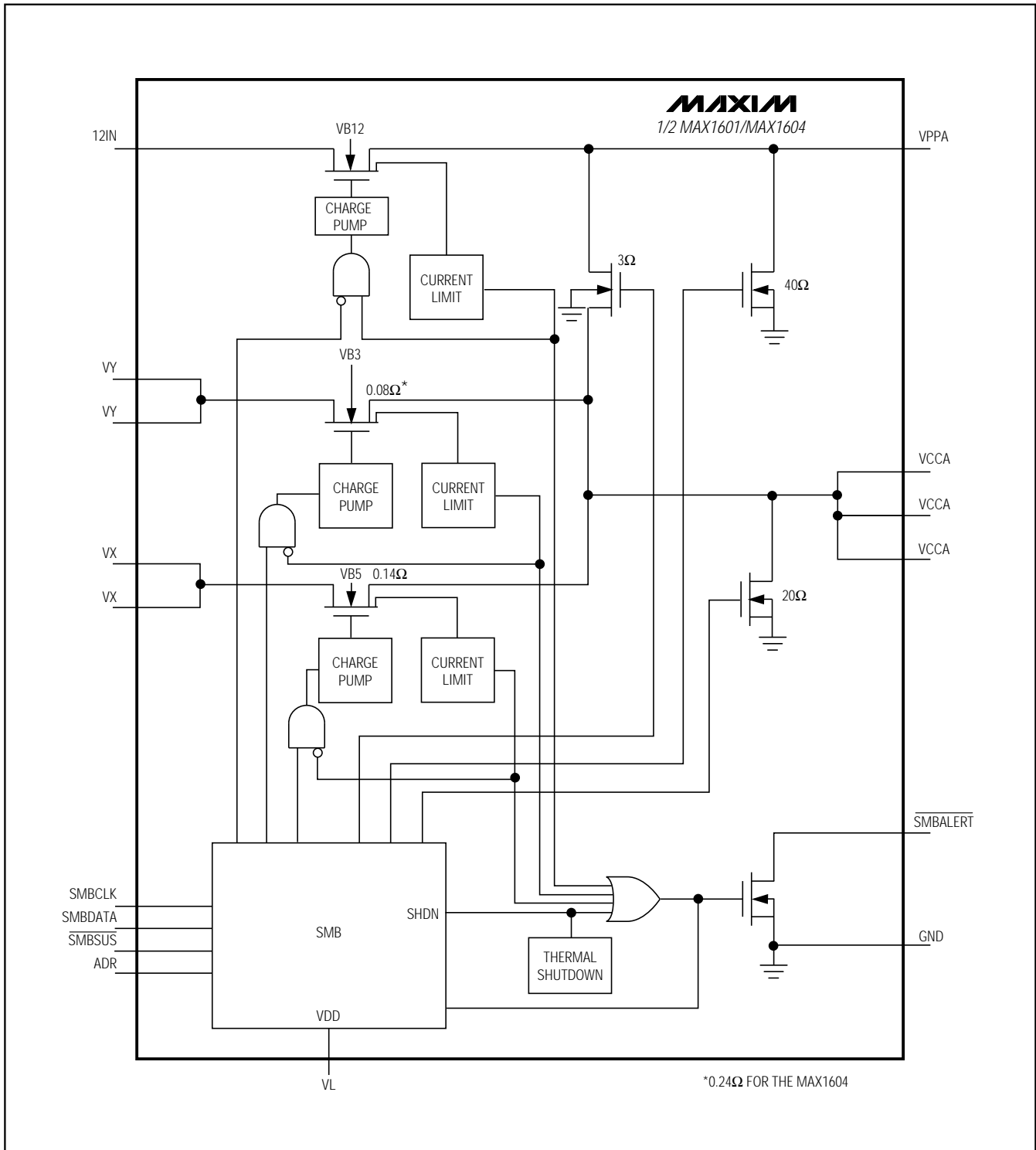


Figure 1. Functional Diagram (one channel of two)

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

MAX1601/MAX1604

## Detailed Description

The MAX1601/MAX1604 power-switching ICs contain a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two Cardbus or PC Card host sockets. The MAX1601/MAX1604 differ only in the VY switch on-resistance. Figure 1 is the detailed block diagram.

The power-input pins (VY, VX, 12IN<sub>-</sub>) are completely independent. Low inrush current is guaranteed by controlled switch rise times. VCC's 100 $\mu$ s minimum output rise time is 100% tested with a 1 $\mu$ F capacitive load, and VPP's 1ms minimum rise time is guaranteed with a 0.1 $\mu$ F load. These respective capacitive loads are chosen as worst-case card-insertion parameters. The internal switching control allows VCC and VPP rise times to be controlled, and makes them nearly independent of resistive and capacitive loads (see rise-time photos in the *Typical Operating Characteristics*). Fall times are a function of loading, and are compensated by internal circuitry.

Power savings is automatic: internal charge pumps draw very low current when the VCC switches are static. Standby mode reduces switch supply current to 1 $\mu$ A. Driving the VL pin low with an external logic gate (master shutdown) reduces total supply current to 1 $\mu$ A (Figure 2).

### Operating Modes

The MAX1601/MAX1604 have three operating modes: normal, standby, and shutdown. Normal mode supplies the selected outputs with their appropriate supply voltages. Standby mode places all switches at ground, high impedance, or a combination of the two. Shutdown mode turns all switches off, and puts the VCC and VPP outputs into a high-impedance state. Pull VL low to enter shutdown mode. To ensure a 0.05V/ $\mu$ s fall rate on VL, use a 1k $\Omega$  series resistor and a 0.1 $\mu$ F capacitor to ground (Figure 2).

### Overcurrent Protection

Peak detecting circuitry protects both the VCC and VPP switches against overcurrent conditions. When current through any switch exceeds the internal current limit (4A for VCC switches and 200mA for VPP switches), the switch turns off briefly, then turns on again at the controlled rise rate. If the overcurrent condition lasts more than 2 $\mu$ s, the SMBALERT output latches

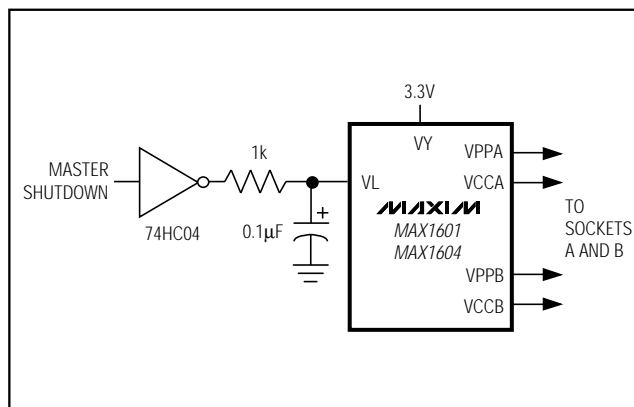


Figure 2. Master Shutdown Circuit

low. A continuous short-circuit condition results in a pulsed output current until thermal shutdown is reached. SMBALERT is open-drain and requires an external pull-up resistor.

### Thermal Shutdown

If the IC junction temperature rises above +150°C, the thermal shutdown circuitry opens all switches, including the GND switches, and SMBALERT is pulled low. When the temperature falls below +130°C, the switches turn on again at the controlled rise rate. If the overcurrent condition remains, the part cycles between thermal shutdown and overcurrent.

### Undervoltage Lockout

If the VX or VY switch input voltage drops below 1.5V, the associated switch turns off and SMBALERT goes low. For example, if VY is 3.3V and VX is 0V, and if the interface controller selects VY, the VCCA output will be 3.3V. If VX is selected, VCCA changes to a high-impedance output and SMBALERT goes low.

When a voltage is initially applied to 12IN<sub>-</sub>, it must be greater than 8V to allow the switch to operate. Operation continues until the voltage falls below 2V (the VPP output is high impedance).

When VL drops to less than 2.3V, all switches are turned off and the VCC and VPP outputs are high impedance.

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

## SMBus™ Interface Operation

The SMBus serial interface is a two-wire interface with multi-mastering capability, intended to control low-speed peripheral devices in low-power portable equipment applications. SMBus is similar to I<sup>2</sup>C™ and AccessBus, but has slightly different logic threshold voltage levels, different fixed addresses, and a suspend-mode register capability. To obtain a complete set of specifications on the SMBus interface, call Intel at (800) 253-3696 and ask for product code SBS5220.

### SMBus Addressing

These dual-channel PC Card switch devices respond to two of four different addresses, depending on the state of the ADR address pin. Normal writing to the device is done by transmitting one of four addresses, followed by a single data byte, to program the channel selected. Write transmissions to the interrupt pointer address are not supported by these devices. Reading from the device is done by transmitting one of two addresses cor-

responding to either the A channel address (which will provide data about faults for both A and B channels) or to the interrupt pointer address (discussed later).

The normal start condition consists of a high-to-low transition on SMBDATA while SMBCLK is high. The 7-bit address is followed by a bit that designates a read or write operation: high = read, low = write. If the 7-bit address matches one of the supported function addresses, the IC issues an acknowledge pulse by pulling the SMBDATA line low. If the address is not valid, the IC stays off of the bus and ignores any data on the bus until a new start condition is detected. Once the IC receives a valid address that includes a write bit, it expects to receive one additional byte of data. If a stop condition or new start condition is detected before a complete byte of data is clocked in, the IC interprets this as an error and all of the data is rejected and lost. SMBDATA and SMBCLK are Schmitt triggered and can accommodate slower edges. However, rising edges should still be faster than 1μs, and falling edges should be faster than 300ns.

**Table 1. SMBus Addressing**

SMB ADDRESS	ADR PIN	WRITE FUNCTION	READ FUNCTION
0001100	Don't care	N/A	Interrupt Pointer
1010000	Grounded	Channel A	Channel A/B faults
1010001	Grounded	Channel B	Channel A/B faults
1010010	Tied to VL	Channel A	Channel A/B faults
1010011	Tied to VL	Channel B	Channel A/B faults

### SMBus Write Operations

If the IC receives a valid address immediately followed by a write bit, the IC becomes a slave receiver. The slave IC generates a first acknowledge after the address and write bit, and a second acknowledge after the command byte. A stop condition following the command (data) byte causes immediate execution of the command, unless the data included a low SUS/OP bit. If the data included a low SUS/OP bit, the command is stored in the suspend-mode register and is executed only when the SMBSUS pin is pulled low (Figure 3).

**Table 2. Command Format for Channel A Write Operations (address 1010000 or 1010010)**

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: high = operation, low = suspend.
6	VCCAON	0	Turns on VCCA when high, pulls VCCA to GND when low.
5	VCCA3/5	0	If VCCA is on, a high connects VY to VCCA, and a low connects VX to VCCA.
4	VCCAHiZ	0	Puts VCCA in a high-impedance state when high. Overrides VCCAON.
3	VPPAON	0	Turns on VPPA when high, pulls VPPA to GND when low.
2	VPPAPGM	0	If VPPA is on, a high connects VPPA to I2INA, and a low connects VPPA to VCCA.
1	VPPAHiZ	0	Puts VPPA in a high-impedance state when high. Overrides VPPAON.
0 (LSB)	MASKFLT	0	Masks fault interrupts from both channel A and channel B when high.

I<sup>2</sup>C is a trademark of Philips Corp.

SMBus is a trademark of Intel Corp.

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MAX1601/MAX1604

**Table 3. Command Format for Channel B Write Operations (address 1010001 or 1010011)**

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: high = operation, low = suspend.
6	VCCBON	0	Turns on VCCB when high, pulls VCCB to GND when low.
5	VCCB3/5	0	If VCCB is on, a high connects VY to VCCB, and a low connects VX to VCCB.
4	VCCBHIZ	0	Puts VCCB in a high-impedance state when high. Overrides VCCBON.
3	VPPBON	0	Turns on VPPB when high, pulls VPPB to GND when low.
2	VPPBPGM	0	If VPPB is on, a high connects VPPB to 12INB, and a low connects VPPB to VCCB.
1	VPPBHIZ	0	Puts VPPB in a high-impedance state when high. Overrides VPPBON.
0 (LSB)	RFU	0	Reserved for future use.

**Table 4. Read Format for Interrupt Pointer Address (0001100)**

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	ADD7	0	ADD7 to ADD1 provide a return address for any interrupt query. For these devices, the return addresses are: 1010000 = Channel A, ADD = low 1010001 = Channel B, ADD = low 1010010 = Channel A, ADD = high 1010011 = Channel B, ADD = high
6	ADD6	0	
5	ADD5	0	
4	ADD4	0	
3	ADD3	0	
2	ADD2	0	
1	ADD1	0	
0 (LSB)	ADD0	0	

**Table 5. Read Format for Power Switch Address (1010000 or 1010010)**

BIT	NAME	POR STATE	LATCHED?	FUNCTION
7 (MSB)	CATFAULT	0	Y	Indicates catastrophic (thermal or undervoltage lockout) fault when high.
6	FAULT1	0	Y	Indicates VCCA overcurrent/undervoltage lockout when high.
5	FAULT2	0	Y	Indicates VPPA overcurrent/undervoltage lockout when high.
4	FAULT3	0	Y	Indicates VCCB overcurrent/undervoltage lockout when high.
3	FAULT4	0	Y	Indicates VPPB overcurrent/undervoltage lockout when high.
2	SIG/DUAL	0	N	Indicates dual part (single-channel devices would read 1).
1	RFU	0	N	Reserved for future use.
0 (LSB)	RFU	0	N	Reserved for future use.

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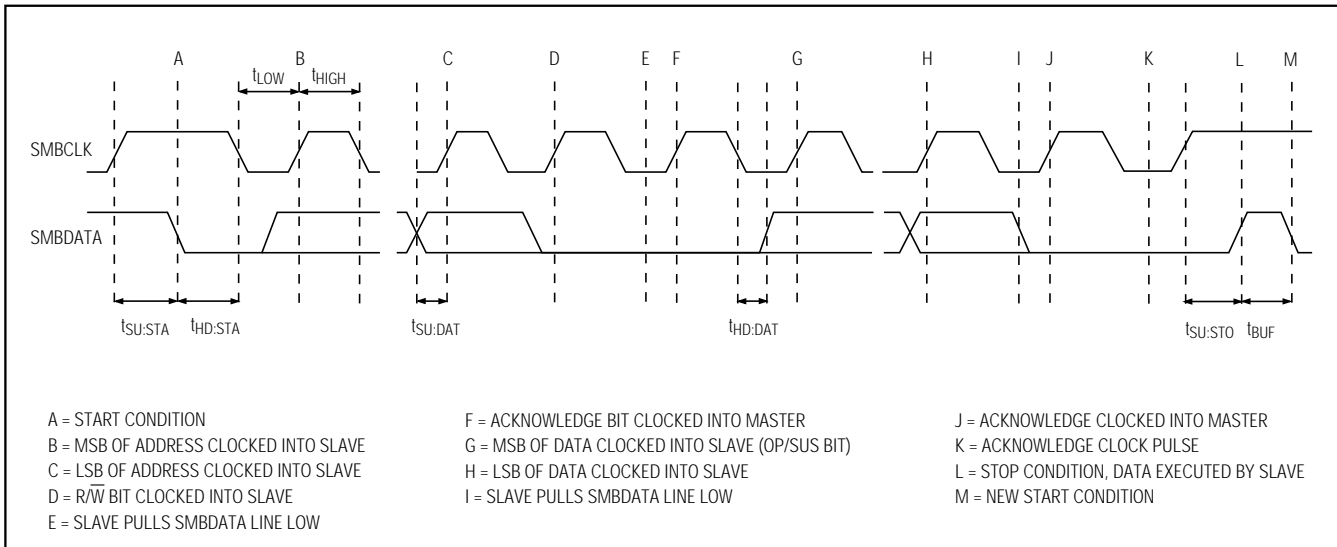


Figure 3. SMBus Write Timing Diagram

## SMBus Read Operations

If the IC receives a valid address that includes a read bit, the IC becomes a slave transmitter. After receiving the address data, the IC generates an acknowledge during the acknowledge clock pulse and drives the SMBDATA line in sync with SMBCLK. The SMB protocol requires that the master end the read transmission by not acknowledging during the acknowledge bit of SMBCLK. These PC Card ICs support the repeated start-condition method for changing data-transfer direction; that is, a write transmission followed by a repeated start instead of a stop condition prepares the IC for data reading (Figure 4).

## SMBus Interrupts

These PC Card power-switch ICs are slave devices only, and never initiate communications except by asserting an interrupt (by pulling  $\overline{\text{SMBALERT}}$  low). Interrupts are generated only for reporting fault conditions, including overcurrent at VCCA, VCCB, VPPA, or VPPB, undervoltage lockout, and IC thermal overload. If an interrupt occurs, it can be an indication of impending system failure. The host system can react by going into suspend mode or taking other action. It can come back later to interrogate the IC via the interrupt pointer to determine status or perform corrective action (such as disabling the appropriate power switch that might be connected to a shorted PC card). The fastest method for turning off the switches in response to a

fault condition is to cycle the voltage on VL in order to generate a power-on reset (which clears all of the SMBus registers). Note that the SMBus registers retain their data even if the main VX/VY supplies are turned off, provided that VL remains powered.

When a fault occurs,  $\overline{\text{SMBALERT}}$  is immediately asserted and latched low. If the fault is momentary and disappears before the IC is serviced, the data is still latched in the interrupt pointer and  $\overline{\text{SMBALERT}}$  remains asserted. Normally, the master (host system or PCMCIA digital controller) now sends out the interrupt pointer address (00011000) followed by a read bit.  $\overline{\text{SMBALERT}}$  is cleared and the PC Card IC responds by putting out its address on the bus. If the fault persists,  $\overline{\text{SMBALERT}}$  is re-asserted, but the data in the fault registers is not reloaded. The data in the fault latches only reflects the first time  $\overline{\text{SMBALERT}}$  is asserted.

When the part enters operating mode, a false interrupt flag may be issued. The user needs to send the interrupt address to clear the false interrupt.

Normally, the master sends out the appropriate PC Card switch address on the bus, followed by a read bit. The data in the fault registers is then clocked out onto the bus (which also clears the fault registers). If the fault persists, the fault bits and  $\overline{\text{SMBALERT}}$  are latched again.

# Dual-Channel CardBus and PCMCIA Power Switches with SMBus™ Serial Interface

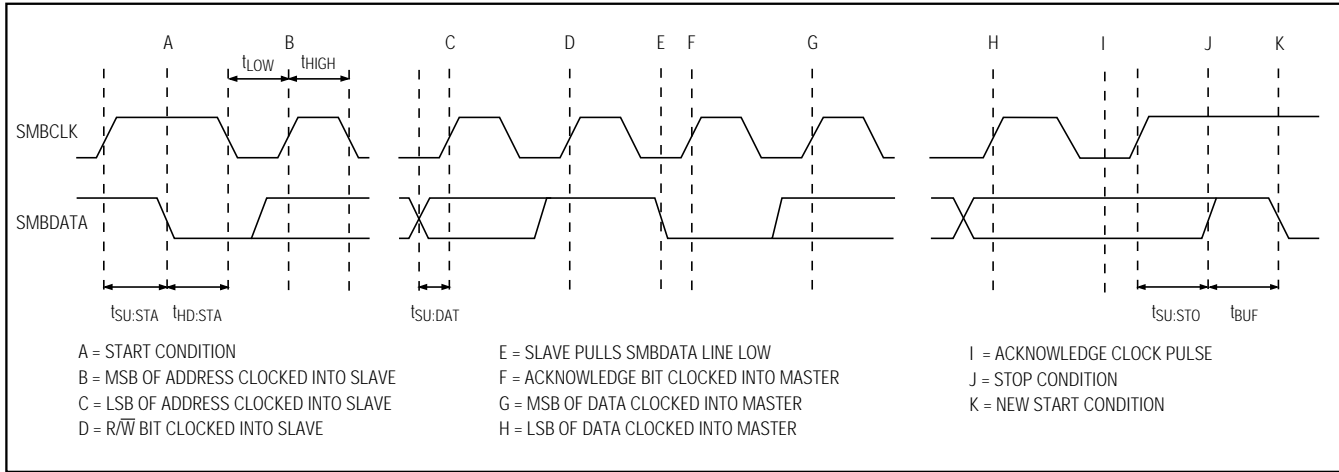


Figure 4. SMBus Read Timing Diagram

The interrupt pointer address provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. The host can read the interrupt pointer to determine which slave device generated an  $\overline{SMBALERT}$  interrupt signal. The interrupt pointer address can activate several different slave devices simultaneously, similar to an  $I^2C$  general call. Any slave device that generated an interrupt attempts to identify itself by putting its own address on the bus during the first read byte. If more than one slave attempts to respond, bus arbitration rules apply and the device with the lower address code wins. The losing device won't generate an acknowledge and will continue to hold the  $\overline{SMBALERT}$  line low until serviced, which implies that the host interrupt input must be level sensitive.

## Applications Information

### Supply Bypassing

Bypass the VY, VX, and 12IN\_ inputs with ceramic 0.1 $\mu$ F capacitors. Bypass the VCC\_ and VPP\_ outputs with a 0.1 $\mu$ F capacitor for noise reduction and ESD protection.

### Power-Up

Apply power to the VL input before any of the switch inputs. If VX, VY, or 12IN receive power before VL rises above 2.8V, the supply current may be artificially high (about 5mA). When the voltage on VL is greater than 2.8V (operating mode), the part consumes its specified 24 $\mu$ A. To avoid power sequencing, diode-OR VX and VY to VL through a 1k $\Omega$  resistor (Figure 5). Take care not to allow VL to drop below the 2.8V maximum under-voltage lockout threshold.

### Changing SMBCLK and SMBDATA Simultaneously

When clocking data into the MAX1601/MAX1604, SMBDATA must not fall before SMBCLK. Otherwise, the MAX1601/MAX1604 may interpret this as a start condition. Even when SMBDATA and SMBCLK fall at the same instant, different fall times for the two signals may cause the erroneous generation of a start condition. To ensure that SMBDATA transitions after the falling edge of SMBCLK, add an RC network to SBMDATA (Figure 6).

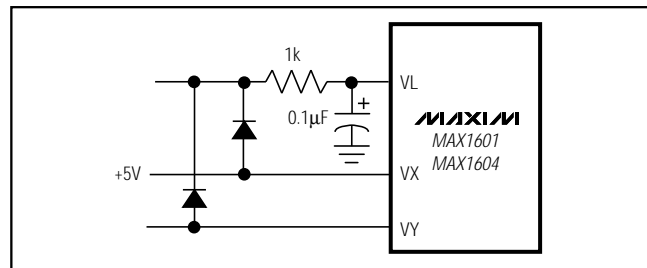


Figure 5. Powering from Either VX or VY

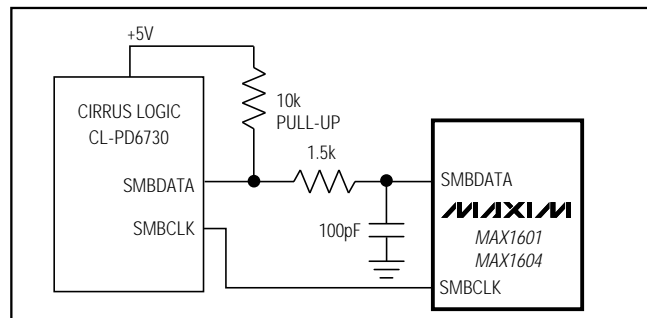
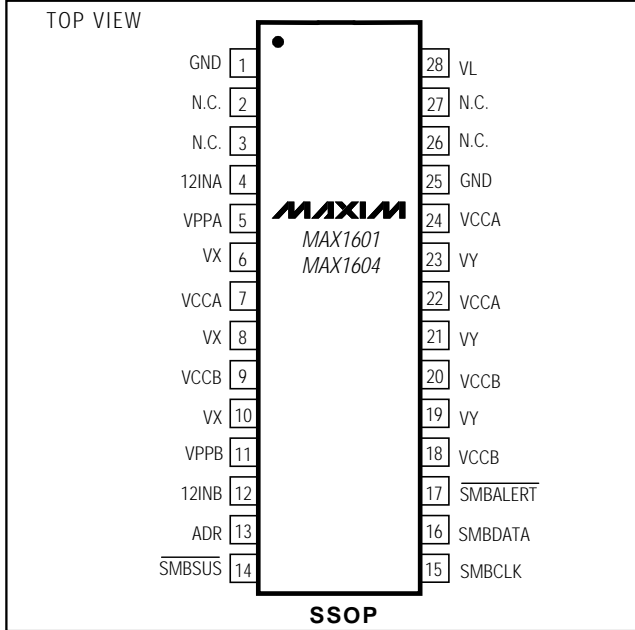


Figure 6. Application with Cirrus Logic Interface

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## Pin Configuration

## Chip Information



TRANSISTOR COUNT: 4372

## Package Information

**SSOP  
SHRINK  
SMALL-OUTLINE  
PACKAGE**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

21-0056A

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