THE DATASHEET OF

ADS1202IPWT

SBAS275B – DECEMBER 2002 – REVISED JULY 2004

Motor Control Current Shunt 1-Bit, 10MHz, 2nd-Order, Delta-Sigma Modulator

FEATURES

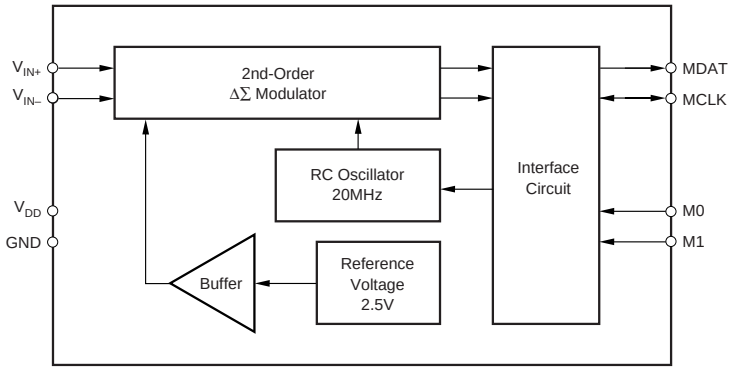
- **16-BIT RESOLUTION**
- **13-BIT LINEARITY**
- **RESOLUTION/SPEED TRADE-OFF:**
  10-Bit Effective Resolution with 20μs Signal Delay (12-bit with 77μs)
- **±250mV INPUT RANGE WITH SINGLE 5V SUPPLY**
- **2% INTERNAL REFERENCE VOLTAGE**
- **2% GAIN ERROR**
- **FLEXIBLE SERIAL INTERFACE WITH FOUR DIFFERENT MODES**
- **IMPLEMENTED TWINNED BINARY CODING AS SPLIT PHASE OR MANCHESTER CODING FOR ONE LINE INTERFACING**
- **OPERATING TEMPERATURE RANGE:**
  –40°C to +85°C

APPLICATIONS

- **MOTOR CONTROL**
- **CURRENT MEASUREMENT**
- **INDUSTRIAL PROCESS CONTROL**
- **INSTRUMENTATION**
- **SMART TRANSMITTERS**
- **PORTABLE INSTRUMENTS**
- **WEIGHT SCALES**
- **PRESSURE TRANSDUCERS**

DESCRIPTION

The ADS1202 is a precision, 80dB dynamic range, delta-sigma (ΔΣ) modulator operating from a single +5V supply. The differential inputs are ideal for direct connections to transducers or low-level signals. With the appropriate digital filter and modulator rate, the device can be used to achieve 16-bit Analog-to-Digital (A/D) conversion with no missing codes. Effective resolution of 12 bits can be maintained with a digital filter bandwidth of 10kHz at a modulator rate of 10MHz. The ADS1202 is designed for use in medium resolution measurement applications including current measurements, smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation. It is available in a TSSOP-8 package.



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature (unless otherwise noted)[1]

Supply Voltage, GND to V_{DD}	–0.3V to 6V
Analog Input Voltage Range	GND – 0.4V to V_{DD} + 0.3V
Digital Input Voltage Range	GND – 0.3V to V_{DD} + 0.3V
Power Dissipation	0.25W
Operating Virtual Junction Temperature Range, T_J	–40°C to +150°C
Operating Free-Air Temperature Range, T_A	–40°C to +85°C
Storage Temperature Range, T_{STG}	–65°C to +150°C
Lead Temperature 1.6mm (1/16") from Case for 10s	+260°C

NOTE: (1) Stresses beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

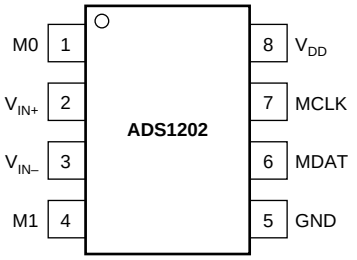
PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM GAIN ERROR (%)	PACKAGE-LEAD	SPECIFIED PACKAGE DESIGNATOR[1]	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1202	12	±2	TSSOP-8	PW	–40°C to +85°C	ADS1202I	ADS1202IPWT	Tape and Reel, 250
ADS1202	"	"	"	"	"	"	ADS1202IPWR	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATION

Top View TSSOP



PIN DESCRIPTIONS

PIN NUMBER	NAME	DESCRIPTION
1	M0	Mode Input
2	V_{IN}+	Analog Input: Noninverting Input
3	V_{IN}–	Analog Input: Inverting Input
4	M1	Mode Input
5	GND	Power Supply Ground
6	MDAT	Modulator Data Output
7	MCLK	Modulator Clock Input or Output
8	V_{DD}	Power Supply, +5V Nominal

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	4.75	5.0	5.25	V
Analog Input Voltage, V_{IN}	–250		+250	mV
Operating Common-Mode Signal, V_{CM}	0		5	V
External Clock[1]	16	20	24	MHz
Operating Junction Temperature Range	–40		105	°C

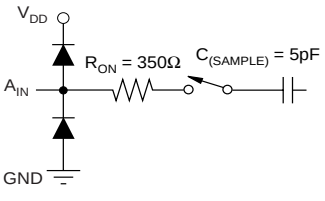
NOTE: (1) With reduced accuracy, minimum clock can go up to 500kHz.

DISSIPATION RATING

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C[1]	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
TSSOP-8	483.6mW	3.868mW/°C	309.5mW	251.4mW

NOTE: (1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$). Thermal resistances are not production tested and are for informational purposes only.

EQUIVALENT INPUT CIRCUIT



Diode Turn on Voltage: 0.35V

Equivalent Analog Input Circuit

Equivalent Digital Input Circuit

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to +85°C, V_{DD} = 5V, +In = –250mV to 250mV, –In = 0V, and MCLK = 10MHz, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1202IPW MIN	ADS1202IPW TYP(1)	ADS1202IPW MAX	UNITS
RESOLUTION			16			Bits
DC ACCURACY						
Integral Nonlinearity(2)	INL			±3	±12	LSB
				0.005	0.018	%
Differential Linearity(3)	DNL				±1	LSB
Input Offset(4)	V_{OS}			±300	±1000	µV
Input Offset Drift	TCV_{OS}			2	8	µV/°C
Gain Error(4)	G_{ERR}			±0.25	±2	%
Gain Error Drift	TCG_{ERR}			20		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.75V < V_{DD} < 5.25V		80		dB
ANALOG INPUT						
Full-Scale Range	FSR	+In – (–In)			±320	mV
Operating Common-Mode Signal(3)			–0.1		5	V
Input Capacitance		Common-Mode		3		pF
Input Leakage Current					±1	nA
Differential Input Resistance		Equivalent		28		kΩ
Differential Input Capacitance				5		pF
Common-Mode Rejection Ratio	CMRR	At DC		90		dB
		V_{IN} = ±1.25Vp-p at 50kHz		85		dB
INTERNAL VOLTAGE REFERENCE						
Reference Voltage	V_{OUT}	Scale to 320mV	2.450	2.5	2.550	V
Accuracy(4)		Scale to 320mV			±2	%
Reference Temperature Drift	dV_{OUT}/dT			±20		ppm/°C
PSRR				80		dB
Startup Time				0.1		ms
INTERNAL CLOCK FOR MODES, 0, 1, AND 2						
Clock Frequency			8	10	12	MHz
EXTERNAL CLOCK FOR MODE 3						
Clock Frequency			16	20	24	MHz
AC ACCURACY						
Signal-to-Noise Ratio + Distortion	SINAD	V_{IN} = ±250mVp-p at 5kHz		70		dB
Signal-to-Noise Ratio	SNR	V_{IN} = ±250mVp-p at 5kHz	67	70.5		dB
Total Harmonic Distortion	THD	V_{IN} = ±250mVp-p at 5kHz		–84		dB
Spurious Free Dynamic Range	SFDR	V_{IN} = ±250mVp-p at 5kHz		84		dB
DIGITAL INPUT						
Logic Family				TTL with Schmitt Trigger		
High-Level Input Voltage	V_{IH}		2.6		V_{DD} + 0.3	V
Low-Level Input Voltage	V_{IL}		–0.3		0.8	V
High-Level Input Current	I_{IH}	V_I = V_{DD}		0.005	2.5	µA
Low-Level Input Current	I_{IL}	V_I = GND	–2.5	0.005		µA
Input Capacitance	C_J			5		pF
DIGITAL OUTPUT						
High-Level Digital Output	V_{OH}	V_{DD} = 4.5V, I_O = –5mA	4.6			V
		V_{DD} = 4.5V, I_O = –15mA	3.9			V
Low-Level Digital Output	V_{OL}	V_{DD} = 4.5V, I_O = 5mA			0.4	V
		V_{DD} = 4.5V, I_O = 15mA			1.1	V
Output Capacitance	C_O			5		pF
Load Capacitance	C_L				30	pF
POWER SUPPLY						
Supply Voltage	V_{DD}		4.5	5	5.5	V
Operating Supply Current	I_{CC}	Mode 0		8	9.5	mA
		Mode 3		6	7.5	mA
Power Dissipation		V_{DD} = 5V, Mode 0		40	47.5	mW
		V_{DD} = 5V, Mode 3		30	37.5	mW
OPERATING TEMPERATURE			–40		+85	°C

NOTES: (1) All typical values are at T_A = +25°C. (2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the transfer curve for V_{IN}+ = –250mV to +250mV, expressed either as the number of LSBs or as a percent of measured input range (500mV). (3) Ensured by design. (4) Maximum values, including temperature drift, are ensured over the full specified temperature range.

TIMING DIAGRAMS

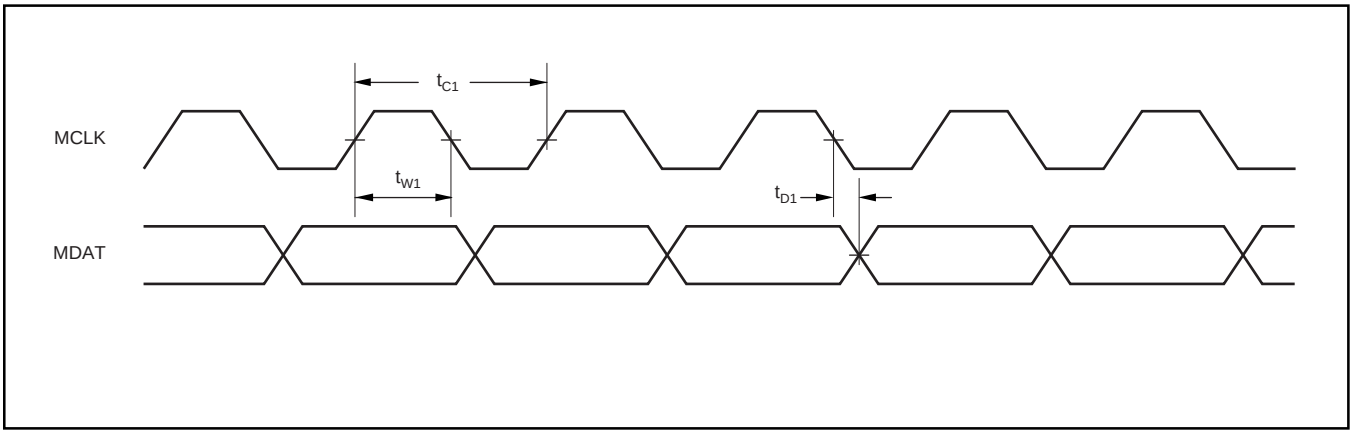


DIAGRAM 1: Mode 0 Operation.

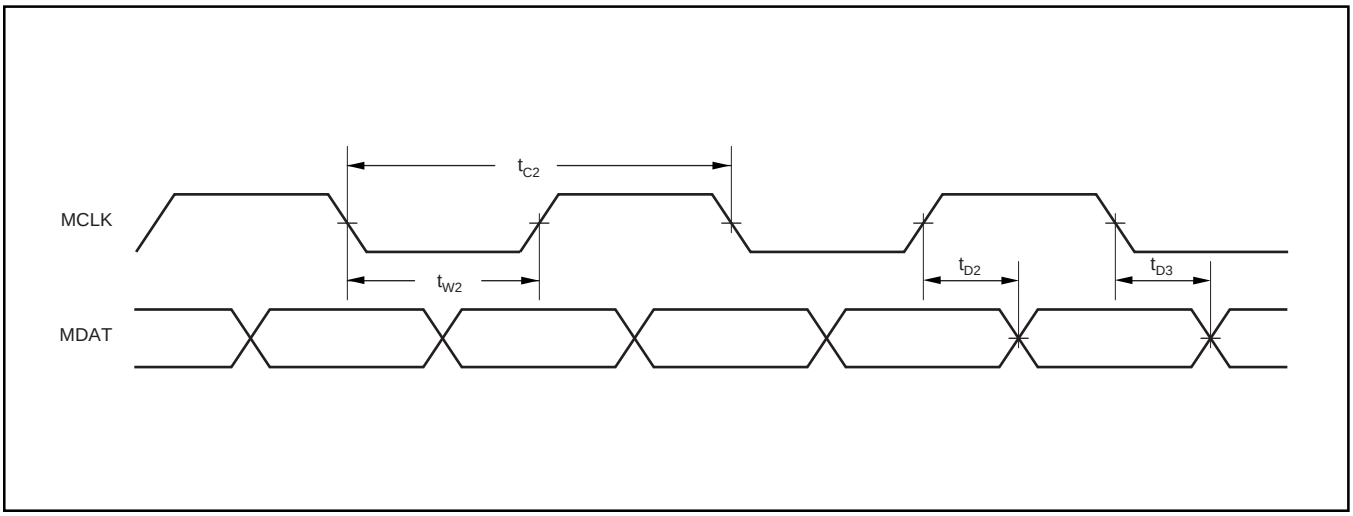


DIAGRAM 2: Mode 1 Operation.

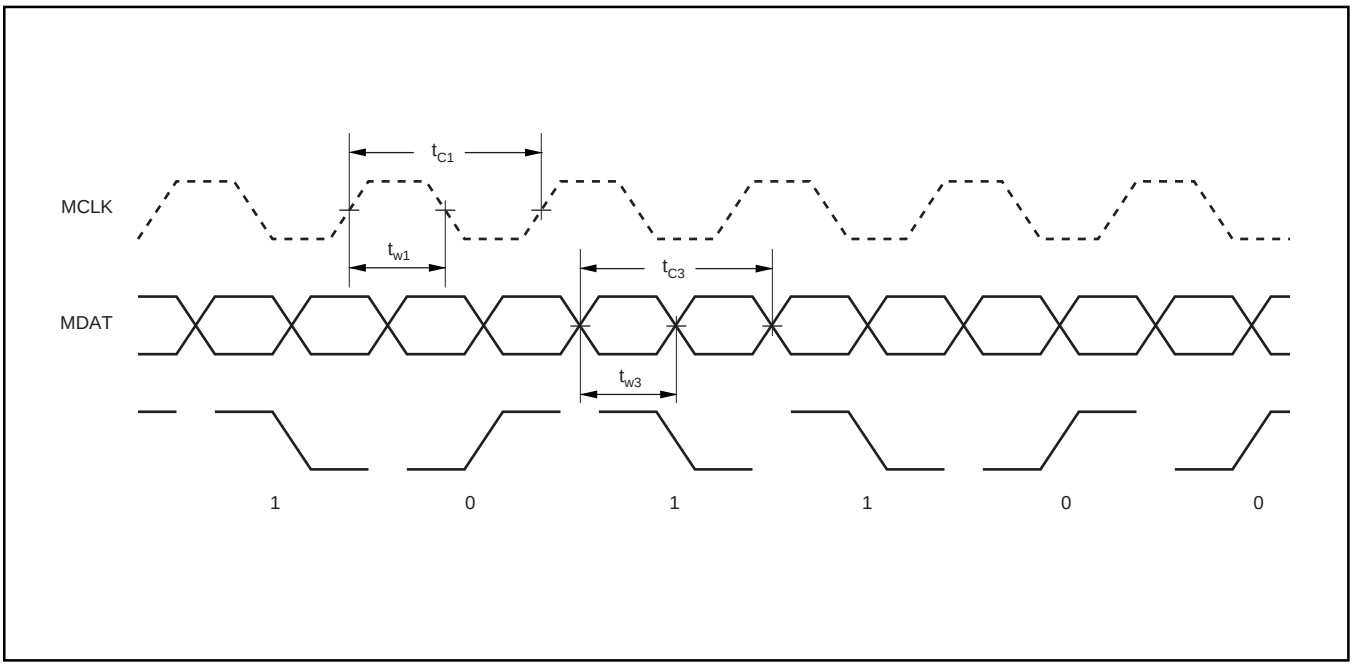


DIAGRAM 3: Mode 2 Operation.

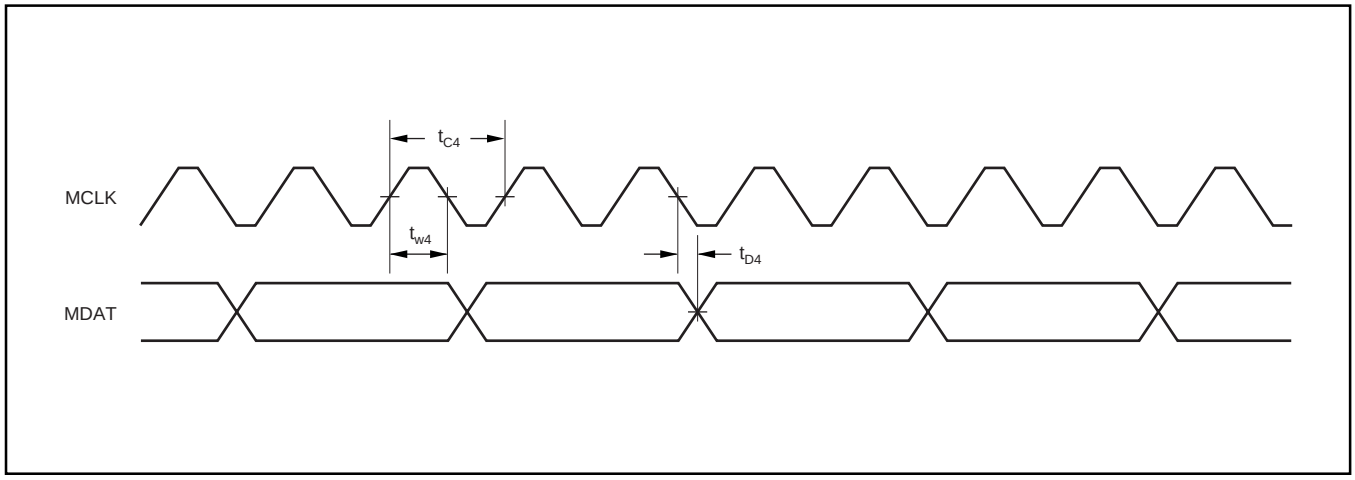


DIAGRAM 4: Mode 3 Operation.

TIMING CHARACTERISTICS

over recommended operating free-air temperature range –40°C to +85°C, V_{DD} = 5V, and MCLK = 10MHz, unless otherwise noted.

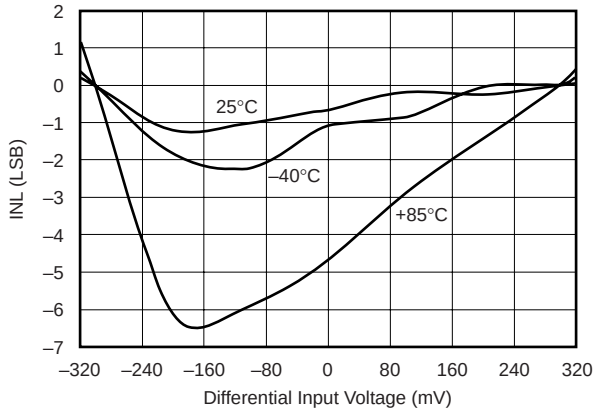
SPEC	DESCRIPTION	MODE	MIN	MAX	UNITS
t_{C1}	Clock Period	0	83	125	ns
t_{W1}	Clock HIGH Time	0	$t_{C1}/2 - 5$	$t_{C1}/2 + 5$	ns
t_{D1}	Data delay after falling edge of clock	0	–2	2	ns
t_{C2}	Clock Period	1	166	250	ns
t_{W2}	Clock HIGH Time	1	$t_{C2}/2 - 5$	$t_{C2}/2 + 5$	ns
t_{D2}	Data delay after rising edge of clock	1	–2	2	ns
t_{D3}	Data delay after falling edge of clock	1	–2	2	ns
t_{C3}	Clock Period	2	83	125	ns
t_{W3}	Clock HIGH Time	2	$t_{C3}/2 - 5$	$t_{C3}/2 + 5$	ns
t_{C4}	Clock Period	3	41	62	ns
t_{W4}	Clock HIGH Time	3	10	$t_{C4} - 10$	ns
t_{D4}	Data delay after falling edge of clock	3	0	10	ns
t_{R1}	Rise Time of Clock	3	0	10	ns
t_{F1}	Fall Time of Clock	3	0	10	ns

NOTE: All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See timing diagrams 1 thru 4.

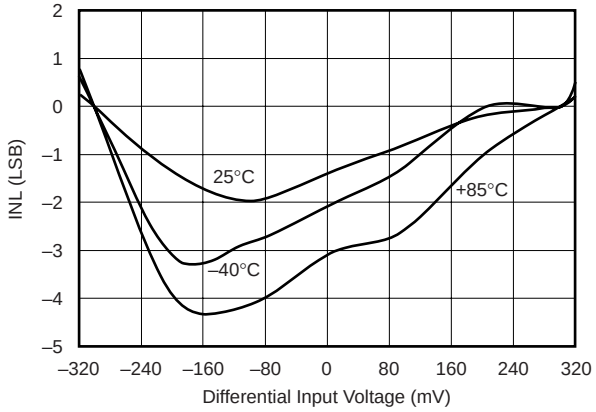
TYPICAL CHARACTERISTICS

V_{DD} = 5V, +In = –250mV to 250mV, –In = 0V, and MCLK = 10MHz, unless otherwise noted.

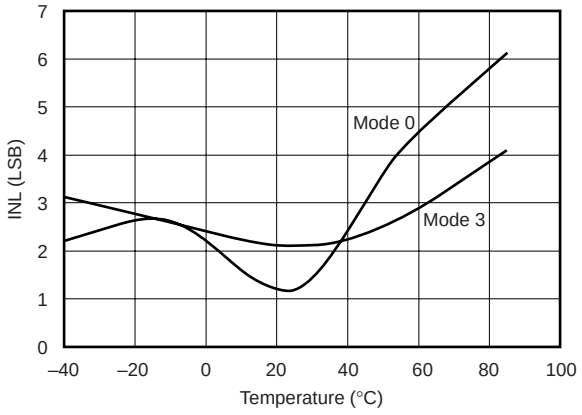
INTEGRAL NONLINEARITY vs INPUT SIGNAL (Mode 0)



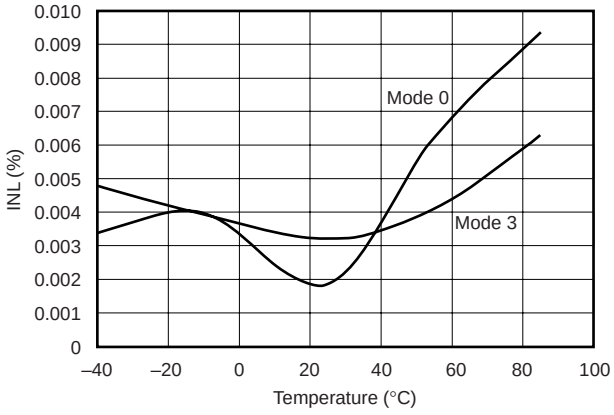
INTEGRAL NONLINEARITY vs INPUT SIGNAL (Mode 3)



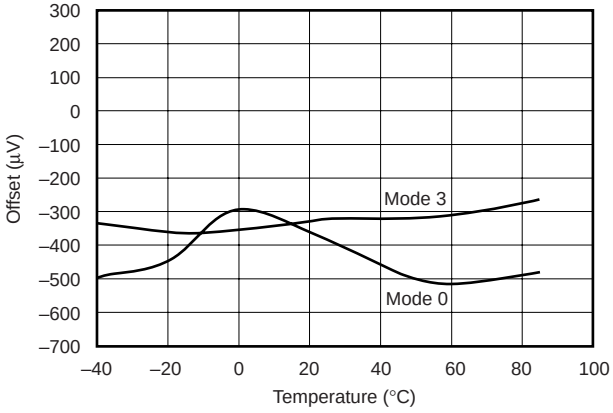
INTEGRAL NONLINEARITY vs TEMPERATURE



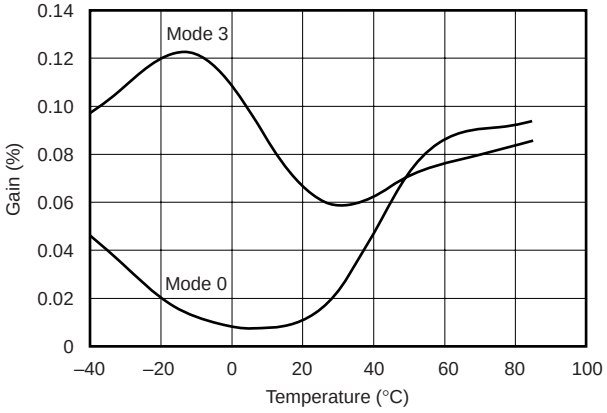
INTEGRAL NONLINEARITY vs TEMPERATURE



OFFSET vs TEMPERATURE



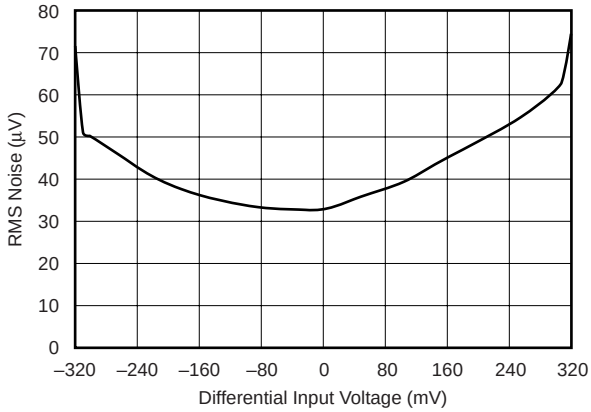
GAIN vs TEMPERATURE



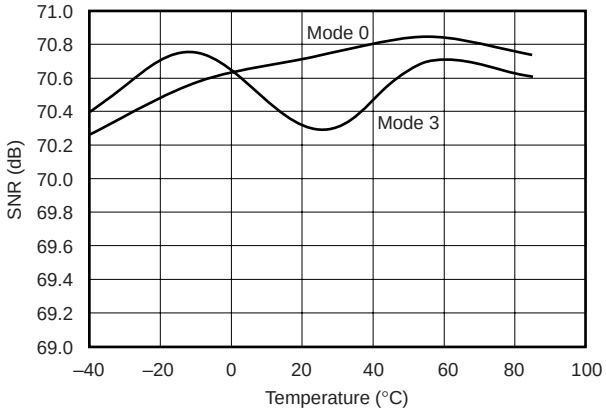
TYPICAL CHARACTERISTICS (Cont.)

V_{DD} = 5V, +In = –250mV to 250mV, –In = 0V, and MCLK = 10MHz, unless otherwise noted.

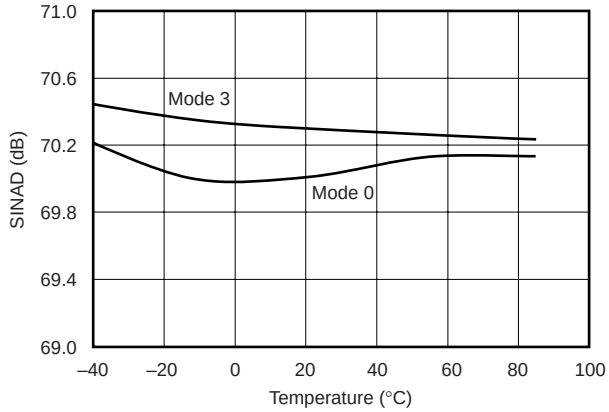
RMS NOISE vs INPUT VOLTAGE LEVEL



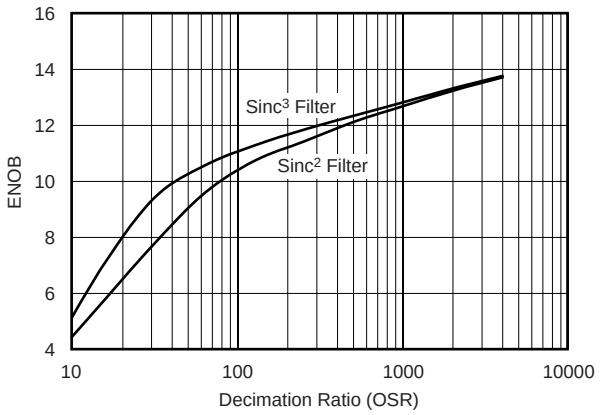
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



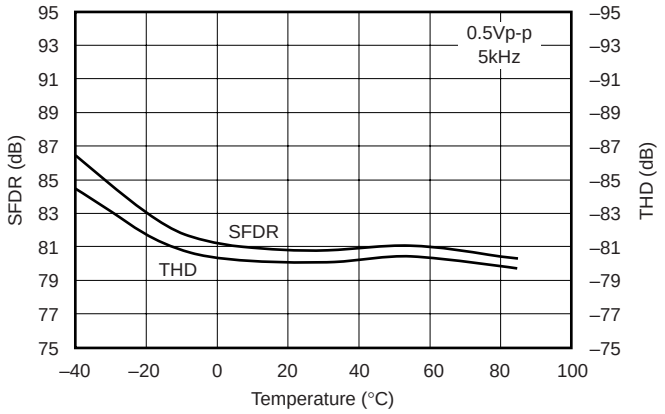
SIGNAL-TO-NOISE + DISTORTION
vs TEMPERATURE



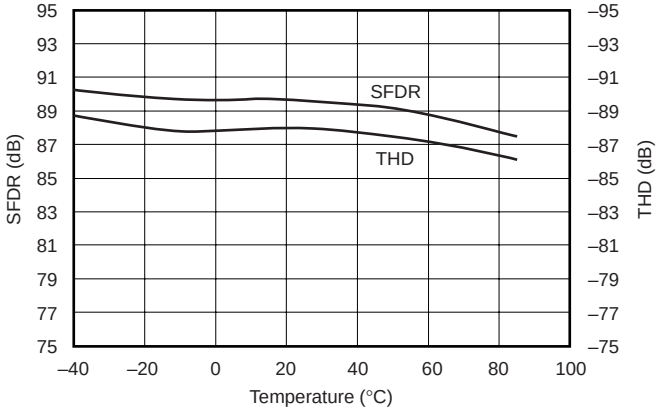
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



SPURIOUS-FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs TEMPERATURE (Mode 0)



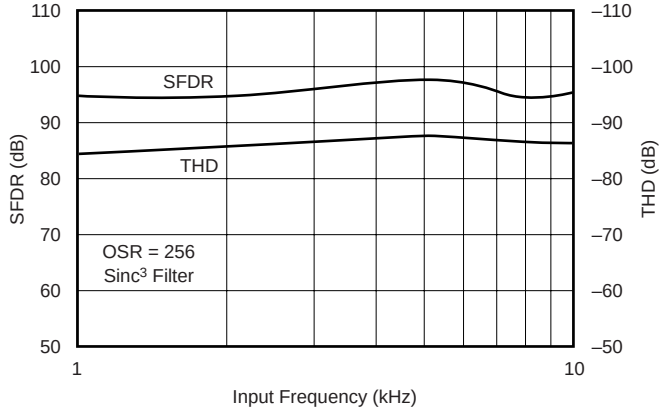
SPURIOUS-FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs TEMPERATURE (Mode 3)



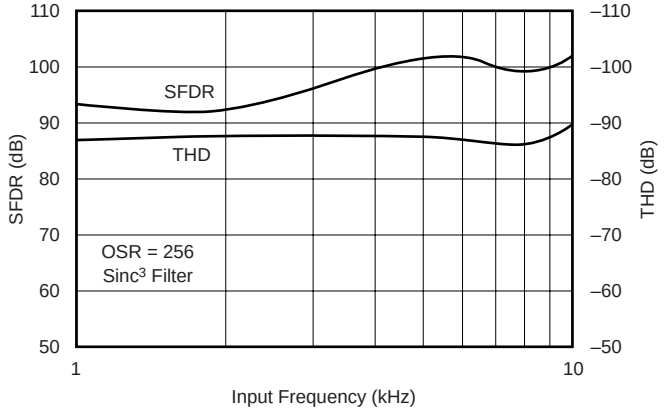
TYPICAL CHARACTERISTICS (Cont.)

V_{DD} = 5V, +In = –250mV to 250mV, –In = 0V, and MCLK = 10MHz, unless otherwise noted.

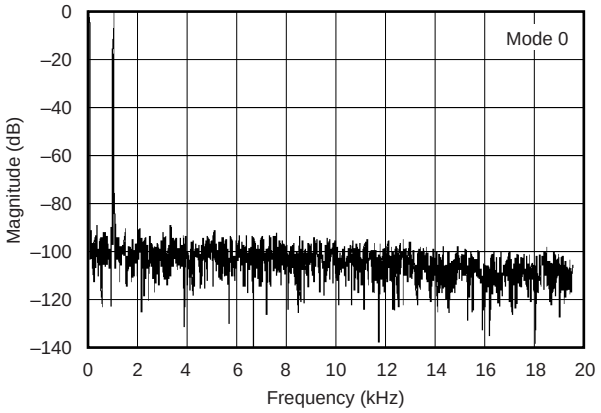
SPURIOUS-FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY (Mode 0)



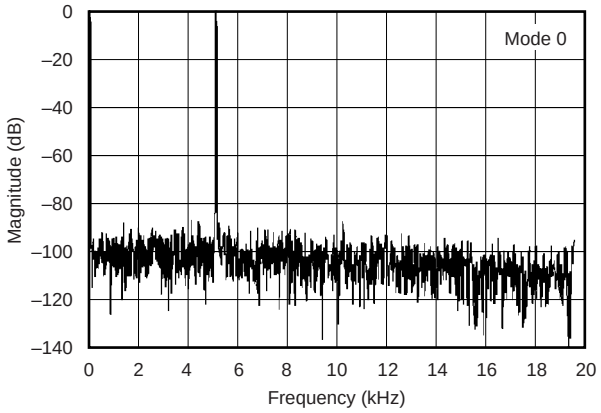
SPURIOUS-FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY (Mode 3)



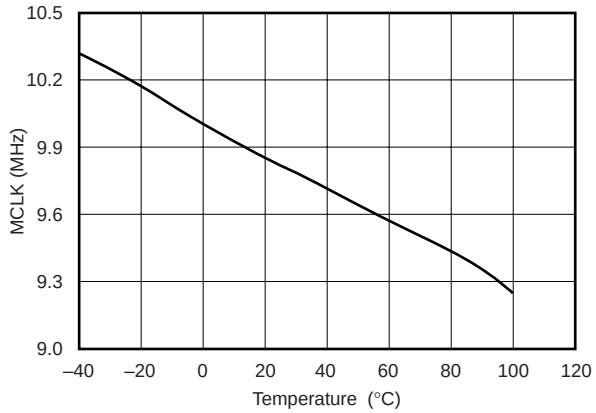
FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 1kHz, 0.5Vp-p)



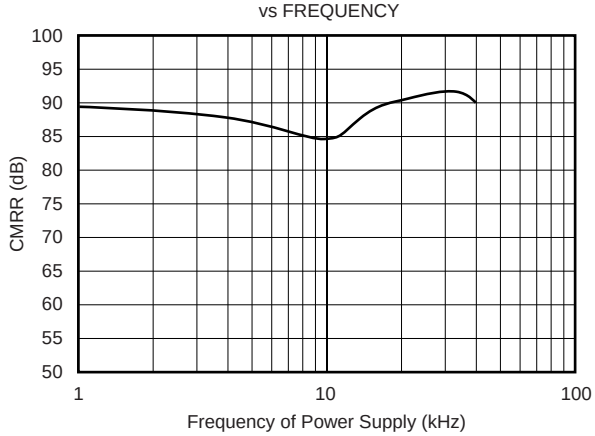
FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 5kHz, 0.5Vp-p)



CLOCK FREQUENCY vs TEMPERATURE



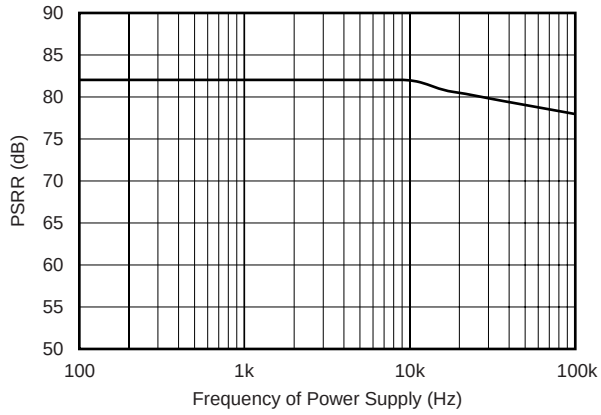
COMMON-MODE REJECTION RATIO
vs FREQUENCY



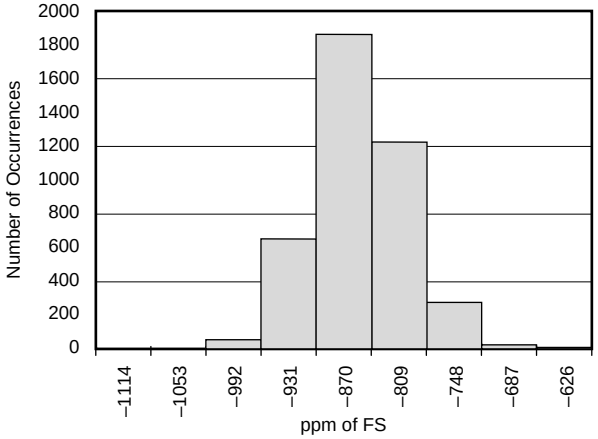
TYPICAL CHARACTERISTICS (Cont.)

V_{DD} = 5V, +In = –250mV to 250mV, –In = 0V, and MCLK = 10MHz, unless otherwise noted.

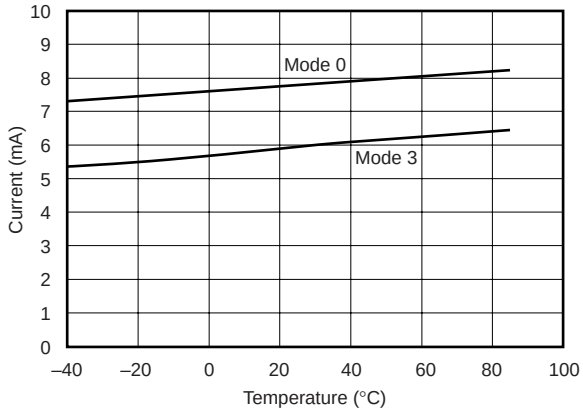
POWER-SUPPLY REJECTION RATIO
vs FREQUENCY



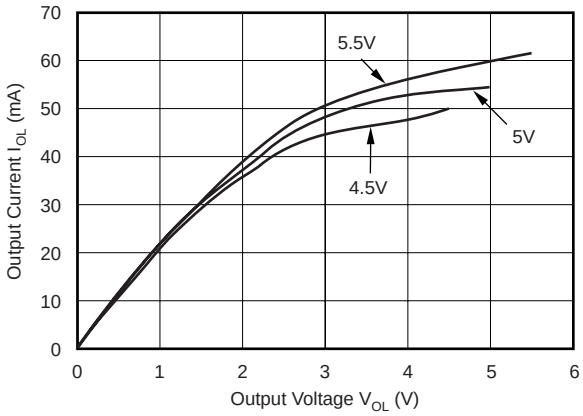
HISTOGRAM OF OUTPUT DATA



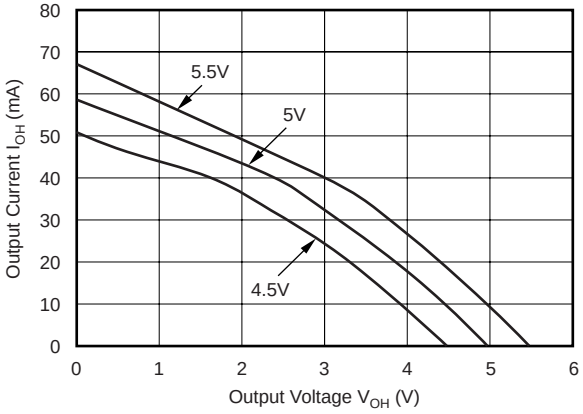
POWER-SUPPLY CURRENT vs TEMPERATURE



MCLK AND MDAT
TYPICAL SINK CURRENT



MCLK AND MDAT
TYPICAL SOURCE CURRENT



GENERAL DESCRIPTION

The ADS1202 is a single-channel, 2nd-order, CMOS analog modulator designed for medium- to high-resolution conversions from dc to 39kHz with an oversampling ratio (OSR) of 256. The output of the converter (MDAT) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage. The combination of an ADS1202 and a Digital Signal Processor (DSP) that is programmed to implement a digital filter results in a medium-resolution A/D converter system. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 85dB with OSR = 256.

THEORY OF OPERATION

The differential analog input of the ADS1202 is implemented with a switched capacitor circuit. This switched capacitor circuit implements a 2nd-order modulator stage, which digitizes the input signal into a 1-bit output stream. The sample clock (MCLK) provides the switched capacitor network and modulator clock signal for the A/D conversion process, as well as the output data-framing clock. The clock source can be internal as well as external. Different frequencies for this clock allow for a variety of solutions and signal bandwidths (however, this can only be utilized in mode 3). The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream, which accurately represents the analog input voltage over time, appears at the output of the converter.

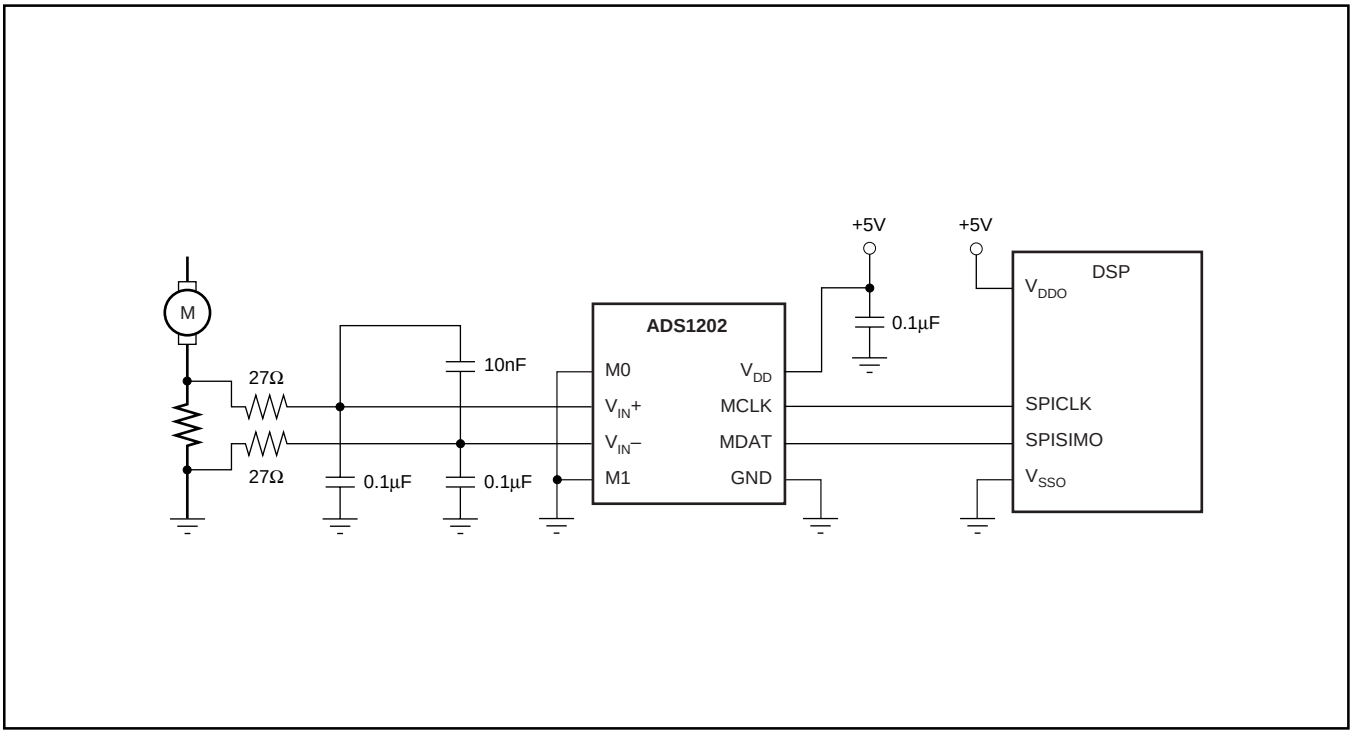


FIGURE 1. Connection Diagram for the ADS1202 Delta-Sigma Modulator Including DSP.

ANALOG INPUT STAGE

Analog Input

The input design topology of the ADS1202 is based on a fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (90dB), and excellent power-supply rejection. The input impedance of the analog input is dependent on the input capacitor and modulator clock frequency (MCLK), which is also the sampling frequency of the modulator. Figure 2 shows the basic input structure of the ADS1202. The relationship between the input impedance of the ADS1202 and the modulator clock frequency is:

$$A_{IN}(\Omega) = \frac{10^{12}}{7 \bullet f_{MCLK}(MHz)} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is HIGH. In this case, it is possible for a portion of the signal to be lost across this external source impedance. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signal to the ADS1202. Under no conditions should the current into or out of the analog inputs exceed 10mA. The absolute input voltage range must stay in the range GND – 0.4V to V_{DD} + 0.3V. If either of the inputs exceeds these limits, the input protection diodes on the front end of the converter will begin to turn on. In addition, the linearity of the device is ensured only when the analog voltage applied to either input resides within the range defined by –320mV and +320mV.

Modulator

The modulator sampling frequency (CLK) can be operated over a range of a few MHz to 12MHz in mode 3. The frequency of MCLK can be decreased to adjust for the clock requirements of the application. The external MCLK must have double the modulator frequency.

The modulator topology is fundamentally a 2nd-order, charge-balancing A/D converter, as the one conceptualized in Figure 3. The analog input voltage and the output of the 1-bit Digital-to-Analog Converter (DAC) are differentiated, providing an analog voltage at X_2 and X_3. The voltage at X_2 and X_3 are presented to their individual integrators. The output of these integrators progress in a negative or positive direction. When the value of the signal at X_4 equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative, depending on its original state. When the output value of the comparator switches from HIGH to LOW or vice versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X_6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

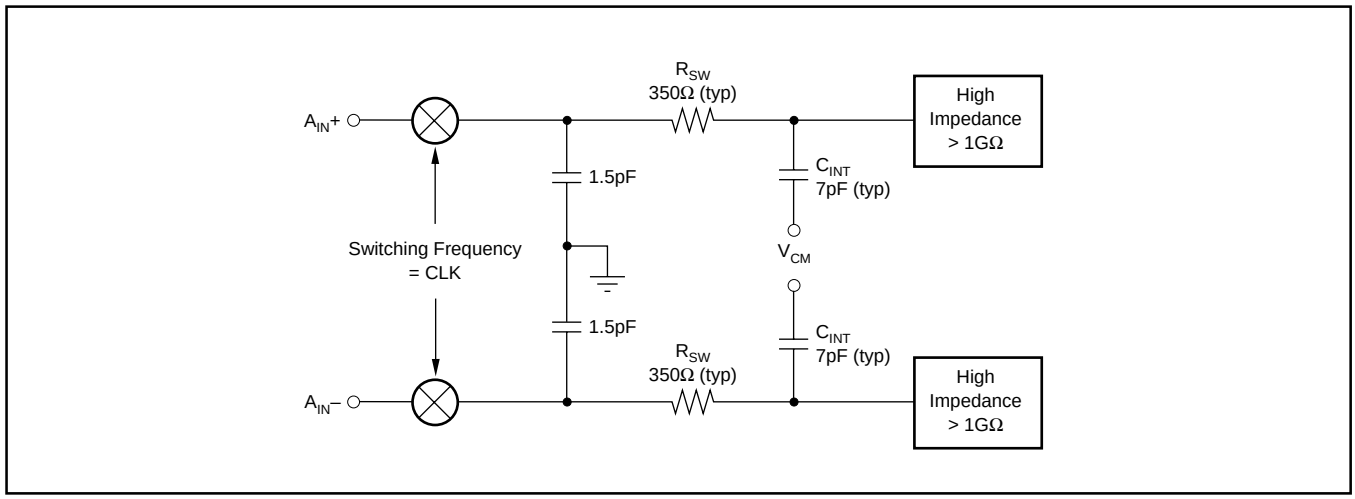


FIGURE 2. Input Impedance of the ADS1202.

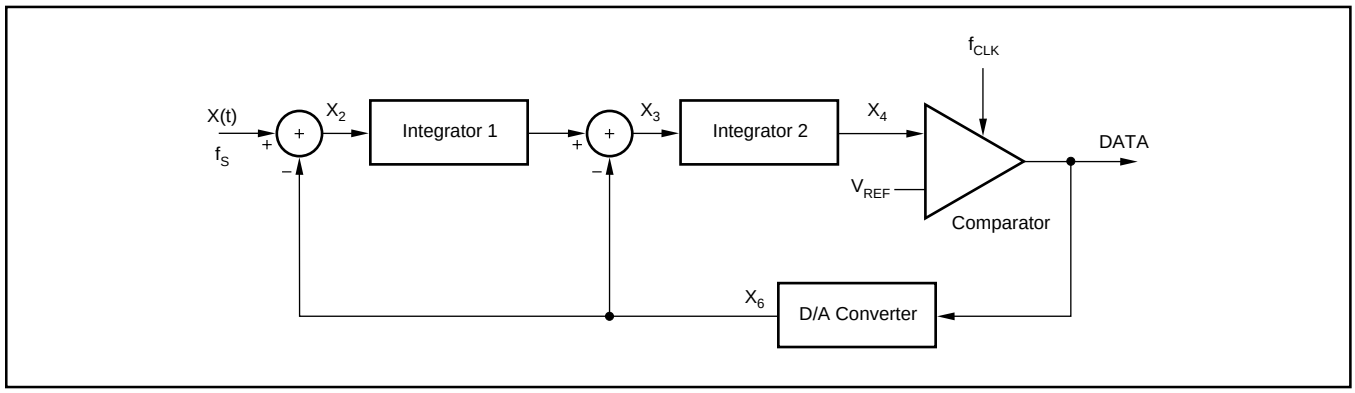


FIGURE 3. Block Diagram of the 2nd-Order Modulator.

DIGITAL OUTPUT

The timing diagram for the ADS1202 data retrieval is shown in the Timing Diagrams. When an external clock is applied to MCLK, it is used as a system clock by the ADS1202, as well as a framing clock for data out (this procedure, however, can only be utilized in mode 3). The modulator output data, which is a serial stream, is available on the MDAT pin. Typically, MDAT is read on the falling edge of MCLK.

An input differential signal of 0V will ideally produce a stream of ones and zeros that are HIGH 50% of the time and LOW 50% of the time. A differential input of 256mV will produce a stream of ones and zeros that are HIGH 80% of the time. A differential input of –256mV will produce a stream of ones and zeros that are HIGH 20% of the time. The input voltage versus the output modulator signal is shown in Figure 4.

DIGITAL INTERFACE

INTRODUCTION

The analog signal that is connected to the input of the delta-sigma modulator is converted using the clock signal (CLK) applied to the modulator. The result of the conversion, or modulation, is the output signal DATA from the delta-sigma modulator.

In most applications where direct connection is realized between the delta-sigma modulator and the DSP or μC, two standard signals are provided. The MDAT and MCLK signals provide the easiest means of connection. If it is required to reduce the number of connection lines, having two signals is sometimes not an optimal solution.

The receiver, DSP, or other control circuit must sample the output data signal from the modulator at the precise sampling instant. To do this, sampling a clock signal at the receiver is needed in order to synchronize with the clock signal at the transmitter. The delta-sigma modulator clock signal, receiver, filter, and clock must be synchronized. Three general methods can be used to obtain this synchronization. The first method has the delta-sigma modulator and the filter receive the clock signal from the master clock. The second method has the delta-sigma modulator transmit the clock signal together with the data signal. The third method has the filter derive the clock signal from the received waveform itself.

An ideal solution is a delta-sigma modulator with a flexible interface, such as the ADS1202, which can provide flexible output format on the output lines MCLK and MDAT, thus covering different modes of operation. The signal type that can be provided is selected with control signals M0 and M1.

FLEXIBLE DELTA-SIGMA INTERFACE

Figure 5 illustrates the flexible interface of the ADS1202 delta-sigma converter. The control signals M0 and M1 are entered in the decoder that decodes the input code and selects the desired mode of operation. Five output signals from the decoder control the RC oscillator, multiplexer MUX1, multiplexer MUX2, multiplexer MUX3, and multiplexer MUX4.

MUX1 is controlled by the decoder signal. When the internal RC oscillator is used, the control signal from the decoder enables the RC oscillator. At the same time, MUX1 uses the INTCLK signal as a source for the output signal from MUX1, which is entering the code generator. If the external clock is used, the control signal from the decoder disables the internal RC oscillator and the control signal from the decoder, and positions MUX1 so that EXTCLK provides the output signal from MUX1 as the input in the code generator.

MUX2 selects the output clock, OCLK. The control signal coming from the decoder controls the output clock. Two signals come from the code generator as a half clock frequency, CLK/2, and as a quarter clock frequency, CLK/4, and provide MUX2 with the input signal. The control signal will select two different output modes on the OCLK signal as half clock or quarter clock.

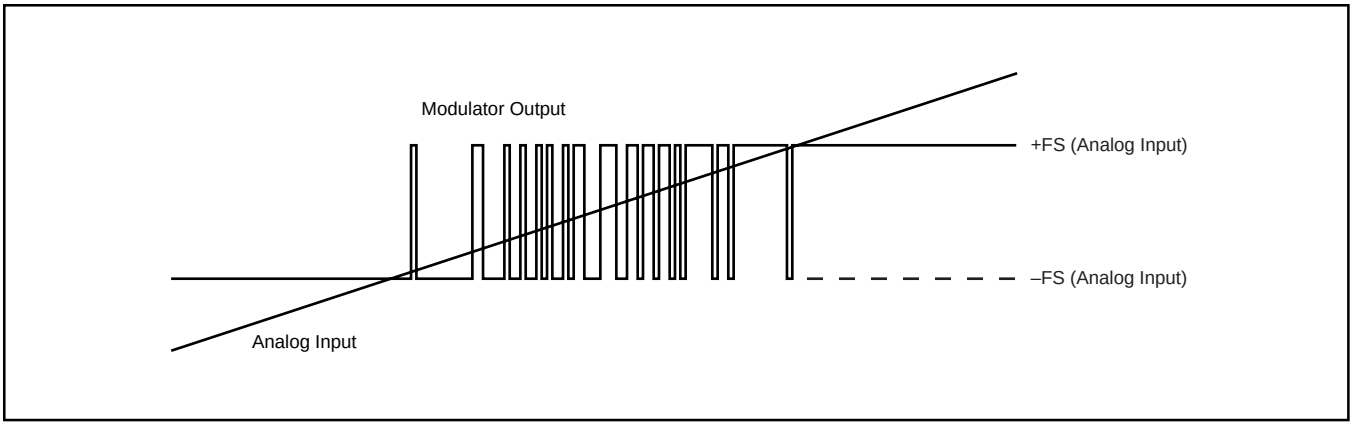


FIGURE 4. Analog Input Versus Modulator Output of the ADS1201.

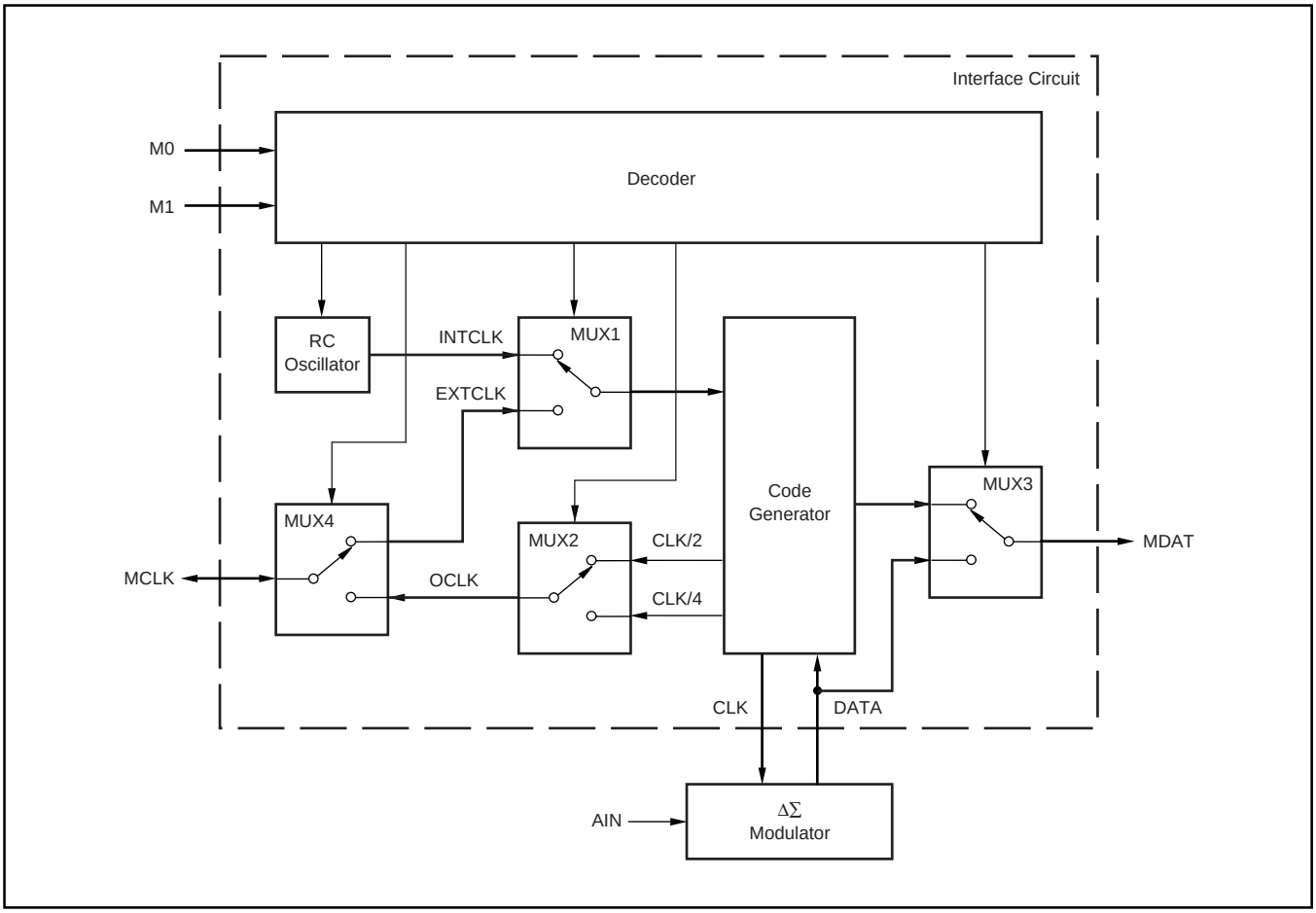


FIGURE 5. Flexible Interface Block Diagram.

The code generator receives the clock signal from MUX1 and generates the delta-sigma modulator clock (CLK) divided as half clock (CLK/2) and quarter clock (CLK/4). At the same time, the continuous data stream (DATA) coming from the delta-sigma modulator is elaborated by the Code Generator. Twinned binary coding (also known as split phase or Manchester coding) is implemented and then output from the code generator to MUX3.

MUX3 selects the source of the output bit stream data, MDAT. The control signal coming from the decoder controls the input source of MDAT. Two signals are coming in to the MUX3, one directly from the delta-sigma modulator and the other from the code generator. The control signal from the decoder can select two different output modes on the signal MDAT: a bit stream from a delta-sigma modulator, or twinned binary coding of the same signal.

The last control signal from the decoder controls MUX4. MUX2 selects the input or output clock, the MCLK signal. The control signal coming from the decoder controls the direction of the clock. One signal entering MUX4 from MUX2 comes as a clock signal OCLK. Another signal leaves MUX4 and provides an input to MUX1 as an external clock, EXTCLK.

The control signal from the decoder can select two different modes on MCLK, one as an output of the internal clock signal and another as the input for the external clock signal.

As a function of two control signals (M0 and M1), the decoder circuit, using five control signals, will set multiplexers in order to obtain the desired mode of operation.

DIFFERENT MODES OF OPERATION

Figure 5 presents mode selectors (input signals M0 and M1) that enter the flexible interface circuit and decoder that decodes the input code, and select the desired mode of operation. With two control lines it is possible to select four different modes of operation mode 0, mode 1, mode 2, and mode 3, which are shown in Table I.

MODE	DEFINITION	M1	MO
0	Internal Clock, Synchronous Data Output	LOW	LOW
1	Internal Clock, Synchronous Data Output, Half Output Clock Frequency	LOW	HIGH
2	Internal Clock, Manchester Coded Data Output	HIGH	LOW
3	External Clock, Synchronous Data Output	HIGH	HIGH

TABLE I. Mode Definition and Description.

Mode 0

In mode 0 both input signals, M0 and M1, are LOW. The control signal coming from the decoder enables the internal RC oscillator that provides the clock signal INTCLK as an input to MUX1. The control signal coming from the decoder also positions MUX1 so that the output signal, which is an input signal for the code generator, is INTCLK. Another control signal from the decoder circuit positions MUX3 so that the source for the output signal MDAT is the signal arriving directly from the delta-sigma modulator, DATA. MUX2 is positioned for the mode controlled by the signal coming from the decoder so output signal OCLK is CLK/2. The signal timings for mode 0 operation are presented in Figure 6. In this mode, the DSP or μC read MDAT data on every rising edge of the MCLK output clock.

Mode 1

In mode 1, the input signal M0 is HIGH and M1 is LOW (see Table I). The first control signal coming from the decoder enables the internal RC oscillator that provides clock signal INTCLK as an input to MUX1. The second control signal coming from the decoder positions MUX1 so that the output signal that is the input signal to the code generator is INTCLK. The output signal from the delta-sigma modulator, DATA, is also the MDAT signal coming from the modulator because the control signal from the decoder positions MUX3 for that operation. MUX2 is positioned for the mode controlled by the control signal coming from the decoder with an OCLK of CLK/2. Output clock signal MCLK comes through MUX4 from MUX2 as OCLK or CLK/2. The signal timings for mode 1 operation are presented in Figure 7. In this mode, the DSP or μC read data on every edge, rising and falling, of the output clock.

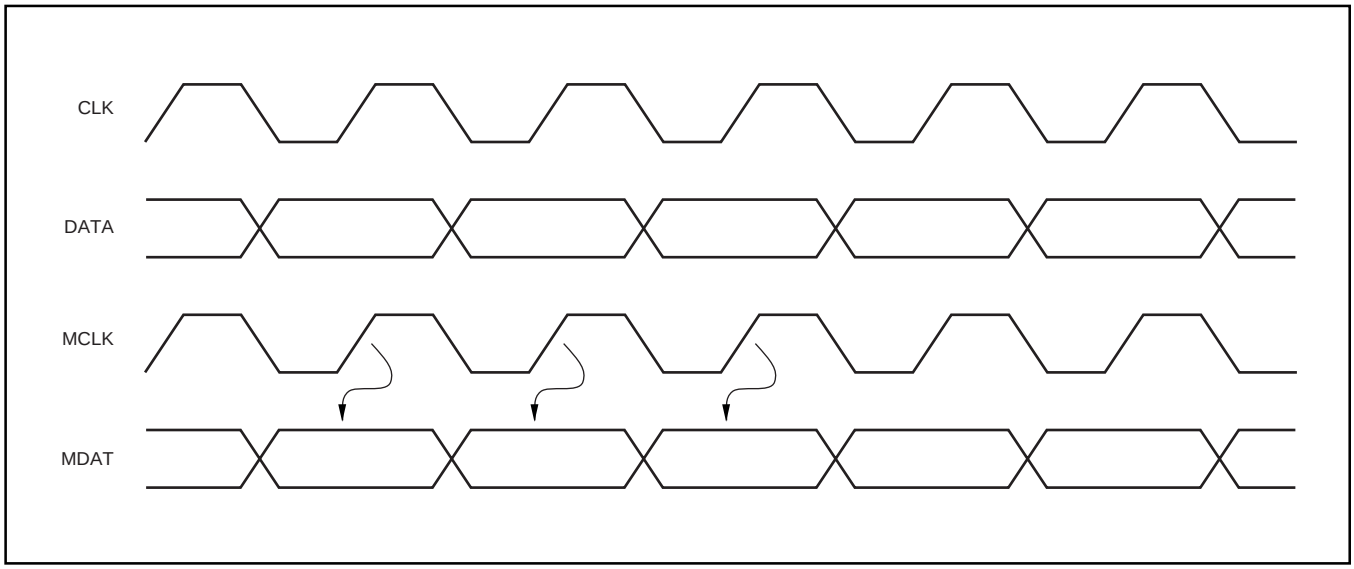


FIGURE 6. Signal Timing in Mode 0.

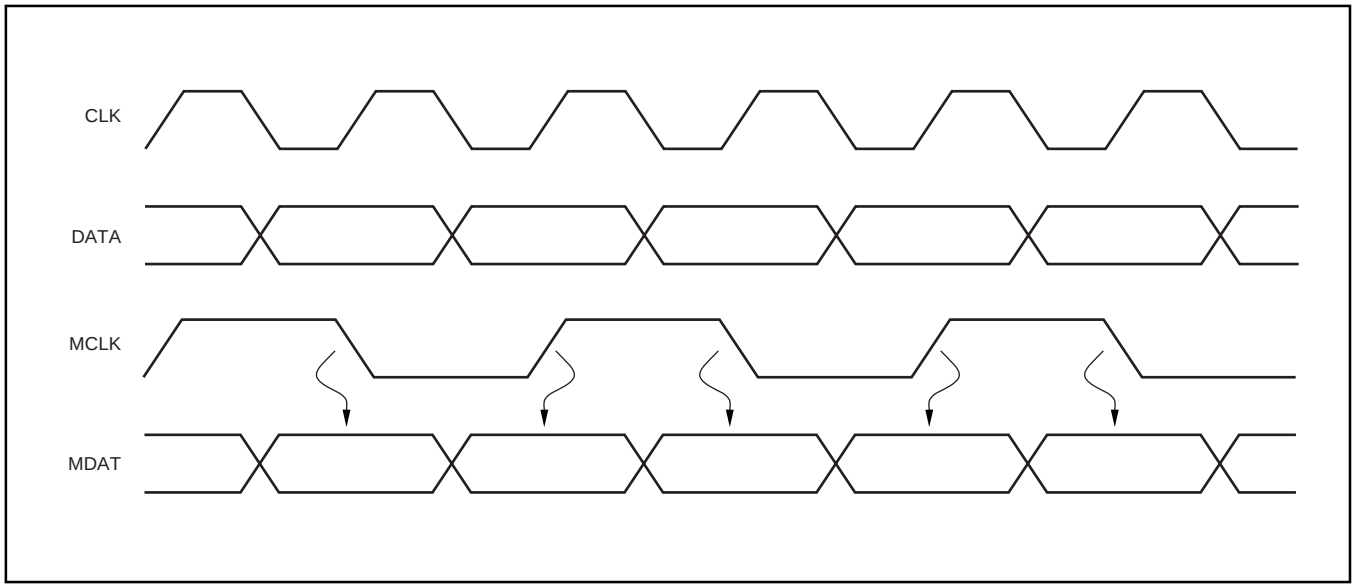


FIGURE 7. Signal Timing in Mode 1.

Mode 2

In mode 2, M0 is low and M1 is HIGH (see Table I). The control signal coming from the decoder enables the internal RC oscillator that provides the clock signal INTCLK as an input to MUX1. Another control signal coming from the decoder positions MUX1 so that the output signal that is the input signal to the code generator is INTCLK. The output signal MDAT comes from the code generator because the control signal from the decoder positions MUX3 for that operation. The DATA signal coming from the delta-sigma modulator enters the code generator, where it combines with the clock signal, and twinned binary coding is implemented as split phase or Manchester coding, providing the output signal for MUX3. The MCLK output clock is not active, as multiplexers MUX2 and MUX4 are positioned for this mode controlled by the control signals coming from the decoder. The signals timings for mode 2 operation are presented in Figure 8. In this mode, the DSP or µC need to derive the clock signal from the received waveform itself. Different clock recovery networks can be implemented.

Mode 3

Mode 3 is similar to mode 0; the only difference is that an external clock (EXTCLK) is provided. In mode 3, both input signals M0 and M1 are HIGH (see Table I). The control signal coming from the decoder disables the internal RC oscillator. The input signal EXTCLK provides the clock signal as an input to MUX1. The control signal coming from the decoder positions MUX1 so that the output signal that is the input signal to the code generator is EXTCLK. The output signal MDAT is the DATA signal coming directly from the delta-sigma modulator because the control signal from the decoder positions MUX3 for that operation. The signal timings for mode 3 operation are presented in Figure 9. In this mode, the DSP or µC read data on every falling edge of the input clock.

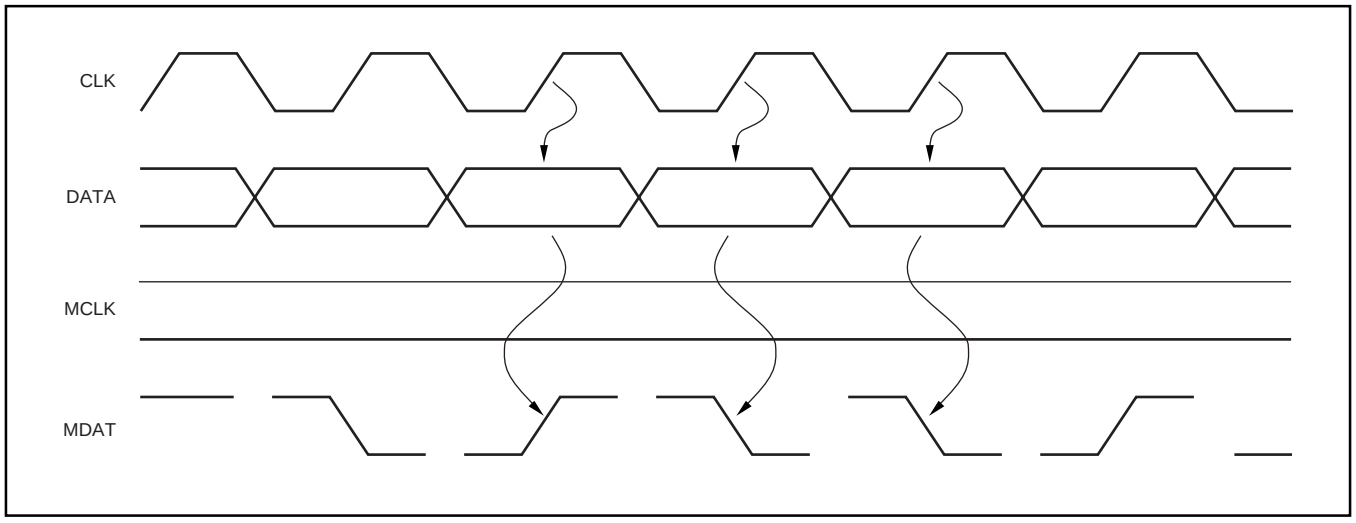


FIGURE 8. Signal Timing in Mode 2.

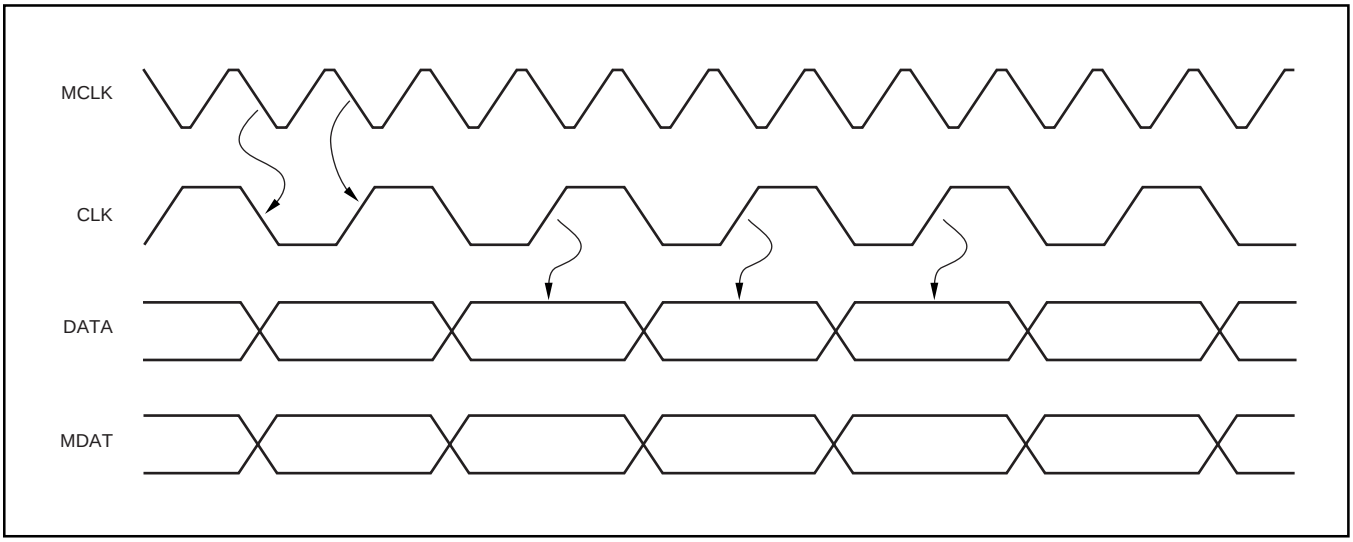


FIGURE 9. Signal Timing in Mode 3.

APPLICATIONS

Mode 0 operation in a typical application is shown in Figure 10. Measurement of the motor phase current is done via the shunt resistor. For better performance, both signals are filtered. R_2 and C_2 filter noise on the noninverting input signal, R_3 and C_3 filter noise on the inverting input signal, and C_4 in combination with R_2 and R_3 filter the common-mode input noise. In this configuration, the shunt resistor is connected via three wires with the ADS1202.

The power supply is taken from the upper gate driver power supply. A decoupling capacitor of 0.1µF is recommended for filtering the power supply. If better filtering is required, an additional 1µF to 10µF capacitor can be added.

The control lines M0 and M1 are both LOW while the part is operating in mode 0. Two output signals, MCLK and MDAT, are connected directly to the optocoupler. The optocoupler can be connected to transfer a direct or inverse signal because the output stage has the capacity to source and sink the same current. The discharge resistor is not needed in parallel with optocoupler diodes because the output driver has the capacity to keep the LED diode out of the charge.

The DSP can be directly connected at the output of two channels of the optocoupler, C28x or C24x. In this configuration, the signals arriving at C28x or C24x are standard delta-sigma modulator signals and are connected directly to the SPICLK and SPISIMO pins. Being a delta-sigma converter, there is no need to have word sync on the serial data, so an SPI is ideal for connection. McBSP would work as well in SPI mode.

When component reduction is necessary, the ADS1202 can operate in mode 2, as shown in Figure 11. M1 is HIGH and M0 is LOW. Only the noninverting input signal is filtered. R_2 and C_2 filter noise on the input signal. The inverting input is directly connected to the GND pin, which is simultaneously connected to the shunt resistor.

The output signal from the ADS1202 is Manchester coded. In this case, only one signal is transmitted. For that reason, one optocoupler channel is used instead of two channels, as in the previous example of Figure 10. Another advantage of this configuration is that the DSP will use only one line per channel instead of two. That permits the use of smaller DSP packages in the application.

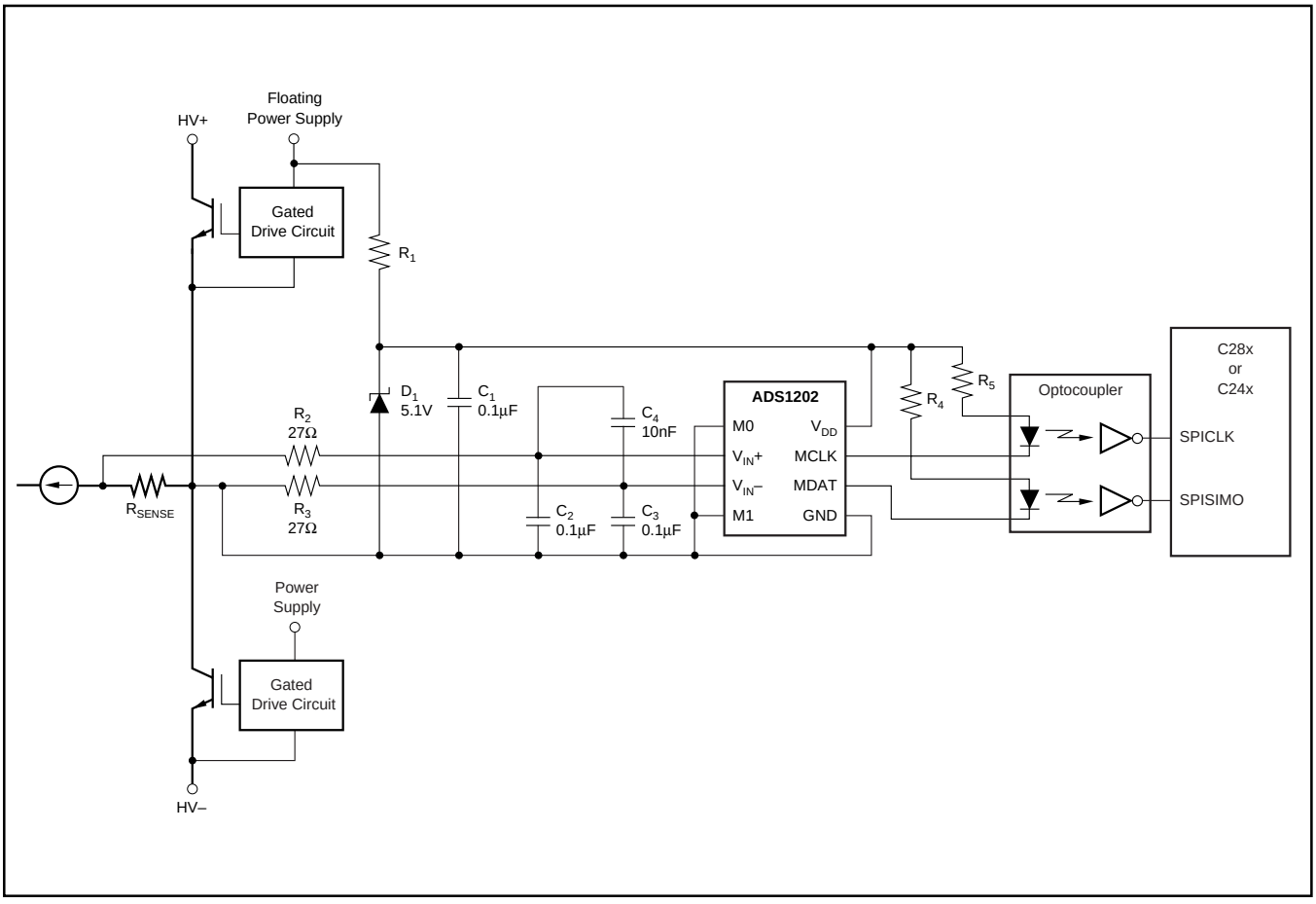


FIGURE 10. Application Diagram in Mode 0.

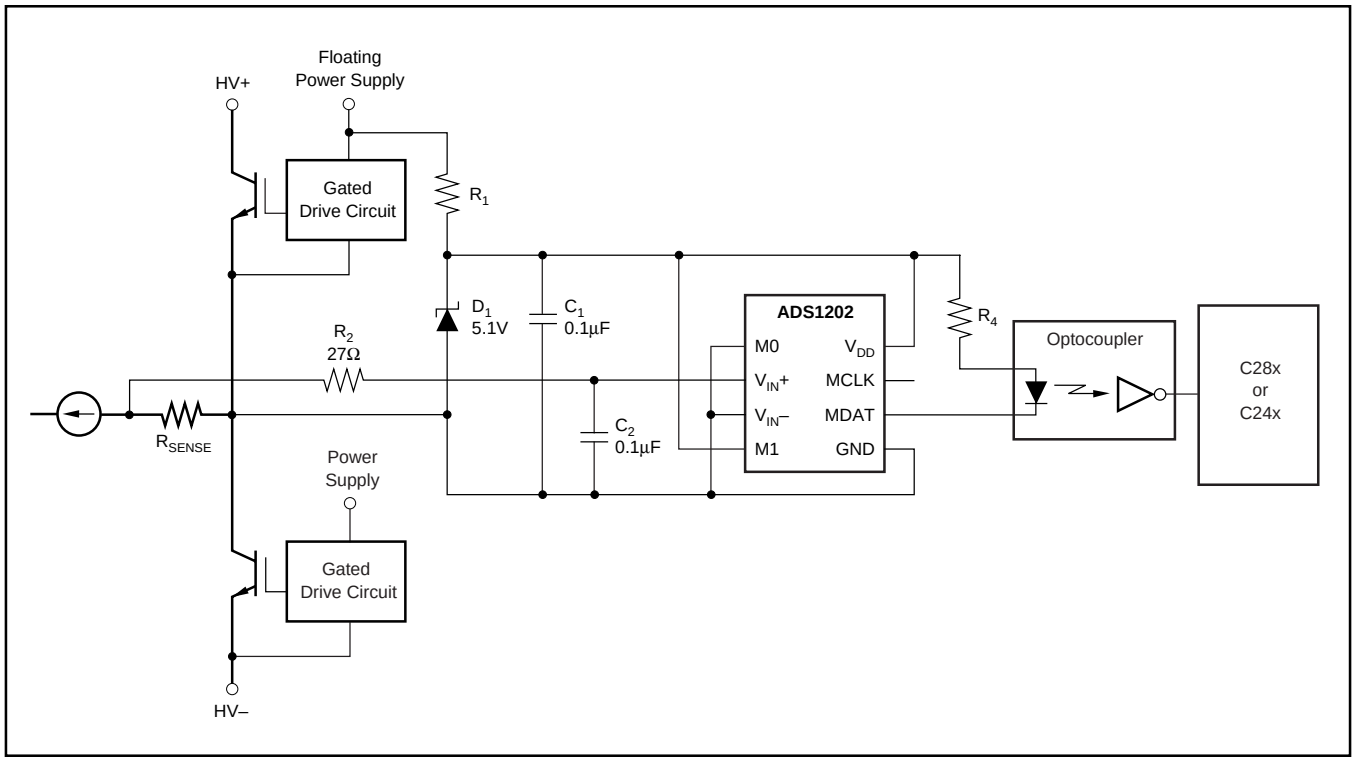


FIGURE 11. Application Diagram in Mode 2.

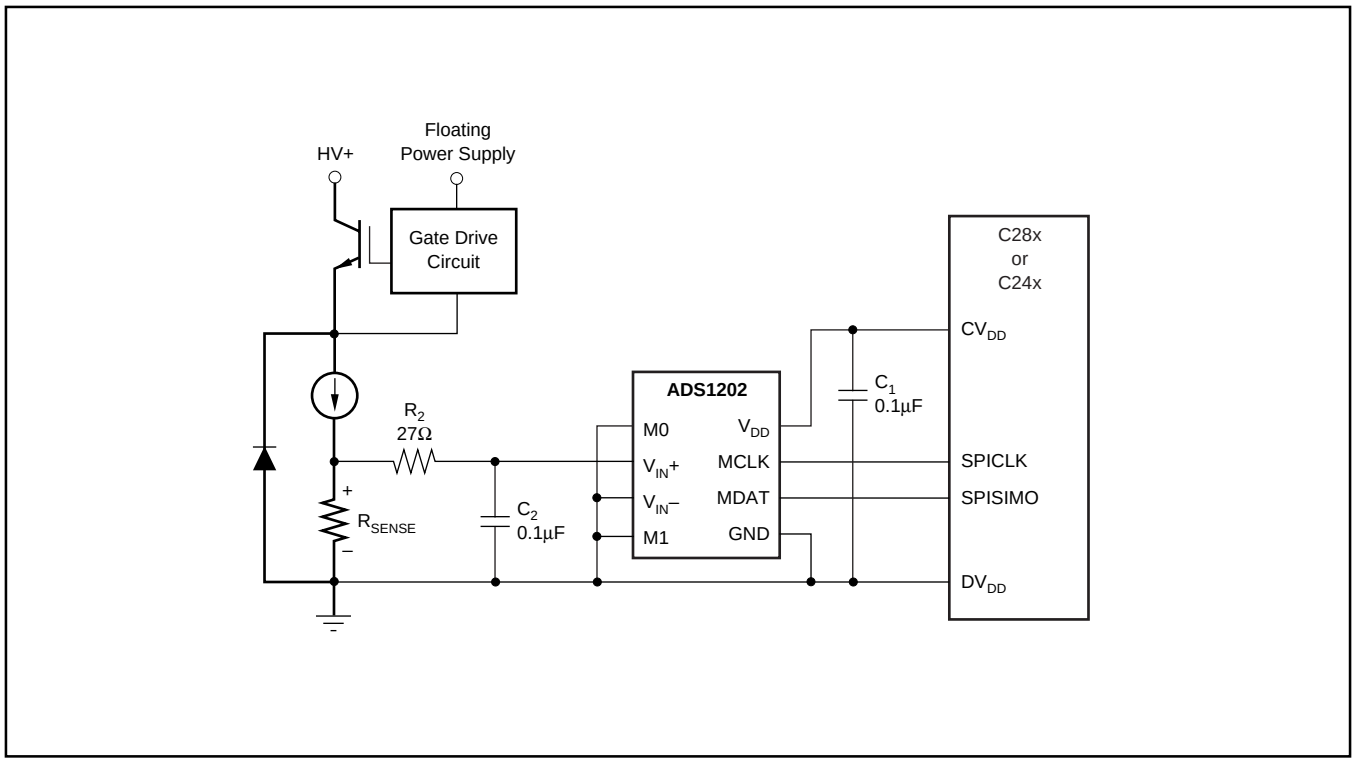


FIGURE 12. Application Diagram without Galvanical Isolation in Mode 0.

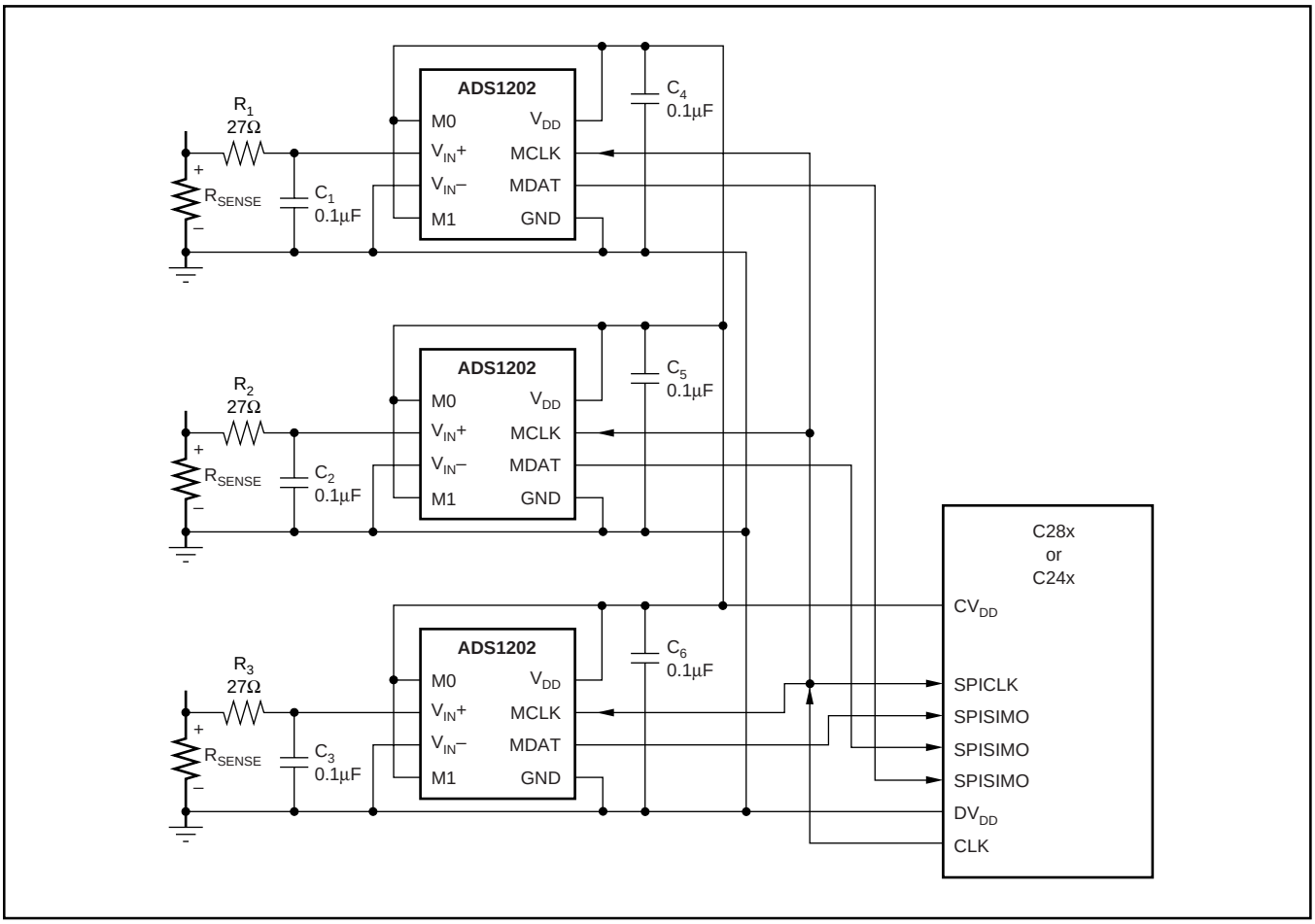


FIGURE 13. Parallel Operation of ADS1202 in Mode 3.

LAYOUT CONSIDERATIONS

POWER SUPPLIES

The ADS1202 requires only one power supply (V_{DD}). If there are separate analog and digital power supplies on the board, a good design approach is to have the ADS1202 connected to the analog power supply. Another possible approach to control the noise is the use of a resistor on the power supply. The connection can be made between the ADS1202 power-supply pins via a 10Ω resistor. The combination of this resistor and the decoupling capacitors between the power-supply pins on the ADS1202 provide some filtering. The analog supply that is used must be well regulated and generate low noise. For designs requiring higher resolution from the ADS1202, power-supply rejection will be a concern. The digital power supply has high-frequency noise that can be capacitively coupled into the analog portion of the ADS1202. This noise can originate from switching power supplies, microprocessors, or digital signal processors. High-frequency noise will generally be rejected by the external digital filter at integer multiples of MCLK. Just below and above these frequencies, noise will alias back into the passband of the digital filter, affecting the conversion result. Inputs to the ADS1202, such as V_{IN}+, V_{IN}–, and MCLK should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current. Experimentation may be the best way to determine the appropriate connection between the ADS1202 and different power supplies.

GROUNDING

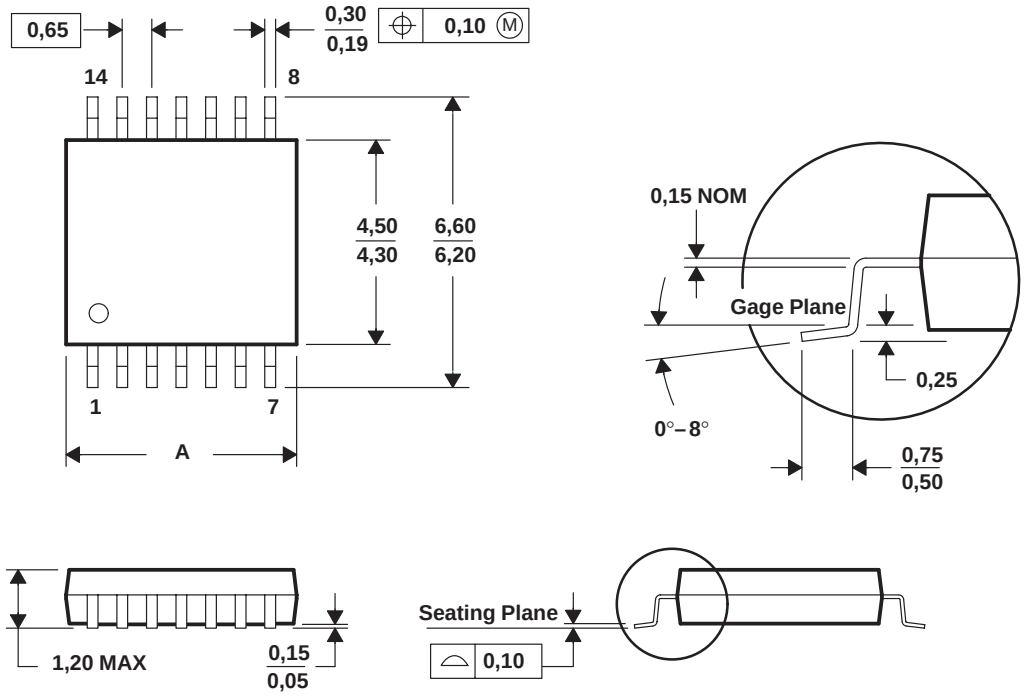
Analog and digital sections of the design must be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. Do not join the ground planes, but connect the two with a moderate signal trace underneath the converter. For multiple converters, connect the two ground planes as close as possible to one central location for all of the converters. In some cases, experimentation may be required to find the best point to connect the two planes together.

DECOUPLING

Good decoupling practices must be used for the ADS1202 and for all components in the design. All decoupling capacitors, specifically the 0.1µF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1µF and 10µF capacitor, in parallel with the 0.1µF ceramic capacitor, must be used to decouple V_{DD} to GND. At least one 0.1µF ceramic capacitor must be used to decouple V_{DD} to GND, as well as for the digital supply on each digital component.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1202IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZ1202	Samples
ADS1202IPWT	ACTIVE	TSSOP	PW	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZ1202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

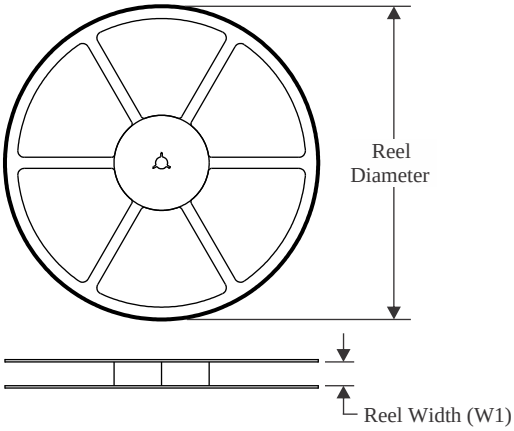
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

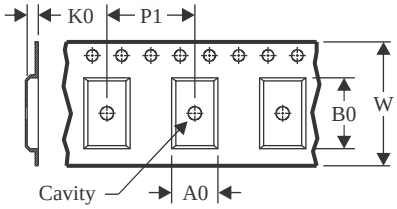
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

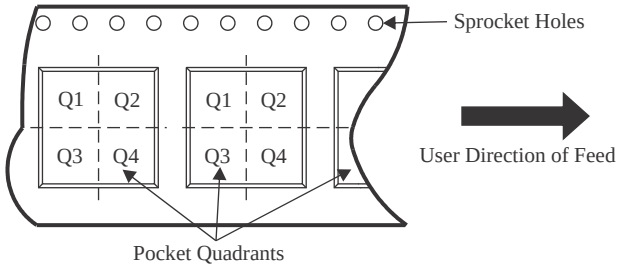


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

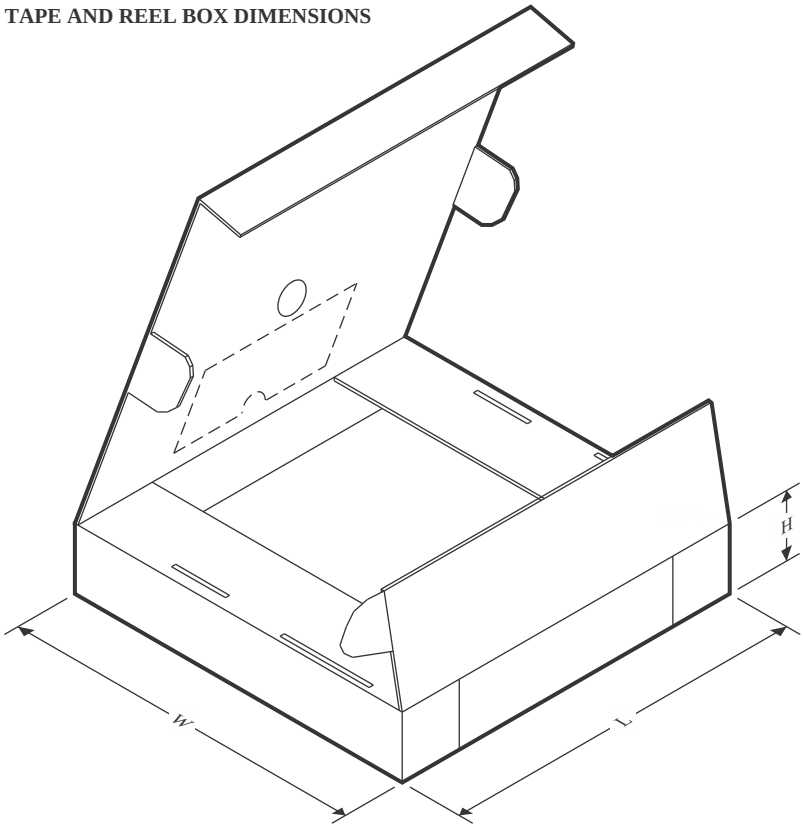
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1202IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

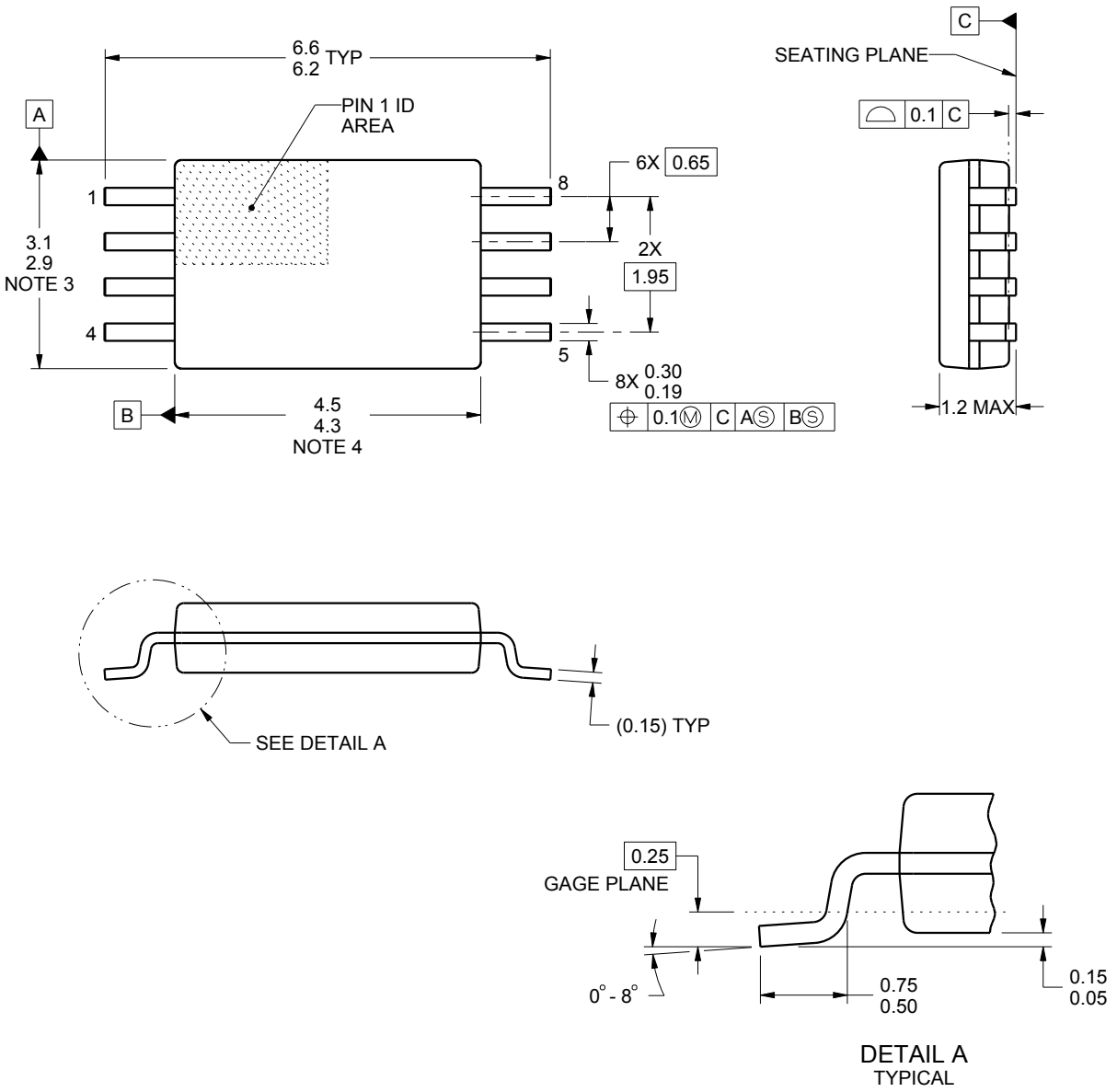
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1202IPWR	TSSOP	PW	8	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0008A

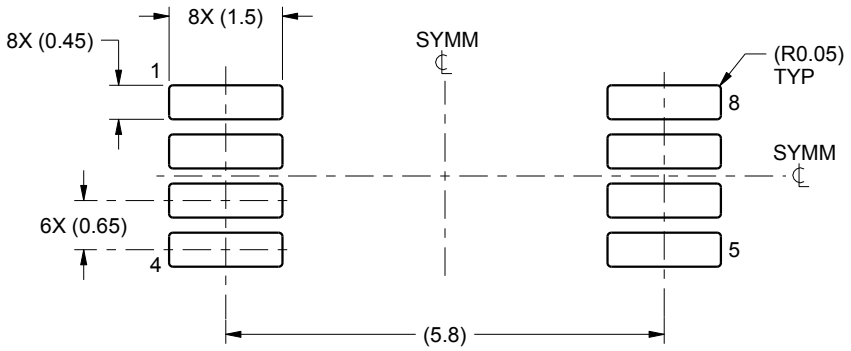
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

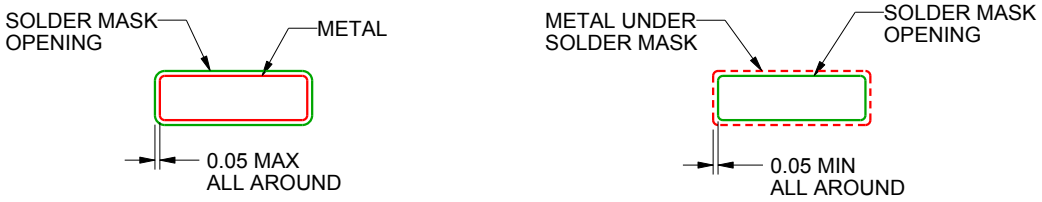


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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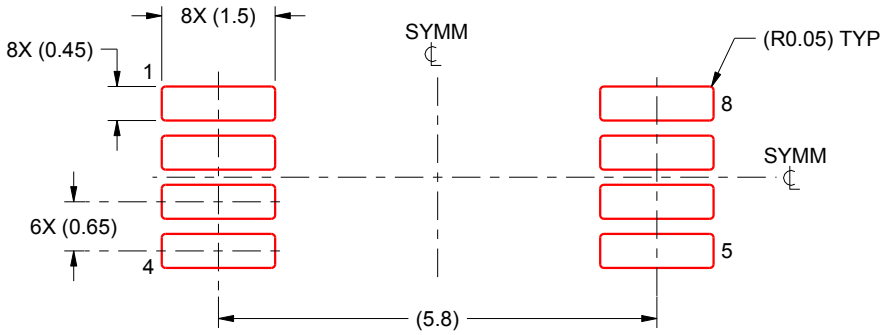
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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