THE DATASHEET OF

EMB1412MYE/NOPB

EMB1412 MOSFET Gate Driver

1 Features

- Compound CMOS and Bipolar Outputs Reduce Output Current Variation
- 7 A Sink/3 A Source Current
- Fast Propagation Times (25 ns Typical)
- Fast Rise and Fall Times (14 ns/12 ns Rise/Fall with 2 nF Load)
- Inverting and Non-Inverting Inputs Provide Either Configuration with a Single Device
- Supply Rail Under-Voltage Lockout Protection
- Dedicated Input Ground (IN_REF) for Split Supply or Single Supply Operation
- Thermally Enhanced 8-Pin VSSOP Package
- Output Swings from V_{CC} to V_{EE} Which can be Negative Relative to Input Ground

2 Applications

- Li-Ion Battery Management Systems
- Hybrid and Electric Vehicles
- Grid Storage
- 48 V Systems Supply
- UPS

3 Description

The EMB1412 MOSFET gate driver provides high peak gate drive current in 8-lead exposed-pad VSSOP package, with improved power dissipation required for high frequency operation. The compound output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 7-A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is provided to prevent damage to the MOSFET due to insufficient gate turn-on voltage. The EMB1412 provides both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive with a single device type.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
EMB1412	HVSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

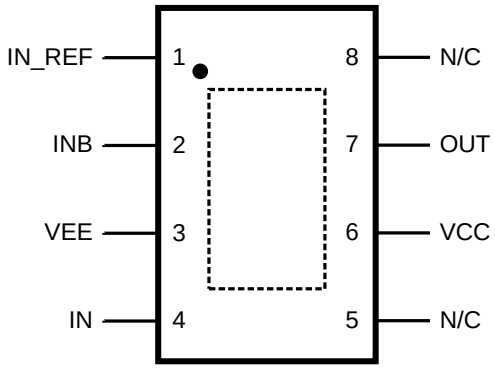
Table of Contents

4 Revision History

Changes from Revision A (May 2013) to Revision B	Page
• Added Handling Ratings Table	4
• Changed layout of National Data Sheet to TI format.	8

5 Pin Configuration and Functions

VSSOP (DGN)
8 Pins
Top View



Pin Functions

PIN	NAME	DESCRIPTION	APPLICATION INFORMATION
1	IN_REF	Ground reference for control inputs	Connect to power ground (VEE) for standard positive only output voltage swing. Connect to system logic ground when VEE is connected to a negative gate drive supply.
2	INB	Inverting input pin	TTL compatible thresholds. Connect to IN_REF when not used.
3	VEE	Power ground for driver outputs	Connect to either power ground or a negative gate drive supply for positive or negative voltage swing.
4	IN	Non-inverting input pin	TTL compatible thresholds. Pull up to VCC when not used.
5, 8	N/C	Not internally connected	
6	VCC	Positive Supply voltage input	Locally decouple to VEE. The decoupling capacitor should be located close to the chip.
7	OUT	Gate drive output	Capable of sourcing 3 A and sinking 7 A. Voltage swing of this output is from VEE to VCC.
- - -	Exposed Pad	Exposed Pad, underside of package	Internally bonded to the die substrate. Connect to VEE ground pin for low thermal impedance.

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
V_{CC} to V_{EE}	−0.3	15	V
V_{CC} to IN_REF	−0.3	15	V
IN/INB to IN_REF	−0.3	15	V
IN_REF to V_{EE}	−0.3	5	V
Maximum junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating Junction Temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		EMB1412 VSSOP (DGN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60(2)	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	4.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The primary goal of the thermal management is to maintain the integrated circuit (IC) junction temperature (T_J) below a specified limit to ensure reliable long term operation. The maximum T_J of IC components should be estimated in worst case operating conditions. The junction temperature can be calculated based on the power dissipated on the IC and the junction to ambient thermal resistance $R_{\theta JA}$ for the IC package in the application board and environment. The $R_{\theta JA}$ is not a given constant for the package and depends on the PCB design and the operating environment.

6.5 Electrical Characteristics

T_J = −40°C to 125°C, V_{CC} = 12 V, INB = IN_REF = V_{EE} = 0 V, No Load on output, unless otherwise specified.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{CC}	V_{CC} Operating Range	V_{CC} – IN_REF and V_{CC} - V_{EE}	3.5		14	V
UVLO	V_{CC} Under-voltage Lockout (rising)	V_{CC} – IN_REF	2.4	3.0	3.5	V
V_{CCH}	V_{CC} Under-voltage Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current			1.0	2.0	mA
CONTROL INPUTS						
V_{IH}	Logic High		2.3			V
V_{IL}	Logic Low				0.8	V
V_{thH}	High Threshold		1.3	1.75	2.3	V
V_{thL}	Low Threshold		0.8	1.35	2.0	V
HYS	Input Hysteresis			400		mV

Electrical Characteristics (continued)

T_J = −40°C to 125°C, V_{CC} = 12 V, INB = IN_REF = V_{EE} = 0 V, No Load on output, unless otherwise specified.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input Current Low	IN = INB = 0 V	-1	0.1	1	µA
I_{IH}	Input Current High	IN = INB = V_{CC}	-1	0.1	1	µA
OUTPUT DRIVER						
R_{OH}	Output Resistance High	I_{OUT} = -10 mA (1)		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = 10 mA (1)		1.4	2.5	Ω
I_{SOURCE}	Peak Source Current	OUT = V_{CC}/2, 200 ns pulsed current		3		A
I_{SINK}	Peak Sink Current	OUT = V_{CC}/2, 200 ns pulsed current		7		A
SWITCHING CHARACTERISTICS						
td1	Propagation Delay Time Low to High, IN/ INB rising (IN to OUT)	C_{LOAD} = 2 nF		25	40	ns
td2	Propagation Delay Time High to Low, IN / INB falling (IN to OUT)	C_{LOAD} = 2 nF		25	40	ns
tr	Rise time	C_{LOAD} = 2 nF		14		ns
tf	Fall time	C_{LOAD} = 2 nF		12		ns
LATCHUP PROTECTION						
	AEC –Q100, METHOD 004	T_J = 150°C		500		mA
THERMAL RESISTANCE						
$R_{\theta JA}$	Junction to Ambient, 0 LFPM Air Flow	VSSOP Package		60		°C/W
$R_{\theta JC}$	Junction to Case	VSSOP Package		4.7		°C/W

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

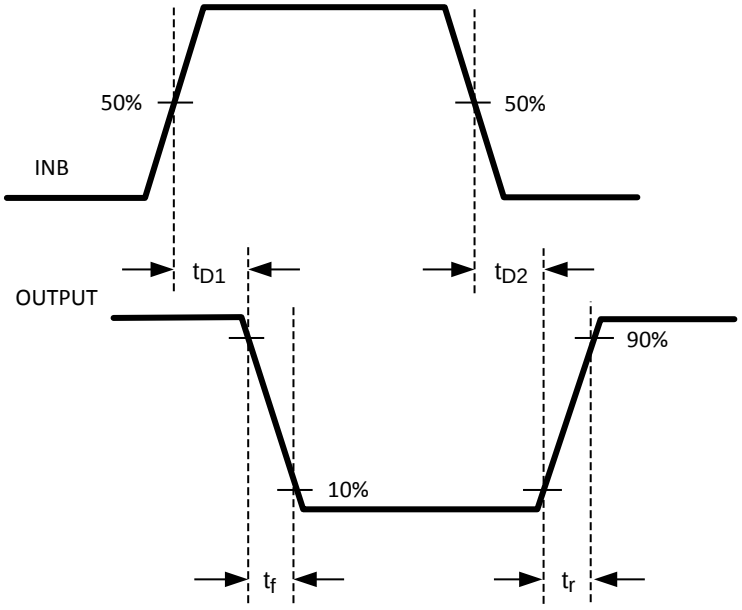


Figure 1. (A) Inverting

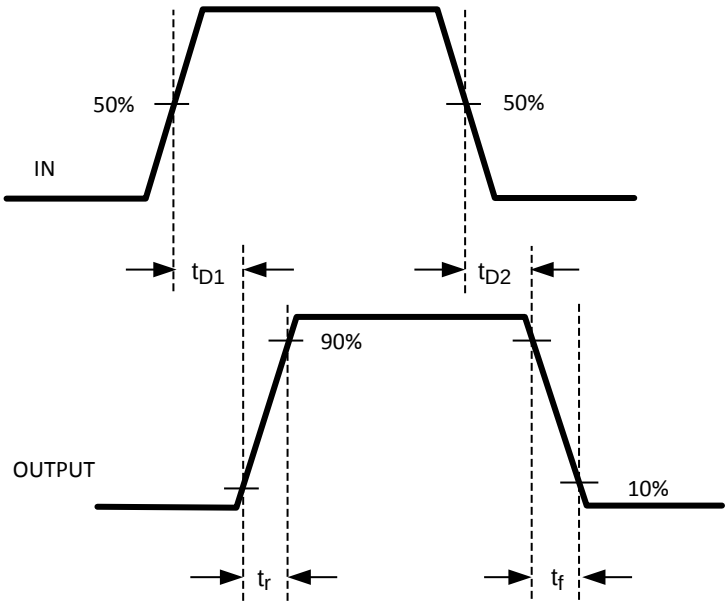


Figure 2. (B) Non-Inverting

7 Detailed Description

7.1 Overview

The EMB1412 is a high speed, high peak current (7 A) single channel MOSFET driver. The high peak output current of the EMB1412 will switch power MOSFETs on and off with short rise and fall times, thereby reducing switching losses considerably. The EMB1412 includes both inverting and non-inverting inputs that give the user flexibility to drive the MOSFET with either active low or active high logic signals. The driver output stage consists of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical Miller plateau region of the MOSFET V_{GS}, while the MOS device provides rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the VEE pin.

The control inputs of the driver are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and separate input/output ground pins provide the option of single supply or split supply configurations. When driving the MOSFET gates from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground.

The isolated input and output stage grounds provide the capability to drive the MOSFET to a negative V_{GS} voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the EMB1412 inputs. The VEE pin is connected to a negative bias supply that can range from the IN_REF potential to as low as 14 V below the V_{CC} gate drive supply. For reliable operation, the maximum voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14 V.

The minimum recommended operating voltage between V_{CC} and IN_REF is 3.5 V. An Under-Voltage Lock Out (UVLO) circuit is included in the EMB1412 which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.8 V the driver is disabled and the output pin is held in the low state. The driver will resume normal operation when the V_{CC} to IN_REF differential voltage exceeds 3 V.

8 Layout

8.1 Layout Guidelines

Attention must be given to board layout when using EMB1412. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the VCC and VEE pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET.
2. Proper grounding is crucial. The driver needs a very low impedance path for current return to ground avoiding inductive loops. Two paths for returning current to ground are a) between EMB1412 IN_REF pin and the ground of the circuit that controls the driver inputs and b) between EMB1412 VEE pin and the source of the power MOSFET being driven. Both paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. These ground paths should be distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the EMB1412. With rise and fall times in the range of 10 to 30 nsec, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated when driving large capacitive loads.
3. If either channel is not being used, the respective input pin (IN or INB) should be connected to either V_{EE} or V_{CC} to avoid spurious output signals.

8.2 Thermal Performance

The primary goal of the thermal management is to maintain the integrated circuit (IC) junction temperature (T_J) below a specified limit to ensure reliable long term operation. The maximum T_J of IC components should be estimated in worst case operating conditions. The junction temperature can be calculated based on the power dissipated on the IC and the junction to ambient thermal resistance $R_{\theta JA}$ for the IC package in the application board and environment. The $R_{\theta JA}$ is not a given constant for the package and depends on the PCB design and the operating environment.

9 Device and Documentation Support

9.1 Trademarks

All trademarks are the property of their respective owners.

9.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
EMB1412MY/NOPB	LIFEBUY	HVSSOP	DGN	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SA3B	
EMB1412MYE/NOPB	LIFEBUY	HVSSOP	DGN	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SA3B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

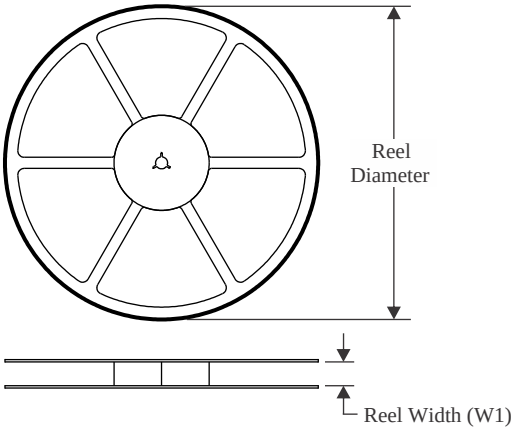
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

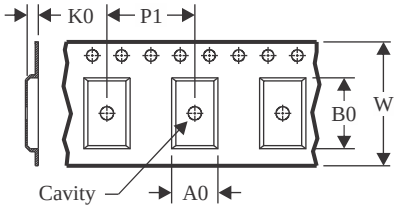
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

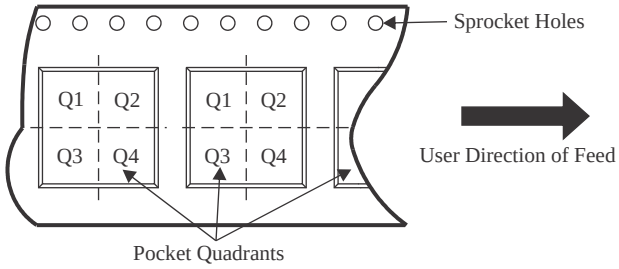


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

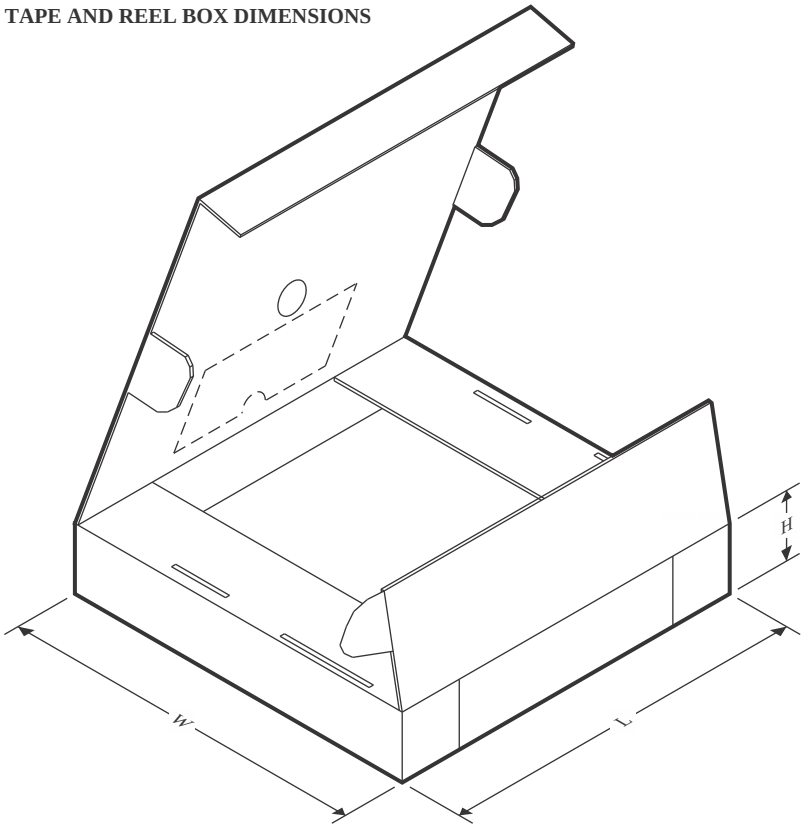
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
EMB1412MY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
EMB1412MYE/NOPB	HVSSOP	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

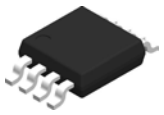


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
EMB1412MY/NOPB	HVSSOP	DGN	8	1000	210.0	185.0	35.0
EMB1412MYE/NOPB	HVSSOP	DGN	8	250	210.0	185.0	35.0

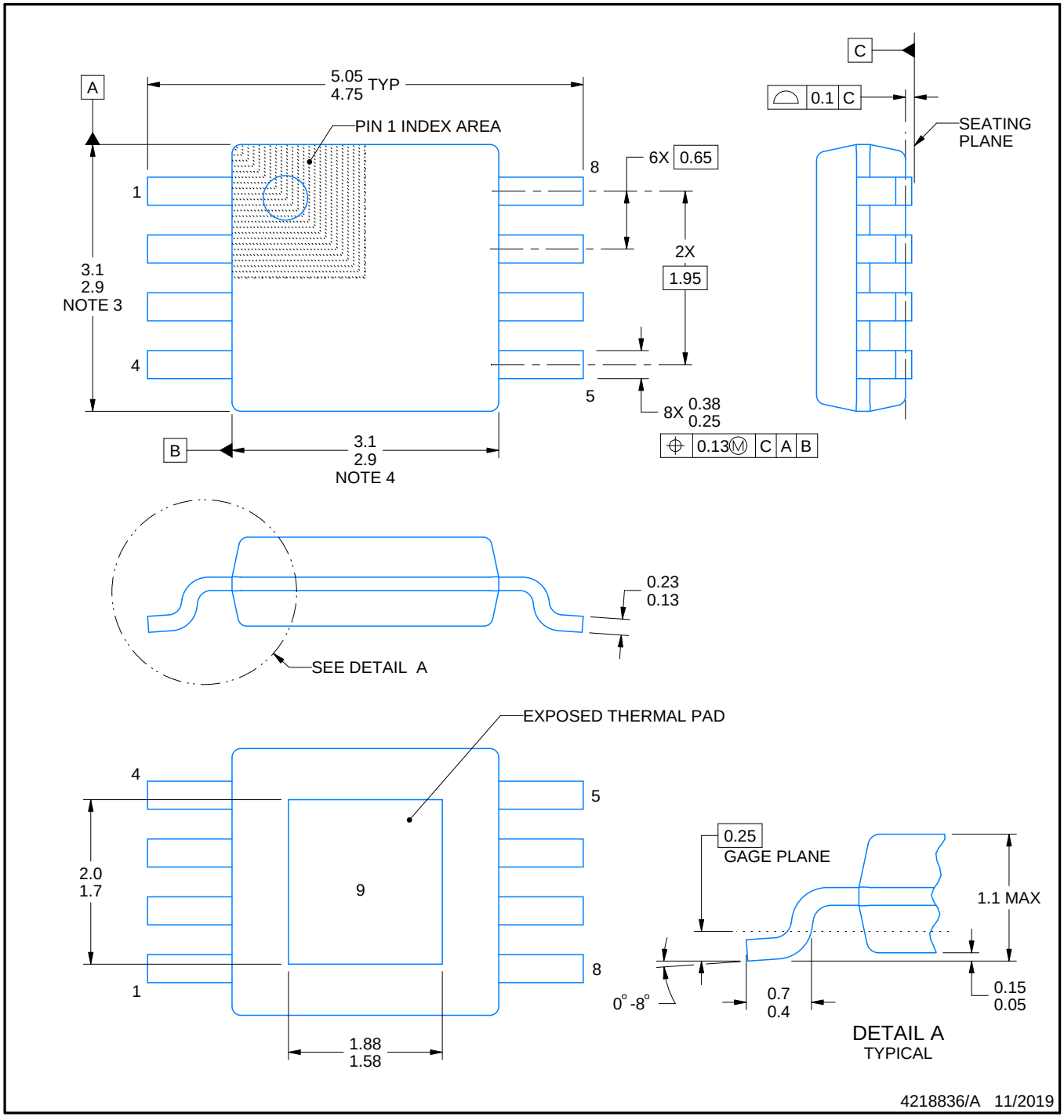
PACKAGE OUTLINE

DGN0008A



PowerPAD™ VSSOP - 1.1 mm max height

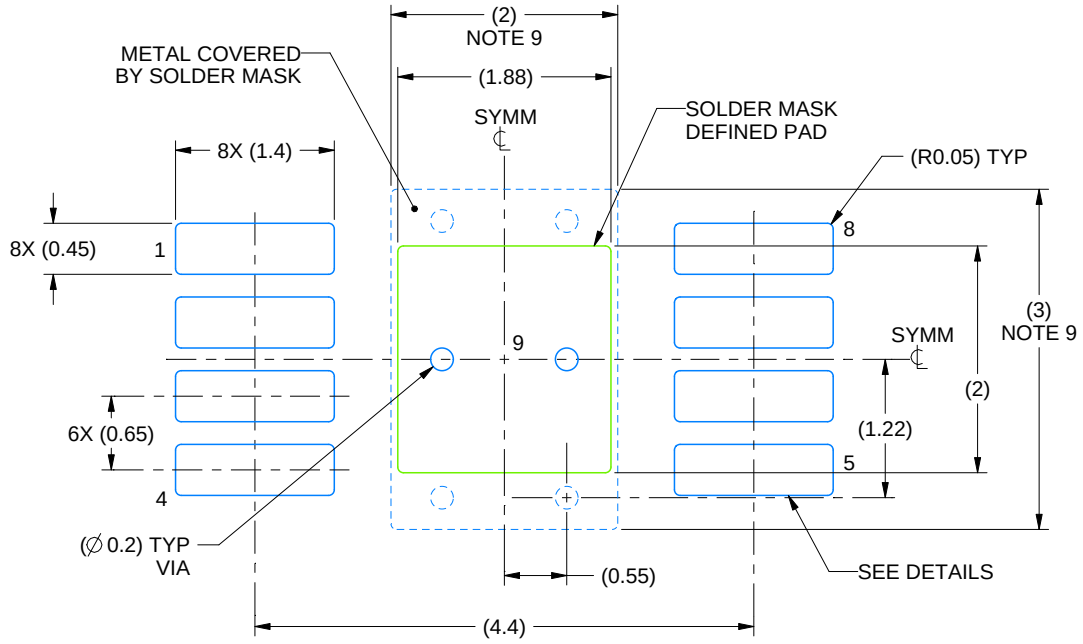
SMALL OUTLINE PACKAGE



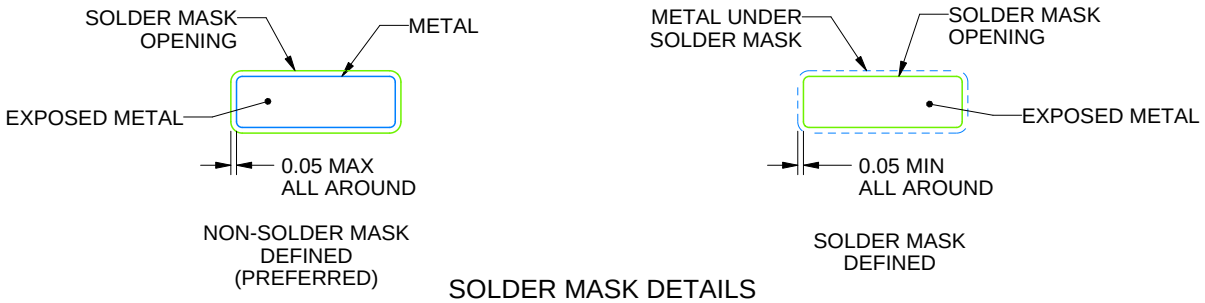
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

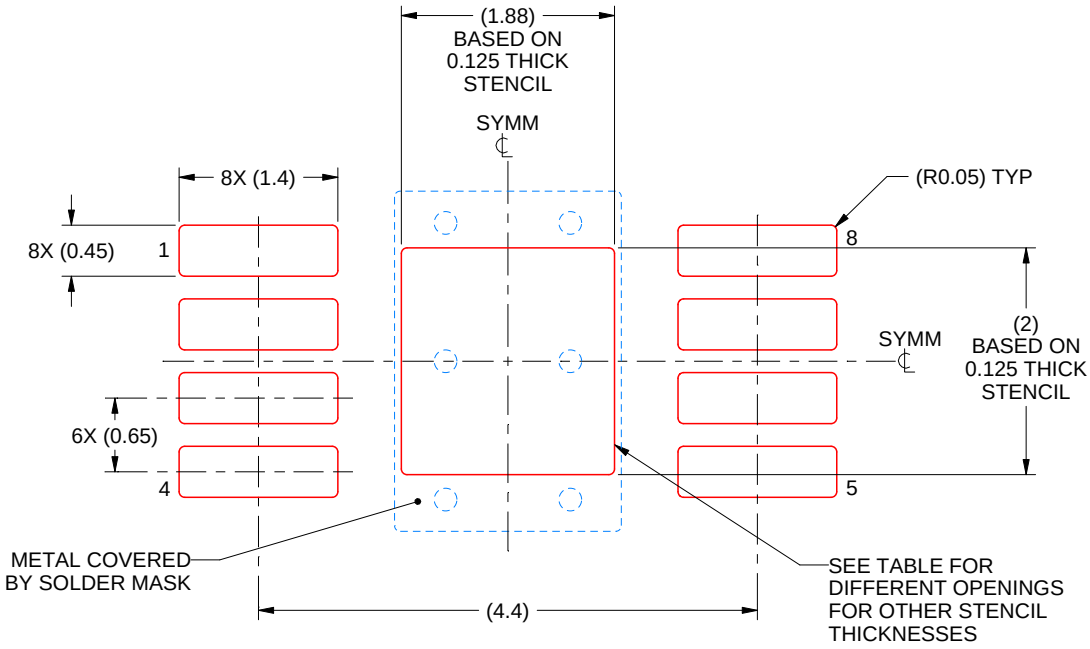
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

4218836/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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