WINSOURCE ELECTRONICS

THE DATASHEET OF

DS1212Q

DS1212
Nonvolatile Controller x 16 Chip

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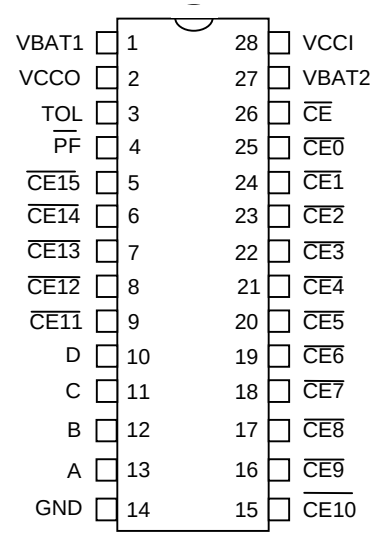
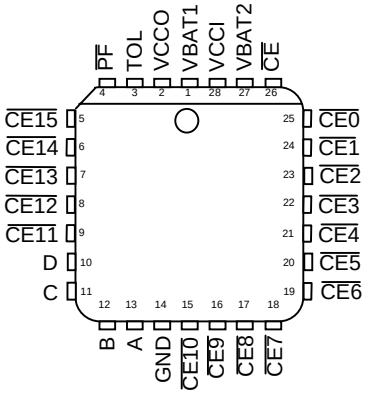
FEATURES

- Converts full CMOS RAM into nonvolatile memory
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power-fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power-fail detection
- Optional 28-pin PLCC surface mount package
- Optional industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT



28-Pin DIP (600-mil)
See Mech. Drawings Section



28-Pin PLCC
See Mech. Drawings Section

PIN DESCRIPTION

A, B, C, D	- Address Inputs
$\overline{CE}$	- Chip Enable
$\overline{CE0}$ - $\overline{CE15}$	- Chip Enable Outputs
GND	- Ground
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
TOL	- Power Supply Tolerance
V_{CCI}	- +5V Supply
V_{CCO}	- RAM Supply
$\overline{PF}$	- Power Fail

DESCRIPTION

The DS1212 Nonvolatile Controller x16 Chip is a CMOS circuit that solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply the RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process that affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 Nonvolatile Controller chip and lithium batteries, nonvolatile RAM operation can be achieved for up to 16 CMOS memories.

OPERATION

The DS1212 performs six circuit functions required to decode and battery back up a bank of up to 16 RAMs. First, the 4-to-16 decoder provides selection of one of 16 RAMs. Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function the DS1212 provides is power-fail detection. It constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.75 volts or 4.5 volts, depending on the level of tolerance Pin 3, a precision comparator outputs a power-fail detect signal to the decoder/chip enable logic and the $\overline{PF}$ signal is driven low. The $\overline{PF}$ signal will remain low until V_{CCI} is back in normal limits.

The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$ - $\overline{CE15}$) to within 0.2 volts of V_{CCI} or battery supply. If $\overline{CE}$ is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents corruption of data. Power-fail detection occurs in the range of 4.75 volts to 4.5 volts with tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power-fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4-to-16 decoder, shown in Figure 1.

The fifth function the DS1212 performs is a battery status warning so that data loss is avoided. Each time the circuit is powered up, the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted.

The sixth function of the DS1212 provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

NONVOLATILE CONTROLLER/DECODER Figure 1

INPUTS					OUTPUTS																
$\overline{CE}$	D	C	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	$\overline{CE5}$	$\overline{CE6}$	$\overline{CE7}$	$\overline{CE8}$	$\overline{CE9}$	$\overline{CE10}$	$\overline{CE11}$	$\overline{CE12}$	$\overline{CE13}$	$\overline{CE14}$	$\overline{CE15}$	$\overline{PF}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
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L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
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L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
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L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = High Level

L = Low Level

X = Irrelevant

Note: V_{CCI} input is 250 mV lower when TOL PIN3 = V_{CCO}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 3 = V_{CCO} Supply Voltage	V_{CCO}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} = 4.75 to 5.5V PIN 3 = GND)
(0°C to 70°C; V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Current @ V_{CCO}= V_{CCI}-0.2	I_{CCO1}			80	mA	1, 4 ,10
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CE0}$ - $\overline{CE15}$, $\overline{PF}$ Output @ 2.4V	I_{OH}	-1.0			mA	5
$\overline{CE0}$ - $\overline{CE15}$, $\overline{PF}$ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CCO})	V_{CCTP}	4.25	4.37	4.49	V	1

(0°C to 70°C; V_{CCI} < V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE0}$ -CE15 Output	V_{OHL}	V_{BAT}-0.2			V	3, 7
Battery Current	I_{BAT}			0.1	µA	2, 3
Battery Backup Current @ V_{CCO} = V_{BAT1} – 0.5V	I_{CC2}			100	µA	6, 10, 11

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

(0°C to 70°C; V_{CCI} = 4.75 to 5.5V, PIN 3 = GND)
(0°C to 70°C; V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

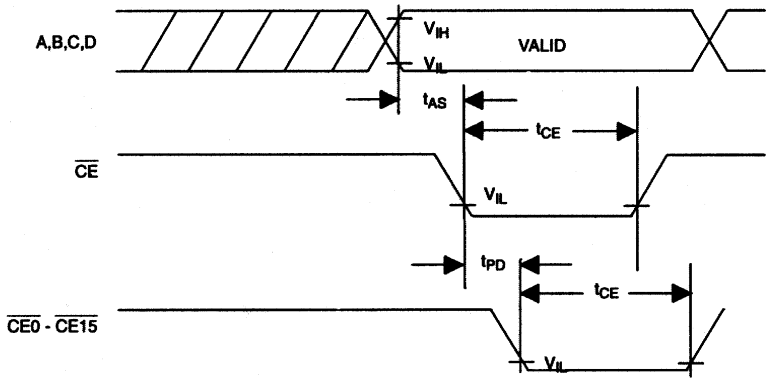
AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

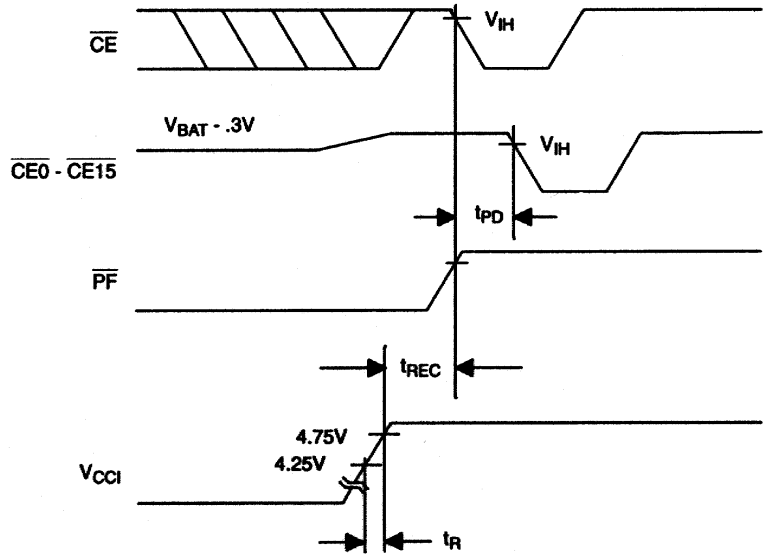
(0°C to 70°C; V_{CCI} < 4.75V, PIN 3 = GND)
(0°C to 70°C; V_{CCI} < 4.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power-Down	t_F	300			µs	
V_{CC} Slew Rate Power-Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power-Up	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7, 8
Power Fail to $\overline{PF}$ Low	t_{PFL}	300			µs	

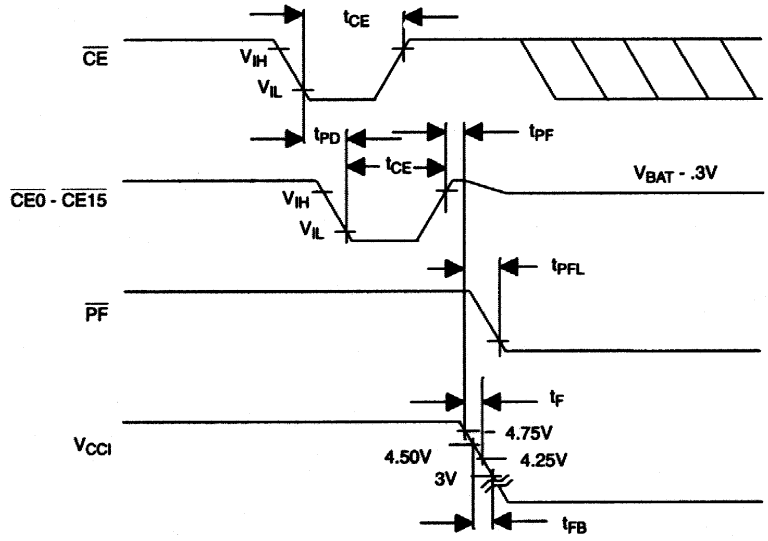
TIMING DIAGRAM: DECODER



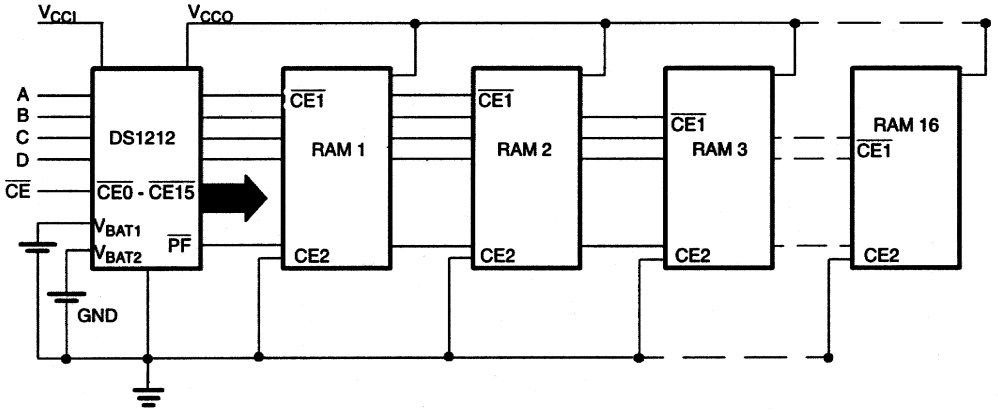
TIMING DIAGRAM: POWER-UP



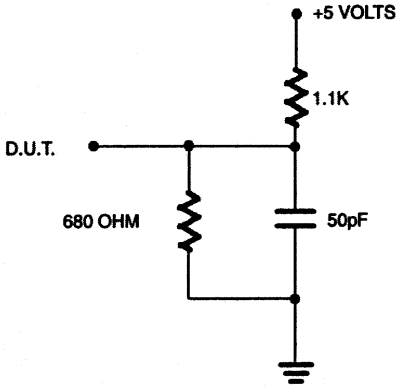
TIMING DIAGRAM: POWER-DOWN



TYPICAL APPLICATION Figure 2



OUTPUT LOAD Figure 3



NOTES:

1. All voltages referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE15}$ open.
4. I_{CC01} is the maximum average load which the DS1212 can supply to the memories.
5. Measured with a load as shown in Figure 3.
6. I_{CC02} is the maximum average load current which the DS1212 can supply to the memories in the battery backup mode.
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE15}$ can only sustain leakage current in the battery backup mode.
8. t_{CE} max. must be met to ensure data integrity on power loss.
9. t_{AS} is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$ - $\overline{CE15}$) will be defined by inputs A through D with a propagation delay of t_{PD} from an A through D input change.
10. For applications where higher currents are required, please see the Battery Manager chip data sheet (DS1259).
11. The DS1212 has a 5 kohm resistor in series with the battery input. As current from the battery increases over 100 µA, the voltage drop will increase proportionately. The device cannot be damaged by higher currents in the battery path.

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