



**THE DATASHEET OF  
AT17LV002-10TQC**



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## Features

- EE Reprogrammable 2,097,152 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- In-System Programmable via 2-wire Bus
- Simple Interface to SRAM FPGAs
- Compatible with Atmel AT6000, AT40K and AT94K Devices, Altera FLEX<sup>®</sup>, APEX<sup>™</sup> Devices, Lucent ORCA<sup>®</sup> FPGAs, Xilinx XC3000<sup>™</sup>, XC4000<sup>™</sup>, XC5200<sup>™</sup>, Spartan<sup>®</sup>, Virtex<sup>™</sup> FPGAs
- Cascadable Read Back to Support Additional Configurators or Higher-density Arrays
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available in 6 mm x 6 mm x 1 mm 8-lead LAP (Pin-compatible with 8-lead SOIC/VOIC Packages), 20-lead PLCC, 44-lead PLCC and 44-lead TQFP Packages (Pin-compatible Across Product Family)
- Emulation of Atmel's AT24CXXX Serial EEPROMs
- Available in 3.3V ± 10% LV and 5V ± 5% C Versions
- System-friendly READY Pin
- Low-power Standby Mode
- Replacement for AT17C/LV020

## Description

The AT17C002 and AT17LV002 (high-density AT17 Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for programming Field Programmable Gate Arrays. The AT17 Series is packaged in the popular 8-lead LAP, 20-lead PLCC, 44-lead PLCC and the 44-lead TQFP. The AT17 Series family uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices support a write protection mode and a system-friendly READY pin, which signifies a "good" power level to the FPGA and can be used to ensure reliable system power-up.

The AT17 Series Configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming System and Atmel's ATDH2225 ISP Cable.



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## FPGA Configuration EEPROM Memory

2-megabit

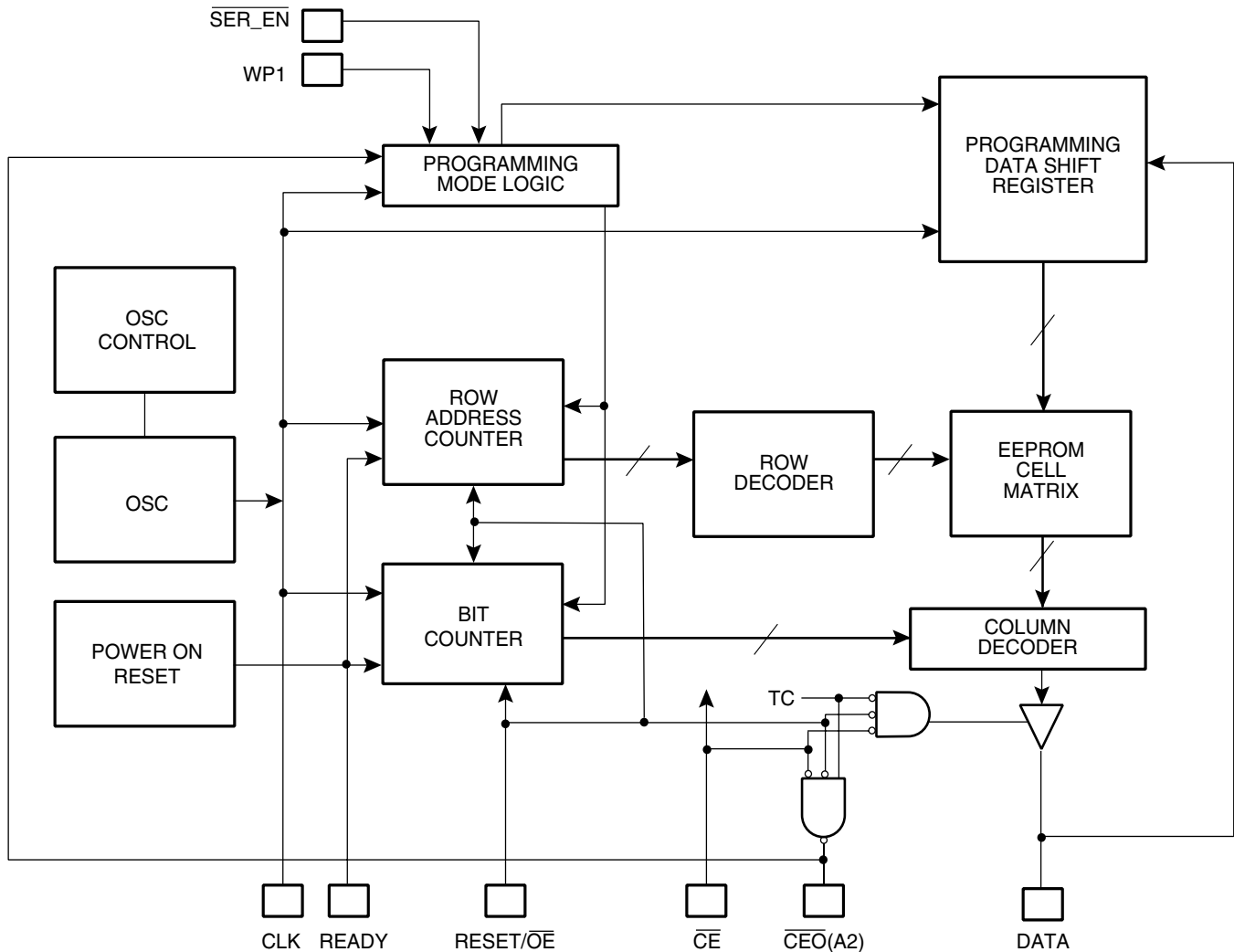
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**AT17C002**  
**AT17LV002**





## Block Diagram



## Device Description

The control signals for the configuration EEPROM ( $\overline{CE}$ ,  $\overline{RESET/OE}$  and  $CCLK$ ) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM  $\overline{RESET/OE}$  and  $\overline{CE}$  pins control the tri-state buffer on the DATA output pin and enable the address counter. When  $\overline{RESET/OE}$  is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The  $\overline{CE}$  pin also controls the output of the AT17 Series Configurator. If  $\overline{CE}$  is held High after the  $\overline{RESET/OE}$  reset pulse, the counter is disabled and the DATA output pin is tri-stated. When  $\overline{OE}$  is subsequently driven Low, the counter and the DATA output pin are enabled. When  $\overline{RESET/OE}$  is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of  $\overline{CE}$ .

When the configurator has driven out all of its data and  $\overline{CEO}$  is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe  $\overline{RESET/OE}$ .

## Pin Configurations

| 8 LAP Pin | 20 PLCC Pin | 44 TQFP Pin | 44 PLCC Pin | Name                         | I/O | Description   |
|-----------|-------------|-------------|-------------|------------------------------|-----|---|
| 1         | 2           | 40          | 2           | DATA                         | I/O | Three-state DATA output for configuration. Open-collector bi-directional pin for programming.   |
| 2         | 4           | 43          | 5           | CLK                          | I   | Clock input. Used to increment the internal address and bit counter for reading and programming.  |
| –         | 5           | 7           | 7           | WP1 <sup>(1)</sup>           | I   | WRITE PROTECT (1). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations.  |
| 3         | 6           | 13          | 19          | $\overline{\text{RESET/OE}}$ | I   | Output Enable (active High) and RESET (active Low) when $\overline{\text{SER\_EN}}$ is High. A Low level on $\overline{\text{RESET/OE}}$ resets both the address and bit counters. A High level (with $\overline{\text{CE}}$ Low) enables the data output driver. The logic polarity of this input is programmable as either $\overline{\text{RESET/OE}}$ or $\overline{\text{RESET/OE}}$ . For most applications, RESET should be programmed active Low. This document describes the pin as $\overline{\text{RESET/OE}}$ . |
| 4         | 8           | 15          | 21          | $\overline{\text{CE}}$       | I   | Chip Enable input (active Low). A Low level (with OE High) allows DCLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will <i>not</i> enable/disable the device in the 2-wire Serial Programming mode ( $\overline{\text{SER\_EN}}$ Low).   |
| 5         | 10          | 18          | 24          | GND                          |     | Ground pin. A 0.2 $\mu\text{F}$ decoupling capacitor between $V_{\text{CC}}$ and GND is recommended.  |
| 6         | 14          | 21          | 27          | $\overline{\text{CEO}}$      | O   | Chip Enable Output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy chain of AT17 Series devices, the $\overline{\text{CEO}}$ pin of one device must be connected to the $\overline{\text{CE}}$ input of the next device in the chain. It will stay Low as long as $\overline{\text{CE}}$ is low and OE is High. It will then follow CE until OE goes Low; thereafter, $\overline{\text{CEO}}$ will stay High until the entire EEPROM is read again.                   |
|           |             |             |             | A2                           | I   | Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pulldown resistor.   |
| –         | 15          | 23          | 29          | READY <sup>(1)</sup>         | O   | Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (Recommend a 4.7 k $\Omega$ pull-up on this pin if used).   |
| 7         | 17          | 35          | 41          | $\overline{\text{SER\_EN}}$  | I   | Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to $V_{\text{CC}}$ .  |
| 8         | 20          | 38          | 44          | $V_{\text{CC}}$              |     | +3.3V/+5V power supply pin.   |

Note: 1. This pin is not available on the 8-lead packages.

## FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The AT17 Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

This document discusses the AT40K, AT40KAL and AT94KAL applications, as well as Xilinx applications.

## Control of Configuration

Most connections between the FPGA device and the AT17 Serial EEPROM are simple and self-explanatory:

- The DATA output of the AT17 Series Configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17 Series Configurator.
- The  $\overline{\text{CEO}}$  output of any AT17 Series Configurator drives the  $\overline{\text{CE}}$  input of the next Configurator in a cascade chain of EEPROMs.
- $\overline{\text{SER\_EN}}$  must be connected to  $V_{\text{CC}}$  (except during ISP).
- The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.

## Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory.

As the last bit from the first Configurator is read, the clock signal to the Configurator asserts its  $\overline{\text{CEO}}$  output Low and disables its DATA line driver. The second Configurator recognizes the Low level on its  $\overline{\text{CE}}$  input and enables its DATA output.

After configuration is complete, the address counters of all cascaded Configurators are reset if the  $\overline{\text{RESET/OE}}$  on each Configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the  $\overline{\text{RESET/OE}}$  input can be tied to its inactive (High) level.

## AT17 Series Reset Polarity

The AT17 Series Configurator allows the user to program the reset polarity as either  $\overline{\text{RESET/OE}}$  or  $\overline{\text{RESET/OE}}$ . This feature is supported by industry-standard programmer algorithms.

## Programming Mode

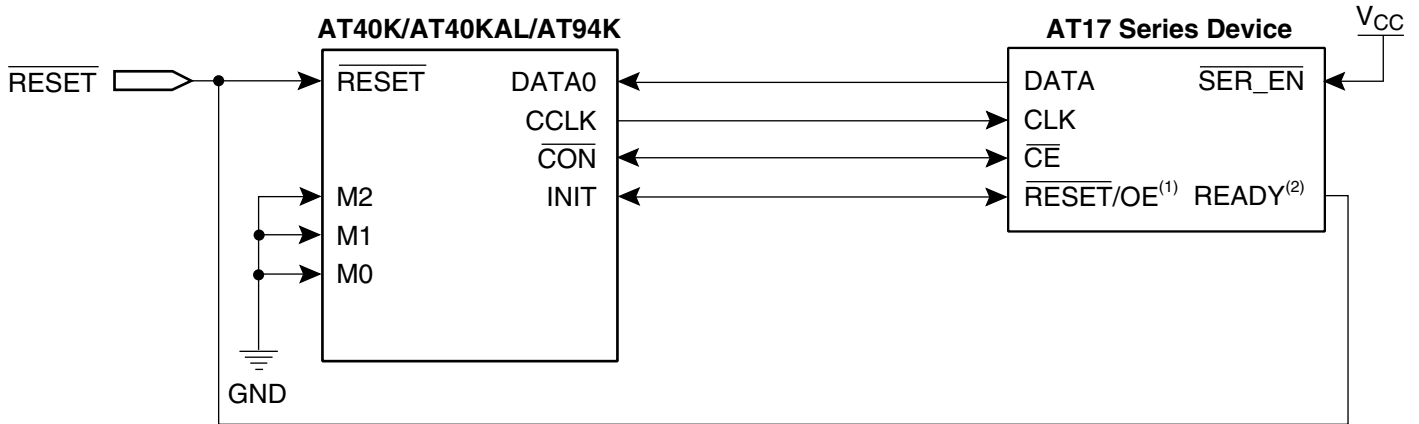
The programming mode is entered by bringing  $\overline{\text{SER\_EN}}$  Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at  $V_{\text{CC}}$  supply only. Programming super voltages are generated inside the chip. The AT17C parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.3V nominal.

## Standby Mode

The AT17C/LV002 Series Configurator enters a low-power standby mode whenever  $\overline{\text{CE}}$  is asserted High. In this mode, the Configurator consumes less than 0.5 mA of current at 5V. The output remains in a high-impedance state regardless of the state of the  $\overline{\text{OE}}$  input.

## Example Circuits

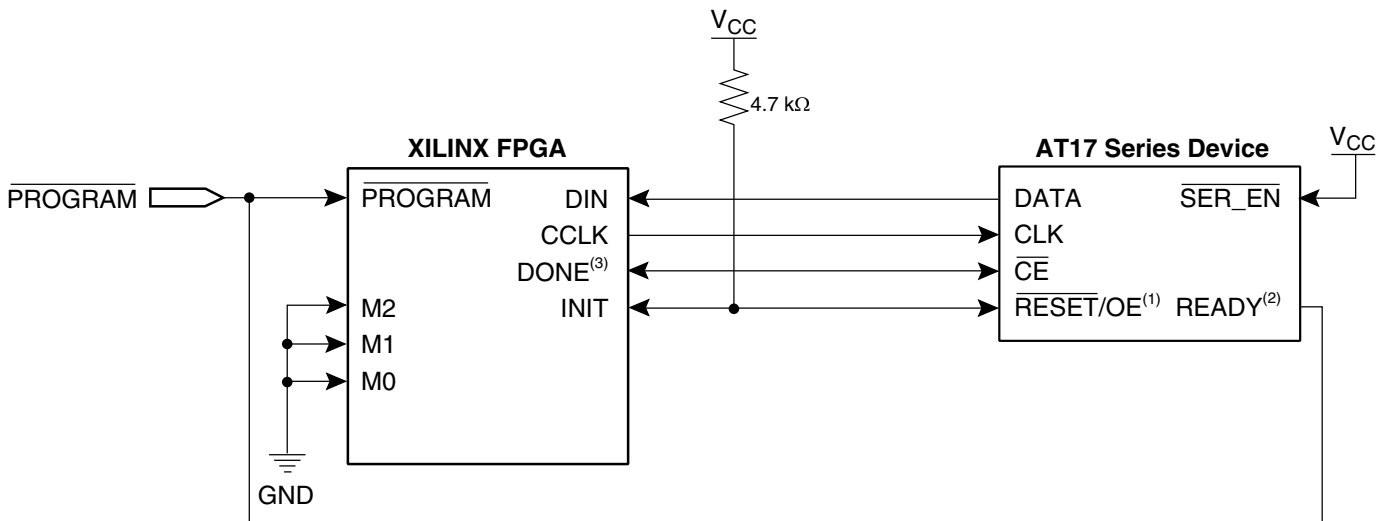
**Figure 1.** AT17 Series Device for Programming PSLI Devices



- Notes:
1. Reset polarity must be set to active Low.
  2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.

The FPGA  $\overline{\text{CON/DONE}}$  output drives the  $\overline{\text{CE}}$  input of the AT17 Series Configurator, while the  $\overline{\text{RESET/OE}}$  input is driven by the FPGA  $\overline{\text{INIT}}$  pin. This connection works under all normal circumstances, even when the user aborts the configuration before  $\overline{\text{CON/DONE}}$  has gone High. A Low level on the  $\overline{\text{RESET/OE}}$  input, during FPGA reset, clears the configurator's internal address pointer so that the reconfiguration starts at the beginning.

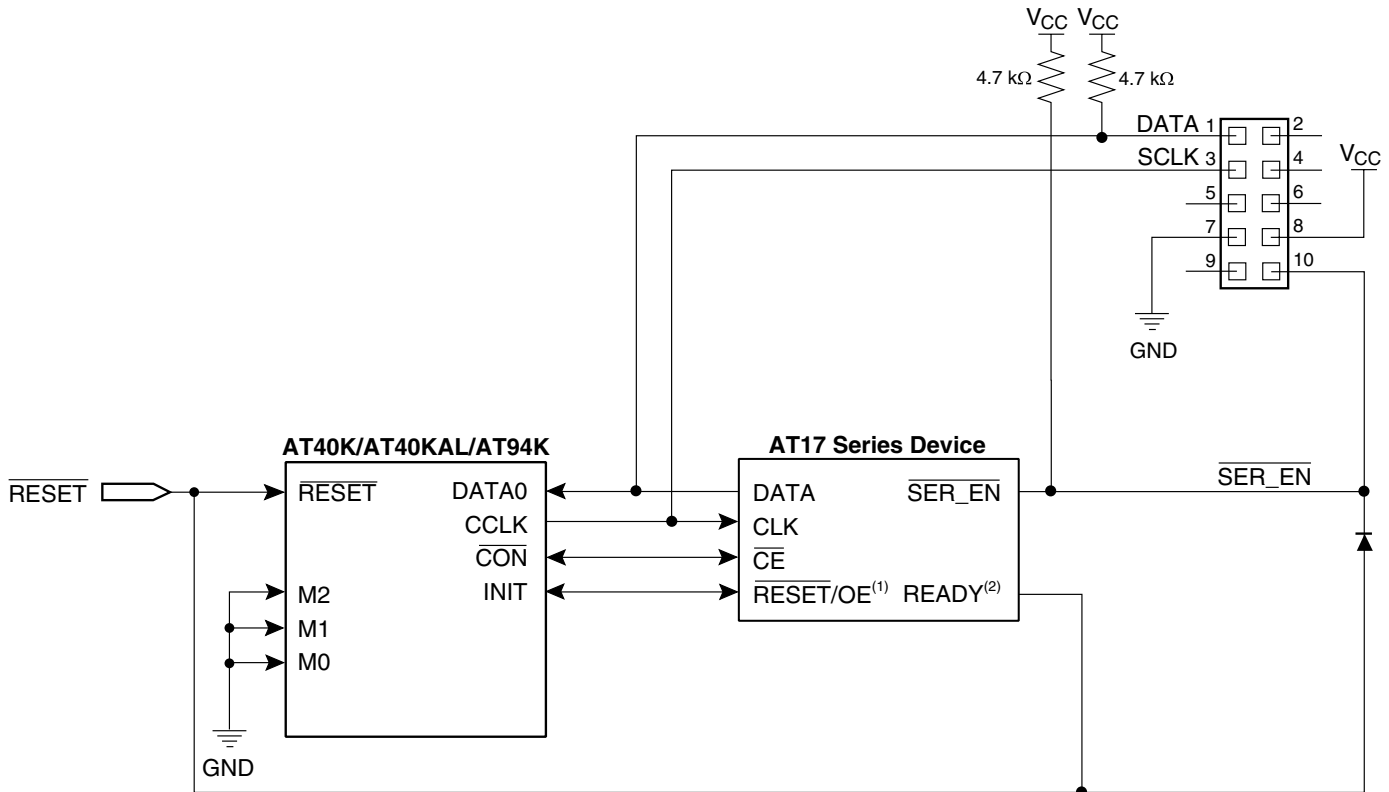
**Figure 2.** Drop-In Replacement of XC17/ATT17 PROMs for Xilinx/Lucent FPGA Applications



- Notes:
1. Reset polarity must be set to active Low.
  2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.
  3. An internal pull-up resistor is enabled here for DONE.

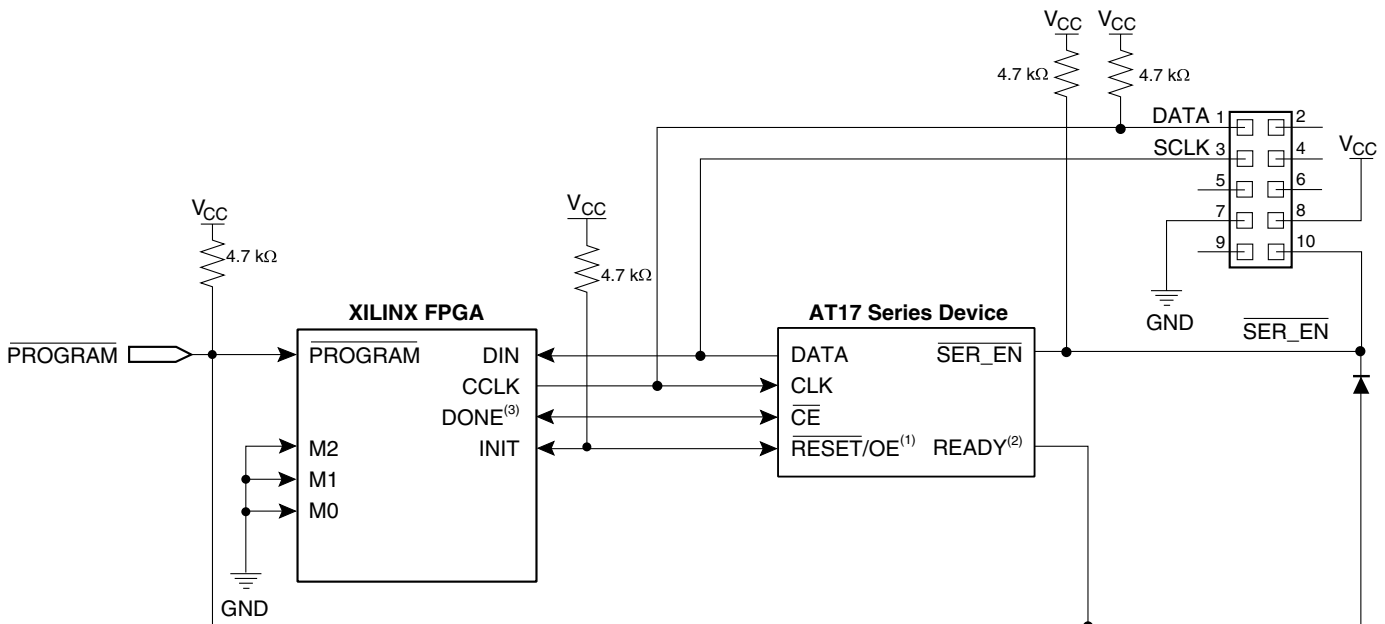
For details of ISP, please refer to the “Programming Specification for Atmel's AT17 and AT17A Series FPGA Configuration EEPROMs”, available on the Atmel web site, at <http://www.atmel.com/atmel/acrobat/doc0437.pdf>.

**Figure 3.** In-System Programming of AT17 Series for PSLI Applications



- Notes:
1. Reset polarity must be set to active Low.
  2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.

**Figure 4.** In-System Programming of AT17 Series for Xilinx/Lucent FPGA Applications



- Notes:
1. Reset polarity must be set to active Low.
  2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.
  3. An internal pull-up resistor is enabled here for DONE.



## Absolute Maximum Ratings\*

|   |                          |
|---|--------------------------|
| Operating Temperature .....                             | -55°C to +125°C          |
| Storage Temperature .....                               | -65°C to +150°C          |
| Voltage on Any Pin<br>with Respect to Ground .....      | -0.1V to $V_{CC} + 0.5V$ |
| Supply Voltage ( $V_{CC}$ ) .....                       | -0.5V to +7.0V           |
| Maximum Soldering Temp. (10 sec. @ 1/16 in.).....       | 260°C                    |
| ESD ( $R_{ZAP} = 1.5K, C_{ZAP} = 100 \text{ pF}$ )..... | 2000V                    |

\*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Operating Conditions

| Symbol   | Description |  | AT17C002 |      | AT17LV002 |     | Units |
|----------|-------------|--|----------|------|-----------|-----|-------|
|          |             |  | Min      | Max  | Min       | Max |       |
| $V_{CC}$ | Commercial  | Supply voltage relative to GND,<br>-0°C to +70°C   | 4.75     | 5.25 | 3.0       | 3.6 | V     |
|          | Industrial  | Supply voltage relative to GND,<br>-40°C to +85°C  | 4.5      | 5.5  | 3.0       | 3.6 | V     |
|          | Military    | Supply voltage relative to GND,<br>-55°C to +125°C | 4.5      | 5.5  | 3.0       | 3.6 | V     |

## DC Characteristics

 $V_{CC} = 5V \pm 5\%$  Commercial,  $5V \pm 10\%$  Industrial/Military

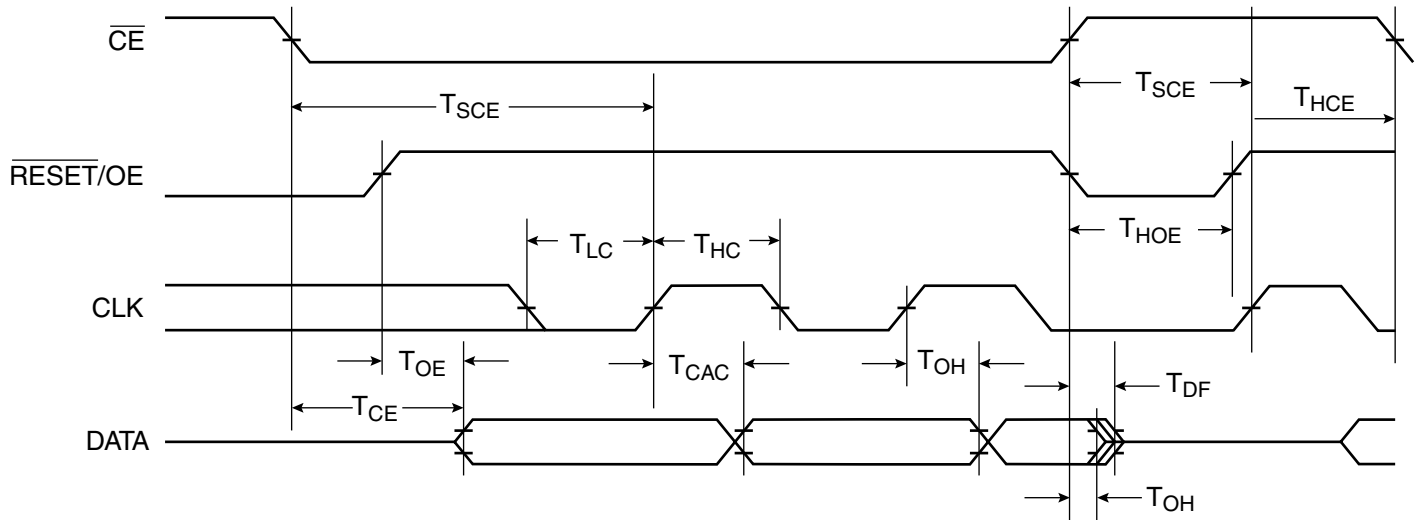
| Symbol     | Description   |                       | Min  | Max      | Units   |
|------------|---|-----------------------|------|----------|---------|
| $V_{IH}$   | High-Level Input Voltage                                    |                       | 2.0  | $V_{CC}$ | V       |
| $V_{IL}$   | Low-level input voltage                                     |                       | 0.0  | 0.8      | V       |
| $V_{OH}$   | High-level Output Voltage ( $I_{OH} = -4$ mA)               | Commercial            | 3.86 |          | V       |
| $V_{OL}$   | Low-level Output Voltage ( $I_{OL} = +4$ mA)                |                       |      | 0.32     | V       |
| $V_{OH}$   | High-level Output Voltage ( $I_{OH} = -4$ mA)               | Industrial            | 3.76 |          | V       |
| $V_{OL}$   | Low-level Output Voltage ( $I_{OL} = +4$ mA)                |                       |      | 0.37     | V       |
| $V_{OH}$   | High-level Output Voltage ( $I_{OH} = -4$ mA)               | Military              | 3.7  |          | V       |
| $V_{OL}$   | Low-level Output Voltage ( $I_{OL} = +4$ mA)                |                       |      | 0.4      | V       |
| $I_{CCA}$  | Supply Current, Active Mode                                 |                       |      | 10       | mA      |
| $I_L$      | Input or Output Leakage Current ( $V_{IN} = V_{CC}$ or GND) |                       | -10  | 10       | $\mu$ A |
| $I_{CCS1}$ | Supply Current, Standby Mode, CMOS                          | Commercial            |      | 0.5      | mA      |
|            |   | Industrial/Military   |      | 0.75     | mA      |
| $I_{CCS2}$ | Supply Current, Standby Mode, TTL                           | Commercial/Industrial |      | 1        | mA      |

## DC Characteristics

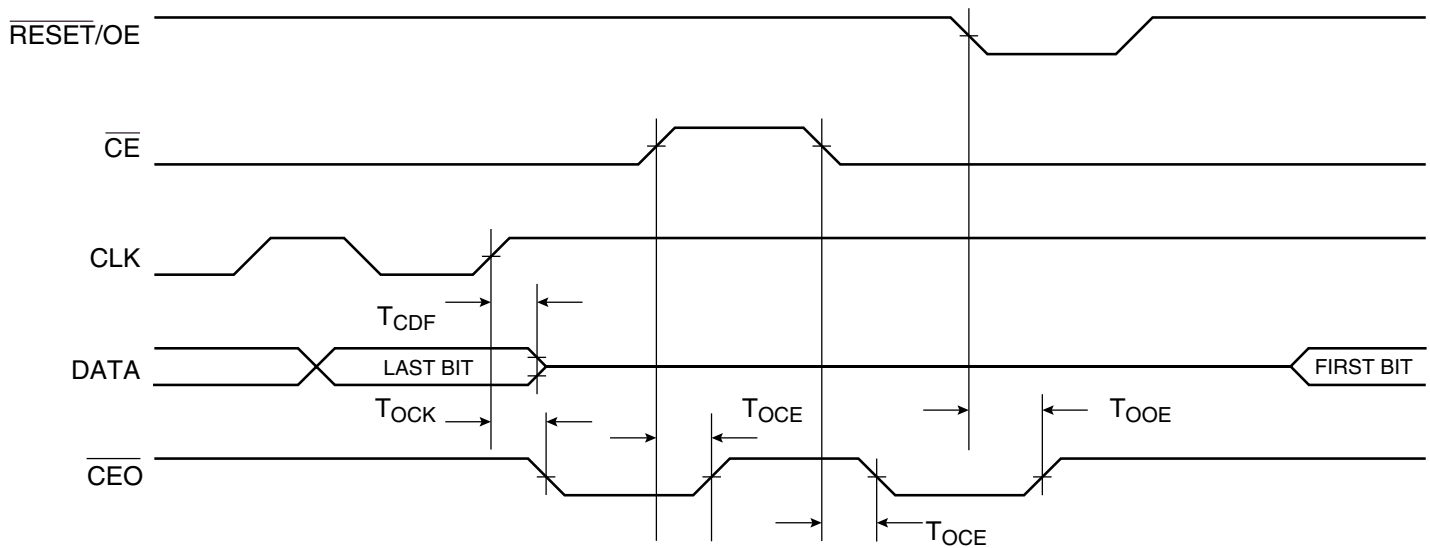
 $V_{CC} = 3.3V \pm 10\%$ 

| Symbol    | Description   |                     | Min | Max      | Units   |
|-----------|---|---------------------|-----|----------|---------|
| $V_{IH}$  | High-level input voltage                                    |                     | 2.0 | $V_{CC}$ | V       |
| $V_{IL}$  | Low-level input voltage                                     |                     | 0.0 | 0.8      | V       |
| $V_{OH}$  | High-level Output Voltage ( $I_{OH} = -2.5$ mA)             | Commercial          | 2.4 |          | V       |
| $V_{OL}$  | Low-level Output Voltage ( $I_{OL} = +3$ mA)                |                     |     | 0.4      | V       |
| $V_{OH}$  | High-level Output Voltage ( $I_{OH} = -2$ mA)               | Industrial          | 2.4 |          | V       |
| $V_{OL}$  | Low-level Output Voltage ( $I_{OL} = +3$ mA)                |                     |     | 0.4      | V       |
| $V_{OH}$  | High-level Output Voltage ( $I_{OH} = -2$ mA)               | Military            | 2.4 |          | V       |
| $V_{OL}$  | Low-level Output Voltage ( $I_{OL} = +2.5$ mA)              |                     |     | 0.4      | V       |
| $I_{CCA}$ | Supply Current, Active Mode                                 |                     |     | 5        | mA      |
| $I_L$     | Input or Output Leakage Current ( $V_{IN} = V_{CC}$ or GND) |                     | -10 | 10       | $\mu$ A |
| $I_{CCS}$ | Supply Current, Standby Mode                                | Commercial          |     | 200      | $\mu$ A |
|           |   | Industrial/Military |     | 200      | $\mu$ A |

## AC Characteristics



## AC Characteristics when Cascading



## AC Characteristics for AT17C002

$V_{CC} = 5V \pm 5\%$  Commercial,  $V_{CC} = 5V \pm 10\%$  Industrial/Military

| Symbol          | Description   | Commercial |     | Industrial/Military <sup>(1)</sup> |     | Units |
|-----------------|---|------------|-----|------------------------------------|-----|-------|
|                 |   | Min        | Max | Min                                | Max |       |
| $T_{OE}^{(2)}$  | OE to Data Delay  |            | 30  |                                    | 35  | ns    |
| $T_{CE}^{(2)}$  | $\overline{CE}$ to Data Delay                                     |            | 45  |                                    | 45  | ns    |
| $T_{CAC}^{(2)}$ | CLK to Data Delay   |            | 50  |                                    | 50  | ns    |
| $T_{OH}$        | Data Hold From $\overline{CE}$ , OE or CLK                        | 0          |     | 0                                  |     | ns    |
| $T_{DF}^{(3)}$  | $\overline{CE}$ or OE to Data Float Delay                         |            | 50  |                                    | 50  | ns    |
| $T_{LC}$        | CLK Low Time  | 20         |     | 20                                 |     | ns    |
| $T_{HC}$        | CLK High Time   | 20         |     | 20                                 |     | ns    |
| $T_{SCE}$       | $\overline{CE}$ Setup Time to CLK (to guarantee proper counting)  | 20         |     | 25                                 |     | ns    |
| $T_{HCE}$       | $\overline{CE}$ Hold Time from CLK (to guarantee proper counting) | 0          |     | 0                                  |     | ns    |
| $T_{HOE}$       | OE High Time (guarantees counter is reset)                        | 20         |     | 20                                 |     | ns    |
| $F_{MAX}$       | Maximum Input Clock Frequency                                     | 15         |     | 15                                 |     | MHz   |

- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test load = 50 pF.
  3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.

## AC Characteristics for AT17C002 when Cascading

$V_{CC} = 5V \pm 5\%$  Commercial/ $V_{CC} = 5V \pm 10\%$  Industrial/Military

| Symbol          | Description                                     | Commercial |     | Industrial/Military <sup>(1)</sup> |     | Units |
|-----------------|---|------------|-----|------------------------------------|-----|-------|
|                 |   | Min        | Max | Min                                | Max |       |
| $T_{CDF}^{(3)}$ | CLK to Data Float Delay                         |            | 50  |                                    | 50  | ns    |
| $T_{OCK}^{(2)}$ | CLK to $\overline{CEO}$ Delay                   |            | 35  |                                    | 40  | ns    |
| $T_{OCE}^{(2)}$ | $\overline{CE}$ to $\overline{CEO}$ Delay       |            | 35  |                                    | 35  | ns    |
| $T_{OOE}^{(2)}$ | $\overline{RESET}/OE$ to $\overline{CEO}$ Delay |            | 30  |                                    | 30  | ns    |
| $F_{MAX}$       | Maximum Input Clock Frequency                   | 12.5       |     | 12.5                               |     | MHz   |

- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test load = 50 pF.
  3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.



## AC Characteristics for AT17LV002

$V_{CC} = 3.3V \pm 10\%$

| Symbol          | Description   | Commercial |     | Industrial/Military <sup>(1)</sup> |     | Units |
|-----------------|---|------------|-----|------------------------------------|-----|-------|
|                 |   | Min        | Max | Min                                | Max |       |
| $T_{OE}^{(2)}$  | OE to Data Delay  |            | 50  |                                    | 55  | ns    |
| $T_{CE}^{(2)}$  | $\overline{CE}$ to Data Delay                                     |            | 55  |                                    | 60  | ns    |
| $T_{CAC}^{(2)}$ | CLK to Data Delay   |            | 55  |                                    | 60  | ns    |
| $T_{OH}$        | Data Hold From $\overline{CE}$ , OE or CLK                        | 0          |     | 0                                  |     | ns    |
| $T_{DF}^{(3)}$  | $\overline{CE}$ or OE to Data Float Delay                         |            | 50  |                                    | 50  | ns    |
| $T_{LC}$        | CLK Low Time  | 25         |     | 25                                 |     | ns    |
| $T_{HC}$        | CLK High Time   | 25         |     | 25                                 |     | ns    |
| $T_{SCE}$       | $\overline{CE}$ Setup Time to CLK (to guarantee proper counting)  | 30         |     | 35                                 |     | ns    |
| $T_{HCE}$       | $\overline{CE}$ Hold Time from CLK (to guarantee proper counting) | 0          |     | 0                                  |     | ns    |
| $T_{HOE}$       | OE High Time (guarantees counter is reset)                        | 25         |     | 25                                 |     | ns    |
| $F_{MAX}$       | Maximum Input Clock Frequency                                     | 15         |     | 10                                 |     | MHz   |

- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test load = 50 pF.
  3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.

## AC Characteristics for AT17LV002 when Cascading

$V_{CC} = 3.3V \pm 10\%$

| Symbol          | Description                                     | Commercial |     | Industrial/Military <sup>(1)</sup> |     | Units |
|-----------------|---|------------|-----|------------------------------------|-----|-------|
|                 |   | Min        | Max | Min                                | Max |       |
| $T_{CDF}^{(3)}$ | CLK to Data Float Delay                         |            | 50  |                                    | 50  | ns    |
| $T_{OCK}^{(2)}$ | CLK to $\overline{CEO}$ Delay                   |            | 50  |                                    | 55  | ns    |
| $T_{OCE}^{(2)}$ | $\overline{CE}$ to $\overline{CEO}$ Delay       |            | 35  |                                    | 40  | ns    |
| $T_{OOE}^{(2)}$ | $\overline{RESET}/OE$ to $\overline{CEO}$ Delay |            | 35  |                                    | 35  | ns    |
| $F_{MAX}$       | Maximum Input Clock Frequency                   | 12.5       |     | 10                                 |     | MHz   |

- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test load = 50 pF.
  3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.

**Thermal Resistance Coefficients<sup>(1)</sup>**

| Package Type                          |      | $\theta_{JC}$ [°C/W] | $\theta_{JA}$ [°C/W]<br>Airflow = 0 ft/min |
|---------------------------------------|------|----------------------|--|
| Leadless Array Package (LAP)          | 8CN4 | 45                   | 159.60                                     |
| Plastic Leaded Chip Carrier (PLCC)    | 20J  | 35                   | 90   |
| Thin Plastic Quad Flat Package (TQFP) | 44A  | 17                   | 62   |
| Plastic Leaded Chip Carrier (PLCC)    | 44J  | 15                   | 50   |

Note: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site, at <http://www.atmel.com/atmel/acrobat/doc0636.pdf>.



## Ordering Information – 5V Devices

| Memory Size | Ordering Code  | Package | Operation Range               |
|-------------|----------------|---------|-------------------------------|
| 2-Mbit      | AT17C002-10CC  | 8CN4    | Commercial<br>(0°C to 70°C)   |
|             | AT17C002-10JC  | 20J     |                               |
|             | AT17C002-10TQC | 44A     |                               |
|             | AT17C002-10BJC | 44J     |                               |
|             | AT17C002-10CI  | 8CN4    | Industrial<br>(-40°C to 85°C) |
|             | AT17C002-10JI  | 20J     |                               |
|             | AT17C002-10TQI | 44A     |                               |
|             | AT17C002-10BJI | 44J     |                               |

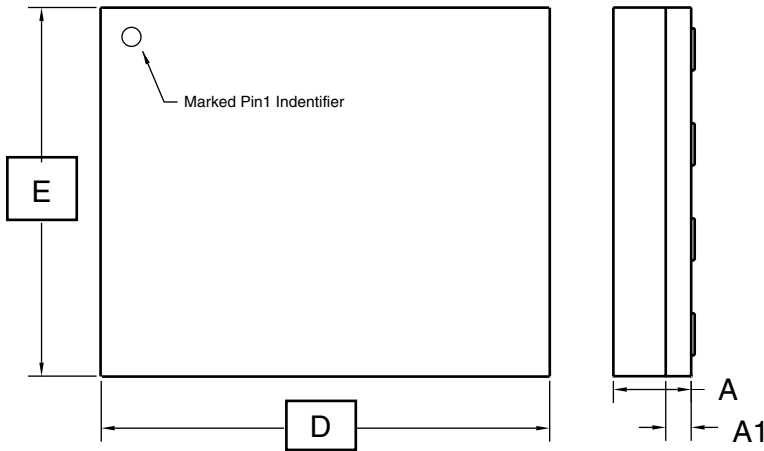
## Ordering Information – 3.3V Devices

| Memory Size | Ordering Code   | Package | Operation Range               |
|-------------|-----------------|---------|-------------------------------|
| 2-Mbit      | AT17LV002-10CC  | 8CN4    | Commercial<br>(0°C to 70°C)   |
|             | AT17LV002-10JC  | 20J     |                               |
|             | AT17LV002-10TQC | 44A     |                               |
|             | AT17LV002-10BJC | 44J     |                               |
|             | AT17LV002-10CI  | 8CN4    | Industrial<br>(-40°C to 85°C) |
|             | AT17LV002-10JI  | 20J     |                               |
|             | AT17LV002-10TQI | 44A     |                               |
|             | AT17LV002-10BJI | 44J     |                               |

| Package Type |  |
|--------------|--|
| <b>8CN4</b>  | 8-lead, 6 mm x 6 mm x 1 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOIC Packages |
| <b>20J</b>   | 20-lead, Plastic J-leaded Chip Carrier (PLCC)  |
| <b>44A</b>   | 44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP)  |
| <b>44J</b>   | 44-lead, Plastic J-leaded Chip Carrier (PLCC)  |

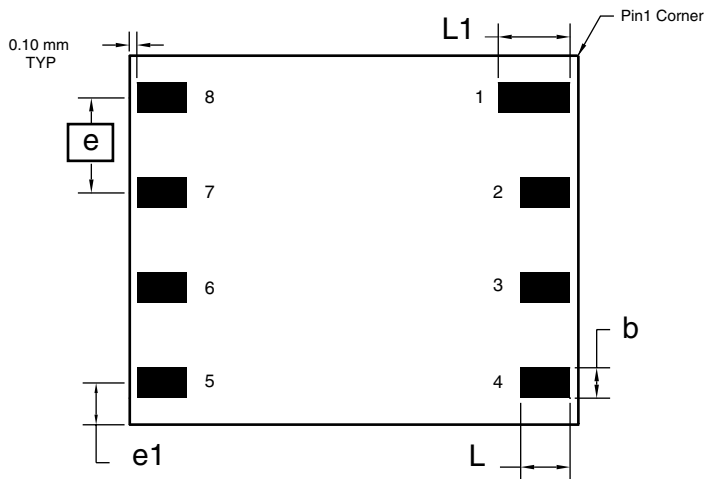
Packaging Information

8CN4 – LAP



Top View

Side View



Bottom View

COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE |
|--------|----------|------|------|------|
| A      | 0.94     | 1.04 | 1.14 |      |
| A1     | 0.30     | 0.34 | 0.38 |      |
| b      | 0.45     | 0.50 | 0.55 | 1    |
| D      | 5.89     | 5.99 | 6.09 |      |
| E      | 4.89     | 5.99 | 6.09 |      |
| e      | 1.27 BSC |      |      |      |
| e1     | 1.10 REF |      |      |      |
| L      | 0.95     | 1.00 | 1.05 | 1    |
| L1     | 1.25     | 1.30 | 1.35 | 1    |

Note: 1. Metal Pad Dimensions.

11/14/01



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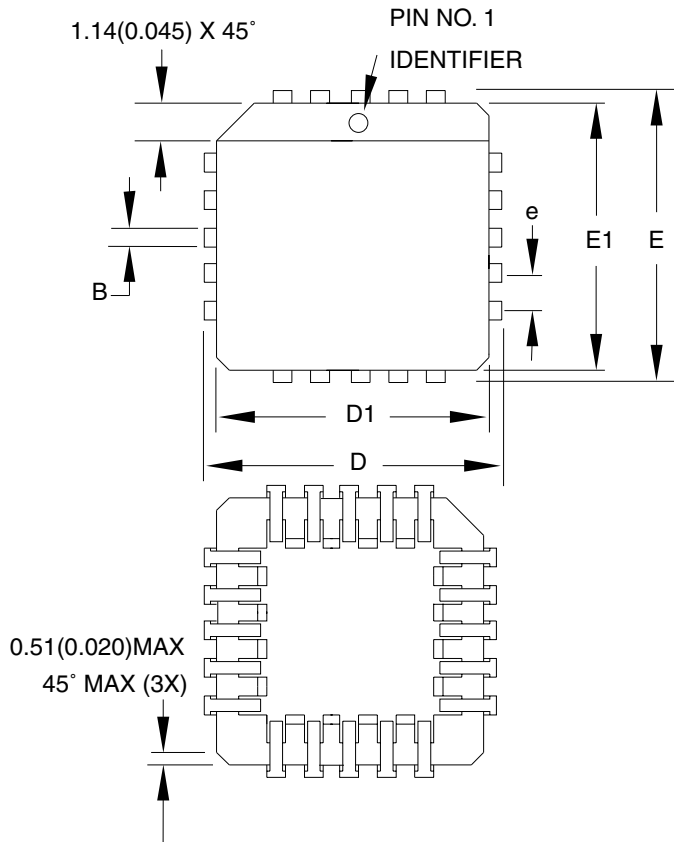
**TITLE**  
8CN4, 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27 mm,  
Leadless Array Package (LAP)

**DRAWING NO.**  
8CN4

**REV.**  
A



# 20J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | –   | 4.572  |        |
| A1     | 2.286     | –   | 3.048  |        |
| A2     | 0.508     | –   | –      |        |
| D      | 9.779     | –   | 10.033 |        |
| D1     | 8.890     | –   | 9.042  | Note 2 |
| E      | 9.779     | –   | 10.033 |        |
| E1     | 8.890     | –   | 9.042  | Note 2 |
| D2/E2  | 7.366     | –   | 8.382  |        |
| B      | 0.660     | –   | 0.813  |        |
| B1     | 0.330     | –   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)**

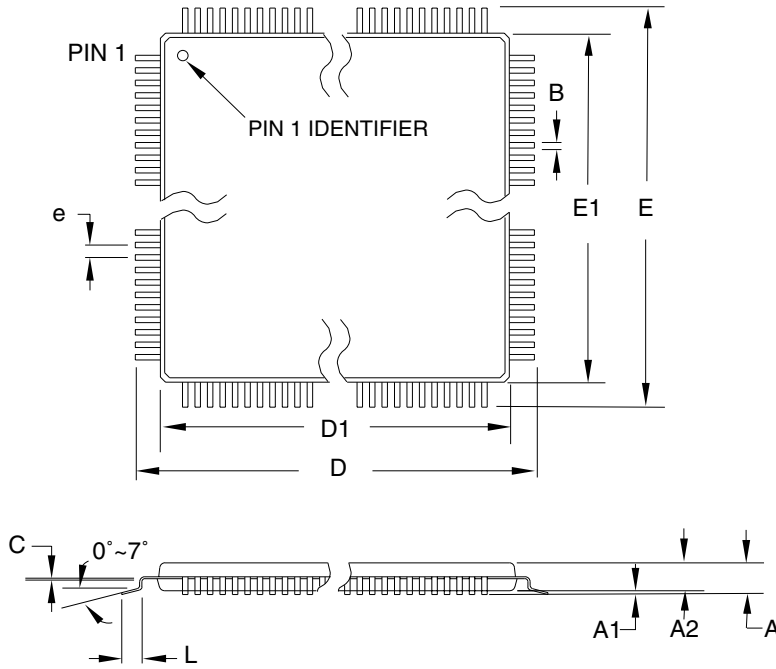
**DRAWING NO.**

20J

**REV.**

B

44A – TQFP




**COMMON DIMENSIONS**  
(Unit of Measure = mm)

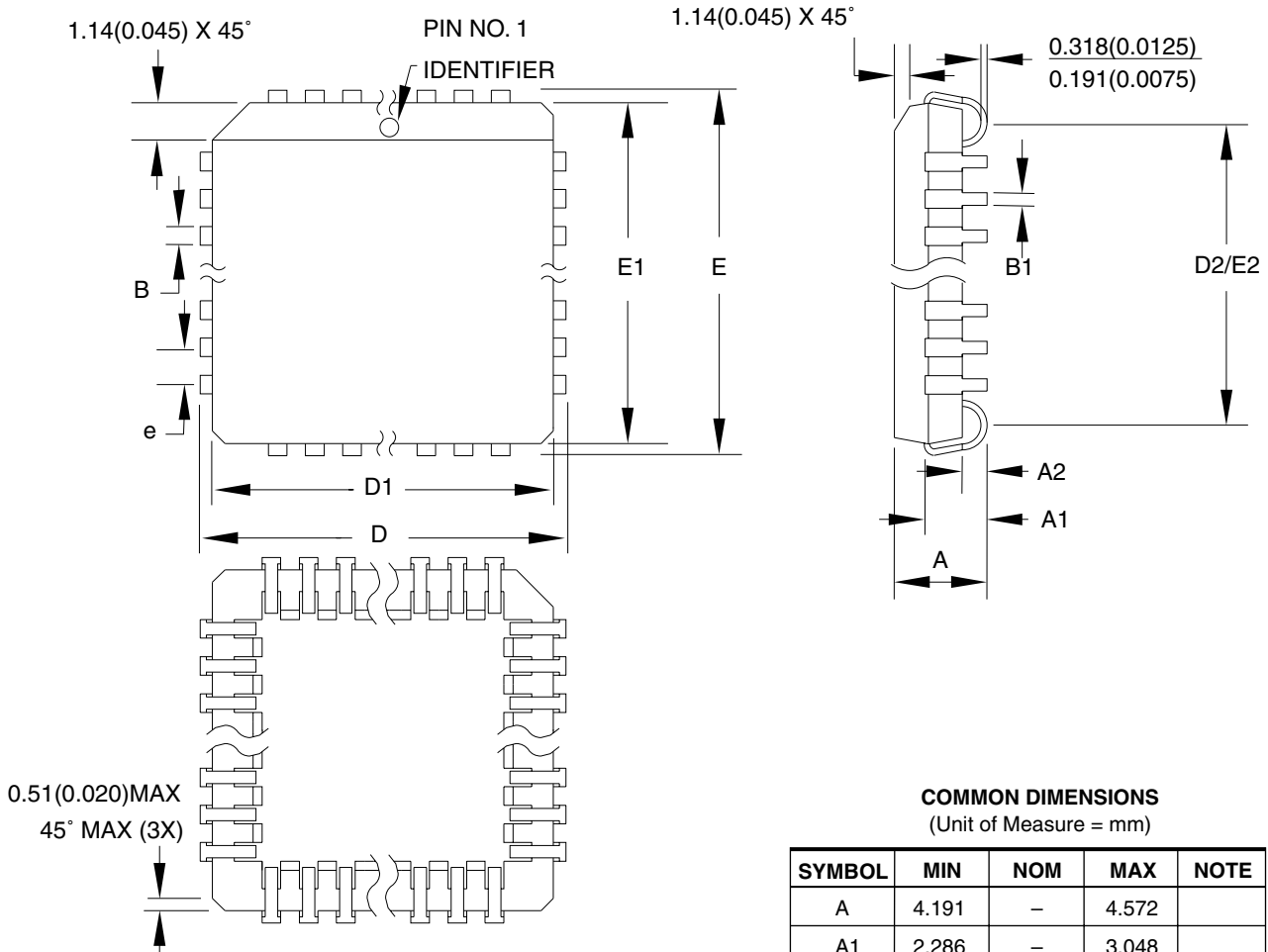
| SYMBOL | MIN      | NOM   | MAX   | NOTE   |
|--------|----------|-------|-------|--------|
| A      | -        | -     | 1.20  |        |
| A1     | 0.05     | -     | 0.15  |        |
| A2     | 0.95     | 1.00  | 1.05  |        |
| D      | 11.75    | 12.00 | 12.25 |        |
| D1     | 9.90     | 10.00 | 10.10 | Note 2 |
| E      | 11.75    | 12.00 | 12.25 |        |
| E1     | 9.90     | 10.00 | 10.10 | Note 2 |
| B      | 0.30     | -     | 0.45  |        |
| C      | 0.09     | -     | 0.20  |        |
| L      | 0.45     | -     | 0.75  |        |
| e      | 0.80 TYP |       |       |        |

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

|  |  |                    |             |
|--|--|--------------------|-------------|
|  2325 Orchard Parkway<br>San Jose, CA 95131 | <b>TITLE</b><br>44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness,<br>0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | <b>DRAWING NO.</b> | <b>REV.</b> |
|  |  | 44A                | B           |

# 44J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | –   | 4.572  |        |
| A1     | 2.286     | –   | 3.048  |        |
| A2     | 0.508     | –   | –      |        |
| D      | 17.399    | –   | 17.653 |        |
| D1     | 16.510    | –   | 16.662 | Note 2 |
| E      | 17.399    | –   | 17.653 |        |
| E1     | 16.510    | –   | 16.662 | Note 2 |
| D2/E2  | 14.986    | –   | 16.002 |        |
| B      | 0.660     | –   | 0.813  |        |
| B1     | 0.330     | –   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)**

**DRAWING NO.**

44J

**REV.**

B



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