



THE DATASHEET OF TMS320C44PDB50



- **Highest Performance Floating-Point Digital Signal Processor (DSP)**
 - TMS320C44-60:
33-ns Instruction Cycle Time,
330 MOPS, 60 MFLOPS,
30 MIPS, 336M Bytes/s
 - TMS320C44-50:
40-ns Instruction Cycle Time
- **Four Communication Ports**
- **Six-Channel Direct Memory Address (DMA) Coprocessor**
- **Single-Cycle Conversion to and From IEEE-754 Floating-Point Format**
- **Single Cycle, $1/x$, $1/\sqrt{x}$**
- **Source-Code Compatible With C3x and C4x**
- **Single-Cycle 40-Bit Floating-Point, 32-Bit Integer Multipliers**
- **Twelve 40-Bit Registers, Eight Auxiliary Registers, 14 Control Registers, and Two Timers**
- **IEEE-1149.1[†] (JTAG) Boundary-Scan Compatible**
- **Two Identical External Data and Address Buses Supporting Shared Memory Systems and High Data-Rate, Single-Cycle Transfers**
 - High Port-Data Rate of 120M Bytes/s (TMS320C44-60) (Each Bus)
 - 128M-Byte Program/Data/Peripheral Address Space
 - Memory-Access Request for Fast, Intelligent Bus Arbitration
 - Separate Address-Bus, Data-Bus, and Control-Enable Pins
 - Four Sets of Memory-Control Signals Support Different Speed Memories in Hardware
- **Fabricated Using 0.72- μ m Enhanced Performance Implanted CMOS (EPIC[™]) Technology by Texas Instruments (TI[™])**
- **Separate Internal Program-, Data-, and DMA-Coprocessor Buses for Support of Massive Concurrent I/O of Program and Data, Thereby Maximizing Sustained CPU Performance**
- **IDLE2 Clock-Stop Power-Down Mode**
- **Communication-Port-Direction Pin**
- **On-Chip Program Cache and Dual-Access/Single-Cycle RAM for Increased Memory-Access Performance**
 - 512-Byte Instruction Cache
 - 8K Bytes of Single-Cycle Dual-Access Program or Data RAM
 - ROM-Based Boot Loader Supports Program Bootup Using 8-, 16-, or 32-Bit Memories or One of the Communication Ports
- **Software-Communication-Port Reset**
- **$\overline{\text{NMI}}$ With Bus-Grant Feature**
- **304-Pin Plastic Quad Flatpack (PDB Suffix) (Commercial Temperature)**
- **388-Pin Plastic Ball Grid Array (GFW Suffix) (Commercial Temperature)**
- **388-Pin Plastic Ball Grid Array (GFW Suffix) (Industrial Temperature)**

description

The TMS320C44 DSP is a 32-bit, floating-point processor manufactured in 0.72- μ m double-level-metal CMOS technology. The TMS320C44 is part of the TMS320C4x generation of DSPs from Texas Instruments. The on-chip parallel-processing capabilities of the C44 make the immense floating-point performance required by many applications achievable.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] IEEE Standard 1149.1–1990 Standard Test-Access Port and Boundary-Scan Architecture.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TMS320C44 DIGITAL SIGNAL PROCESSOR

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operation

The C44 has four on-chip communication ports for processor-to-processor communication with no external hardware and simple communication software. This allows connectivity with no external-glue logic. The communication ports remove input/output bottlenecks, and the independent smart 6-channel DMA coprocessor is able to handle the CPU input/output burden.

To fit the C40 into a 304-pin PQFP package (thermally enhanced plastic quad flatpack), two communication ports are removed and the external local and global address buses are reduced to 24 address lines each. In this case, both the bond pads and driver circuits are removed, decreasing die size and power consumption. Otherwise, functionality remains the same as the rest of the C4x family.

The communication-port token and data-strobe control lines are internally connected to avoid spurious data, boot-up, and power consumption problems.

functions

This section lists signal descriptions for the C44 device: each signal, number of pins, operating mode(s) (that is, input, output, or high-impedance state as indicated by I, O, or Z, respectively), and function. The signals are grouped according to function.

Pin Functions

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
GLOBAL-BUS EXTERNAL INTERFACE (73 pins)			
D31 – D0	32	I/O/Z	32-bit data port of the global-bus external interface
DE	1	I	Data-bus-enable signal for the global-bus external interface
A23 – A0	24	O/Z	24-bit address port of the global-bus external interface
AE	1	I	Address-bus-enable signal for the global-bus external interface
STAT3 – STAT0	4	O	Status signals for the global-bus external interface
LOCK	1	O	Lock signal for the global-bus external interface
STRB0‡	1	O/Z	Access strobe 0 for the global-bus external interface
R/W0‡	1	O/Z	Read/write signal for STRB0 accesses
PAGE0‡	1	O/Z	Page signal for STRB0 accesses
RDY0‡	1	I	Ready signal for STRB0 accesses
CE0‡	1	I	Control enable for the STRB0, PAGE0, and R/W0 signals
STRB1‡	1	O/Z	Access strobe 1 for the global-bus external interface
R/W1‡	1	O/Z	Read/write signal for STRB1 accesses
PAGE1‡	1	O/Z	Page signal for STRB1 accesses
RDY1‡	1	I	Ready signal for STRB1 accesses
CE1‡	1	I	Control enable for the STRB1, PAGE1, and R/W1 signals
LOCAL-BUS EXTERNAL INTERFACE (73 pins)			
LD31 – LD0	32	I/O/Z	32-bit data port of the local-bus external interface
LDE	1	I	Data-bus-enable signal for the local-bus external interface
LA23 – LA0	24	O/Z	24-bit address port of the local-bus external interface
LAE	1	I	Address-bus-enable signal for the local-bus external interface
LSTAT3 – LSTAT0	4	O	Status signals for the local-bus external interface
LLOCK	1	O	Lock signal for the local-bus external interface

† I = input, O = output, Z = high impedance

‡ The effective address range is defined by the local/global STRB ACTIVE bits in the memory interface-control registers.



Pin Functions (Continued)

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
LOCAL-BUS EXTERNAL INTERFACE (73 pins) (Continued)			
$\overline{\text{LSTRB0}}^\ddagger$	1	O/Z	Access strobe 0 for the local-bus external interface
LR/ $\overline{\text{W0}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB0}}$ accesses
LPAGE0	1	O/Z	Page signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LRDY0}}$	1	I	Ready signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LCE0}}$	1	I	Control enable for the $\overline{\text{LSTRB0}}$, LPAGE0, and LR/ $\overline{\text{W0}}$ signals
$\overline{\text{LSTRB1}}^\ddagger$	1	O/Z	Access strobe 1 for the local-bus external interface
LR/ $\overline{\text{W1}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB1}}$ accesses
LPAGE1	1	O/Z	Page signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LRDY1}}$	1	I	Ready signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LCE1}}$	1	I	Control enable for the $\overline{\text{LSTRB1}}$, LPAGE1, and LR/ $\overline{\text{W1}}$ signals
COMMUNICATION PORT 1 INTERFACE (13 pins)			
C1D7–C1D0	8	I/O	Communication port 1 data bus
$\overline{\text{CREQ1}}$	1	I/O	Communication port 1 token-request signal
$\overline{\text{CACK1}}$	1	I/O	Communication port 1 token-request-acknowledge signal
$\overline{\text{CSTRB1}}$	1	I/O	Communication port 1 data-strobe signal
$\overline{\text{CRDY1}}$	1	I/O	Communication port 1 data-ready signal
CDIR1	1	O	Communication port 1 direction signal
COMMUNICATION PORT 2 INTERFACE (13 pins)			
C2D7–C2D0	8	I/O	Communication port 2 data bus
$\overline{\text{CREQ2}}$	1	I/O	Communication port 2 token-request signal
$\overline{\text{CACK2}}$	1	I/O	Communication port 2 token-request-acknowledge signal
$\overline{\text{CSTRB2}}$	1	I/O	Communication port 2 data-strobe signal
$\overline{\text{CRDY2}}$	1	I/O	Communication port 2 data-ready signal
CDIR2	1	O	Communication port 2 direction signal
COMMUNICATION PORT 4 INTERFACE (13 pins)			
C4D7–C4D0	8	I/O	Communication port 4 data bus
$\overline{\text{CREQ4}}$	1	I/O	Communication port 4 token-request signal
$\overline{\text{CACK4}}$	1	I/O	Communication port 4 token-request-acknowledge signal
$\overline{\text{CSTRB4}}$	1	I/O	Communication port 4 data-strobe signal
$\overline{\text{CRDY4}}$	1	I/O	Communication port 4 data-ready signal
CDIR4	1	O	Communication port 4 direction signal
COMMUNICATION PORT 5 INTERFACE (13 pins)			
C5D7–C5D0	8	I/O	Communication port 5 data bus
$\overline{\text{CREQ5}}$	1	I/O	Communication port 5 token-request signal
$\overline{\text{CACK5}}$	1	I/O	Communication port 5 token-request-acknowledge signal
$\overline{\text{CSTRB5}}$	1	I/O	Communication port 5 data-strobe signal
$\overline{\text{CRDY5}}$	1	I/O	Communication port 5 data-ready signal
CDIR5	1	O	Communication port 5 direction signal

† I = input, O = output, Z = high impedance

‡ The effective address range is defined by the local/global STRB ACTIVE bits in the memory interface-control registers.

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Pin Functions (Continued)

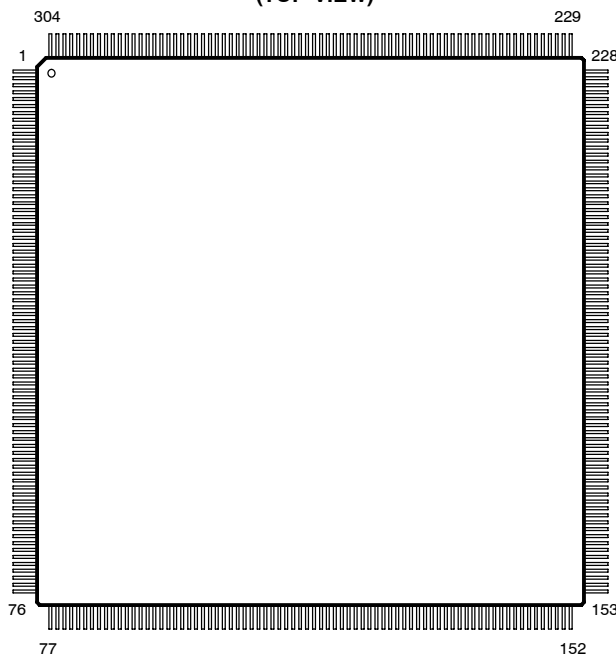
SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
INTERRUPTS, I/O FLAGS, RESET, TIMER (12 pins)			
IIOF3 – IIOF0	4	I/O	Interrupt and I/O flags
NMI	1	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is sensitive to a low-going edge.
IACK	1	O	Interrupt acknowledge
RESET	1	I	Reset signal
RESETLOC1 RESETLOC0	2	I	Reset-vector location
ROMEN	1	I	On-chip ROM enable (0 = disable, 1 = enable)
TCLK0	1	I/O	Timer 0
TCLK1	1	I/O	Timer 1
CLOCK (4 pins)			
X1	1	O	Crystal
X2 / CLKIN	1	I	Crystal/oscillator
H1	1	O	H1 clock
H3	1	O	H3 clock
POWER (71 pins)			
CV _{SS}	17	I	Ground
DV _{SS}	17	I	Ground
IV _{SS}	6	I	Ground
DV _{DD}	22	I	5-V _{DC} supply
VSUBS	1	I	Substrate (tie to ground)
V _{DDL}	4	I	5-V _{DC} supply
V _{SSL}	4	I	Ground
EMULATION (7 pins)			
TCK	1	I	IEEE 1149.1 test port clock
TDI	1	I	IEEE 1149.1 test port data in
TDO	1	O/Z	IEEE 1149.1 test port data out
TMS	1	I	IEEE 1149.1 test port mode select
$\overline{\text{TRST}}$	1	I	IEEE 1149.1 test port reset
EMU0	1	I/O	Emulation pin 0
EMU1	1	I/O	Emulation pin 1

† I = input, O = output, Z = high impedance

‡ The effective address range is defined by the local/global STRB ACTIVE bits in the memory interface-control registers.



304-PIN PDB PLASTIC QUAD FLATPACK
(TOP VIEW)



PDB Package Pin Assignments — Alphabetical Listing

NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.
A0	149	C2D7	34	CV _{SS}	134	D24	137
A1	150	C4D0	87	CV _{SS}	117	D25	138
A2	151	C4D1	88	CV _{SS}	102	D26	140
A3	152	C4D2	90	CV _{SS}	78	D27	141
A4	154	C4D3	92	CV _{SS}	62	D28	142
A5	155	C4D4	94	CV _{SS}	44	D29	143
A6	156	C4D5	97	CV _{SS}	25	D30	144
A7	157	C4D6	99	CV _{SS}	7	D31	145
A8	158	C4D7	100	CV _{SS}	282	\overline{DE}	89
A9	159	C5D0	37	CV _{SS}	262	DV _{DD}	139
A10	160	C5D1	39	CV _{SS}	247	DV _{DD}	124
A11	162	C5D2	41	CV _{SS}	230	DV _{DD}	109
A12	165	C5D3	42	CV _{SS}	218	DV _{DD}	96
A13	166	C5D4	45	CV _{SS}	202	DV _{DD}	83
A14	167	C5D5	46	CV _{SS}	182	DV _{DD}	67
A15	168	C5D6	47	CV _{SS}	164	DV _{DD}	51
A16	169	C5D7	48	D0	104	DV _{DD}	40
A17	170	$\overline{CACK1}$	13	D1	105	DV _{DD}	28
A18	171	$\overline{CACK2}$	21	D2	106	DV _{DD}	17
A19	174	$\overline{CACK4}$	73	D3	107	DV _{DD}	302
A20	175	$\overline{CACK5}$	50	D4	108	DV _{DD}	288
A21	176	CDIR1	19	D5	110	DV _{DD}	272

PDB Package Pin Assignments — Alphabetical Listing (Continued)

PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
LA2	234	LD15	208	NC	199		
LA3	235	LD16	210	NC	214		
LA4	237	LD17	211	NC	303		
LA5	238	LD18	212	NC	304		
LA6	239	LD19	213	NMI	3		
LA7	240	LD20	215	PAGE0	60		
LA8	241	LD21	216	PAGE1	72		
LA9	242	LD22	219	RDY0	91		
LA10	243	LD23	220	RDY1	98		
LA11	245	LD24	221	RESET	54		
LA12	248	LD25	222	RESETLOC0	55		
LA13	249	LD26	224	RESETLOC1	56		
LA14	250	LD27	225	ROMEN	12		
LA15	251	LD28	226	R/W0	59		
LA16	252	LD29	227	R/W1	70		

PDB Package Pin Assignments — Numerical Listing

PIN		PIN		PIN		PIN	
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
1	NC	41	C5D2	81	TRST	121	V _{DDL}
2	IV _{SS}	42	C5D3	82	TMS	122	D13
3	NMI	43	DV _{SS}	83	DV _{DD}	123	D14
4	IIOF3	44	CV _{SS}	84	CSTRB4	124	DV _{DD}
5	IIOF2	45	C5D4	85	CRDY4	125	D15
6	DV _{SS}	46	C5D5	86	TCK	126	IV _{SS}
7	CV _{SS}	47	C5D6	87	C4D0	127	D16
8	CRDY1	48	C5D7	88	C4D1	128	D17
9	IIOF1	49	CREQ5	89	DE	129	D18
10	IIOF0	50	CACK5	90	C4D2	130	D19
11	CREQ1	51	DV _{DD}	91	RDY0	131	D20
12	ROMEN	52	CSTRB5	92	C4D3	132	D21
13	CACK1	53	CRDY5	93	CE0	133	DV _{SS}
14	CSTRB1	54	RESET	94	C4D4	134	CV _{SS}
15	CDIR5	55	RESETLOC0	95	LOCK	135	D22
16	CDIR4	56	RESETLOC1	96	DV _{DD}	136	D23
17	DV _{DD}	57	AE	97	C4D5	137	D24
18	CDIR2	58	STRB0	98	RDY1	138	D25
19	CDIR1	59	R/W0	99	C4D6	139	DV _{DD}
20	CREQ2	60	PAGE0	100	C4D7	140	D26
21	CACK2	61	STAT3	101	CE1	141	D27
22	CSTRB2	62	CV _{SS}	102	CV _{SS}	142	D28
23	CRDY2	63	DV _{SS}	103	DV _{SS}	143	D29
24	DV _{SS}	64	STAT2	104	D0	144	D30



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PDB Package Pin Assignments — Numerical Listing (Continued)

NO.	PIN	NAME	NO.	PIN	NAME	NO.	PIN	NAME
25		CV _{SS}	65		IV _{SS}	105		D1
26		C2D0	66		STAT1	106		D2
27		C2D1	67		DV _{DD}	107		D3
28		DV _{DD}	68		STAT0	108		D4
29		C2D2	69		STRB $\bar{1}$	109		DV _{DD}
30		C2D3	70		R/ \bar{W} 1	110		D5
31		C2D4	71		\bar{C} REQ4	111		D6
32		C2D5	72		PAGE1	112		D7
33		C2D6	73		\bar{C} ACK4	113		D8
34		C2D7	74		EMU1	114		D9
35		IV _{SS}	75		EMU0	115		D10
36		V _{SSL}	76		TDI	116		DV _{SS}
37		C5D0	77		NC	117		CV _{SS}
38		V _{DDL}	78		CV _{SS}	118		D11
39		C5D1	79		DV _{SS}	119		V _{SSL}
40		DV _{DD}	80		TDO	120		D12
161		DV _{DD}	201		DV _{SS}	241		LA8
162		A11	202		CV _{SS}	242		LA9
163		DV _{SS}	203		LD11	243		LA10
164		CV _{SS}	204		LD12	244		DV _{DD}
165		A12	205		LD13	245		LA11
166		A13	206		LD14	246		DV _{SS}
167		A14	207		DV _{DD}	247		CV _{SS}
168		A15	208		LD15	248		LA12
169		A16	209		IV _{SS}	249		LA13
170		A17	210		LD16	250		LA14
171		A18	211		LD17	251		LA15
172		DV _{DD}	212		LD18	252		LA16
173		NC	213		LD19	253		LA17
174		A19	214		NC	254		LA18
175		A20	215		LD20	255		LA19
176		A21	216		LD21	256		DV _{DD}
177		A22	217		DV _{SS}	257		LA20
178		A23	218		CV _{SS}	258		LA21
179		DV _{SS}	219		LD22	259		LA22
180		NC	220		LD23	260		LA23
181		NC	221		LD24	261		DV _{SS}
182		CV _{SS}	222		LD25	262		CV _{SS}
183		LD0	223		DV _{DD}	263		X2 / CLKIN
184		LD1	224		LD26	264		X1
185		LD2	225		LD27	265		V _{SSL}
186		LD3	226		LD28	266		H1
187		LD4	227		LD29	267		V _{DDL}



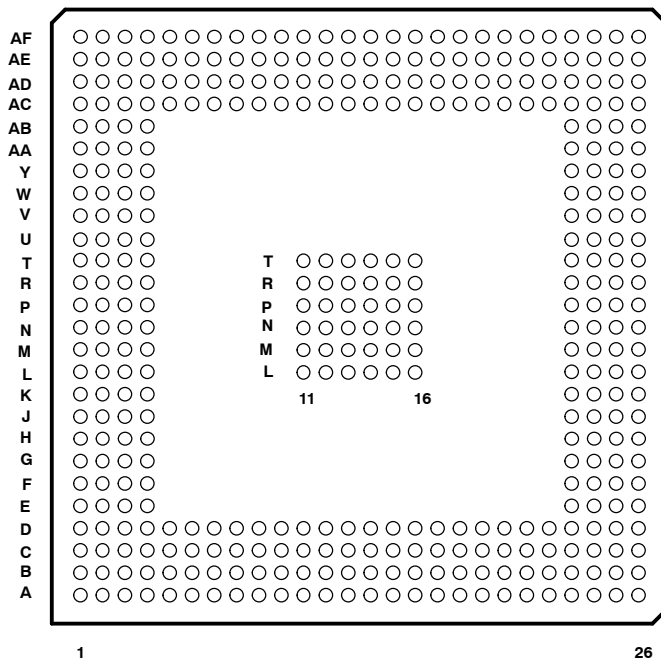
PDB Package Pin Assignments — Numerical Listing (Continued)

NO.	PIN	NAME	NO.	PIN	NAME	NO.	PIN	NAME	NO.	PIN	NAME
188		DV _{DD}	228		LD30	268		H3			
189		NC	229		LD31	269		C1D0			
190		NC	230		CV _{SS}	270		$\overline{\text{ACK}}$			
191		V _{DDL}	231		DV _{SS}	271		C1D1			
192		LD5	232		LA0	272		DV _{DD}			
193		V _{SSL}	233		LA1	273		LSTAT3			
194		LD6	234		LA2	274		C1D2			
195		LD7	235		LA3	275		LSTAT2			
196		LD8	236		DV _{DD}	276		C1D3			
197		LD9	237		LA4	277		LSTAT1			
198		NC	238		LA5	278		C1D4			
199		NC	239		LA6	279		LSTAT0			
200		LD10	240		LA7	280		C1D5			

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388-PIN GFW BALL GRID ARRAY (BOTTOM VIEW)



- NOTES:
- A. N/C = No connection to this frame pin
 - B. Numbers around the detail in this figure are ball pin numbers.
 - C. V_{SS} ground potential ring is connected to the BGA ball pins as listed:
A1, A2, A26, B2, B25, B26, C3, C24, D4, D9, D14, D19, D23, H4, J23, L11 – L16, M11 – M16, N4, P23, V4, W23, AC4, AC8, AC13, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26. (The following V_{SS} pins are also thermal connections)
L11 – L16, T11 – T16, M11 – M16, N11 – N16, P11 – P16, R11 – R16.
 - D. V_{DD} power potential ring is connected to the BGA ball pins as listed:
D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AA23, AC6, AC11, AC16, AC21.

GFW Package Pin Assignments Numerical Listing by Ball Pin Number

NO.	PIN	NAME	NO.	PIN	NAME	NO.	PIN	NAME	NO.	PIN	NAME
A1		V_{SS}	B17		LD13	D7		N/C	G25		N/C
A2		V_{SS}	B18		N/C	D8		A15	G26		N/C
A3		N/C	B19		LD16	D9		V_{SS}	H1		N/C
A4		A7	B20		LD19	D10		A21	H2		D22
A5		N/C	B21		N/C	D11		V_{DD}	H3		D21
A6		N/C	B22		LD25	D12		N/C	H4		V_{SS}
A7		A14	B23		LD27	D13		N/C	H23		LA11
A8		A18	B24		LD29	D14		V_{SS}	H24		LA10
A9		N/C	B25		V_{SS}	D15		LD6	H25		LA13
A10		A22	B26		V_{SS}	D16		V_{DD}	H26		LA12
A11		N/C	C1		A1	D17		N/C	J1		D19
A12		LD1	C2		A2	D18		N/C	J2		D20
A13		N/C	C3		V_{SS}	D19		V_{SS}	J3		D17
A14		N/C	C4		A4	D20		N/C	J4		N/C
A15		LD9	C5		A6	D21		V_{DD}	J23		V_{SS}

† Thermal connection



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GFW Package Pin Assignments Numerical Listing by Ball Pin Number (Continued)

PIN		PIN		PIN		PIN	
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
A16	N/C	C6	A10	D22	LD24	J24	N/C
A17	LD11	C7	N/C	D23	V _{SS}	J25	LA16
A18	LD14	C8	A13	D24	N/C	J26	LA14
A19	LD15	C9	A17	D25	LA3	K1	D16
A20	LD18	C10	A19	D26	LA1	K2	D18
A21	LD20	C11	A23	E1	D29	K3	N/C
A22	LD22	C12	N/C	E2	V _(SUB)	K4	N/C
A23	N/C	C13	LD2	E3	D30	K23	LA17
A24	LD28	C14	LD4	E4	D31	K24	LA15
A25	LD30	C15	LD5	E23	LA2	K25	N/C
A26	V _{SS}	C16	LD8	E24	LA0	K26	LA18
B1	A3	C17	N/C	E25	LA5	L1	D14
B2	V _{SS}	C18	LD12	E26	LA4	L2	D15
B3	A5	C19	N/C	F1	N/C	L3	D12
B4	A9	C20	LD17	F2	D28	L4	V _{DD}
B5	A11	C21	LD21	F3	D26	L11	V _{SS} [†]
B6	A12	C22	LD23	F4	V _{DD}	L12	V _{SS} [†]
B7	A16	C23	LD26	F23	V _{DD}	L13	V _{SS} [†]
B8	N/C	C24	V _{SS}	F24	N/C	L14	V _{SS} [†]
B9	A20	C25	N/C	F25	LA9	L15	V _{SS} [†]
B10	N/C	C26	LD31	F26	LA7	L16	V _{SS} [†]
B11	LD0	D1	N/C	G1	D24	L23	V _{DD}
B12	LD3	D2	A0	G2	D25	L24	LA19
B13	N/C	D3	N/C	G3	D23	L25	LA23
B14	LD7	D4	V _{SS}	G4	D27	L26	LA21
B15	LD10	D5	A8	G23	LA8	M1	N/C
B16	N/C	D6	V _{DD}	G24	LA6	M2	D13
M3	N/C	R3	D3	W1	N/C	AC11	V _{DD}
M4	D11	R4	D1	W2	C4D5	AC12	C5D3
M11	V _{SS} [†]	R11	V _{SS} [†]	W3	RDY0	AC13	V _{SS}
M12	V _{SS} [†]	R12	V _{SS} [†]	W4	CE0	AC14	N/C
M13	V _{SS} [†]	R13	V _{SS} [†]	W23	V _{SS}	AC15	C2D2
M14	V _{SS} [†]	R14	V _{SS} [†]	W24	LLOCK	AC16	V _{DD}
M16	V _{SS} [†]	R15	V _{SS} [†]	W25	LAE	AC17	N/C
M15	V _{SS} [†]	R16	V _{SS} [†]	W26	N/C	AC18	V _{SS}
M23	LA20	R23	TACK	Y1	C4D3	AC19	N/C
M24	LA22	R24	H3	Y2	C4D4	AC20	CAK1
M25	X2CLKIN	R25	C1D2	Y3	C4D0	AC21	V _{DD}
M26	N/C	R26	LSTAT3	Y4	DE	AC22	N/C
N1	N/C	T1	D2	Y23	LRDY1	AC23	V _{SS}
N2	N/C	T2	D4	Y24	N/C	AC24	LRW0
N3	D7	T3	N/C	Y25	TCLK0	AC25	LSTRB0

† Thermal connection

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GFW Package Pin Assignments Numerical Listing by Ball Pin Number (Continued)

NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME
N4	V _{SS}	T4	V _{DD}	Y26	TCLK1	AC26	LPAGE0
N11	V _{SS} [†]	T11	V _{SS} [†]	AA1	C4D1	AD1	N/C
N12	V _{SS} [†]	T12	V _{SS} [†]	AA2	C4D2	AD2	N/C
N13	V _{SS} [†]	T13	V _{SS} [†]	AA3	CSTRB4	AD3	V _{SS}
N14	V _{SS} [†]	T14	V _{SS} [†]	AA4	V _{DD}	AD4	PAGE1
N15	V _{SS} [†]	T15	V _{SS} [†]	AA23	V _{DD}	AD5	STAT0
N16	V _{SS} [†]	T16	V _{SS} [†]	AA24	LCE1	AD6	STAT2
N23	H1	T23	V _{DD}	AA25	LPAGE1	AD7	PAGE0
N24	N/C	T24	N/C	AA26	LDE	AD8	RESETLOC1
N25	N/C	T25	LSTAT1	AB1	CRDY4	AD9	CSTRB5
N26	N/C	T26	LSTAT2	AB2	TCK	AD10	C5D7
P1	D8	U1	N/C	AB3	TDO	AD11	N/C
P2	D10	U2	D0	AB4	TMS	AD12	N/C
P3	D5	U3	C4D6	AB23	LCE0	AD13	N/C
P4	D9	U4	CE1	AB24	LSTRB1	AD14	C2D7
P11	V _{SS} [†]	U23	C1D4	AB25	LRDY0	AD15	C2D4
P12	V _{SS} [†]	U24	C1D3	AB26	LRW1	AD16	C2D1
P13	V _{SS} [†]	U25	N/C	AC1	TRST	AD17	CRDY2
P14	V _{SS} [†]	U26	LSTAT0	AC2	N/C	AD18	CDIR1
P15	V _{SS} [†]	V1	RDY1	AC3	N/C	AD19	CDIR5
P16	V _{SS} [†]	V2	C4D7	AC4	V _{SS}	AD20	CREQ1
P23	V _{SS}	V3	LOCK	AC5	STRB1	AD21	CRDY1
P24	X1	V4	V _{SS}	AC6	V _{DD}	AD22	IIOF3
P25	C1D1	V23	C1D7	AC7	N/C	AD23	N/C
P26	C1D0	V24	C1D5	AC8	V _{SS}	AD24	V _{SS}
R1	N/C	V25	C1D6	AC9	STRB0	AD25	N/C
R2	D6	V26	N/C	AC10	CACK5	AD26	N/C
AE1	V _{SS}	AE14	C5D1	AF1	V _{SS}	AF14	C5D0
AE2	V _{SS}	AE15	N/C	AF2	TD1	AF15	C2D6
AE3	EMU0	AE16	C2D5	AF3	EMU1	AF16	C2D3
AE4	CACK4	AE17	N/C	AF4	CREQ4	AF17	C2D0
AE5	RW1	AE18	N/C	AF5	N/C	AF18	CSTRB2
AE6	STAT1	AE19	CACK2	AF6	N/C	AF19	CREQ2
AE7	N/C	AE20	CDIR2	AF7	STAT3	AF20	CDIR4
AE8	RW0	AE21	CSTRB1	AF8	AE	AF21	ROMEN
AE9	RESETLOC0	AE22	IIOF0	AF9	RESET	AF22	IIOF1
AE10	CRDY5	AE23	N/C	AF10	N/C	AF23	IIOF2
AE11	CREQ5	AE24	NMI	AF11	C5D6	AF24	N/C
AE12	C5D5	AE25	V _{SS}	AF12	C5D4	AF25	V _{SS}
AE13	N/C	AE26	N/C	AF13	C5D2	AF26	V _{SS}

† Thermal connection



GFW Package Pin Assignments Alphabetical Listing by Ball Pin Function

PIN		PIN		PIN		PIN	
NO.	FUNCTION	NO.	FUNCTION	NO.	FUNCTION	NO.	FUNCTION
D2	A0	AA1	C4D1	P3	D5	E25	LA5
C1	A1	AA2	C4D2	R2	D6	G24	LA6
C2	A2	Y1	C4D3	N3	D7	F26	LA7
B1	A3	Y2	C4D4	P1	D8	G23	LA8
C4	A4	W2	C4D5	P4	D9	F25	LA9
B3	A5	U3	C4D6	P2	D10	H24	LA10
C5	A6	V2	C4D7	M4	D11	H23	LA11
A4	A7	AF14	C5D0	L3	D12	H26	LA12
D5	A8	AE14	C5D1	M2	D13	H25	LA13
B4	A9	AF13	C5D2	L1	D14	J26	LA14
C6	A10	AC12	C5D3	L2	D15	K24	LA15
B5	A11	AF12	C5D4	K1	D16	J25	LA16
B6	A12	AE12	C5D5	J3	D17	K23	LA17
C8	A13	AF11	C5D6	K2	D18	K26	LA18
A7	A14	AD10	C5D7	J1	D19	L24	LA19
D8	A15	AC20	$\overline{\text{CACK1}}$	J2	D20	M23	LA20
B7	A16	AE19	$\overline{\text{CACK2}}$	H3	D21	L26	LA21
C9	A17	AE4	$\overline{\text{CACK4}}$	H2	D22	M24	LA22
A8	A18	AC10	$\overline{\text{CACK5}}$	G3	D23	L25	LA23
C10	A19	AD18	CDIR1	G1	D24	W25	$\overline{\text{LAE}}$
B9	A20	AE20	CDIR2	G2	D25	AB23	$\overline{\text{LCE0}}$
D10	A21	AF20	CDIR4	F3	D26	AA24	$\overline{\text{LCE1}}$
A10	A22	AD19	CDIR5	G4	D27	B11	LD0
C11	A23	W4	$\overline{\text{CE0}}$	F2	D28	A12	LD1
AF8	$\overline{\text{AE}}$	U4	$\overline{\text{CE1}}$	E1	D29	C13	LD2
P26	C1D0	AD21	$\overline{\text{CRDY1}}$	E3	D30	B12	LD3
P25	C1D1	AD17	$\overline{\text{CRDY2}}$	E4	D31	C14	LD4
R25	C1D2	AB1	$\overline{\text{CRDY4}}$	Y4	$\overline{\text{DE}}$	C15	LD5
U24	C1D3	AE10	$\overline{\text{CRDY5}}$	AE3	EMU0	D15	LD6
U23	C1D4	AD20	$\overline{\text{CREQ1}}$	AF3	EMU1	B14	LD7
V24	C1D5	AF19	$\overline{\text{CREQ2}}$	N23	H1	C16	LD8
V25	C1D6	AF4	$\overline{\text{CREQ4}}$	R24	H3	A15	LD9
V23	C1D7	AE11	$\overline{\text{CREQ5}}$	R23	$\overline{\text{IACK}}$	B15	LD10
AF17	C2D0	AE21	$\overline{\text{CSTRB1}}$	AE22	IIOF0	A17	LD11
AD16	C2D1	AF18	$\overline{\text{CSTRB2}}$	AF22	IIOF1	C18	LD12
AC15	C2D2	AA3	$\overline{\text{CSTRB4}}$	AF23	IIOF2	B17	LD13
AF16	C2D3	AD9	$\overline{\text{CSTRB5}}$	AD22	IIOF3	A18	LD14
AD15	C2D4	U2	D0	E24	LA0	A19	LD15
AE16	C2D5	R4	D1	D26	LA1	B19	LD16
AF15	C2D6	T1	D2	E23	LA2	C20	LD17
AD14	C2D7	R3	D3	D25	LA3	A20	LD18
Y3	C4D0	T2	D4	E26	LA4	B20	LD19

† Thermal connection



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GFW Package Pin Assignments Alphabetical Listing by Ball Pin Function (Continued)

PIN		PIN		PIN		PIN	
NO.	FUNCTION	NO.	FUNCTION	NO.	FUNCTION	NO.	FUNCTION
A21	LD20	AC7	N/C	G25	N/C	AB2	TCK
C21	LD21	AD1	N/C	G26	N/C	Y25	TCLK0
A22	LD22	AD11	N/C	H1	N/C	Y26	TCLK1
C22	LD23	AD12	N/C	J24	N/C	AF2	TD1
D22	LD24	AD13	N/C	J4	N/C	AB3	TDO
B22	LD25	AD2	N/C	K25	N/C	AB4	TMS
C23	LD26	AD23	N/C	K3	N/C	AC1	TRST
B23	LD27	AD25	N/C	K4	N/C	AA23	V _{DD}
A24	LD28	AD26	N/C	M1	N/C	AA4	V _{DD}
B24	LD29	AE13	N/C	M26	N/C	AC11	V _{DD}
A25	LD30	AE15	N/C	M3	N/C	AC16	V _{DD}
C26	LD31	AE17	N/C	N1	N/C	AC21	V _{DD}
AA26	LDE	AE18	N/C	N2	N/C	AC6	V _{DD}
W24	LOCK	AE23	N/C	N24	N/C	D11	V _{DD}
V3	LOCK	AE26	N/C	N25	N/C	D16	V _{DD}
AC26	LPAGE0	AE7	N/C	N26	N/C	D21	V _{DD}
AA25	LPAGE1	AF10	N/C	R1	N/C	D6	V _{DD}
AB25	LRDY0	AF24	N/C	T24	N/C	F23	V _{DD}
Y23	LRDY1	AF5	N/C	T3	N/C	F4	V _{DD}
AC24	LRW0	AF6	N/C	U1	N/C	L23	V _{DD}
AB26	LRW1	B10	N/C	U25	N/C	L4	V _{DD}
U26	LSTAT0	B13	N/C	V26	N/C	T23	V _{DD}
T25	LSTAT1	B16	N/C	W1	N/C	T4	V _{DD}
T26	LSTAT2	B18	N/C	W26	N/C	A1	V _{SS}
R26	LSTAT3	B21	N/C	Y24	N/C	A2	V _{SS}
AC25	LSTRB0	B8	N/C	AE24	NMI	A26	V _{SS}
AB24	LSTRB1	C12	N/C	AD7	PAGE0	B2	V _{SS}
A11	N/C	C17	N/C	AD4	PAGE1	B25	V _{SS}
A13	N/C	C19	N/C	W3	RDY0	B26	V _{SS}
A14	N/C	C25	N/C	V1	RDY1	C24	V _{SS}
A16	N/C	C7	N/C	AF9	RESET	C3	V _{SS}
A23	N/C	D1	N/C	AE9	RESETLOC0	D14	V _{SS}
A3	N/C	D12	N/C	AD8	RESETLOC1	D19	V _{SS}
A5	N/C	D13	N/C	AF21	ROMEN	D23	V _{SS}
A6	N/C	D17	N/C	AE8	RW0	D4	V _{SS}
A9	N/C	D18	N/C	AE5	RW1	D9	V _{SS}
AC14	N/C	D20	N/C	AD5	STAT0	H4	V _{SS}
AC17	N/C	D24	N/C	AE6	STAT1	J23	V _{SS}
AC19	N/C	D3	N/C	AD6	STAT2	L11	V _{SS} [†]
AC2	N/C	D7	N/C	AF7	STAT3	L12	V _{SS} [†]
AC22	N/C	F1	N/C	AC9	STRB0	L13	V _{SS} [†]
AC3	N/C	F24	N/C	AC5	STRB1	L14	V _{SS} [†]
L15	V _{SS} [†]	N4	V _{SS}	T11	V _{SS} [†]	AD24	V _{SS}

† Thermal connection



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GFW Package Pin Assignments Alphabetical Listing by Ball Pin Function (Continued)

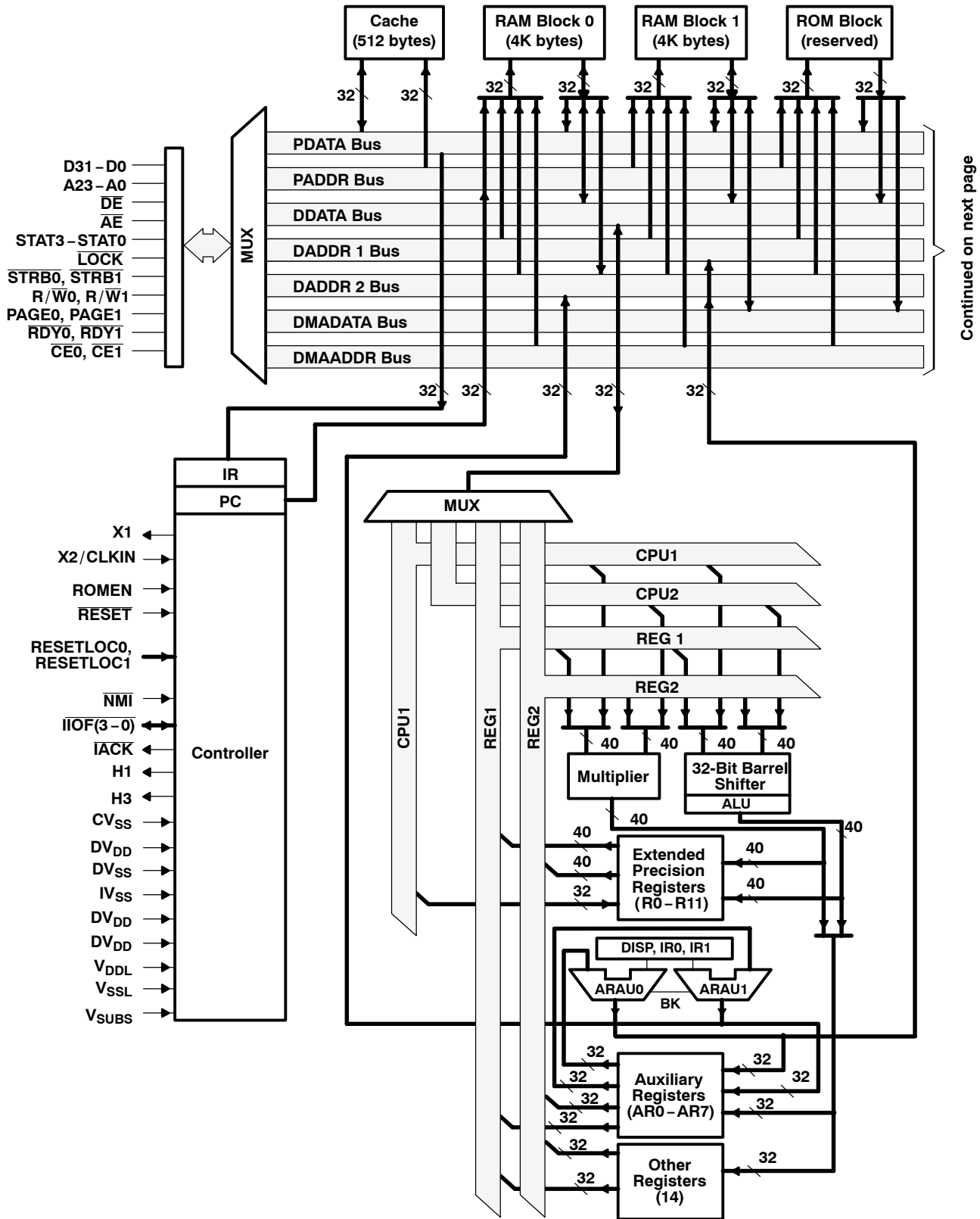
PIN		PIN		PIN		PIN	
NO.	FUNCTION	NO.	FUNCTION	NO.	FUNCTION	NO.	FUNCTION
L16	V _{SS} [†]	P11	V _{SS} [†]	T12	V _{SS} [†]	AE1	V _{SS}
M11	V _{SS} [†]	P12	V _{SS} [†]	T13	V _{SS} [†]	AE2	V _{SS}
M12	V _{SS} [†]	P13	V _{SS} [†]	T14	V _{SS} [†]	AE25	V _{SS}
M13	V _{SS} [†]	P14	V _{SS} [†]	T15	V _{SS} [†]	AF1	V _{SS}
M14	V _{SS} [†]	P15	V _{SS} [†]	T16	V _{SS} [†]	AF25	V _{SS}
M15	V _{SS} [†]	P16	V _{SS} [†]	V4	V _{SS}	AF26	V _{SS}
M16	V _{SS} [†]	P23	V _{SS}	W23	V _{SS}	E2	V _(SUB)
N11	V _{SS} [†]	R11	V _{SS} [†]	AC4	V _{SS}	P24	X1
N12	V _{SS} [†]	R12	V _{SS} [†]	AC8	V _{SS}	M25	X2CLKIN
N13	V _{SS} [†]	R13	V _{SS} [†]	AC13	V _{SS}		
N14	V _{SS} [†]	R14	V _{SS} [†]	AC18	V _{SS}		
N15	V _{SS} [†]	R15	V _{SS} [†]	AC23	V _{SS}		
N16	V _{SS} [†]	R16	V _{SS} [†]	AD3	V _{SS}		

† Thermal connection

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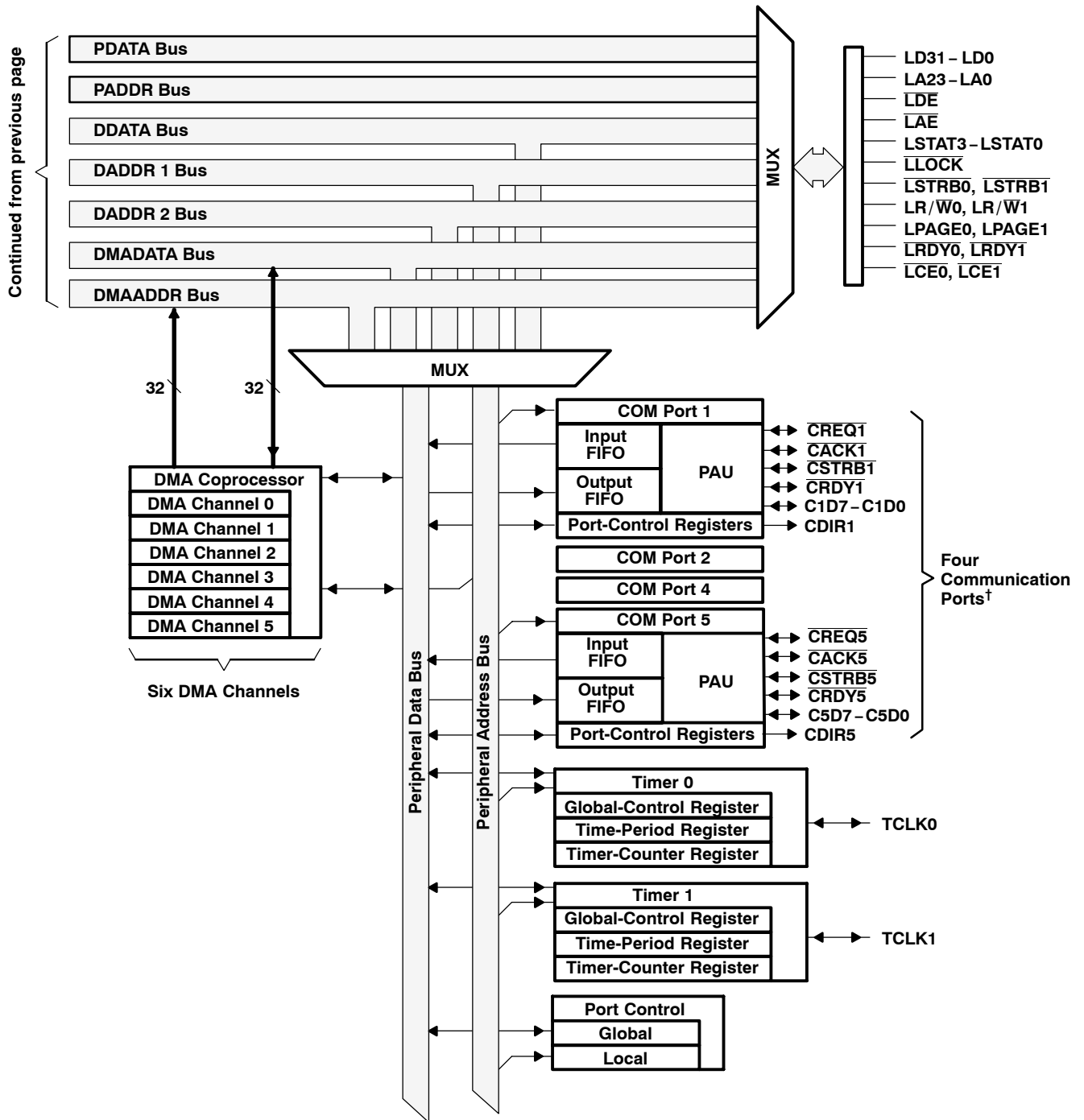
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block diagram



Continued on next page

block diagram (continued)



† Communication ports 0 and 3 are not connected.

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memory map

Figure 1 shows the memory map for the C44. Refer to the *TMS320C4x User's Guide* (literature number SPRU063) for a detailed description of this memory mapping.

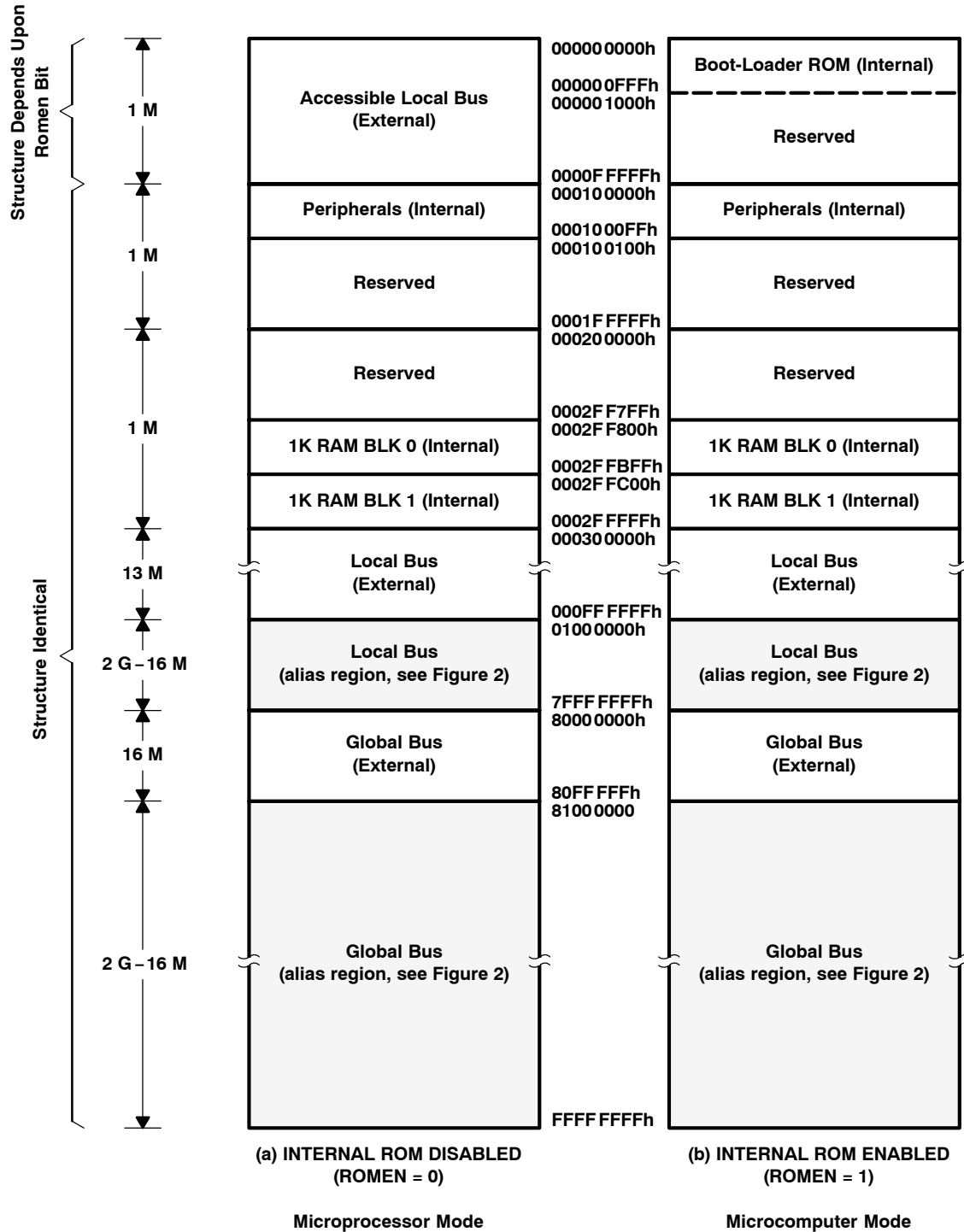


Figure 1. Memory Map for TMS320C44

memory aliasing

The C44 offers global and local addresses of A0–A23 and LA0–LA23, giving an external address reach of $(2 \text{ buses}) \times (2^{24}) = 2^{25}$ words. Since the internal address span of the C44 is 2^{32} words, reading or writing to memory outside of the base-address region causes memory aliasing. Figure 2 shows how the memory pages overlap each other.

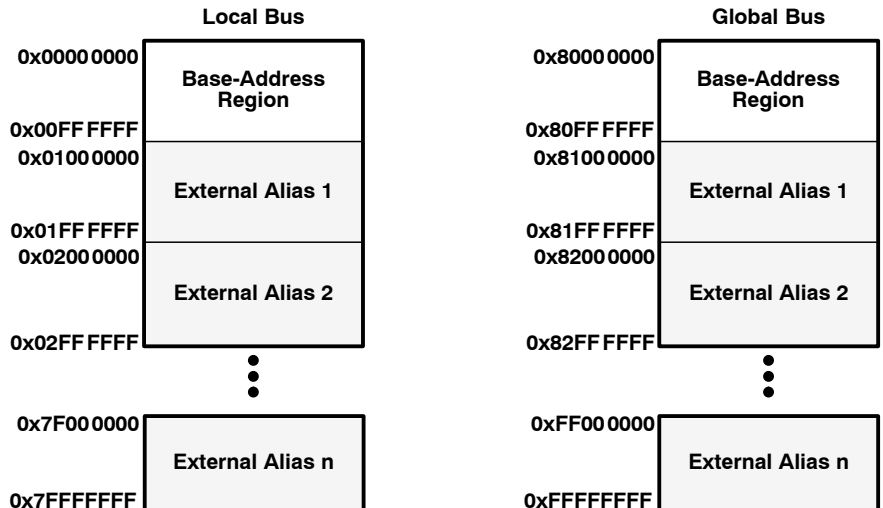


Figure 2. Memory Alias

central processing unit

The C44 CPU is configured for high-speed internal parallelism for the highest sustained performance. The key features of the CPU are:

- Eight operations/cycle:
 - 40-/32-bit floating-point/integer multiply
 - 40-/32-bit floating-point/integer ALU operation
 - Two data accesses
 - Two address-register updates
- Floating-point conversion
- Divide and square-root support
- C3x and C4x assembly-language compatibility
- Byte and halfword accessibility

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DMA coprocessor

The DMA coprocessor allows concurrent I/O and CPU processing for the highest sustained CPU performance. The key features of the DMA coprocessor are:

- Link pointers to allow DMA channels to autoinitialize without CPU intervention
- Parallel CPU operation and DMA transfers
- Six DMA channels to support memory-to-memory data transfers
- Split-mode operation which doubles the available channels to twelve when data transfers to and from a communication port are required

communication ports

The C44 contains four identical high-speed communication ports, each of which provides a bidirectional-communication interface to other C4x devices and external peripherals. The key features of the communication ports are:

- Direct interprocessor communication and processor I/O
- 20M-byte/s bidirectional interface on each communication port for high-speed multiprocessor interface
- Port direction pin (CDIR) to ease interfacing
- Separate input and output 8-word-deep FIFO buffers for processor-to-processor communication and I/O
- Automatic arbitration and handshaking for direct processor-to-processor connection

communication-port direction pin

A port-direction pin (CDIR1, CDIR2, CDIR4, CDIR5) is available for each C44 communication port. When the communication port is in the output mode, CDIRx is driven low. When the communication port is in the input mode, CDIRx is driven high. The truth table for two C44 devices is shown in Table 1. Communication port 1 of CPUA is connected to communication port 4 of CPUB.

Table 1. Truth Table for Two C44 Devices

CDIR1	CDIR4	DESCRIPTION
0	0	Token error
0	1	CPUA is configured to transmit to CPUB.
1	0	CPUB is configured to transmit to CPUA.
1	1	Token exchange overlap, if > 1H then token error

communication-port-software reset

The input and output FIFO levels for a communication port can be flushed by writing at least two back-to-back values to its communication-port software-reset address as specified in Table 2. This software reset flushes any word or byte already present in the FIFOs, but it does not affect the status of the communication-port pins.

Table 2. Communication-Port Software-Reset Address

COMMUNICATION PORT	SOFTWARE-RESET ADDRESS
1	0x0100053
2	0x0100063
4	0x0100083
5	0x0100093

communication-port-software reset (continued)

When used in conjunction with the communication-port direction pins and $\overline{\text{NMI}}$ bus-grant, an effective method of error detection and correction can be achieved. A subroutine showing how to reset communication port 1 is given in Figure 3.

```

; -----;
; RESET1:Flushes FIFOs data for communication port 1;
; -----;
RESET1 push  AR0          ; Save registers
      push  R0           ;
      push  RC           ;
      ldhi  010h,AR0     ; Set AR0 to base address of COM 1
      or   050h,AR0     ;
FLUSH: rpts  1           ; Flush FIFO data with back-to-back write
      sti  R0,*+AR0(3)  ;
      rpts  10          ; Wait
      nop                ;
      ldi  *+AR0(0),R0  ; Check for new data from other port
      and  01FE0h,R0    ;
      bnz  FLUSH        ;
      pop  RC           ; Restore registers
      pop  R0           ;
      pop  AR0          ;
      rets              ; Return

```

Figure 3. Example of Communication-Port-Software Reset

$\overline{\text{NMI}}$ with bus-grant feature

The C44 devices have a software-configurable feature that allows forcing the internal-peripheral bus ready when the $\overline{\text{NMI}}$ signal is asserted. The $\overline{\text{NMI}}$ bus-grant feature is enabled when bits 19 and 18 of the status register (ST) are set to 10b. When enabled, a peripheral bus-grant signal is generated on the falling edge of $\overline{\text{NMI}}$. If $\overline{\text{NMI}}$ is asserted and this feature is not enabled, the CPU stalls on access to the peripheral bus if it is not ready. A stall condition occurs when writing to a full output FIFO or reading an empty input FIFO. This feature is useful in correcting communication-port errors when used in conjunction with the communication-port software-reset feature.

IDLE2 clock-stop power-down mode

The C44 has a clock-stop mode, or power-down mode (IDLE2) to achieve extremely low power consumption. When an IDLE2 instruction is executed, the clocks are halted with H1 held high. (Exiting IDLE2 requires asserting one of the $\overline{\text{IIOF3}}$ – $\overline{\text{IIOF0}}$ pins configured as an external interrupt.) A macro showing how to generate the IDLE2 opcode is given in Figure 4. During this power-down mode:

- No instructions are executed.
- The CPU, peripherals, and internal memory retain their previous state.
- The external-bus outputs are idle. The address lines remain in their previous state; the data lines are in the high-impedance state; and the output-control signals are inactive.

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IDLE2 clock-stop power-down mode (continued)

```

; -----;
; IDLE2: Macro to generate idle2 opcode ;
; -----;
IDLE2      .macro
           .word      06000001h
           .endm

```

Figure 4. Example Software Subroutine Using IDLE2

IDLE2 is exited when one of the five external interrupts ($\overline{\text{NMI}}$ and $\overline{\text{IIOF3}}$ – $\overline{\text{IIOF0}}$) is asserted low for at least four input clocks (two H1 cycles). The clocks then start after a delay of two input clocks (one H1 cycle). The clocks can start in the opposite phase; that is, H1 can be high when H3 was high before the clocks were stopped. However, the H1 and H3 clocks remain 180 degrees out of phase with each other.

During IDLE2 operation, an external interrupt can be recognized and serviced by the CPU if it is enabled before entering IDLE2 and asserted for at least two H1 cycles. For the processor to recognize only one interrupt, the interrupt pin must be configured for edge-trigger mode or asserted less than three cycles in level-trigger mode. Any external interrupt pin can wake up the device from IDLE2, but for the CPU to recognize that interrupt, it must also be enabled. If an interrupt is recognized and executed by the CPU, the instruction following the IDLE2 instruction is not executed until after a return opcode is executed.

When the device is in emulation mode, the CPU executes an IDLE2 instruction as if it were an IDLE instruction. The clocks continue to run for correct operation of the emulator.

boot-loader mode selection

Table 3. Boot-Loader Mode Selection Using Pins $\overline{\text{IIOF3}}$ – $\overline{\text{IIOF0}}$

EXTERNAL PIN				SOURCE PROGRAM LOCATION
$\overline{\text{IIOF3}}$	$\overline{\text{IIOF2}}$	$\overline{\text{IIOF1}}$	$\overline{\text{IIOF0}}$	
1	1	0	1	Load source program from address 0030 0000h
1	0	1	1	Load source program from address 4000 0000h (see Note 1)
1	0	0	1	Load source program from address 80 0000h
0	1	1	1	Load source program from address 8000 0000h (see Note 2)
0	1	0	1	Load source program from address 8040 0000h (see Note 3)
0	0	1	1	Load source program from address 8080 0000h (see Note 4)
0	0	0	1	Reserved (boot-loader program terminates)
1	1	1	1	Load source program from communication port

- NOTES: 1. This selection cause the C44 to drive 0 in the 24 external local address pins and activates the $\overline{\text{LSTRB0}}$ signal.
2. This selection cause the C44 to drive 0 in the 24 external global address pins ando activates the $\overline{\text{STRB0}}$ signal.
3. This selection cause the C44 to drive 0x40 0000 in the 24 external global address pins and activates the $\overline{\text{STRB0}}$ signal.
4. This selection cause the C44 to drive 0x80 0000 in the 24 external global address pins and to activate the $\overline{\text{STRB0}}$ signal.



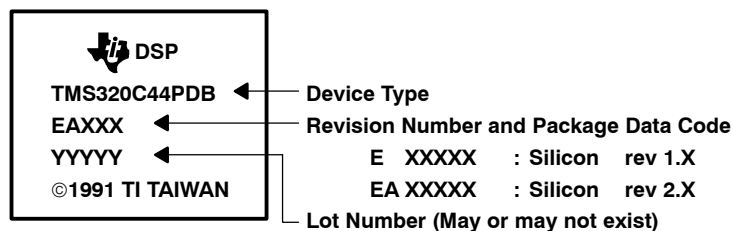
development tools

A key aspect to a parallel-processing implementation is the development tools available. The C44 is supported by a host of parallel-processing tools for developing and simulating code easily and for debugging parallel-processing systems. The code-generation tools include:

- An optimizing ANSI C compiler with a runtime-support library that supports use of communication ports and DMA
- Third party support for C, C++, and Ada compilers
- Several operating systems available for parallel-processing support as well as DMA and communication-port drivers
- Assembler and linker with support for mapping program and data to parallel processors

The simulation tools include a TI software-simulator with a high-level-language debugger interface for simulating a single processor. The hardware development and verification tools consist of the XDS510™ (parallel-processor in-circuit emulator and high-level-language debugger).

silicon revision identification



XDS510 is a trademark of Texas Instruments.

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silicon revision identification (continued)

Table 4. Device Descriptions

DEVICE PART NUMBER	VOLTAGE	OPERATING FREQUENCY	COMM PORTS	PACKAGE
TMS320C40GFL	5 V	50 MHz/40 ns	6	325-pin ceramic PGA
TMS320C40GFL60	5 V	60 MHz/33 ns	6	325-pin ceramic PGA
TMS320C44PDB50	5 V	50 MHz/40 ns	4	304-pin PQFP
TMS320C44PDB60	5 V	60 MHz/33 ns	4	304-pin PQFP
TMS320C44GFW	5 V	50 MHz/40 ns	4	388-pad ball grid array
TMS320C44GFW60	5 V	60 MHz/33 ns	4	388-pad ball grid array
TMS320C44GFWA	5 V	50 MHz/40 ns	4	388-pad ball grid array (industrial temp.)
SMJ320C40GFM40	5 V	40 MHz/50 ns	6	325-pin ceramic PGA
SMJ320C40GFM50	5 V	50 MHz/40 ns	6	325-pin ceramic PGA
SMJ320C40HFHM40	5 V	40 MHz/50 ns	6	352-lead ceramic PGA
SMJ320C40HFHM50	5 V	50 MHz/40 ns	6	352-lead ceramic PGA
SMJ320C40TAM40	5 V	40 MHz/50 ns	6	324 pad TAB tape (encapsulated)
SMJ320C40TBM40	5 V	40 MHz/50 ns	6	324 pad TAB tape (bare die)
TMS320C40TAL50	5 V	50 MHz/40 ns	6	324 pad TAB tape (encapsulated)
SMJ320C40TAM50	5 V	50 MHz/40 ns	6	324 pad TAB tape (encapsulated)
SMJ320C40TBM50	5 V	50 MHz/40 ns	6	324 pad TAB tape (bare die)
TMS320C40TAL60	5 V	60 MHz/33 ns	6	324 pad TAB tape (encapsulated)
SMJ320C40KGDM40	5 V	40 MHz/50 ns	6	Known good die
SMJ320C40KGDM50	5 V	50 MHz/40 ns	6	Known good die
TMS320C40KGDL50	5 V	50 MHz/40 ns	6	Known good die
TMS320C40KGDL60	5 V	60 MHz/33 ns	6	Known good die



absolute maximum ratings over specified temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD} (see Note 5)	– 0.3 V to 7 V
Input voltage range	– 0.3 V to 7 V
Output voltage range	– 0.3 V to 7 V
Operating case temperature range, T_C : (PDB and GFW commercial temperature parts)	0°C to 85°C
(GFWA industrial temperature parts) [‡]	– 40°C to 115°C
Storage temperature range, T_{stg}	– 55°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Assuming C44 nominal power consumption (350 mA) and given the C44 thermal characteristics, the maximum T_C corresponds to 85°C

NOTE 5: All voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM [§]	MAX	UNIT
V_{DD}	Supply voltage (DDV _{DD} , etc.)	4.75	5	5.25	V
V_{IH}	High-level input voltage	X2 / CLKIN		$V_{DD} + 0.3$	V
		\overline{CSTRB} and CRDY pins	2.4	$V_{DD} + 0.3$	
		All other pins	2	$V_{DD} + 0.3$	
V_{IL}	Low-level input voltage	– 0.3		0.8	V
I_{OH}	High-level output current			– 300	μA
I_{OL}	Low-level output current			2	mA
T_C	Operating case temperature	PDB and GFW (commercial)		85	°C
		GFWA (industrial)	– 40	115	

[§] All typical values are at $V_{DD} = 5$ V, T_A (air temperature) = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS [¶]		MIN	TYP [#]	MAX	UNIT
V_{OH}	High-level output voltage	$V_{DD} = \text{MIN}, I_{OH} = \text{MAX}$		2.4	3		V
V_{OL}	Low-level output voltage	$V_{DD} = \text{MIN}, I_{OL} = \text{MAX}$			0.3	0.6	V
I_Z	High-impedance current	$V_{DD} = \text{MAX}$		– 20		20	μA
I_I	Input current	X2/CLKIN only	$V_I = V_{SS} \text{ to } V_{DD}$	– 30		30	μA
		Inputs with internal pullups (see Note 6)		– 400		20	
		All others		– 10		10	
I_{CC}	Supply current	$T_A = 25^\circ\text{C}, V_{DD} = \text{MAX}, f_x = \text{MAX}$ (see Note 7)	C44-40		350	850	mA
			C44-50				
			C44-60		350	950	
C_I	Input capacitance					15	pF
C_O	Output capacitance					15	pF

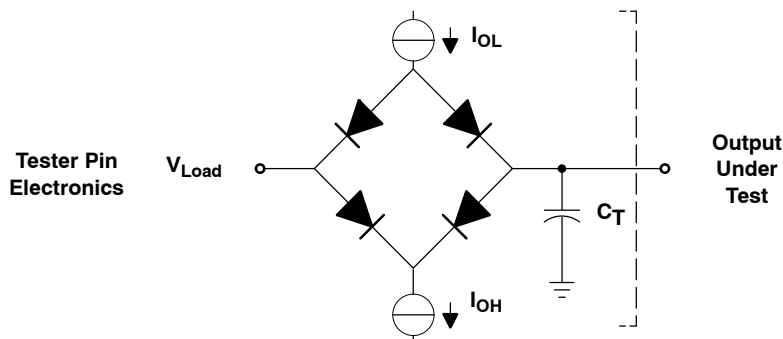
[¶] For conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

[#] All typical values are at $V_{DD} = 3.3$ V, T_A (air temperature) = 25°C.

NOTES: 6. Pins with internal pullup devices: TDI, TCK, TMS. Pin with internal pulldown device: \overline{TRST} .

7. f_x is the input clock frequency. The maximum value (max) for the C44-40, C44-50, and C44-60 is 40, 50 and 60 MHz, respectively.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
 I_{OH} = 300 μ A (all outputs)
 V_{LOAD} = 2.15 V
 C_T = 80 pF typical load-circuit capacitance

Figure 5. Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.
- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.

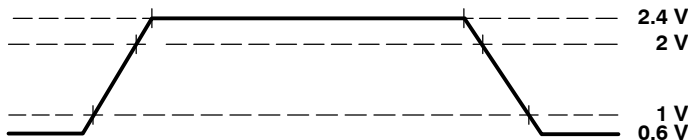


Figure 6. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.92 V (10%) and the level at which the input is said to be high is 1.88 V (90%).
- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.88 V (90%) and the level at which the input is said to be low is 0.92 V (10%).

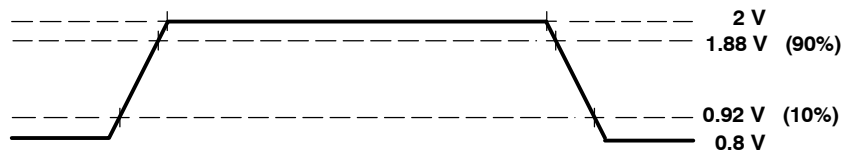


Figure 7. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100. In order to shorten the symbols, pin names that have both global and local applications are generally represented with (L) immediately preceding the basic signal name (for example, (L)RDY represents both the global term RDY and local term LRDY). Other pin names and related terminology have been abbreviated as follows, unless otherwise noted:

A	(L)A23 – (L)A0 or (L)Ax	IACK	$\overline{\text{IACK}}$
AE	$\overline{\text{(L)AE}}$	IF	$\overline{\text{IIOF(3-0)}}$ or $\overline{\text{IIOF}x}$
ASYNCH	Asynchronous reset signals in the high-impedance state	IIOF	$\overline{\text{IIOF(3-0)}}$ or $\overline{\text{IIOF}x}$
BYTE	Byte transfer	LOCK	$\overline{\text{(L)LOCK}}$
CA	$\overline{\text{CACK(1,2,4,5)}}$ or $\overline{\text{CACK}x}$	P	$t_{c(H)}$
CD	C(1,2,4,5)D7 – C(1,2,4,5)D0 or CxDx	PAGE	(L)PAGE0 and (L)PAGE1 or (L)PAGEx
CDIR	CDIR(1,2,4,5) or CDIRx	RDY	$\overline{\text{(L)RDY0}}$, $\overline{\text{(L)RDY1}}$, or $\overline{\text{(L)RDY}x}$
CE	$\overline{\text{(L)CE0}}$, $\overline{\text{(L)CE1}}$, or $\overline{\text{(L)CE}x}$	RESET	RESET
CI	CLKIN	RW	(L)R/ $\overline{\text{W0}}$, (L)R/ $\overline{\text{W1}}$, or (L)R/ $\overline{\text{W}x}$
COMM	Asynchronous reset signals	S	$\overline{\text{(L)STRB0}}$, $\overline{\text{(L)STRB1}}$, or $\overline{\text{(L)STRB}x}$
CONTROL	Control signals	ST	(L)STAT3 – (L)STAT0 or (L)STATx
CRQ	$\overline{\text{CREQ(1,2,4,5)}}$ or $\overline{\text{CREQ}x}$	TCK	TCK
CRDY	$\overline{\text{CRDY(1,2,4,5)}}$ or $\overline{\text{CRDY}x}$	TCLK	TCLK0, TCLK1, or TCLKx
CS	$\overline{\text{CSTRB(1,2,4,5)}}$ or $\overline{\text{CSTRB}x}$	TDO	TDO
D	(L)D31 – (L)D0 or (L)Dx	TMS	TMS/TDI
DE	$\overline{\text{(L)DE}}$	WORD	32-bit word transfer
H	H1, H3		

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timing for X2/CLKIN, H1, H3 (see Figure 8 and Figure 9)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$ Fall time, CLKIN		5		5	ns
2	$t_{w(CIL)}$ Pulse duration, CLKIN low, $t_{c(CI)} = \text{MIN}$	7		5		ns
3	$t_{w(CIH)}$ Pulse duration, CLKIN high, $t_{c(CI)} = \text{MIN}$	7		5		ns
4	$t_{r(CI)}$ Rise time, CLKIN		5		5	ns
5	$t_{c(CI)}$ Cycle time, CLKIN	20	242.5	16.67	242.5	ns
6	$t_{f(H)}$ Fall time, H1 and H3		3		3	ns
7	$t_{w(HL)}$ Pulse duration, H1 and H3 low	$t_{c(CI)} - 6$	$t_{c(CI)} + 6$	$t_{c(CI)} - 6$	$t_{c(CI)} + 6$	ns
8	$t_{w(HH)}$ Pulse duration, H1 and H3 high	$t_{c(CI)} - 6$	$t_{c(CI)} + 6$	$t_{c(CI)} - 6$	$t_{c(CI)} + 6$	ns
9	$t_{r(H)}$ Rise time, H1 and H3		4		4	ns
9.1	$t_{d(HL-HH)}$ Delay time from H1 low to H3 high or from H3 low to H1 high	-1	4	-1	4	ns
10	$t_{c(H)}$ Cycle time, H1 and H3 [†]	40	485	33.3	485	ns

[†] Maximum cycle time is not limited during IDLE2 operation.

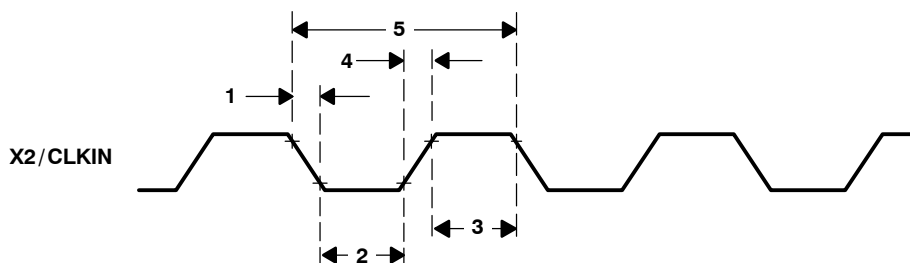


Figure 8. X2/CLKIN Timing

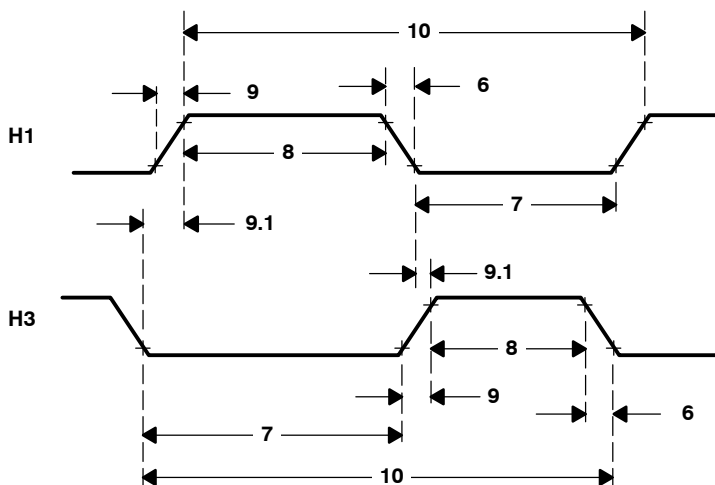


Figure 9. H1 and H3 Timings

memory-read-cycle and memory-write-cycle timing [$\overline{(L)STRBx} = 0$] (see Note 8, Figure 10, and Figure 11)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(H1L-SL)}$ Delay time, H1 low to $\overline{(L)STRBx}$ low	0	9	0	8	ns
2	$t_{d(H1L-SH)}$ Delay time, H1 low to $\overline{(L)STRBx}$ high	0	9	0	8	ns
3	$t_{d(H1H-RWL)}$ Delay time, H1 high to $(L)R/\overline{Wx}$ low	0	9	0	8	ns
4	$t_{d(H1L-A)}$ Delay time, H1 low to $(L)Ax$ valid	0	9	0	8	ns
5	$t_{su(D-H1L)R}$ Setup time, $(L)Dx$ valid before H1 low (read)	10		9		ns
6	$t_{h(H1L-D)R}$ Hold time, $(L)Dx$ after H1 low (read)	0		0		ns
7	$t_{su(RDY-H1L)}$ Setup time, $\overline{(L)RDYx}$ valid before H1 low	20 [†]		18		ns
8	$t_{h(H1L-RDY)}$ Hold time, $\overline{(L)RDYx}$ after H1 low	0		0		ns
8.1	$t_{d(H1L-ST)}$ Delay time, H1 low to $(L)STAT3 - (L)STAT0$ valid		8		8	ns
9	$t_{d(H1H-RWH)W}$ Delay time, H1 high to $(L)R/\overline{Wx}$ high (write)	0	9	0	8	ns
10	$t_{v(H1L-D)W}$ Valid time, $(L)Dx$ after H1 low (write)		16		13	ns
11	$t_{h(H1H-D)W}$ Hold time, $(L)Dx$ after H1 high (write)	0		0		ns
12	$t_{d(H1H-A)}$ Delay time, H1 high to address valid on back-to-back write cycles		9		8	ns

[†] If this setup time is not met, the read/write operation is not assured.

NOTE 8: For consecutive reads, $(L)R/\overline{Wx}$ stays high and $\overline{(L)STRBx}$ stays low.

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memory-read-cycle and memory-write-cycle timing [(L)STRBx = 0] (continued)

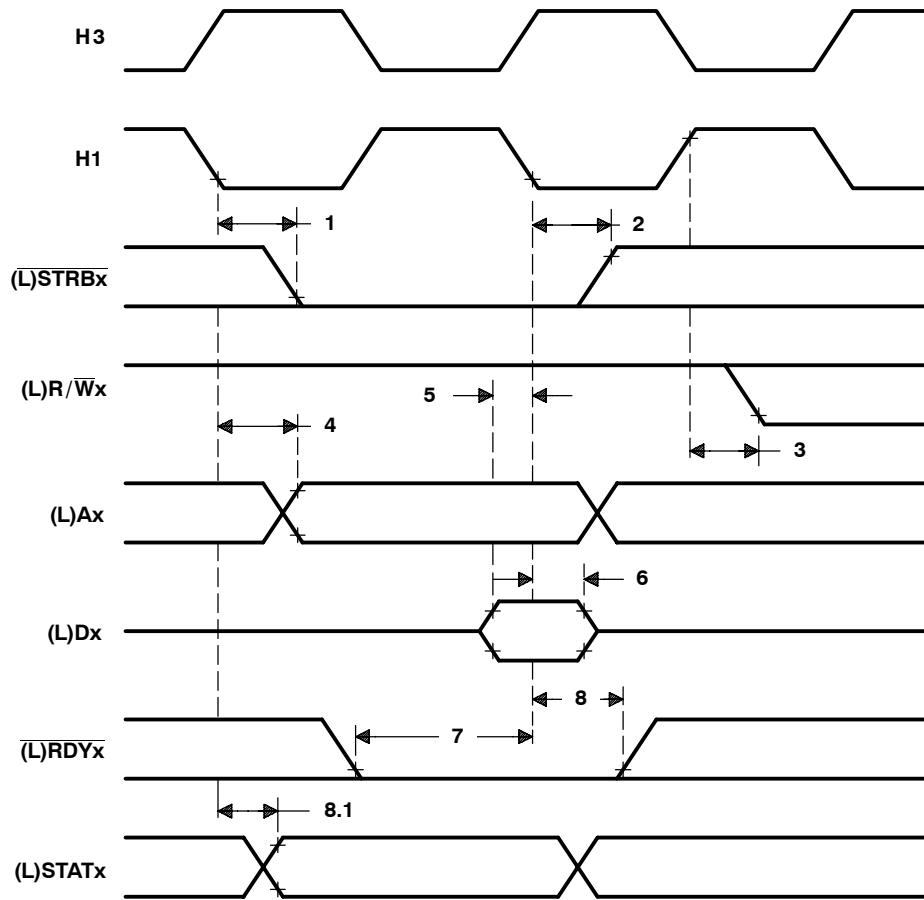


Figure 10. Memory-Read-Cycle Timing [(L)STRBx = 0]

memory-read-cycle and memory-write-cycle timing [(L)STRBx = 0] (continued)

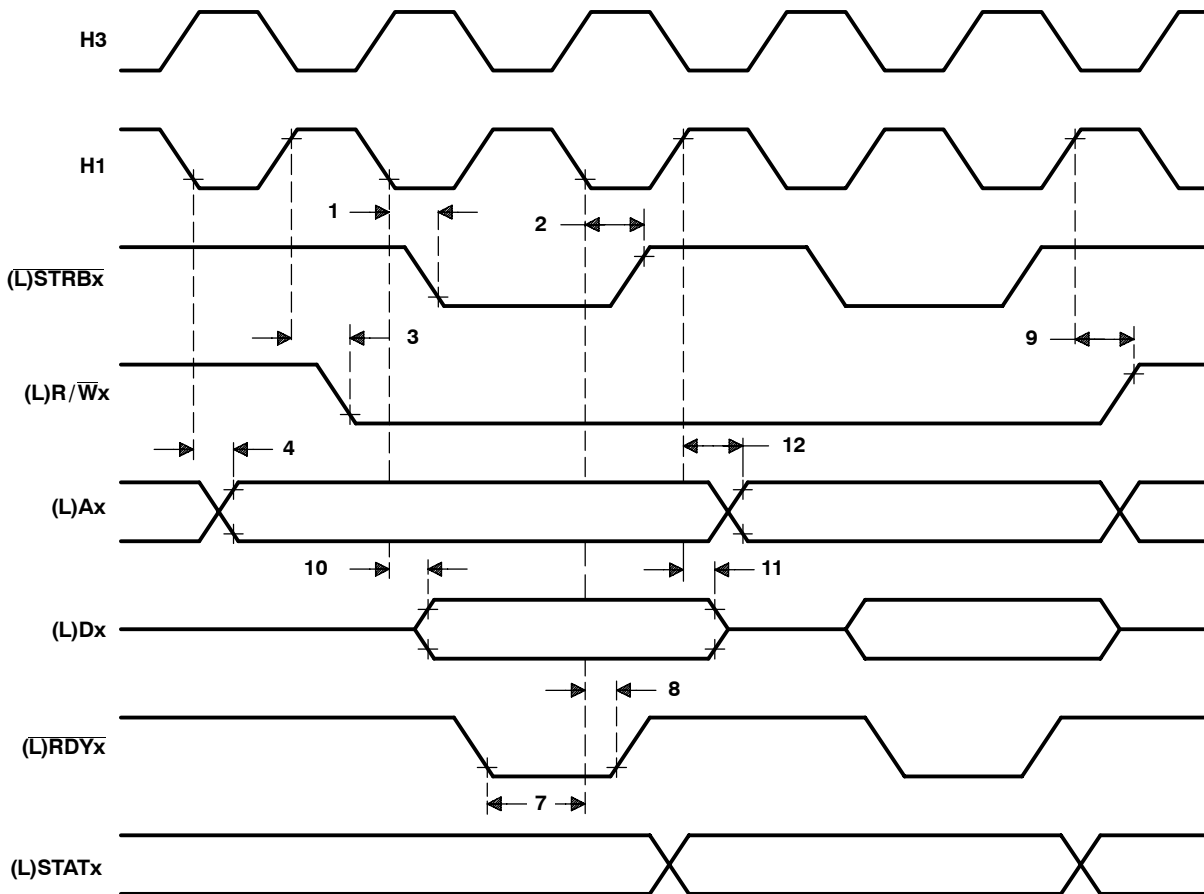


Figure 11. Memory-Write-Cycle Timing [(L)STRBx = 0]

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(L)DE-, (L)AE-, and (L)CEx-enable timing (see Figure 12)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(DEH-DZ)}$	Delay time, (L)DE high to (L)D0 – (L)D31 in the high-impedance state	0	15	0	15	ns
2	$t_{d(DEL-DV)}$	Delay time, (L)DE low to (L)D0 – (L)D31 valid	0	21	0	16	ns
3	$t_{d(AEH-AZ)}$	Delay time, (L)AE high to (L)A0 – (L)A23 in the high-impedance state	0	15	0	15	ns
4	$t_{d(AEL-AV)}$	Delay time, (L)AE low to (L)A0 – (L)A23 valid	0	18	0	16	ns
5	$t_{d(CEH-RWZ)}$	Delay time, (L)CEx high to (L)R/W0, (L)R/W1 in the high-impedance state	0	15	0	15	ns
6	$t_{d(CEL-RWV)}$	Delay time, (L)CEx low to (L)R/W0, (L)R/W1 valid	0	21	0	16	ns
7	$t_{d(CEH-SZ)}$	Delay time, (L)CEx high to (L)STRB0, (L)STRB1 in the high-impedance state	0	15	0	15	ns
8	$t_{d(CEL-SV)}$	Delay time, (L)CEx low to (L)STRB0, (L)STRB1 valid	0 <td 21	0	16	ns	
9	$t_{d(CEH-PAGEZ)}$	Delay time, (L)CEx high to (L)PAGE0, (L)PAGE1 in the high-impedance state	0	15	0	15	ns
10	$t_{d(CEL-PAGEV)}$	Delay time, (L)CEx low to (L)PAGE0, (L)PAGE1 valid	0	21	0	16	ns

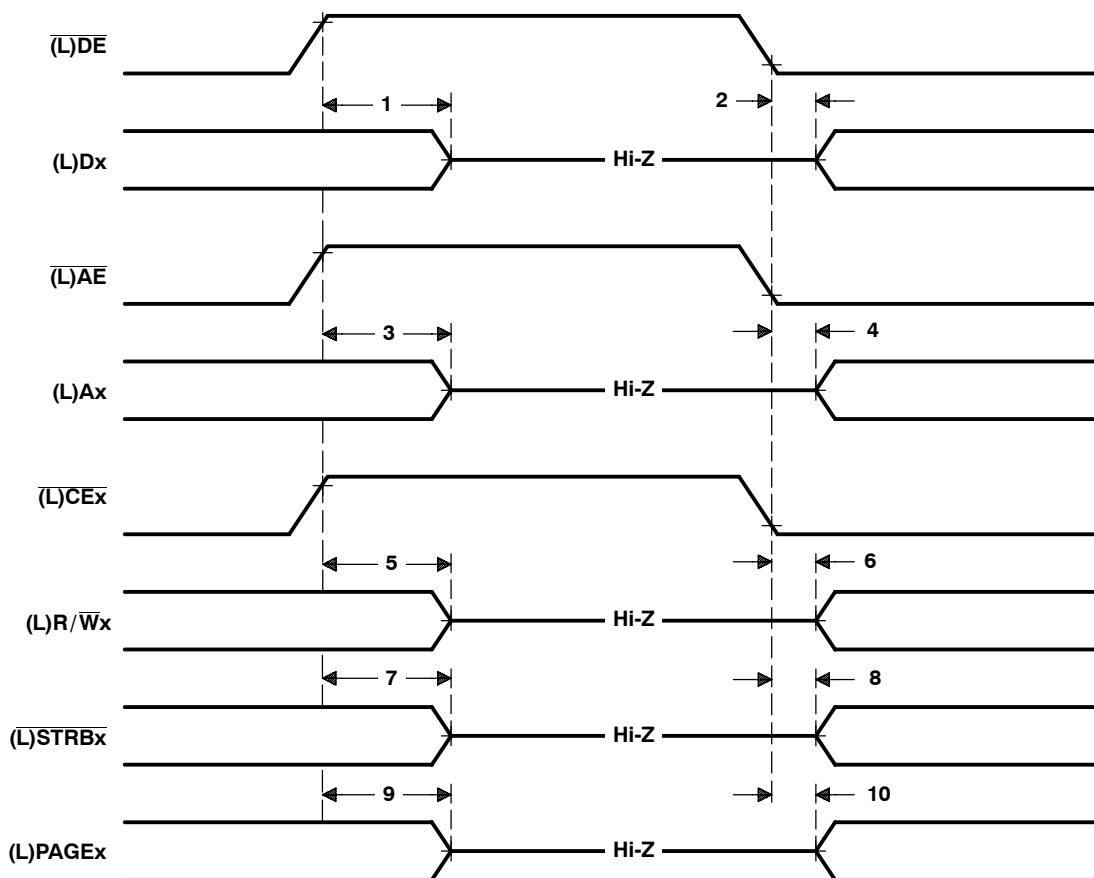


Figure 12. (L)DE-, (L)AE-, and (L)CEx-Enable Timing

timing for $\overline{\text{(L)}}\text{LOCK}$ when executing LDFI or LDII (see Figure 13)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(\text{H1L}-\text{LOCKL})}$ Delay time, H1 low to $\overline{\text{(L)}}\text{LOCK}$ low		8		8	ns

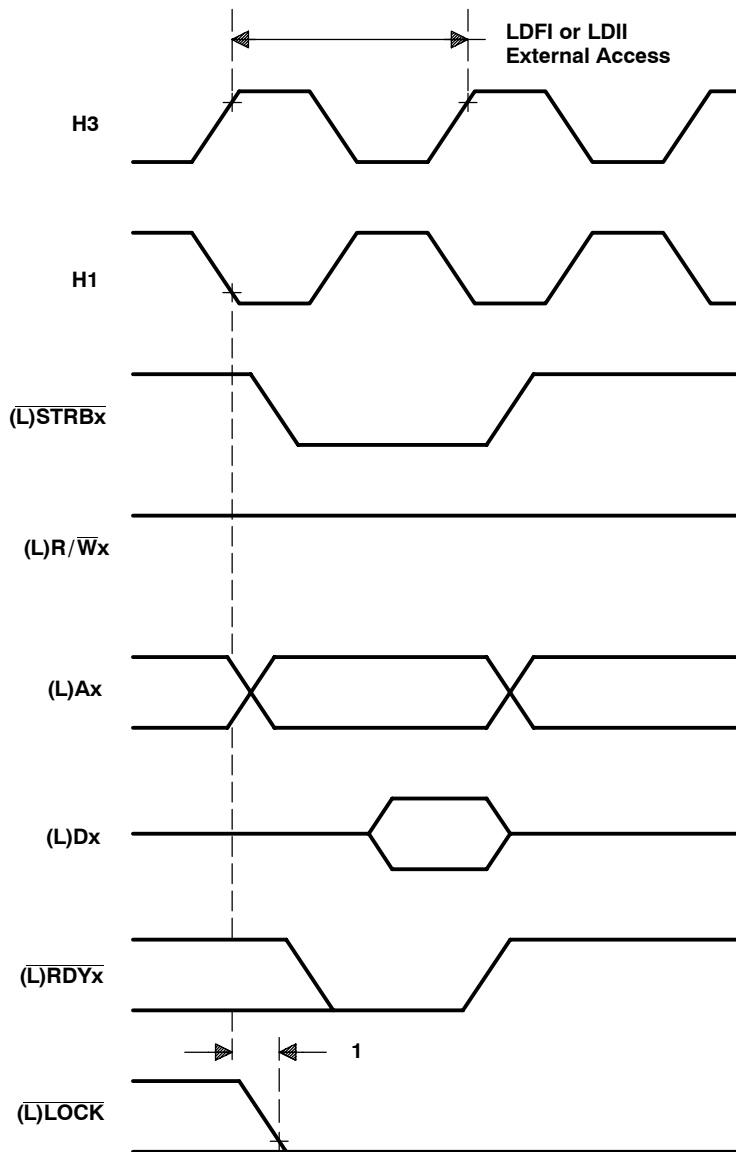


Figure 13. Timing for $\overline{\text{(L)}}\text{LOCK}$ When Executing LDFI or LDII

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timing for $\overline{\text{(L)}}\text{LOCK}$ when executing STFI or STII (see Figure 14)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(\text{H1L}-\text{LOCKH})}$ Delay time, H1 low to $\overline{\text{(L)}}\text{LOCK}$ high		8		8	ns

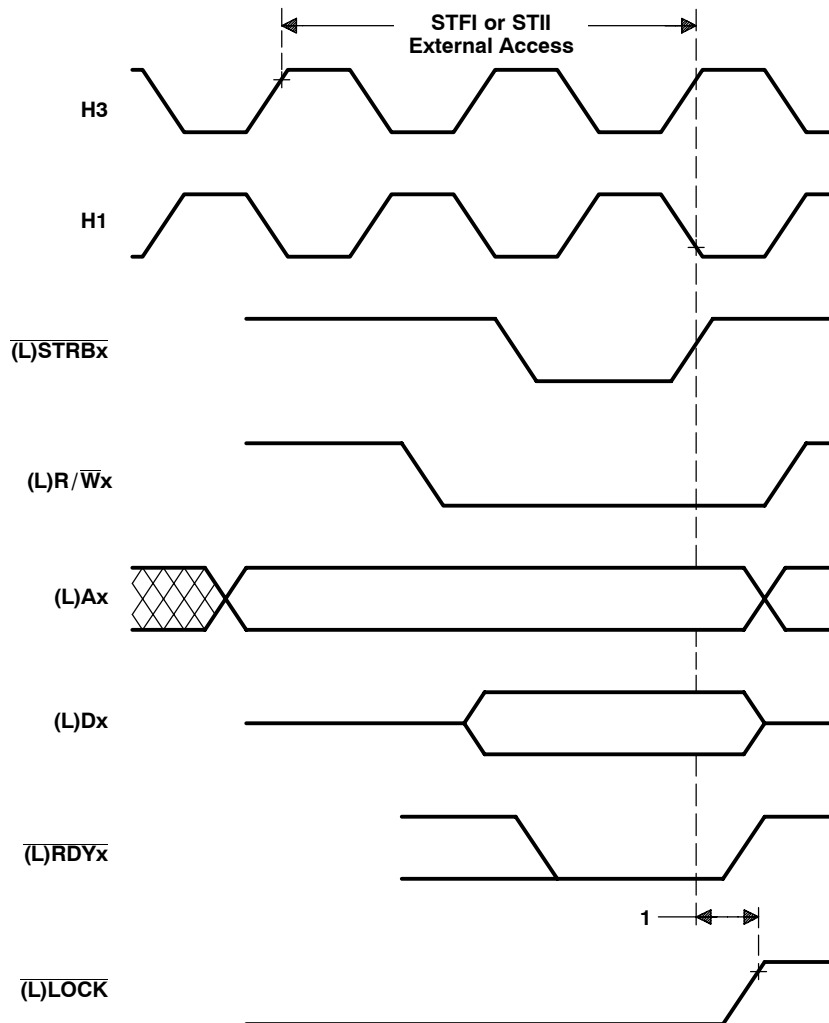


Figure 14. Timing for $\overline{\text{(L)}}\text{LOCK}$ When Executing STFI or STII

timing for $\overline{\text{(L)}}\text{LOCK}$ when executing SIGI (see Figure 15)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(\text{H1L-LOCKL})}$ Delay time, H1 low to $\overline{\text{(L)}}\text{LOCK}$ low		8		8	ns
2	$t_{d(\text{H1L-LOCKH})}$ Delay time, H1 low to $\overline{\text{(L)}}\text{LOCK}$ high		8		8	ns

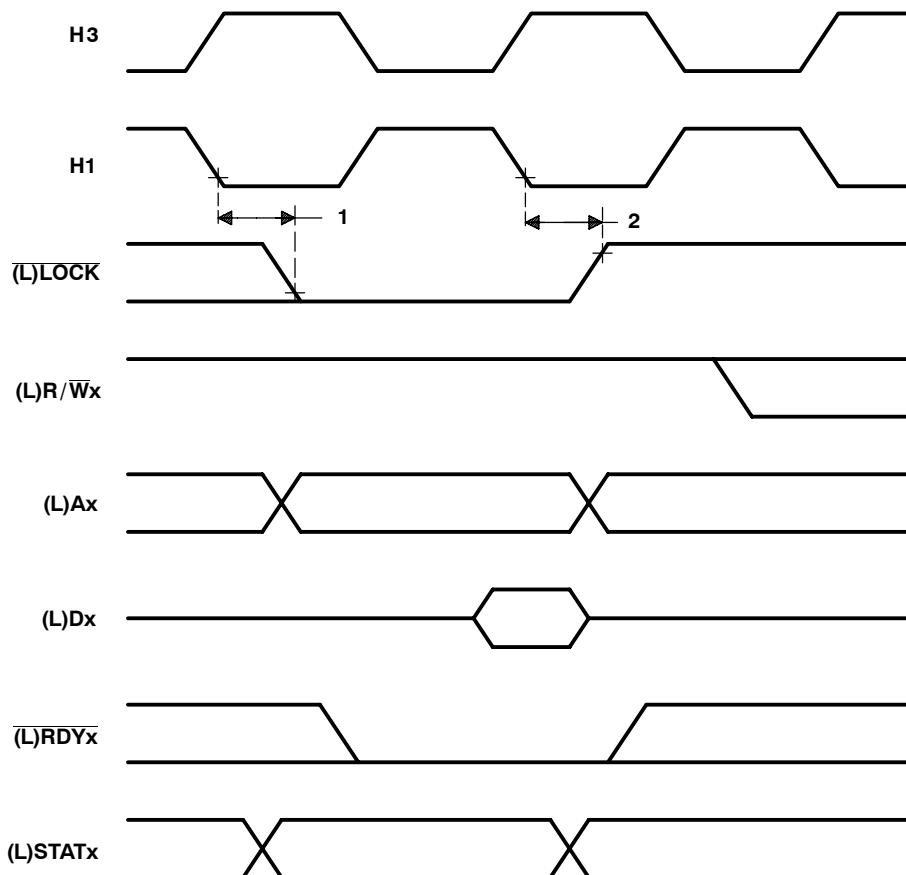


Figure 15. Timing for $\overline{\text{(L)}}\text{LOCK}$ When Executing SIGI

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timing for (L)PAGE0, (L)PAGE1 during memory access to a different page (see Figure 16)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(H1L-PAGEH)}$ Delay time, H1 low to (L)PAGEx high for access to different page	0	9	0	8	ns
2	$t_{d(H1L-PAGEL)}$ Delay time, H1 low to (L)PAGEx low for access to different page	0	9	0	8	ns

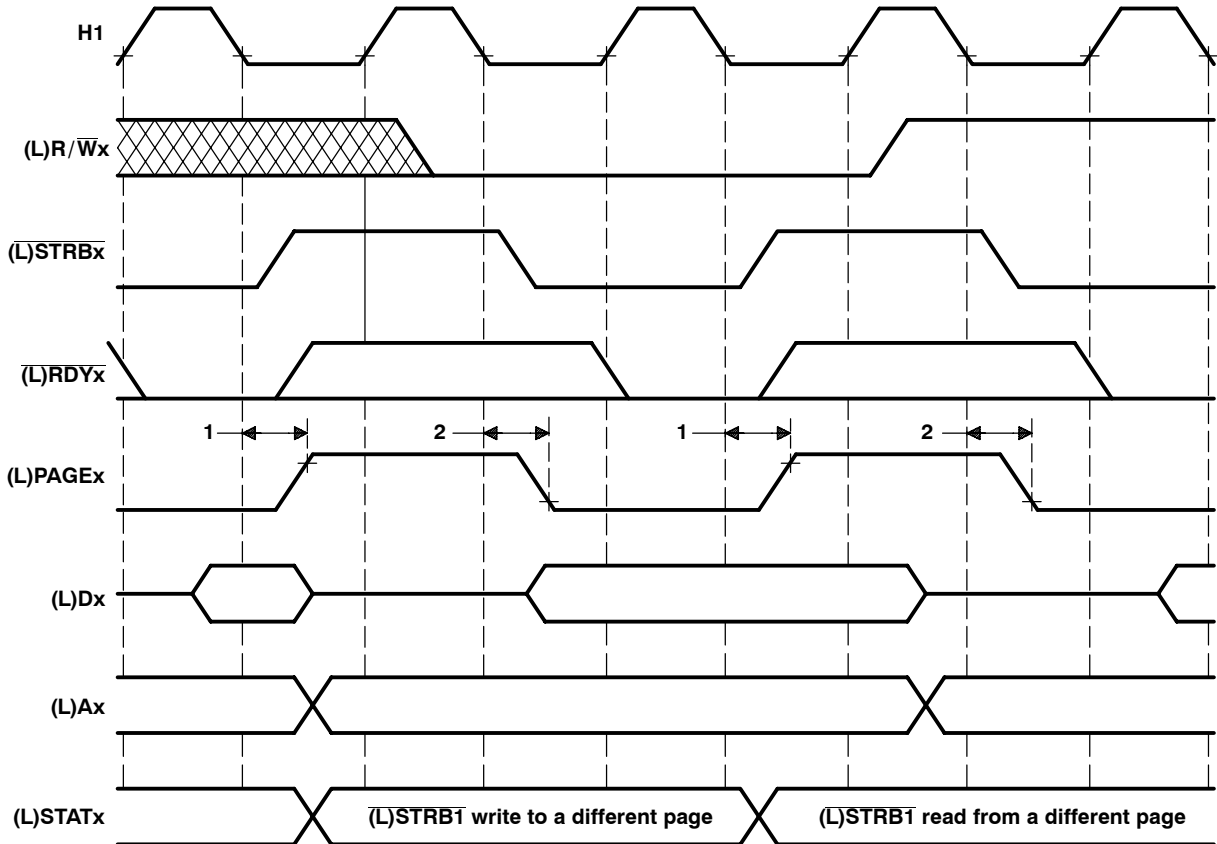


Figure 16. (L)PAGE0, (L)PAGE1 Timing Cycle, Memory Access to a Different Page

timing for the $\overline{\text{IIOF}}_x$ when configured as an output (see Figure 17)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{v(H1L-\text{IIOF})}$ H1 low to $\overline{\text{IIOF}}_x$ valid		14		14	ns

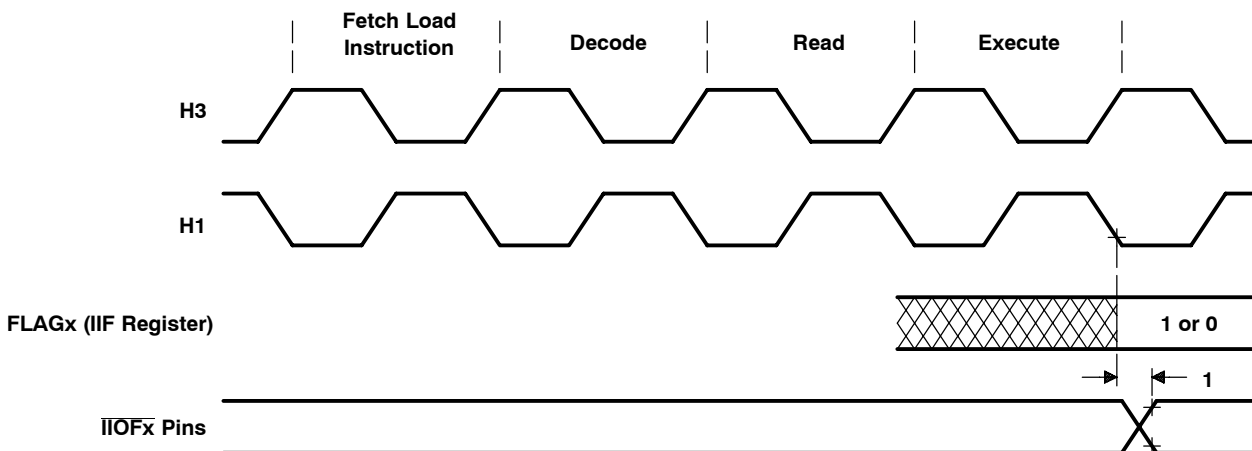


Figure 17. Timing for the $\overline{\text{IIOF}}_x$ When Configured as an Output

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timing of $\overline{\text{IIOF}}_x$ changing from output to input mode (see Figure 18)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{h(H1L-\overline{\text{IIOF}})}$ Hold time, $\overline{\text{IIOF}}_x$ after H1 low		14		14	ns
2	$t_{su(\overline{\text{IIOF}}-H1L)}$ Setup time, $\overline{\text{IIOF}}_x$ before H1 low	11		11		ns
3	$t_{h(H1L-\overline{\text{IIOF}})}$ Hold time, $\overline{\text{IIOF}}_x$ after H1 low	0		0		ns

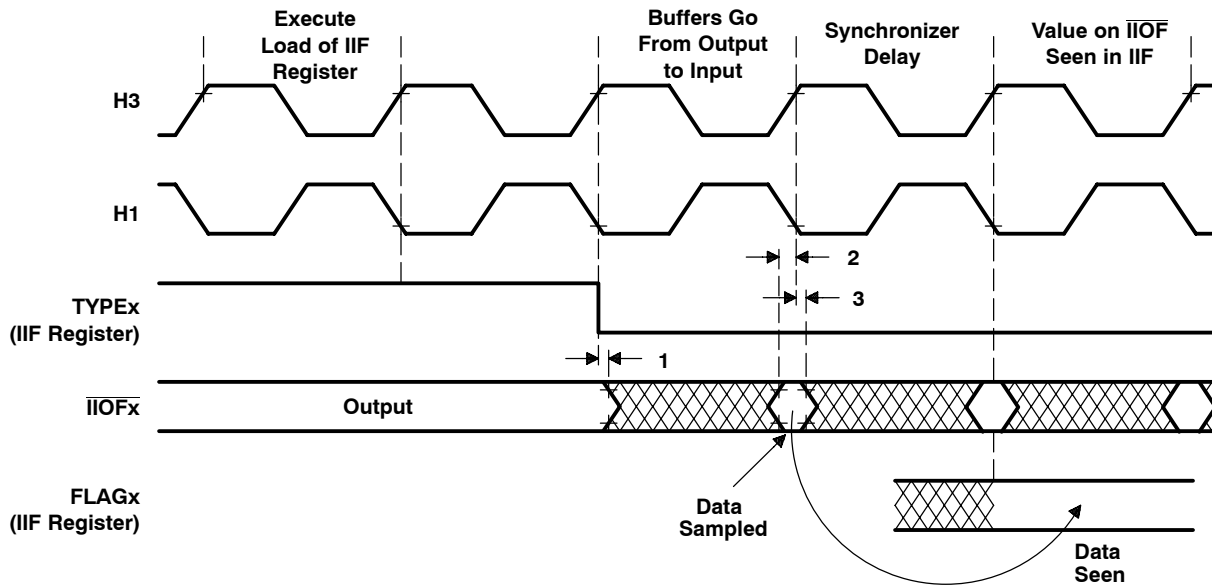


Figure 18. Change of $\overline{\text{IIOF}}_x$ From Output to Input Mode

timing of $\overline{\text{IIOF}}_x$ changing from input to output mode (see Figure 19)

NO.		TMS320C44- 50		TMS320C44- 60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(H1L-IFIO)}$ Delay time, H1 low to $\overline{\text{IIOF}}_x$ switching from input to output		14		14	ns

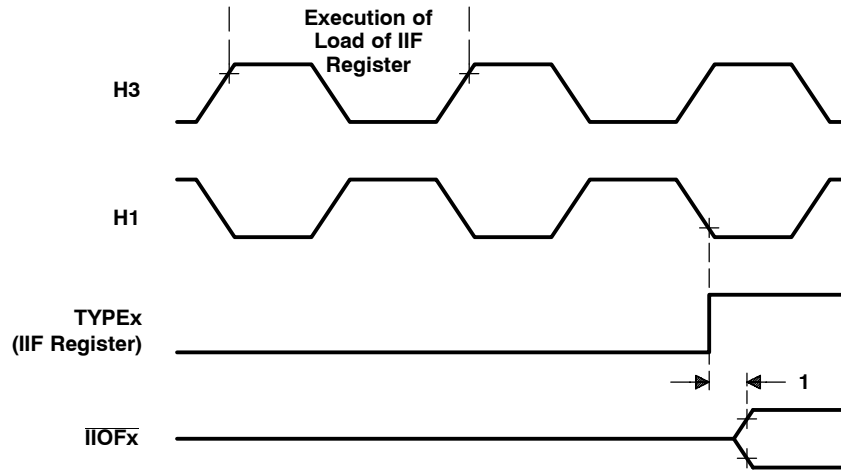
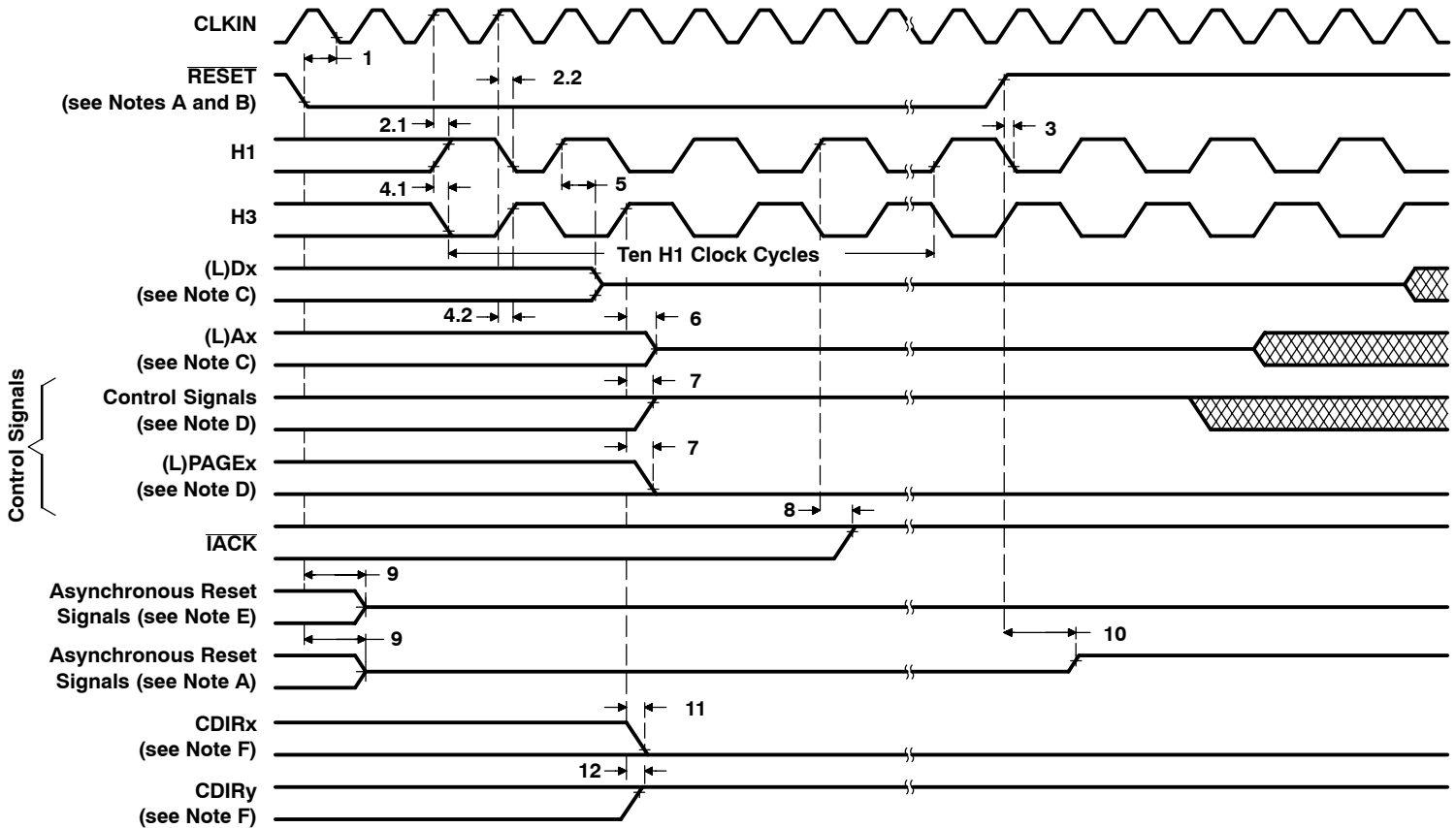


Figure 19. Change of $\overline{\text{IIOF}}_x$ From Input to Output Mode

RESET timing (see Figure 20)

NO.		TMS320C44- 50		TMS320C44- 60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{su}(\overline{\text{RESET}}\text{-C1L})$ Setup time for $\overline{\text{RESET}}$ before CLKIN low	11	$t_{c(CI)}$	11	$t_{c(CI)}$	ns
2.1	$t_{d(CIH-H1H)}$ Delay time, CLKIN high to H1 high	2	10	2	10	ns
2.2	$t_{d(CIH-H1L)}$ Delay time, CLKIN high to H1 low	2	10	2	10	ns
3	$t_{su}(\overline{\text{RESET}}\text{H-H1L})$ Setup time for $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	13		13		ns
4.1	$t_{d(CIH-H3L)}$ Delay time, CLKIN high to H3 low	2	10	2	10	ns
4.2	$t_{d(CIH-H3H)}$ Delay time, CLKIN high to H3 high	2	10	2	10	ns
5	$t_{d(H1H-DZ)}$ Delay time, H1 high to (L)Dx in the high-impedance state		13		13	ns
6	$t_{d(H3H-AZ)}$ Delay time, H3 high to (L)Ax in the high-impedance state		9		9	ns
7	$t_{d(H3H-CONTROLH)}$ Delay time, H3 high to control signals high [low for (L)PAGE]		9		9	ns
8	$t_{d(H1H-IACKH)}$ Delay time, H1 high to $\overline{\text{IACK}}$ high		9		9	ns
9	$t_{d}(\overline{\text{RESET}}\text{L-ASYNCH})$ Delay time, $\overline{\text{RESET}}$ low to asynchronous reset signals in the high-impedance state		21		21	ns
10	$t_{d}(\overline{\text{RESET}}\text{H-COMMH})$ Delay time, $\overline{\text{RESET}}$ high to asynchronous reset signals high		15		15	ns
11	$t_{d}(H1H-CDIRL)$ Delay time,		9		9	ns
12	$t_{d}(H1H-CDIRH)$ Delay time,		9		9	ns



- NOTES: A. Asynchronous reset signals that go to a high logic level after $\overline{\text{RESET}}$ returns to a high state include $\overline{\text{CREQy}}$, $\overline{\text{CACKx}}$, $\overline{\text{CSTRBx}}$, and $\overline{\text{CRDYy}}$ (where x = 1 or 2 and y = 4 or 5).
- B. $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.
- C. For this diagram, (L)Dx includes D31 - D0, LD31 - LD0, and CxD7 - CxD0; (L)Ax includes LA(23 - 0) and A(23 - 0).
- D. Control signals $\overline{\text{LSTRB0}}$, $\overline{\text{LSTRB1}}$, $\overline{\text{STRB0}}$, $\overline{\text{STRB1}}$, $\overline{\text{(L)STAT3-(L)STAT0}}$, $\overline{\text{(L)LOCK}}$, $\overline{\text{(L)R/W0}}$, and $\overline{\text{(L)R/W1}}$ go high while (L)PAGE0 and (L)PAGE1 go low.
- E. Asynchronous reset signals that go into the high-impedance state after RESET goes low include $\overline{\text{TCLK0}}$, $\overline{\text{TCLK1}}$, $\overline{\text{IIOF3-IIOF0}}$, and the communication-port control signals $\overline{\text{CREQx}}$, $\overline{\text{CACKy}}$, $\overline{\text{CSTRBy}}$, and $\overline{\text{CRDYx}}$ (where x = 1 or 2, and y = 4 or 5). At reset, ports 1 and 2 become outputs, and ports 4 and 5 become inputs.
- F. x = 1 or 2 and y = 4 or 5

Figure 20. RESET Timing

timing for $\overline{\text{IIOF}}_x$ interrupt response [$P = t_{c(H)}$] (see Notes 9 and 10 and Figure 21)

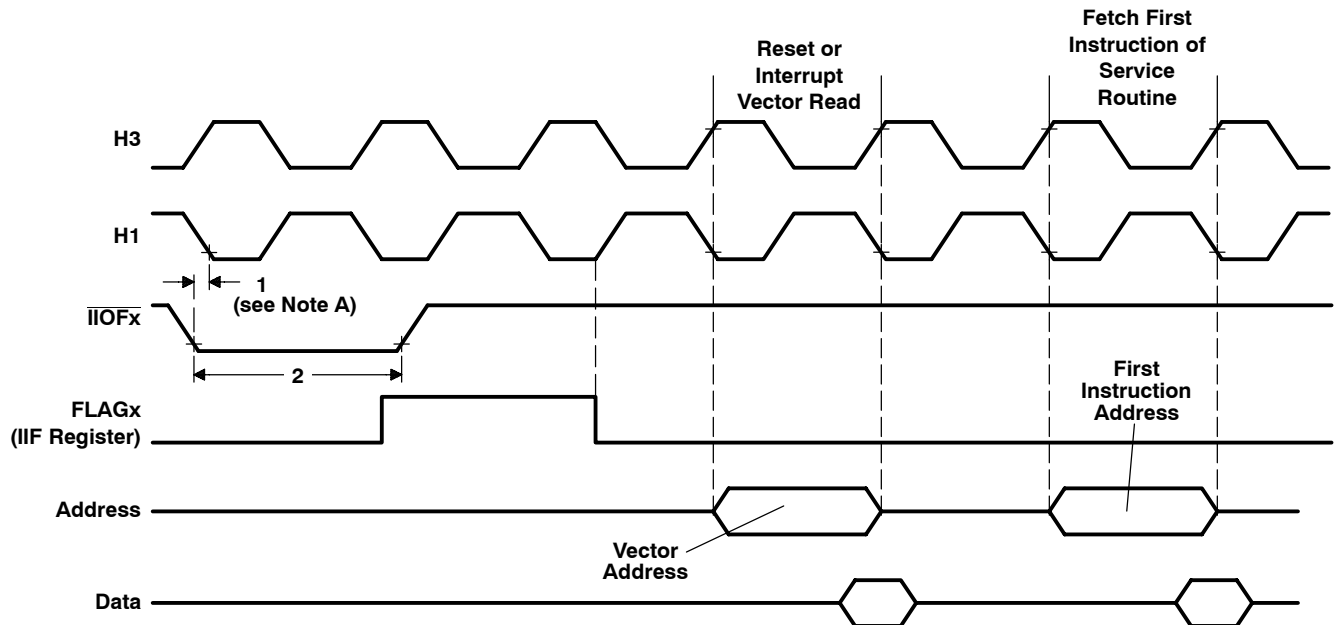
NO.		TMS320C44-50			TMS320C44-60			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
1	$t_{su}(\overline{\text{IIOF}}\text{-H1L})$ Setup time, $\overline{\text{IIOF}}_x$ before H1 low	11 [†]			11 [†]			ns
2	$t_w(\text{INT})$ Pulse duration, to assure one interrupt seen (see Note 11)	P	1.5 P	2 P	P	1.5 P	2 P	ns

[†] If this timing is not met, the interrupt is recognized in the next cycle.

NOTES: 9. $\overline{\text{IIOF}}_x$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.

10. Edge-triggered interrupts require a setup of time (1) and a minimum duration of P. No maximum duration limit exists.

11. Level-triggered interrupts require interrupt-pulse duration of at least 1 P wide (P = one H1 period) to ensure it will be seen. It must be \leq to 2 P wide to ensure it will be responded to only once. Recommended pulse duration is 1.5 P.



NOTE A: The C44 can accept an interrupt from the same source every two H1 clock cycles.

Figure 21. $\overline{\text{IIOF}}_x$ Interrupt-Response Timing [$P = t_{c(H)}$]

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timing for $\overline{\text{IACK}}$ (see Note 12 and Figure 22)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(H1L-IACKL)}$ Delay time, H1 low to $\overline{\text{IACK}}$ low		9		7	ns
2	$t_{d(H1L-IACKH)}$ Delay time, H1 low to $\overline{\text{IACK}}$ high during first cycle of IACK instruction data read		9		7	ns

NOTE 12: The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is, therefore, extended if the bus cycle utilizes wait states.

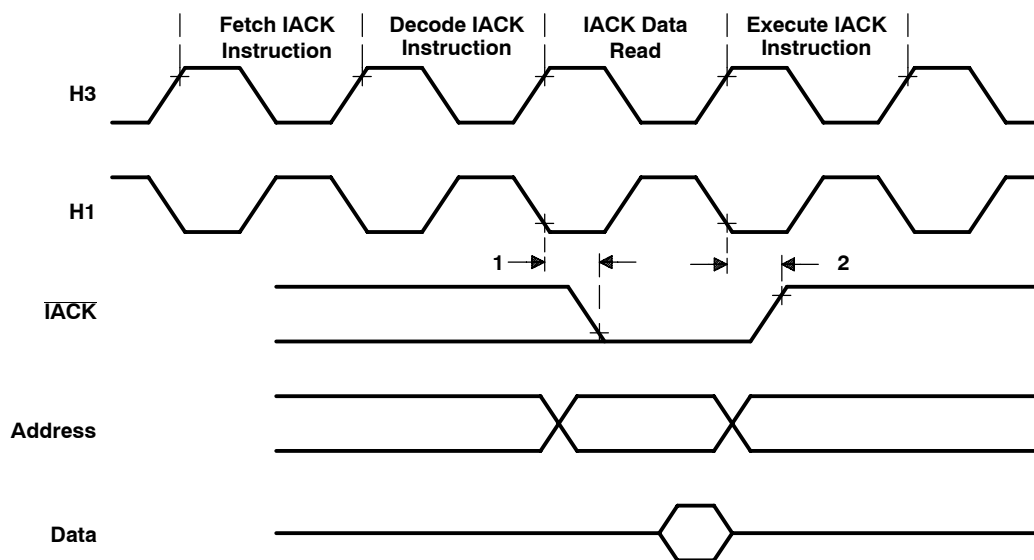


Figure 22. $\overline{\text{IACK}}$ Timing

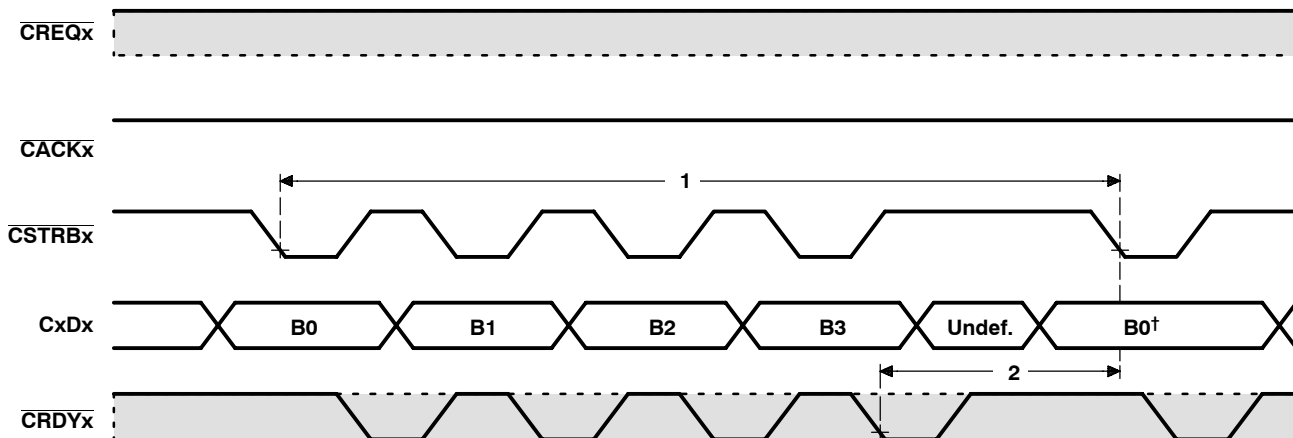
communication-port word-transfer-cycle timing[†] [P = t_{c(H)}] (see Note 13 and Figure 23)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	t _{c(WORD)} [‡] Cycle time, word transfer (4 bytes = 1 word)	1.5 P + 7	2.5 P + 170	1.5 P + 7	2.5 P + 170	ns
2	t _{d(CRDYL-CSL)W} Delay time, CRDYx low to CSTRBx low between back-to-back write cycles	1.5 P + 7	2.5 P + 28	1.5 P + 7	2.5 P + 28	ns

[†] For these timing values, it is assumed that the C4x receiving data is ready to receive data. Line propagation delay is not considered.

[‡] t_{c(WORD)} max = 2.5 P + 28 ns + the maximum summed values of 4 × t_{d(CSL-CRDYL)R}, 3 × t_{d(CRDYL-CSH)}, 3 × t_{d(CSH-CRDYH)R}, and 3 × t_{d(CRDYH-CSL)W} as seen in Figure 24. This timing assumes two C4xs are connected.

NOTE 13: These timings apply only to two communicating C4xs. When a non-C4x device communicates with a C44, timings can be longer. No restriction exists in this case on how slow the transfer could be except when using early silicon (C40 PG 1.x or 2.x). Refer to the CSTRB width restriction section of the *TMS320C4x User's Guide* (literature number SPRU063).



 = When signal is an input (clear = when signal is an output).

[†] Begins byte 0 of the next word.

NOTE A: For correct operation during token exchange, the two communicating C4xs must have CLKIN frequencies within a factor of 2 of each other (in other words, at most, one of the C4xs can be twice as fast as the other).

Figure 23. Communication-Port Word-Transfer-Cycle Timing [P = t_{c(H)}]

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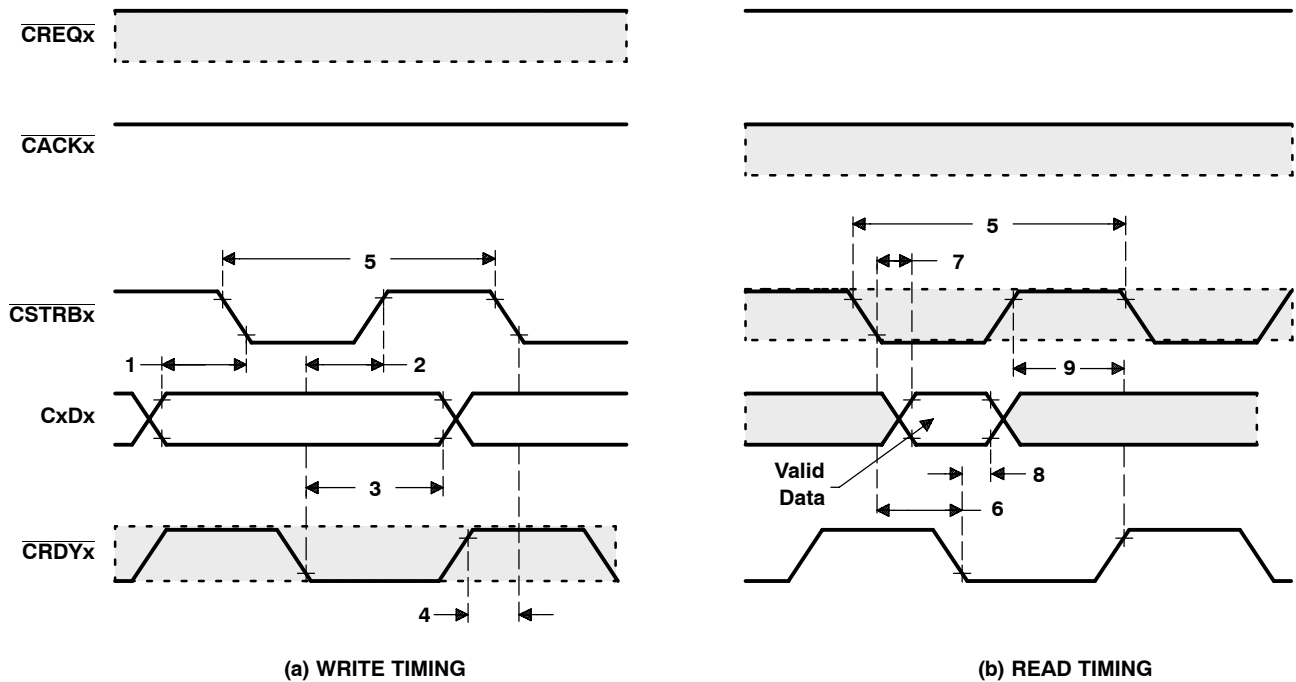
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communication-port byte-cycle timing (write and read) (see Note 14 and Figure 24)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{su(CD-CSL)W}$ Setup time, CxDx valid before \overline{CSTRBx} low (write)	2		2		ns
2	$t_{d(CRDYL-CSH)W}$ Delay time, \overline{CRDYx} low to \overline{CSTRBx} high (write)	0	12	0	12	ns
3	$t_{h(CRDYL-CD)W}$ Hold time, CxDx after \overline{CRDYx} low (write)	2		2		ns
4	$t_{d(CRDYH-CSL)W}$ Delay time, \overline{CRDYx} high to \overline{CSTRBx} low for subsequent bytes (write)	0	12	0	12	ns
5	$t_{c(BYTE)}^\dagger$ Cycle time, byte transfer		44		44	ns
6	$t_{d(CSL-CRDYL)R}$ Delay time, \overline{CSTRBx} low to \overline{CRDYx} low (read)	0	10	0	10	ns
7	$t_{su(CSL-CD)R}$ Setup time, CxDx valid after \overline{CSTRBx} low (read)	0		0		ns
8	$t_{h(CRDYL-CD)R}$ Hold time, CxDx valid after \overline{CRDYx} low (read)	2		2		ns
9	$t_{d(CSH-CRDYH)R}$ Delay time, \overline{CSTRBx} high to \overline{CRDYx} high (read)	0	10	0	10	ns

$^\dagger t_{c(BYTE)} \text{ max} = \text{summed maximum values of } t_{d(CRDY-CSH)}, t_{d(CSL-CRDYL)R}, t_{d(CSH-CRDYH)R}, \text{ and } t_{d(CRDYH-CSL)W}. \text{ This assumes two C4xs are connected.}$

NOTE 14: Communication port timing does not include line length delay.




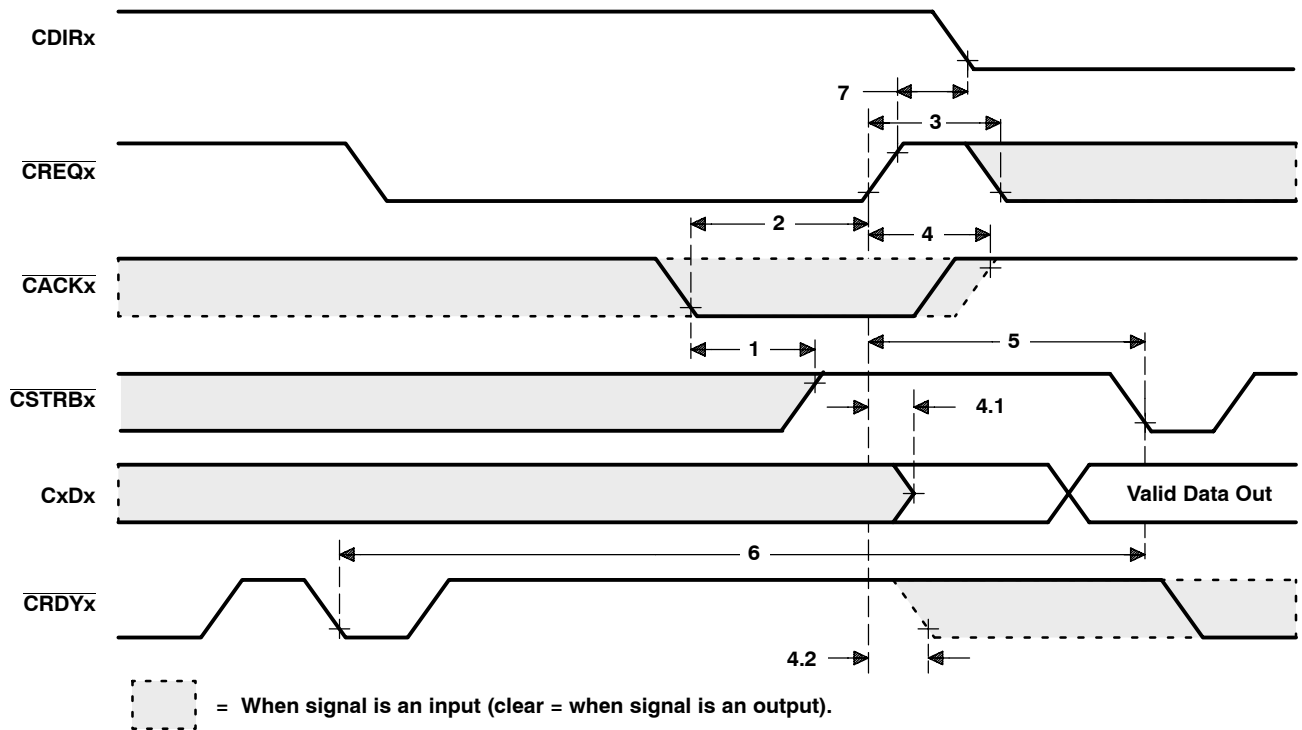
 = When signal is an input (clear = when signal is an output).

Figure 24. Communication-Port Byte-Cycle Timing (Write and Read)

timing for communication-token transfer sequence, input to an output port [$P = t_{c(H)}$]
(see Figure 25)

NO.		MIN	MAX	UNIT
1	$t_{d(CAL-CS)}^{\dagger}$ Delay time, \overline{CACKx} low to \overline{CSTRBx} change from input to a high-level output	$0.5 P + 6$	$1.5 P + 22$	ns
2	$t_{d(CAL-CRQH)}^{\dagger}$ Delay time, \overline{CACKx} low to start of \overline{CREQx} going high for token-request acknowledge	$P + 5$	$2 P + 22$	ns
3	$t_{d(CRQH-CRQ)}^{\dagger}$ Delay time, start of \overline{CREQx} going high to \overline{CREQx} change from output to an input	$0.5 P - 5$	$0.5 P + 13$	ns
4	$t_{d(CRQH-CA)}^{\dagger}$ Delay time, start of \overline{CREQx} going high to \overline{CACKx} change from an input- to an output-level high	$0.5 P - 5$	$0.5 P + 13$	ns
4.1	$t_{d(CRQH-CD)}^{\dagger}$ Delay time, start of \overline{CREQx} going high to $CxDx$ change from input-driven to output-driven	$0.5 P - 5$	$0.5 P + 13$	ns
4.2	$t_{d(CRQH-CRDY)}^{\dagger}$ Delay time, start of \overline{CREQx} going high to \overline{CRDYx} change from an output to an input	$0.5 P - 5$	$0.5 P + 13$	ns
5	$t_{d(CRQH-CSL)}^{\dagger}$ Delay time, start of \overline{CREQx} going high to \overline{CSTRBx} low for start of word-transfer out	$1.5 P - 8$	$1.5 P + 9$	ns
6	$t_{d(CRDYL-CSL)}^{\dagger}$ Delay time, \overline{CRDYx} low at end of word-input to \overline{CSTRBx} low for word-output	$3.5 P + 12$	$5.5 P + 48$	ns
7	$t_{d(CRQH-CDIRL)}$ Delay time, \overline{CREQx} high to $CDIRx$ low, change from input to output	$0.5 P - 5$	$0.5 P + 13$	ns

[†] These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.



NOTE A: Before the token exchange, \overline{CREQx} and \overline{CRDYx} are output signals asserted by the C44 receiving data. \overline{CACKx} , \overline{CSTRBx} , and $CxD7 - CxD0$ are input signals asserted by the device sending data to the C44; these are asynchronous with respect to the H1 clock of the receiving C44. After token exchange, \overline{CACKx} , \overline{CSTRBx} , and $CxD7 - CxD0$ become output signals, and \overline{CREQx} and \overline{CRDYx} become inputs.

Figure 25. Communication-Token Transfer Sequence, Input to an Output Port [$P = t_{c(H)}$]

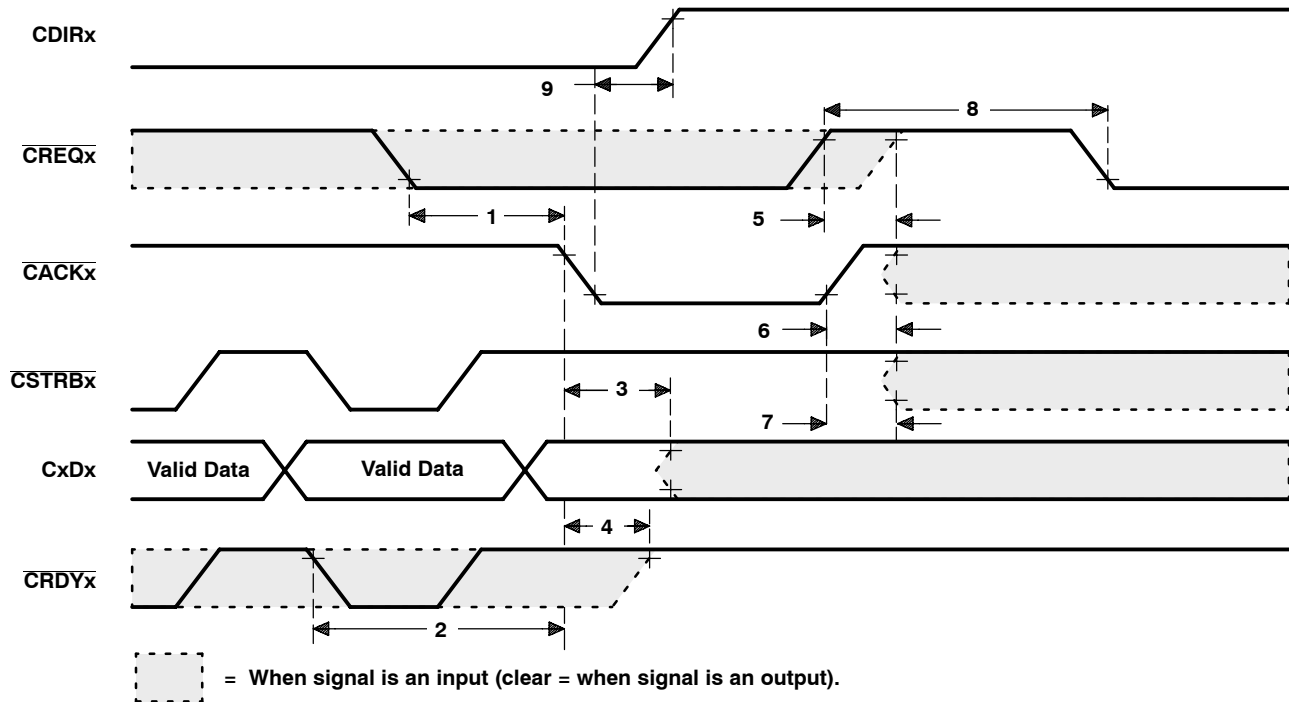
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timing for communication-token transfer sequence, output to an input port [$P = t_{c(H)}$] (see Figure 26)

NO.		MIN	MAX	UNIT
1	$t_{d(CRQL-CAL)T}^{\dagger}$	Delay time, \overline{CREQx} low to start of \overline{CACKx} going low for token-request-acknowledge		ns
2	$t_{d(CRDYL-CAL)T}^{\dagger}$	Delay time, \overline{CRDYx} low at end of word-transfer out to start of \overline{CACKx} going low		ns
3	$t_{d(CAL-CDI)}$	Delay time, start of \overline{CACKx} going low to $CxDx$ change from outputs to inputs		ns
4	$t_{d(CAL-CRDY)T}$	Delay time, start of \overline{CACKx} going low to \overline{CRDYx} change from an input to output, high level		ns
5	$t_{d(CRQH-CRQ)T}^{\dagger}$	Delay time, \overline{CREQx} high to \overline{CREQx} change from an input to output, high level		ns
6	$t_{d(CRQH-CA)T}^{\dagger}$	Delay time, \overline{CREQx} high to \overline{CACKx} change from output to an input		ns
7	$t_{d(CRQH-CS)T}^{\dagger}$	Delay time, \overline{CREQx} high to \overline{CSTRBx} change from output to an input		ns
8	$t_{d(CRQH-CRQL)T}^{\dagger}$	Delay time, \overline{CREQx} high to \overline{CREQx} low for the next token-request		ns
9	$t_{d(CAL-CDIRH)}$	Delay time, \overline{CACKx} low to $CDIRx$ high, change from output to input		ns

[†] These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.



NOTE A: Before the token exchange, \overline{CACKx} , \overline{CSTRBx} , and $CxD7 - CxD0$ are asserted by the C44 sending data. \overline{CREQx} and \overline{CRDYx} are input signals asserted by the C44 receiving data and are asynchronous with respect to the H1 clock of the sending C44. After token exchange, \overline{CREQx} and \overline{CRDYx} become outputs, and \overline{CSTRBx} , \overline{CACKx} , and $CxD7 - CxD0$ become inputs.

Figure 26. Communication-Token Transfer Sequence, Output to an Input Port [$P = t_{c(H)}$]

timer-pin timing (see Note 15 and Figure 27)

NO.		MIN	MAX	UNIT
1	$t_{su}(TCLK-H1L)$ Setup time, TCLKx before H1 low	10		ns
2	$t_h(H1L-TCLK)$ Hold time, TCLKx after H1 low	0		ns
3	$t_d(H1H-TCLK)$ Delay time, TCLKx valid after H1 high		13	ns

NOTE 15: Period and polarity are specified by contents of internal control registers.

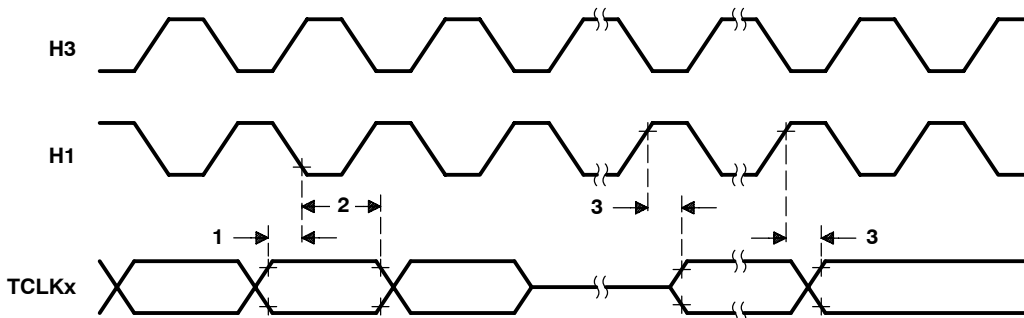


Figure 27. Timer-Pin Timing Cycle

timing for IEEE-1149.1 test access port (see Figure 28)

NO.		TMS320C44 - 50		TMS320C44 - 60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{su}(TMS-TCKH)$ Setup time, TMS/TDI to TCK high	10		10		ns
2	$t_h(TCKH-TMS)$ Hold time, TMS/TDI from TCK high	5		5		ns
3	$t_d(TCKL-TDOV)$ Delay time, TCK low to TDO valid	0	15	0	12	ns

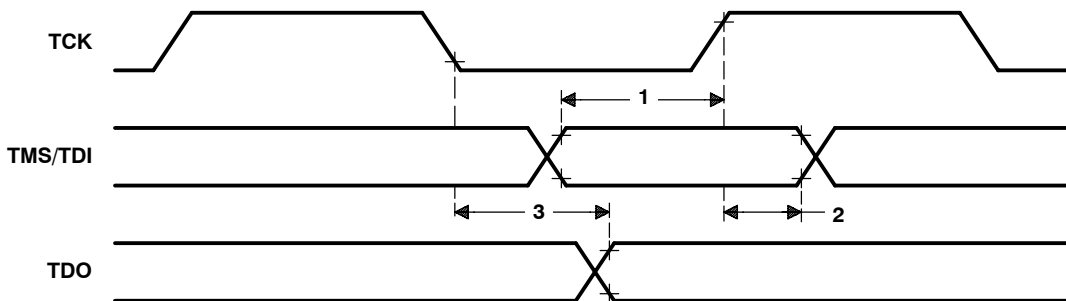


Figure 28. IEEE-1149.1 Test Access Port Timings

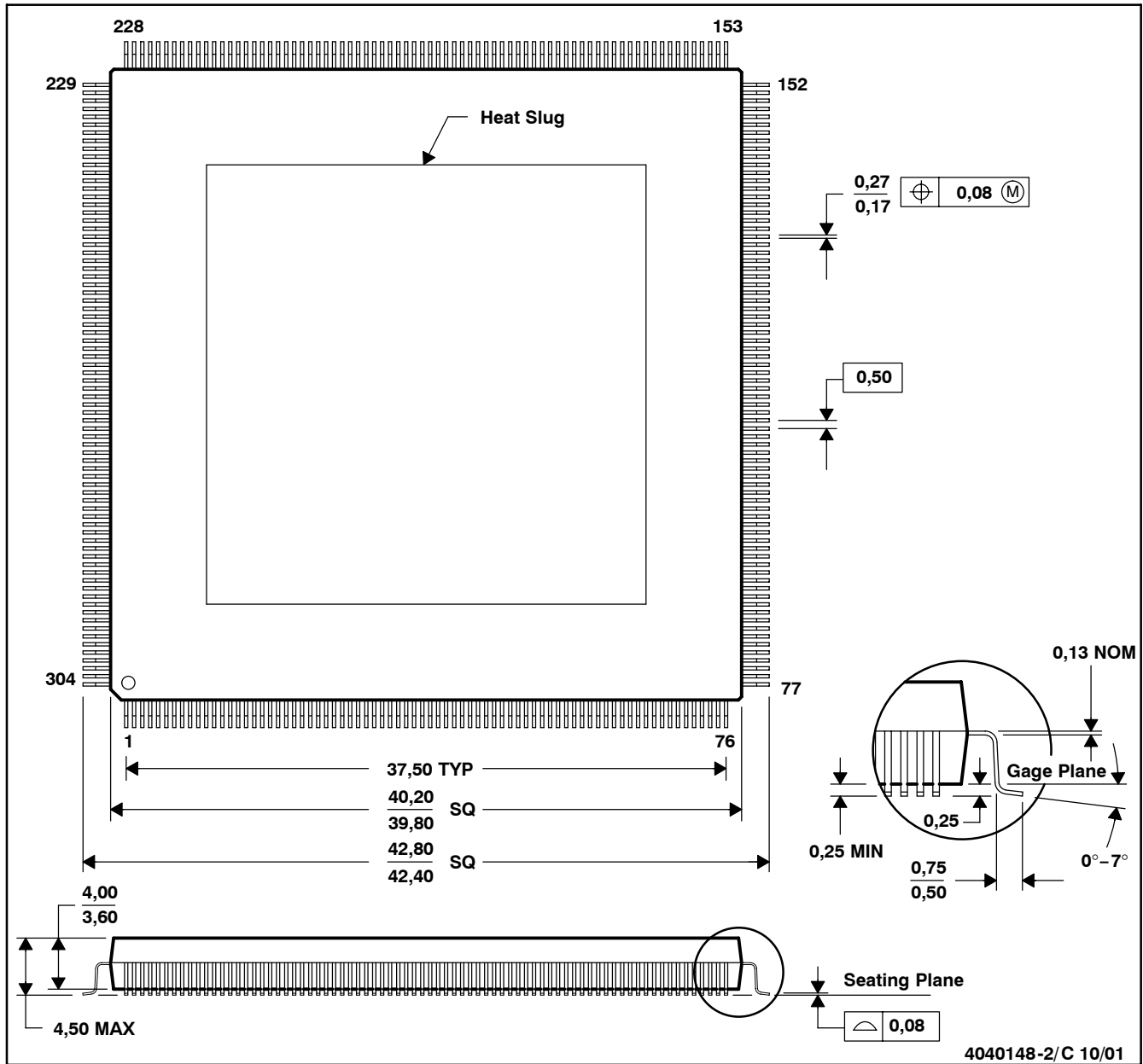
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MECHANICAL DATA

PDB (S-PQFP-G304)

PLASTIC QUAD FLATPACK (DIE DOWN)



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Thermally enhanced molded plastic package with a heat slug (HSL)
 D. Falls within JEDEC MO-143

Thermal Resistance Characteristics

Parameter	°C/W	Air Flow LFPM
$R_{\theta JC}$	0.8	N/A
$R_{\theta JA}$	16	0
$R_{\theta JA}$	14.2	150
$R_{\theta JA}$	12.1	250
$R_{\theta JA}$	10	500

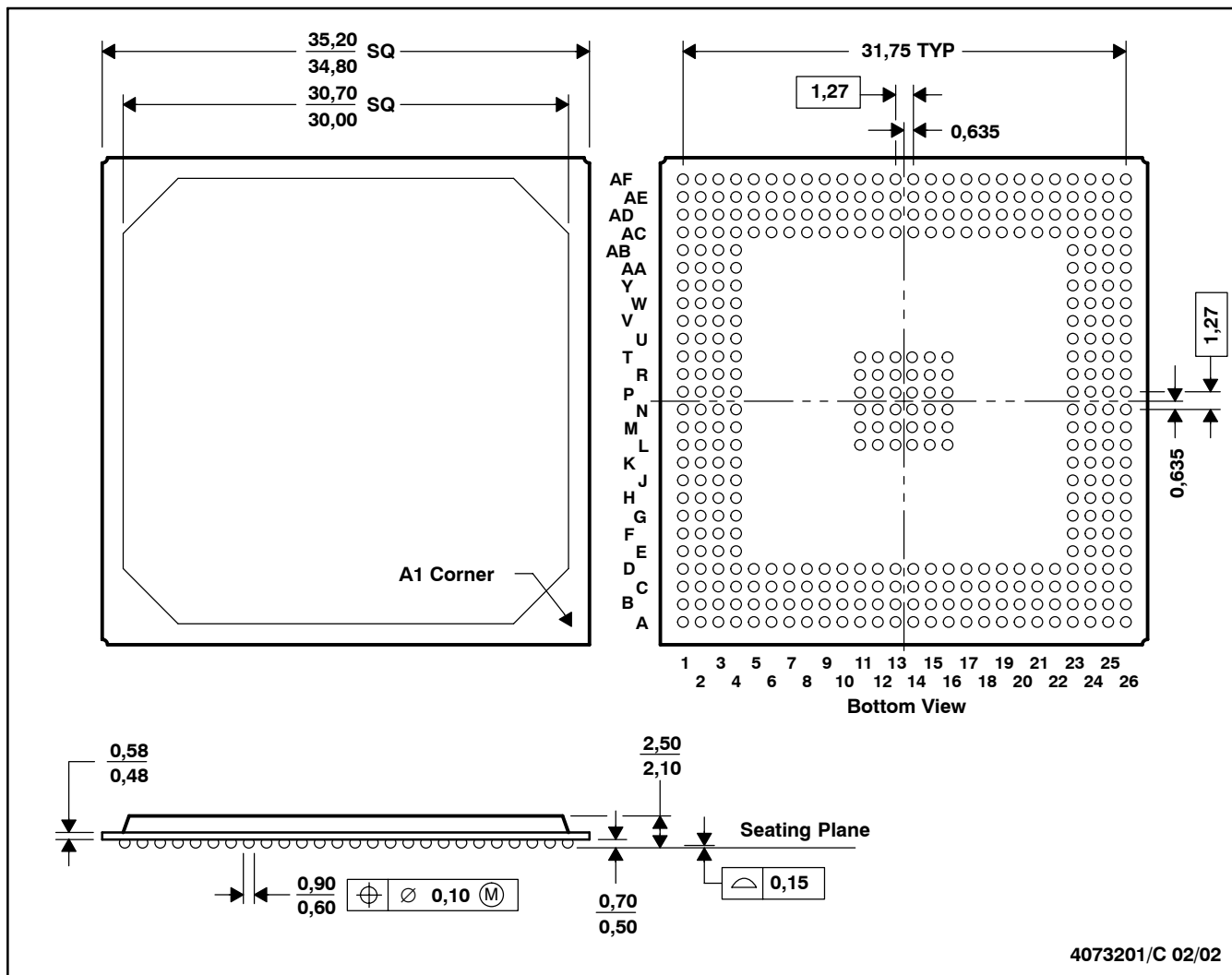


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MECHANICAL DATA

GFW (S-PBGA-N388)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MO-151

Thermal Resistance Characteristics

Parameter	°C/W	Air Flow LFPM
R θ JC	3.7	N/A
R θ JA	18.5	0
R θ JA	16.1	150
R θ JA	15	250
R θ JA	13.4	500

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320C44GFW50	NRND	BGA	GFW	388		TBD	Call TI	Call TI		TMS320C44GFW @ 1990 TI 50	
TMS320C44GFW60	NRND	BGA	GFW	388		TBD	Call TI	Call TI		TMS320C44GFW @ 1990 TI 60	
TMS320C44GFWA	NRND	BGA	GFW	388		TBD	Call TI	Level-4-220C-72 HR		TMS320C44GFW @ 1990 TI A	
TMS320C44PDB50	NRND	HQFP	PDB	304		TBD	Call TI	Call TI		TMS320C44PDB50 @ 1990 TI 50	
TMS320C44PDB60	NRND	HQFP	PDB	304		TBD	Call TI	Call TI		TMS320C44PDB60 @ 1990 TI 60	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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