



**THE DATASHEET OF  
THS3111CDGNR**



# LOW-NOISE, HIGH-VOLTAGE, CURRENT-FEEDBACK OPERATIONAL AMPLIFIERS

 Check for Samples: [THS3110](#) [THS3111](#)

## FEATURES

- **Low Noise**
  - **2-pA/√Hz Noninverting Current Noise**
  - **10-pA/√Hz Inverting Current Noise**
  - **3-nV/√Hz Voltage Noise**
- **High Output Current Drive: 260 mA**
- **High Slew Rate: 1300 V/μs**
  - ( $R_L = 100 \Omega$ ,  $V_O = 8 V_{PP}$ )
- **Wide Bandwidth: 90 MHz ( $G = 2$ ,  $R_L = 100 \Omega$ )**
- **Wide Supply Range: ±5 V to ±15 V**
- **Power-Down Feature: (THS3110 Only)**

## APPLICATIONS

- **Video Distribution**
- **Power FET Driver**
- **Pin Driver**
- **Capacitive Load Driver**

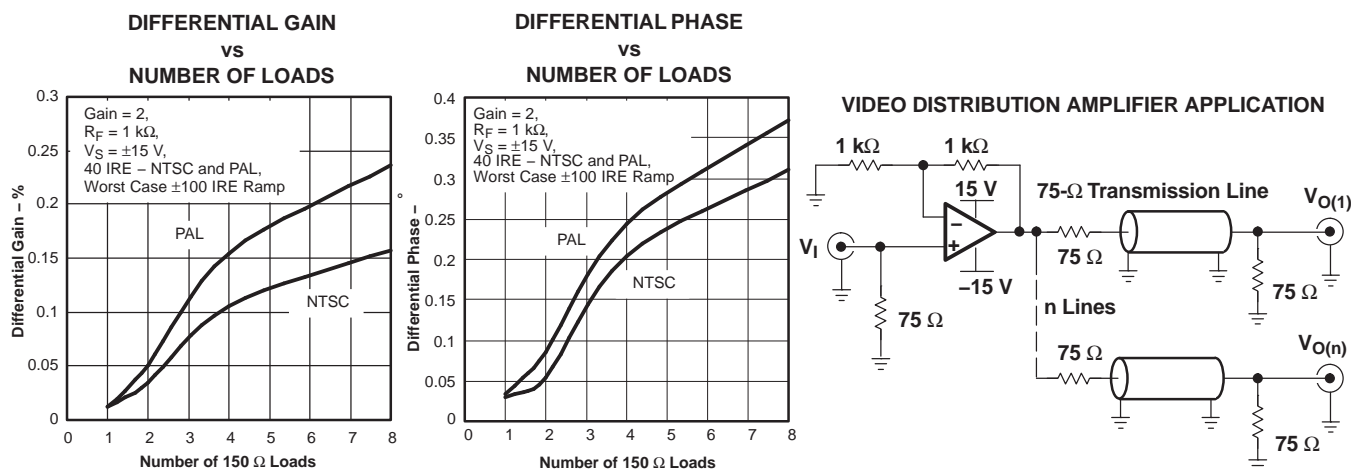
## DESCRIPTION

The THS3110 and THS3111 are low-noise, high-voltage, current-feedback amplifiers designed to operate over a wide supply range of ±5 V to ±15 V for today's high performance applications.

The THS3110 features a power-down pin (PD) that puts the amplifier in low-power standby mode, and lowers the quiescent current from 4.8 mA to 270 μA.

These amplifiers provide well-regulated ac performance characteristics. The unity-gain bandwidth of 100 MHz allows for good distortion characteristics below 10 MHz. Coupled with a high 1300-V/μs slew rate, the THS3110 and THS3111 amplifiers allow for high output voltage swings at high frequencies.

The THS3110 and THS3111 are offered in the SOIC-8 (D) and the MSOP-8 (DGN) packages with PowerPAD™.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

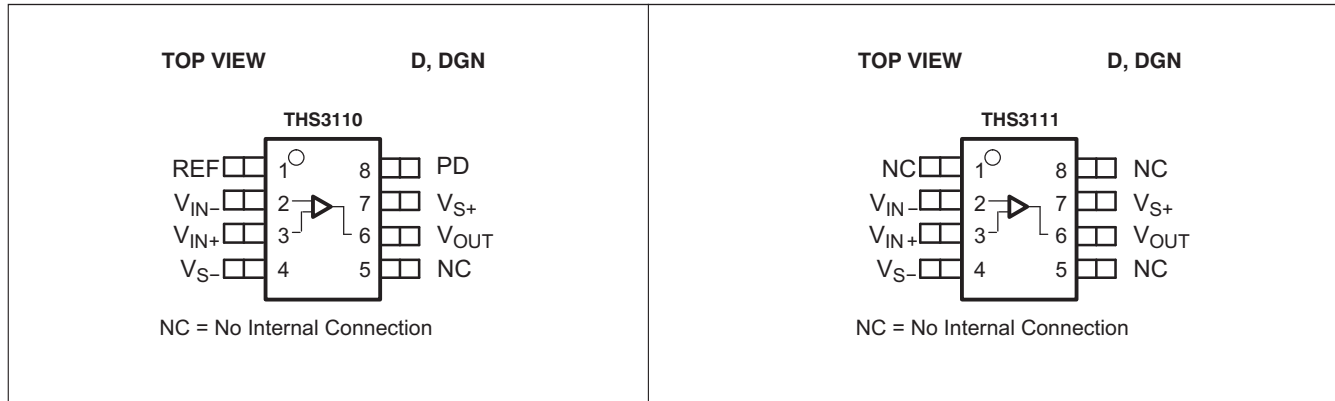
PowerPAD is a trademark of Texas Instruments.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



NOTE: The device with the power-down option defaults to the ON state if no signal is applied to the PD pin. Additionally, the REF pin functional range is from  $V_{S-}$  to  $(V_{S+} - 4 V)$ .

**AVAILABLE OPTIONS<sup>(1)</sup>**

$T_A$	PACKAGED DEVICE			SYMBOL
	PLASTIC SMALL OUTLINE SOIC (D)	PLASTIC MSOP (DGN) <sup>(2)</sup>		
0°C to +70°C	THS3110CD	THS3110CDGN		BJB
	THS3110CDR	THS3110CDGNR		
-40°C to +85°C	THS3110ID	THS3110IDGN		BIR
	THS3110IDR	THS3110IDGNR		
0°C to +70°C	THS3111CD	THS3111CDGN		BJA
	THS3111CDR	THS3111CDGNR		
-40°C to +85°C	THS3111ID	THS3111IDGN		BIS
	THS3111IDR	THS3111IDGNR		

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) The PowerPAD is electrically isolated from all other pins.

**DISSIPATION RATINGS TABLE**

PACKAGE	$\theta_{JC}$ (°C/W)	$\theta_{JA}$ (°C/W)	POWER RATING $T_J = +125^\circ\text{C}$	
			$T_A = +25^\circ\text{C}$	$T_A = +85^\circ\text{C}$
D-8 <sup>(1)</sup>	38.3	95	1.05 W	421 mW
DGN-8 <sup>(2)</sup>	4.7	58.4	1.71 W	685 mW

- (1) These data were taken using the JEDEC standard low-K test PCB. For the JEDEC proposed high-K test PCB, the  $\theta_{JA}$  is 95°C/W with power rating at  $T_A = +25^\circ\text{C}$  of 1.05 W.
- (2) These data were taken using 2 oz. trace and copper pad that is soldered directly to a 3 inch x 3 inch (76,2 mm x 76,2 mm) PCB. For further information, refer to the [Application Information](#) section of this data sheet.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T <sub>A</sub>	Commercial	0		+70	°C
	Industrial	–40		+85	
Operating junction temperature, continuous operating temperature, T <sub>J</sub>		–40		+125	
Normal storage temperature, T <sub>STG</sub>		–40		+85	

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature, unless otherwise noted.

		UNIT
Supply voltage, V <sub>S-</sub> to V <sub>S+</sub>		33 V
Input voltage, V <sub>I</sub>		± V <sub>S</sub>
Differential input voltage, V <sub>ID</sub>		± 4 V
Output current, I <sub>O</sub> <sup>(2)</sup>		300 mA
Continuous power dissipation		See <a href="#">Dissipation Ratings Table</a>
Maximum junction temperature, T <sub>J</sub> <sup>(3)</sup>		+150°C
Maximum junction temperature, continuous operation, long term reliability, T <sub>J</sub> <sup>(4)</sup>		+125°C
Operating free-air temperature, T <sub>A</sub>	Commercial	0°C to +70°C
	Industrial	–40°C to +85°C
Storage temperature, T <sub>stg</sub>		–65°C to +125°C
ESD ratings:		
HBM		900
CDM		1500
MM		200

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The THS3110 and THS3111 may incorporate a PowerPAD on the underside of the chip. This feature acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief [SLMA002](#) for more information about utilizing the PowerPAD™ thermally-enhanced package.
- (3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
- (4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

## ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_L = 100\ \Omega$ , and  $G = 2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			UNIT	MIN/TYP/ MAX
		+25°C	+25°C	0°C to +70°C	-40°C to +85°C		
<b>AC PERFORMANCE</b>							
Small-signal bandwidth, -3 dB	$G = 1$ , $R_F = 1.5\text{ k}\Omega$ , $V_O = 200\text{ mV}_{PP}$	100				MHz	TYP
	$G = 2$ , $R_F = 1\text{ k}\Omega$ , $V_O = 200\text{ mV}_{PP}$	90					
	$G = 5$ , $R_F = 806\ \Omega$ , $V_O = 200\text{ mV}_{PP}$	87					
	$G = 10$ , $R_F = 604\ \Omega$ , $V_O = 200\text{ mV}_{PP}$	66					
0.1-dB bandwidth flatness	$G = 2$ , $R_F = 1.15\text{ k}\Omega$ , $V_O = 200\text{ mV}_{PP}$	45					
Large-signal bandwidth	$G = 5$ , $R_F = 806\ \Omega$ , $V_O = 4\text{ V}_{PP}$	95					
Slew rate (25% to 75% level)	$G = 1$ , $V_O = 4\text{-V step}$ , $R_F = 1.5\text{ k}\Omega$	800				V/ $\mu\text{s}$	TYP
	$G = 2$ , $V_O = 8\text{-V step}$ , $R_F = 1\text{ k}\Omega$	1300					
Slew rate	Recommended maximum SR for repetitive signals <sup>(1)</sup>	900				V/ $\mu\text{s}$	MAX
Rise and fall time	$G = -5$ , $V_O = 10\text{-V step}$ , $R_F = 806\ \Omega$	8				ns	TYP
Settling time to 0.1%	$G = -2$ , $V_O = 2\text{ V}_{PP}$ step	27				ns	TYP
Settling time to 0.01%	$G = -2$ , $V_O = 2\text{ V}_{PP}$ step	250					
<b>Harmonic distortion</b>							
2nd harmonic distortion	$G = 2$ , $R_F = 1\text{ k}\Omega$ , $V_O = 2\text{ V}_{PP}$ , $f = 10\text{ MHz}$	$R_L = 100\ \Omega$	52			dBc	TYP
		$R_L = 1\text{ k}\Omega$	53				
3rd harmonic distortion		$R_L = 100\ \Omega$	48				
		$R_L = 1\text{ k}\Omega$	68				
Input voltage noise	$f > 20\text{ kHz}$	3				nV/ $\sqrt{\text{Hz}}$	TYP
Noninverting input current noise	$f > 20\text{ kHz}$	2				pA/ $\sqrt{\text{Hz}}$	TYP
Inverting input current noise	$f > 20\text{ kHz}$	10				pA/ $\sqrt{\text{Hz}}$	TYP
Differential gain	$G = 2$ , $R_L = 150\ \Omega$ , $R_F = 1\text{ k}\Omega$	NTSC	0.011%				TYP
		PAL	0.013%				
Differential phase		NTSC	0.029°				
		PAL	0.033°				
<b>DC PERFORMANCE</b>							
Transimpedance	$V_O = \pm 3.75\text{ V}$ , gain = 1	1	0.75	0.5	0.5	M $\Omega$	MIN
Input offset voltage	$V_{CM} = 0\text{ V}$	3	10	12	12	mV	MAX
Average offset voltage drift				$\pm 10$	$\pm 10$	$\mu\text{V}/^\circ\text{C}$	TYP
Noninverting input bias current	$V_{CM} = 0\text{ V}$	1	4	6	6	$\mu\text{A}$	MAX
Average bias current drift				$\pm 10$	$\pm 10$	nA/ $^\circ\text{C}$	TYP
Inverting input bias current	$V_{CM} = 0\text{ V}$	1.5	15	20	20	$\mu\text{A}$	MAX
Average bias current drift				$\pm 10$	$\pm 10$	nA/ $^\circ\text{C}$	TYP
Input offset current	$V_{CM} = 0\text{ V}$	2.5	15	20	20	$\mu\text{A}$	MAX
Average offset current drift				$\pm 30$	$\pm 30$	nA/ $^\circ\text{C}$	TYP
<b>INPUT CHARACTERISTICS</b>							
Input common-mode voltage range		$\pm 13.3$	$\pm 13$	$\pm 12.5$	$\pm 12.5$	V	MIN
Common-mode rejection ratio	$V_{CM} = \pm 12.5\text{ V}$	68	62	60	60	dB	MIN
Noninverting input resistance		41				M $\Omega$	TYP
Noninverting input capacitance		0.4				pF	TYP
<b>OUTPUT CHARACTERISTICS</b>							
Output voltage swing	$R_L = 1\text{ k}\Omega$	$\pm 13.5$	$\pm 13$	$\pm 12.5$	$\pm 12.5$	V	MIN
	$R_L = 100\ \Omega$	$\pm 13.4$	$\pm 12.5$	$\pm 12$	$\pm 12$		
Output current (sourcing)	$R_L = 25\ \Omega$	260	200	175	175	mA	MIN
Output current (sinking)	$R_L = 25\ \Omega$	260	200	175	175	mA	MIN
Output impedance	$f = 1\text{ MHz}$ , closed loop	0.15				$\Omega$	TYP

(1) For more information, see the [Application Information](#) section of this data sheet.

## ELECTRICAL CHARACTERISTICS (continued)

$V_S = \pm 15\text{ V}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_L = 100\ \Omega$ , and  $G = 2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			UNIT	MIN/TYP/ MAX
		+25°C	+25°C	0°C to +70°C	-40°C to +85°C		
<b>POWER SUPPLY</b>							
Specified operating voltage		±15	±16	±16	±16	V	MAX
Maximum quiescent current		4.8	6.5	7.5	7.5	mA	MAX
Minimum quiescent current		4.8	3.8	2.5	2.5	mA	MIN
Power-supply rejection (+PSRR)	$V_{S+} = 15.5\text{ V}$ to $14.5\text{ V}$ , $V_{S-} = 15\text{ V}$	75	65	60	60	dB	MIN
Power-supply rejection (-PSRR)	$V_{S+} = 15\text{ V}$ , $V_{S-} = -15.5\text{ V}$ to $-14.5\text{ V}$	69	60	55	55	dB	MIN
<b>POWER-DOWN CHARACTERISTICS (THS3110 Only)</b>							
REF voltage range <sup>(2)</sup>		$V_{S+} - 4$				V	MAX
		$V_{S-}$				V	MIN
Power-down voltage level <sup>(2)</sup>	Enable	$PD \leq$ $REF + 0.8$				V	MIN
	Disable	$PD \geq$ REF $+ 2$				V	MAX
Power-down quiescent current	$PD \geq$ REF + 2 V	270	450	500	500	µA	MAX
PD pin bias current	$V_{PD} = 0\text{ V}$ , REF = 0 V,	11				µA	TYP
	$V_{PD} = 3.3\text{ V}$ , REF = 0 V	11					
Turn-on time delay	90% of final value	4				µs	TYP
Turn-off time delay	10% of final value	6					
Input impedance		3.4    1.7				kΩ    pF	TYP

- (2) For detailed information on the behavior of the power-down circuit, see the [Saving Power with Power-Down Functionality](#) and [Power-Down Reference Pin Operation](#) sections in the [Application Information](#) section of this data sheet.

## ELECTRICAL CHARACTERISTICS

$V_S = \pm 5\text{ V}$ ,  $R_F = 1.15\ \Omega$ ,  $R_L = 100\ \Omega$ , and  $G = 2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			UNIT	MIN/TYP/ MAX	
		+25°C	+25°C	0°C to +70°C	-40°C to +85°C			
<b>AC PERFORMANCE</b>								
Small-signal bandwidth, -3 dB	$G = 1$ , $R_F = 1.5\ \text{k}\Omega$ , $V_O = 200\ \text{mV}_{PP}$	85				MHz	TYP	
	$G = 2$ , $R_F = 1.15\ \text{k}\Omega$ , $V_O = 200\ \text{mV}_{PP}$	78						
	$G = 5$ , $R_F = 806\ \Omega$ , $V_O = 200\ \text{mV}_{PP}$	80						
	$G = 10$ , $R_F = 604\ \Omega$ , $V_O = 200\ \text{mV}_{PP}$	60						
0.1-dB bandwidth flatness	$G = 2$ , $R_F = 1.15\ \text{k}\Omega$ , $V_O = 200\ \text{mV}_{PP}$	15						
Large-signal bandwidth	$G = 5$ , $R_F = 806\ \Omega$ , $V_O = 4\ \text{V}_{PP}$	80						
Slew rate (25% to 75% level)	$G = 1$ , $V_O = 4\text{-V step}$ , $R_F = 1.5\ \text{k}\Omega$	640				V/ $\mu\text{s}$	TYP	
	$G = 2$ , $V_O = 4\text{-V step}$ , $R_F = 1\ \text{k}\Omega$	700						
Slew rate	Recommended maximum SR for repetitive signals <sup>(1)</sup>	900				V/ $\mu\text{s}$	MAX	
Rise and fall time	$G = -5$ , $V_O = 5\text{-V step}$ , $R_F = 806\ \Omega$	7				ns	TYP	
Settling time to 0.1%	$G = -2$ , $V_O = 2\ \text{V}_{PP}$ step	20				ns	TYP	
Settling time to 0.01%	$G = -2$ , $V_O = 2\ \text{V}_{PP}$ step	200						
<b>Harmonic distortion</b>								
2nd harmonic distortion	$G = 2$ , $R_F = 1\ \text{k}\Omega$ , $V_O = 2\ \text{V}_{PP}$ , $f = 10\ \text{MHz}$	$R_L = 100\ \Omega$	55			dBc	TYP	
		$R_L = 1\ \text{k}\Omega$	56					
3rd harmonic distortion		$R_L = 100\ \Omega$	45					
		$R_L = 1\ \text{k}\Omega$	62					
Input voltage noise	$f > 20\ \text{kHz}$	3				nV/ $\sqrt{\text{Hz}}$	TYP	
Noninverting input current noise	$f > 20\ \text{kHz}$	2				pA/ $\sqrt{\text{Hz}}$	TYP	
Inverting input current noise	$f > 20\ \text{kHz}$	10				pA/ $\sqrt{\text{Hz}}$	TYP	
Differential gain	$G = 2$ , $R_L = 150\ \Omega$ , $R_F = 1\ \text{k}\Omega$	NTSC	0.011%				TYP	
		PAL	0.015%					
Differential phase		NTSC	0.020°					
		PAL	0.033°					
<b>DC PERFORMANCE</b>								
Transimpedance	$V_O = \pm 1.25\ \text{V}$ , gain = 1	1	0.75	0.5	0.5	M $\Omega$	MIN	
Input offset voltage	$V_{CM} = 0\ \text{V}$	6	10	12	12	mV	MAX	
Average offset voltage drift				$\pm 10$	$\pm 10$	$\mu\text{V}/^\circ\text{C}$	TYP	
Noninverting input bias current	$V_{CM} = 0\ \text{V}$	1	4	6	6	$\mu\text{A}$	MAX	
Average bias current drift				$\pm 10$	$\pm 10$	nA/ $^\circ\text{C}$	TYP	
Inverting input bias current	$V_{CM} = 0\ \text{V}$	1	8	10	10	$\mu\text{A}$	MAX	
Average bias current drift				$\pm 10$	$\pm 10$	nA/ $^\circ\text{C}$	TYP	
Input offset current	$V_{CM} = 0\ \text{V}$	1	6	8	8	$\mu\text{A}$	MAX	
Average offset current drift				$\pm 20$	$\pm 20$	nA/ $^\circ\text{C}$	TYP	
<b>INPUT CHARACTERISTICS</b>								
Input common-mode voltage range		$\pm 3.2$	$\pm 2.9$	$\pm 2.8$	$\pm 2.8$	V	MIN	
Common-mode rejection ratio	$V_{CM} = \pm 2.5\ \text{V}$	65	62	58	58	dB	MIN	
Noninverting input resistance		35				M $\Omega$	TYP	
Noninverting input capacitance		0.5				pF	TYP	
<b>OUTPUT CHARACTERISTICS</b>								
Output voltage swing	$R_L = 1\ \text{k}\Omega$	$\pm 4$	$\pm 3.8$	$\pm 3.6$	$\pm 3.6$	V	MIN	
	$R_L = 100\ \Omega$	$\pm 3.8$	$\pm 3.7$	$\pm 3.5$	$\pm 3.5$			
Output current (sourcing)	$R_L = 10\ \Omega$	220	150	125	125	mA	MIN	
Output current (sinking)	$R_L = 10\ \Omega$	220	150	125	125	mA	MIN	
Output impedance	$f = 1\ \text{MHz}$ , closed loop	0.15				$\Omega$	TYP	

(1) For more information, see the [Application Information](#) section of this data sheet.

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_S = \pm 5\text{ V}$ ,  $R_F = 1.15\ \Omega$ ,  $R_L = 100\ \Omega$ , and  $G = 2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			UNIT	MIN/TYP/ MAX
		+25°C	+25°C	0°C to +70°C	-40°C to +85°C		
<b>POWER SUPPLY</b>							
Specified operating voltage		±5	±4.5	±4.5	±4.5	V	MIN
Maximum quiescent current		4	6	7	7	mA	MAX
Minimum quiescent current		4	3.2	2	2	mA	MIN
Power-supply rejection (+PSRR)	$V_{S+} = 5.5\text{ V to }4.5\text{ V}$ , $V_{S-} = 5\text{ V}$	71	62	57	57	dB	MIN
Power-supply rejection (-PSRR)	$V_{S+} = 5\text{ V}$ , $V_{S-} = -5.5\text{ V to }-4.5\text{ V}$	66	57	52	52	dB	MIN
<b>POWER-DOWN CHARACTERISTICS (THS3110 Only)</b>							
REF voltage range <sup>(2)</sup>		$V_{S+} - 4$				V	MAX
		$V_{S-}$				V	MIN
Power-down voltage level <sup>(2)</sup>	Enable	$PD \leq \text{REF} + 0.8$				V	MIN
	Disable	$PD \geq \text{REF} + 2$				V	MAX
Power-down quiescent current	$PD \geq \text{REF} + 2\text{ V}$	200	450	500	500	µA	MAX
PD pin bias current	$V_{PD} = 0\text{ V}$ , $\text{REF} = 0\text{ V}$ ,	11				µA	TYP
	$V_{PD} = 3.3\text{ V}$ , $\text{REF} = 0\text{ V}$	11					
Turn-on time delay	90% of final value	4				µs	TYP
Turn-off time delay	10% of final value	6					
Input impedance		$3.4 \parallel 1.7$				kΩ    pF	TYP

- (2) For detailed information on the behavior of the power-down circuit, see the [Power-Down](#) and [Power-down Reference](#) sections in the [Application Information](#) section of this data sheet.

## TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS (±15 V)

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

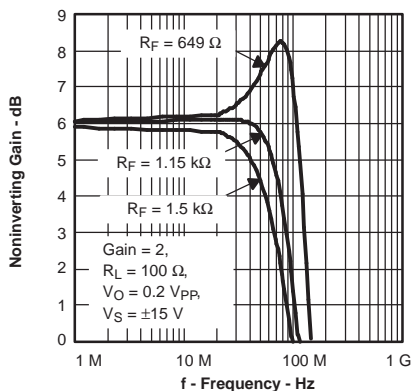


Figure 1.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

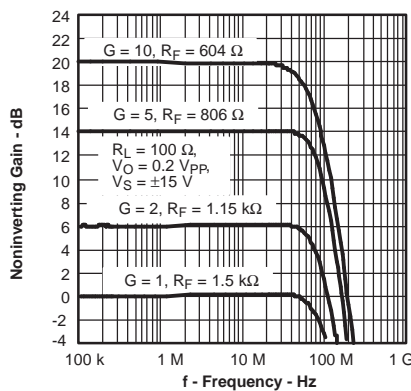


Figure 2.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

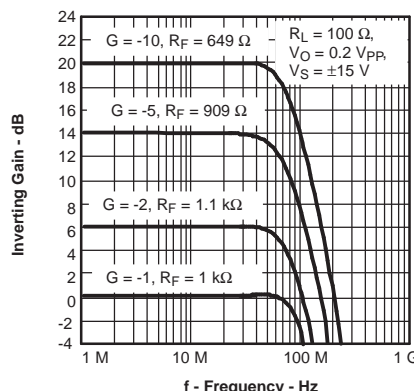


Figure 3.

0.1-dB FLATNESS

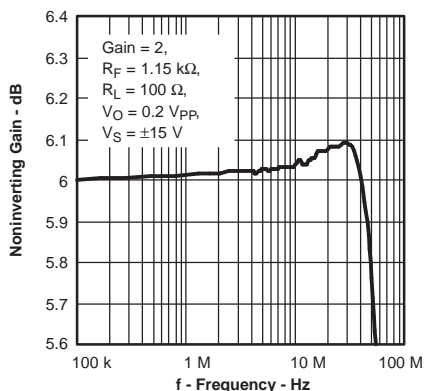


Figure 4.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

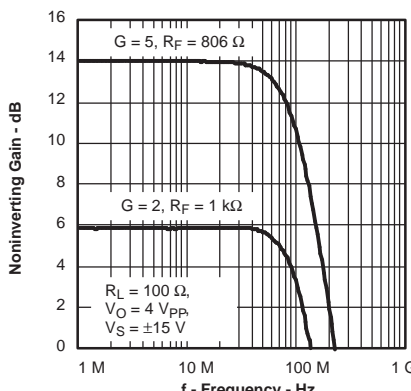


Figure 5.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

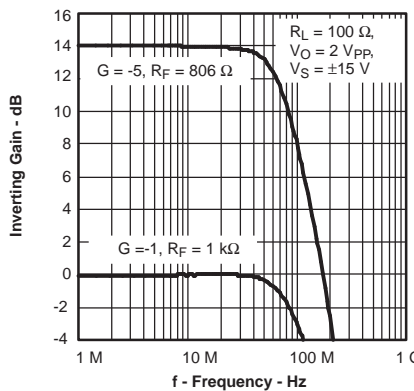


Figure 6.

FREQUENCY RESPONSE CAPACITIVE LOAD

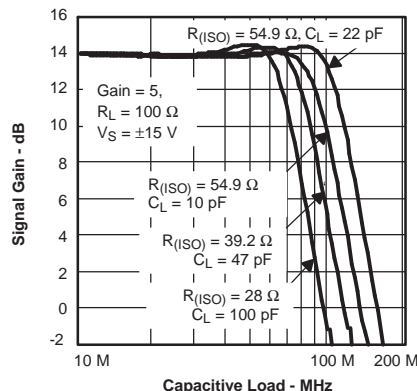


Figure 7.

RECOMMENDED  $R_{ISO}$  vs CAPACITIVE LOAD

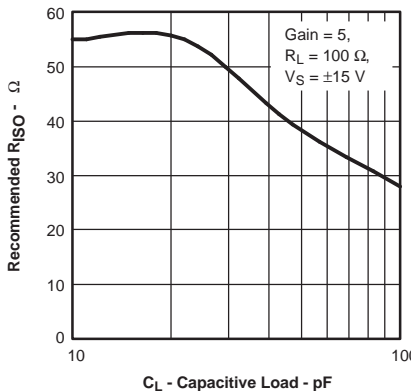


Figure 8.

2nd HARMONIC DISTORTION vs FREQUENCY

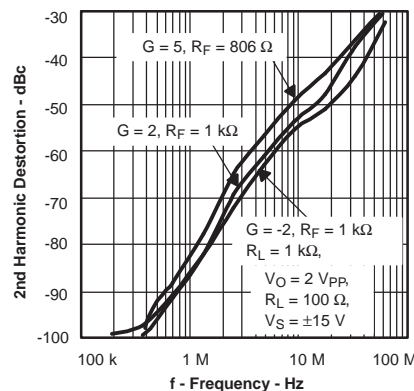


Figure 9.

TYPICAL CHARACTERISTICS ( $\pm 15$  V) (continued)

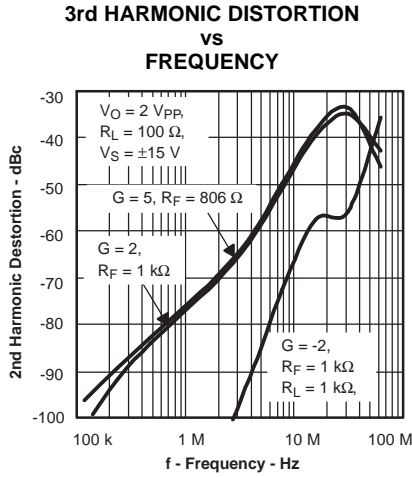


Figure 10.

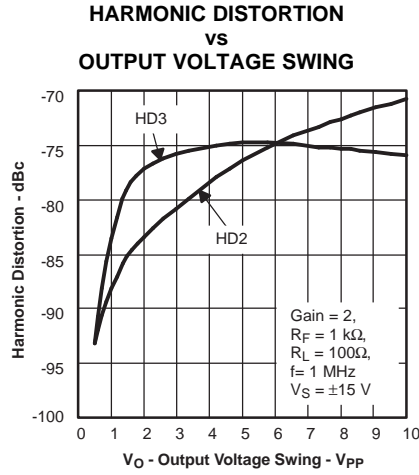


Figure 11.

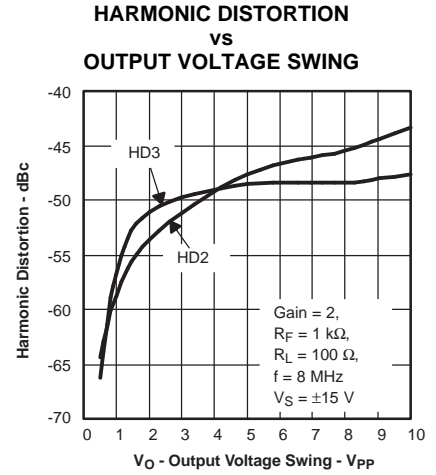


Figure 12.

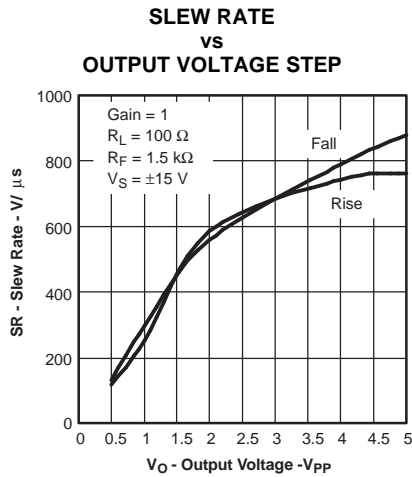


Figure 13.

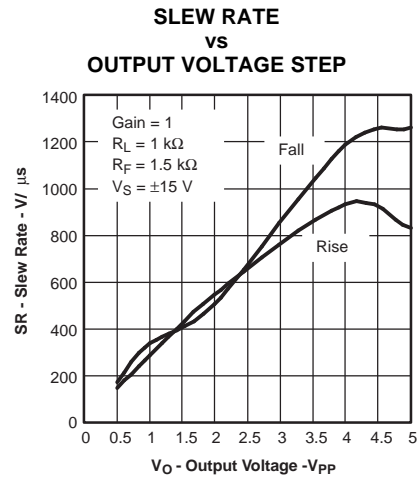


Figure 14.

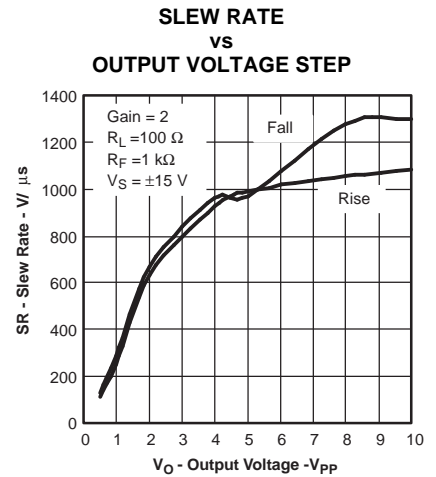


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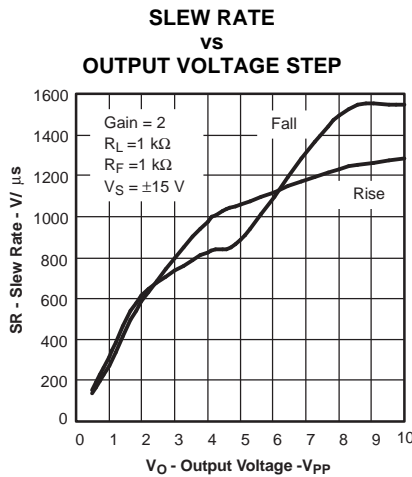


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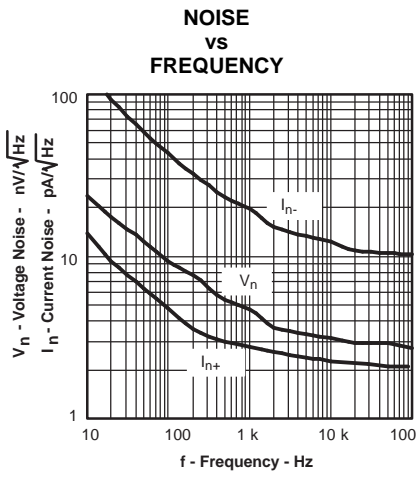


Figure 17.

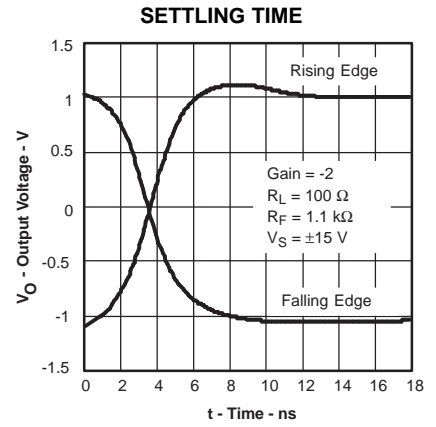


Figure 18.

TYPICAL CHARACTERISTICS ( $\pm 15$  V) (continued)

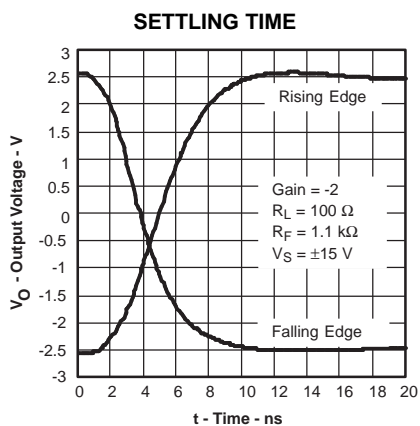


Figure 19.

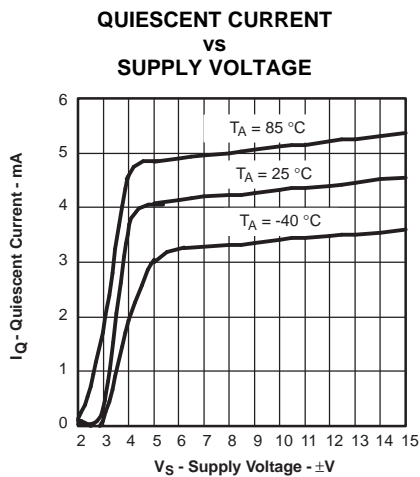


Figure 20.

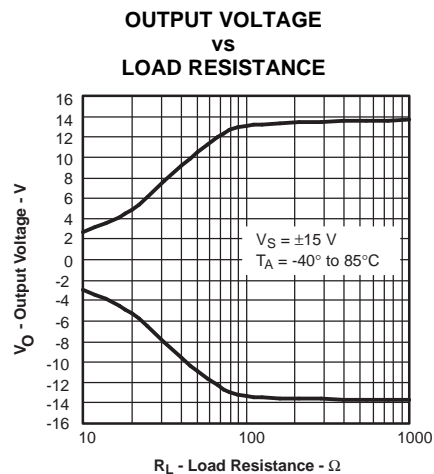


Figure 21.

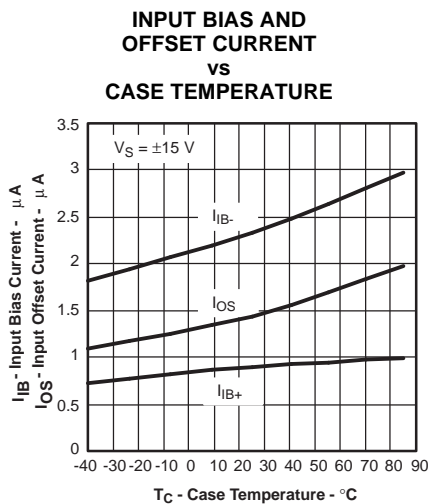


Figure 22.

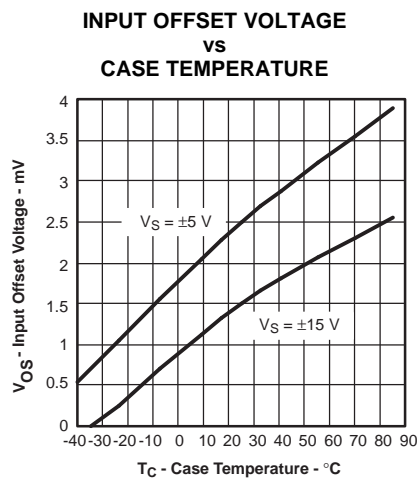


Figure 23.

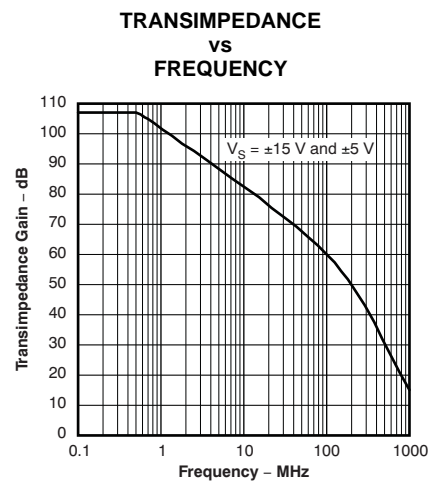


Figure 24.

TYPICAL CHARACTERISTICS ( $\pm 15$  V) (continued)

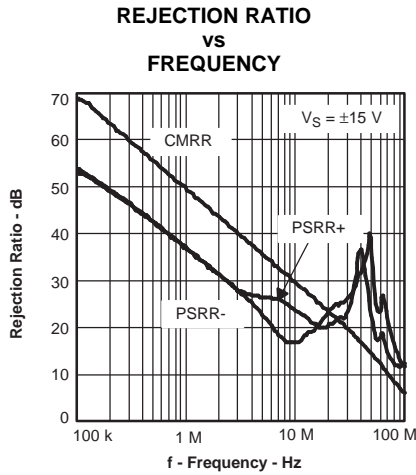


Figure 25.

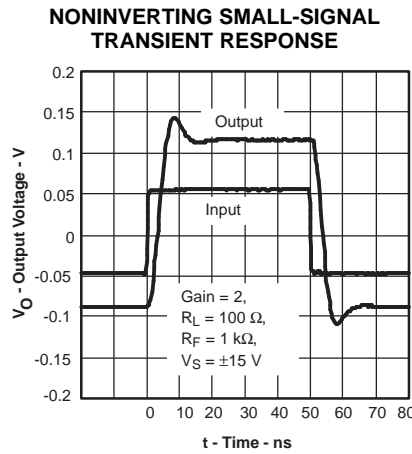


Figure 26.

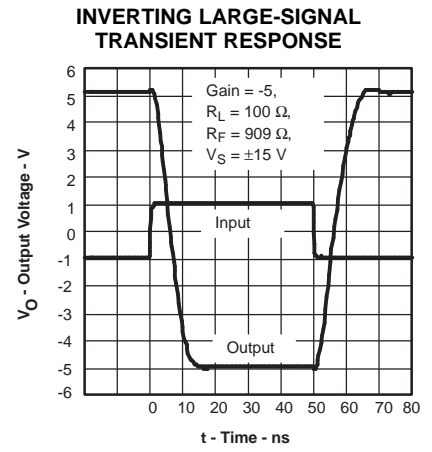


Figure 27.

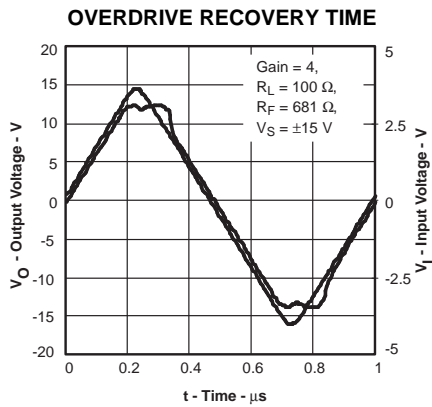


Figure 28.

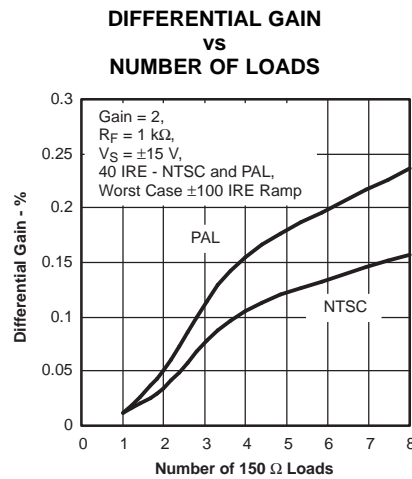


Figure 29.

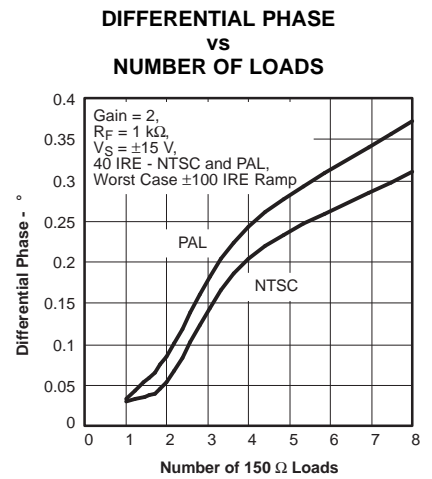


Figure 30.

TYPICAL CHARACTERISTICS ( $\pm 15$  V) (continued)

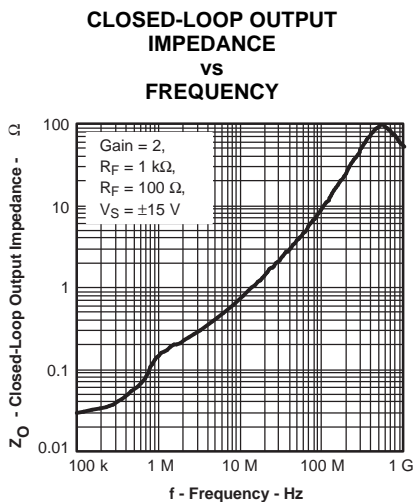


Figure 31.

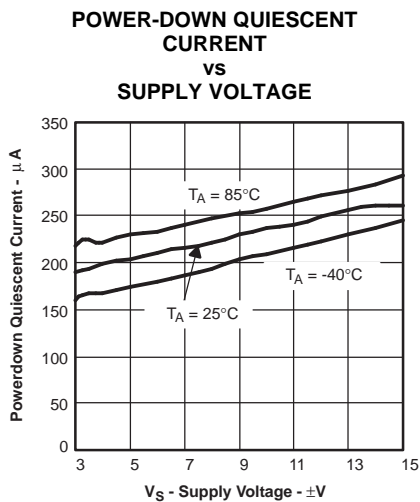


Figure 32.

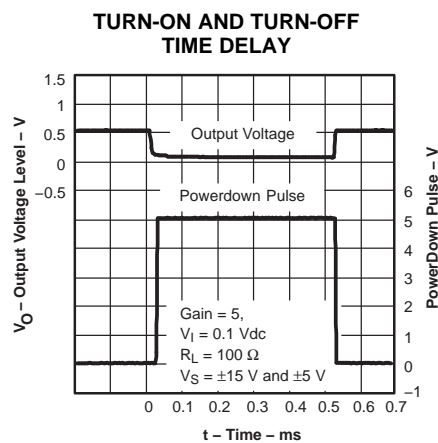


Figure 33.

TYPICAL CHARACTERISTICS ( $\pm 5$  V)

NONINVERTING SMALL-SIGNAL  
FREQUENCY RESPONSE

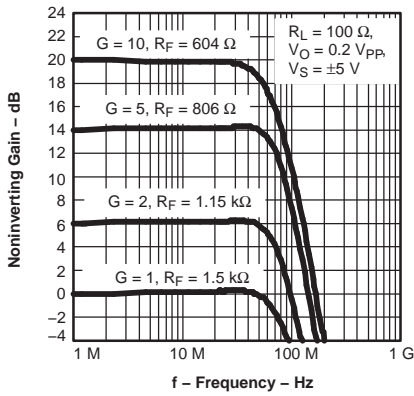


Figure 34.

INVERTING SMALL-SIGNAL  
FREQUENCY RESPONSE

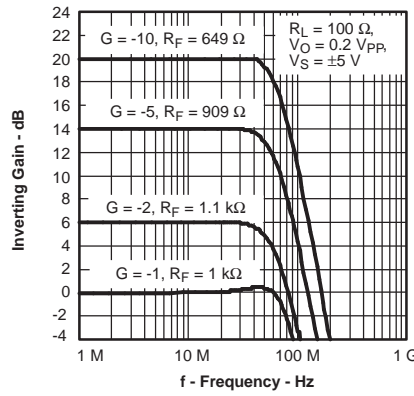


Figure 35.

0.1-dB FLATNESS

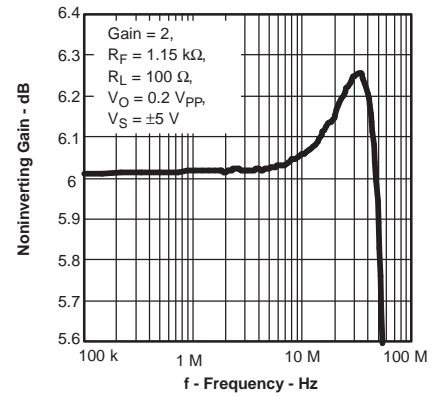


Figure 36.

NONINVERTING LARGE-SIGNAL  
FREQUENCY RESPONSE

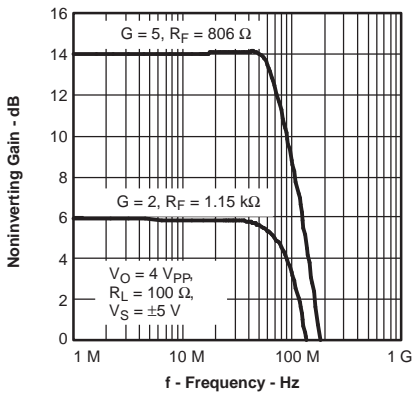


Figure 37.

INVERTING LARGE-SIGNAL  
FREQUENCY RESPONSE

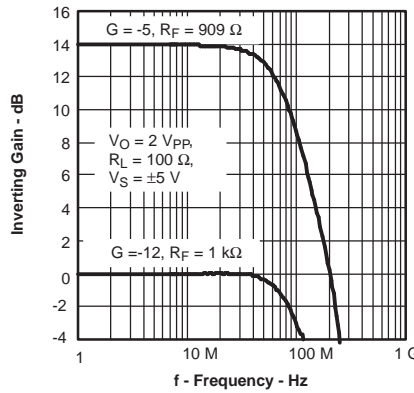


Figure 38.

SLEW RATE  
vs  
OUTPUT VOLTAGE STEP

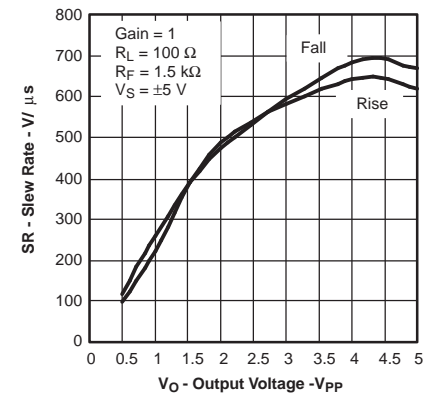


Figure 39.

SLEW RATE  
vs  
OUTPUT VOLTAGE STEP

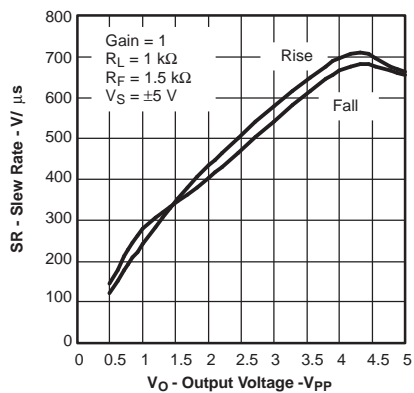


Figure 40.

SLEW RATE  
vs  
OUTPUT VOLTAGE STEP

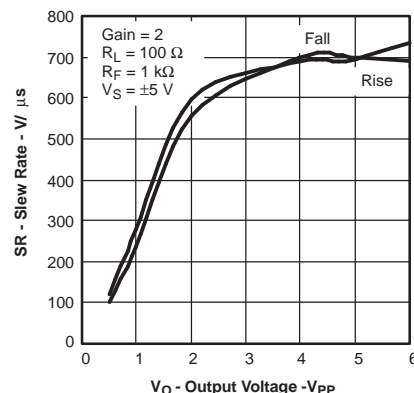


Figure 41.

SLEW RATE  
vs  
OUTPUT VOLTAGE STEP

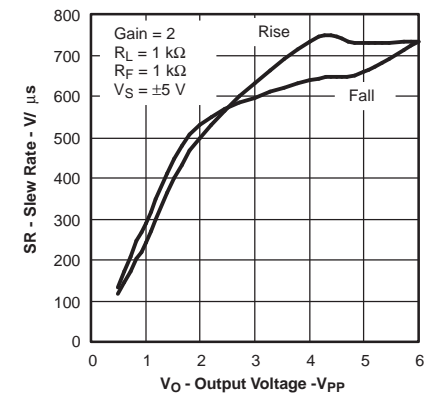


Figure 42.

TYPICAL CHARACTERISTICS ( $\pm 5$  V) (continued)

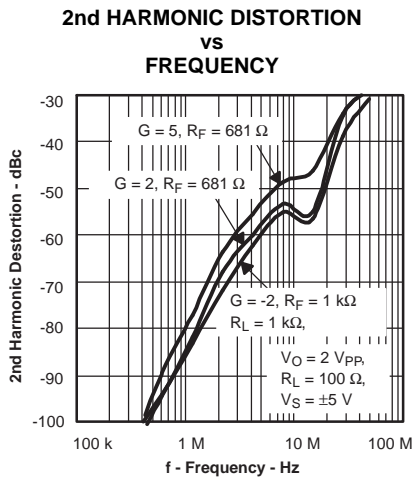


Figure 43.

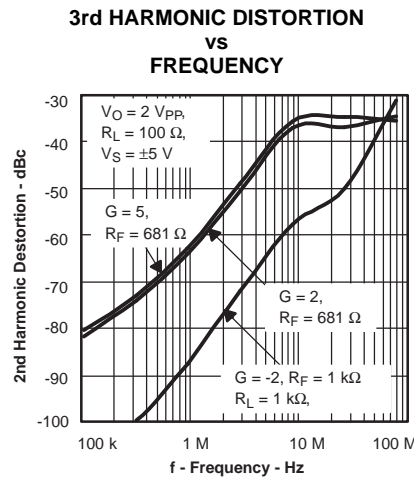


Figure 44.

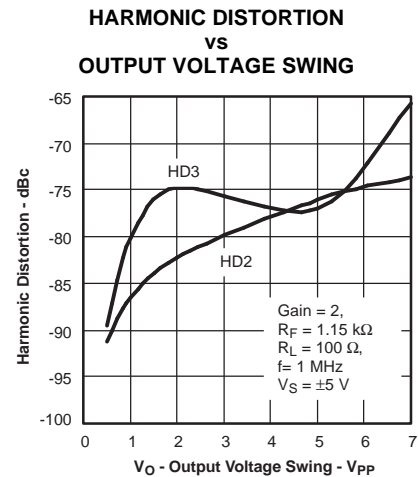


Figure 45.

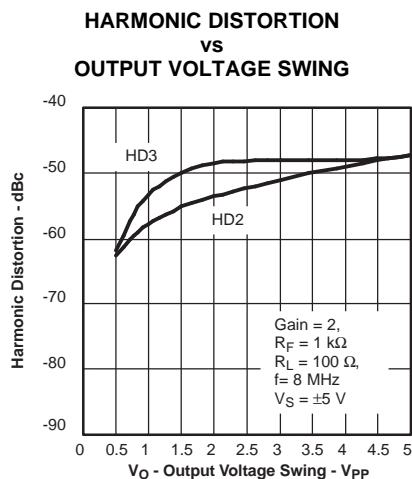


Figure 46.

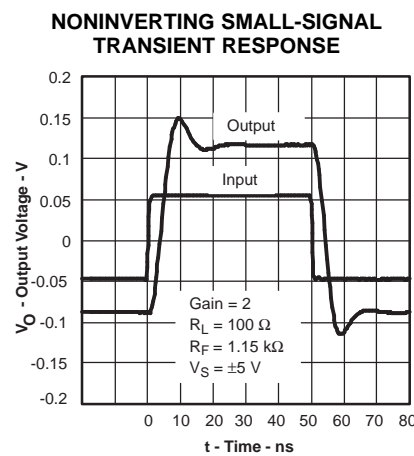


Figure 47.

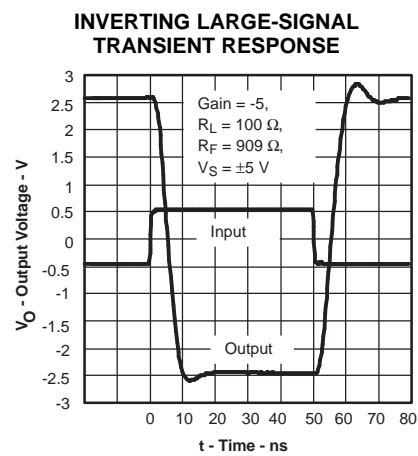


Figure 48.

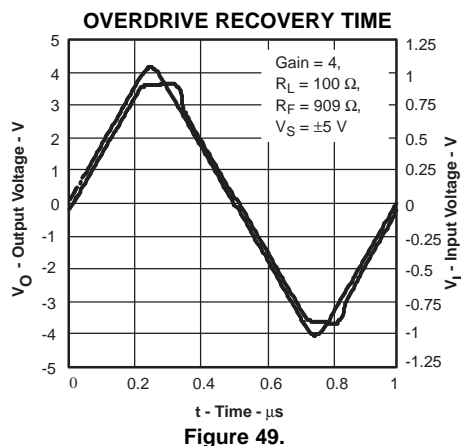


Figure 49.

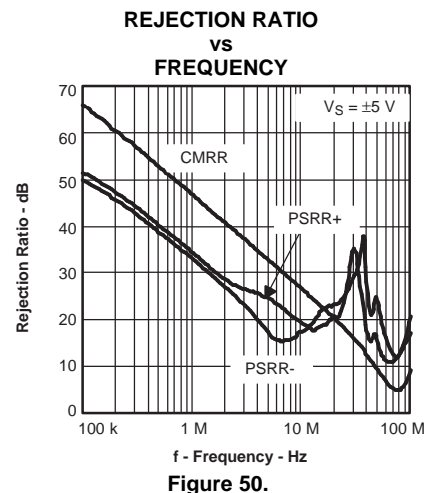


Figure 50.

## APPLICATION INFORMATION

### MAXIMUM SLEW RATE FOR REPETITIVE SIGNALS

The THS3110 and THS3111 are recommended for high slew rate pulsed applications where the internal nodes of the amplifier have time to stabilize between pulses. It is recommended to have at least 20-ns delay between pulses.

The THS3110 and THS3111 are not recommended for applications with repetitive signals (sine, square, sawtooth, or other) that exceed 900 V/μs. Using the part in these applications results in excessive current draw from the power supply and possible device damage.

For applications with high slew rate, repetitive signals, the THS3091 and THS3095 (single), or THS3092 and THS3096 (dual) are recommended.

### WIDEBAND, NONINVERTING OPERATION

The THS3110 and THS3111 are unity-gain stable, 100-MHz, current-feedback operational amplifiers, designed to operate from a ±5-V to ±15-V power supply.

Figure 51 shows the THS3111 in a noninverting gain of 2-V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance.

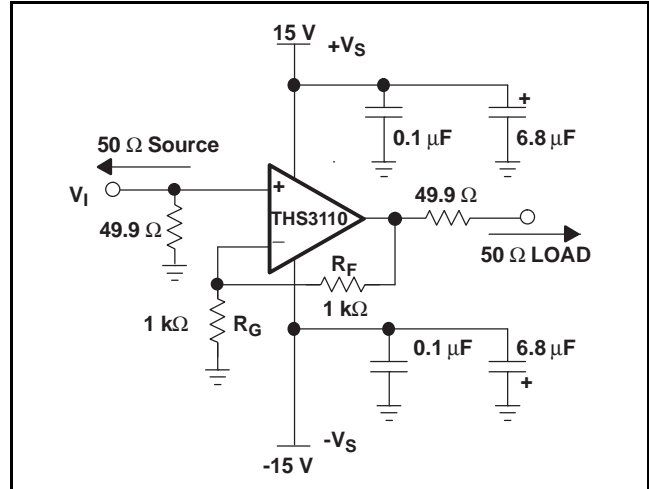


Figure 51. Wideband, Noninverting Gain Configuration

Current-feedback amplifiers are highly dependent on the feedback resistor  $R_F$  for maximum performance and stability. Table 1 shows the optimal gain setting resistors  $R_F$  and  $R_G$  at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for  $R_F$ . Conversely, increasing  $R_F$  decreases the bandwidth, but stability is improved.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3110 AND THS3111 $R_F$ AND $R_G$ VALUES FOR MINIMAL PEAKING WITH $R_L = 100 \Omega$			
GAIN (V/V)	SUPPLY VOLTAGE (V)	$R_G (\Omega)$	$R_F (\Omega)$
1	±15	—	1.5 k
	±5	—	1.5 k
2	±15	1 k	1 k
	±5	1.15 k	1.15 k
5	±15	200	806
	±5	200	806
10	±15	66.5	604
	±5	66.5	604
-1	±15	1 k	1 k
	±5	1 k	1 k
-2	±15 and ±5	549	1.1 k
-5	±15 and ±5	182	909
-10	±15 and ±5	64.9	649

## WIDEBAND, INVERTING OPERATION

Figure 52 shows the THS3111 in a typical inverting gain configuration where the input and output impedances and signal gain from Figure 51 are retained in an inverting circuit configuration.

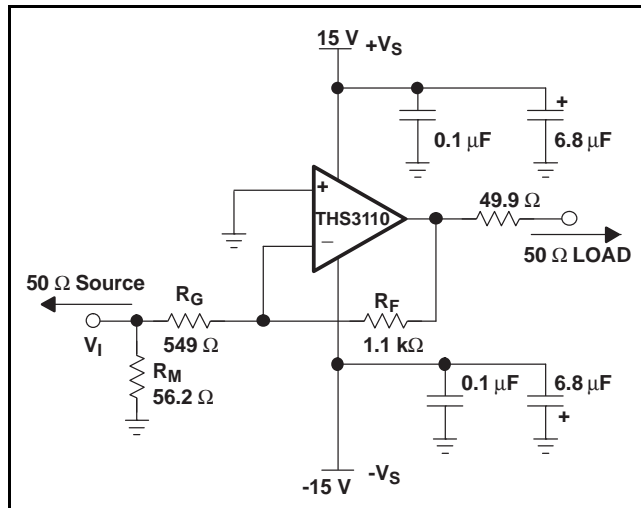


Figure 52. Wideband, Inverting Gain Configuration

## SINGLE-SUPPLY OPERATION

The THS3110 and THS3111 have the capability to operate from a single-supply voltage ranging from 10 V to 30 V. When operating from a single power supply, biasing the input and output at mid-supply allows for the maximum output voltage swing. The circuits shown in Figure 53 shows inverting and noninverting amplifiers configured for single supply operations.

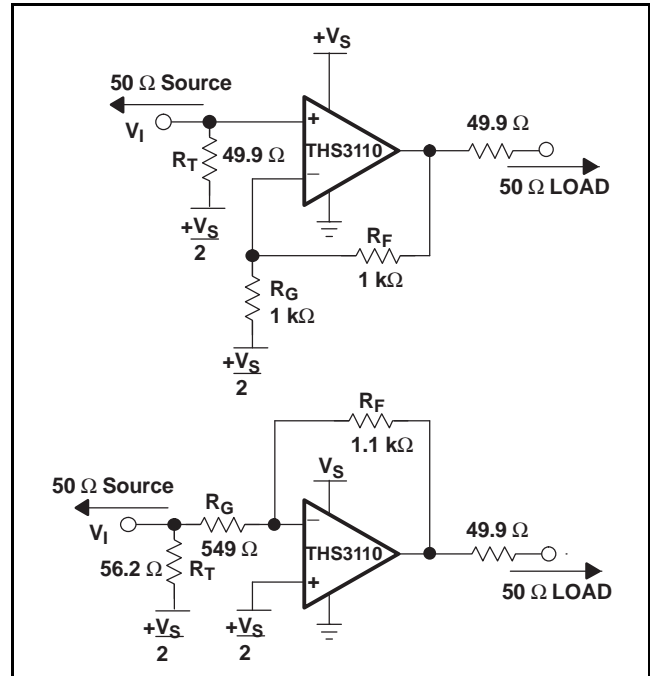


Figure 53. DC-Coupled, Single-Supply Operation

## Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS3110 and THS3111 match the demands for video distribution for delivering video signals down multiple cables. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal, and supports component video and RGB video signals that require fast transition times and fast settling times for high signal quality.

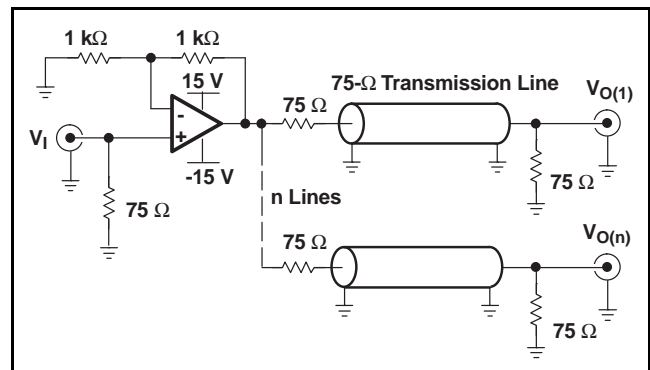


Figure 54. Video Distribution Amplifier Application

### Driving Capacitive Loads

Applications such as FET drivers and line drivers can be highly capacitive and cause stability problems for high-speed amplifiers.

Figure 55 through Figure 61 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier feedback path. See Figure 55 for recommended resistor values versus capacitive load.

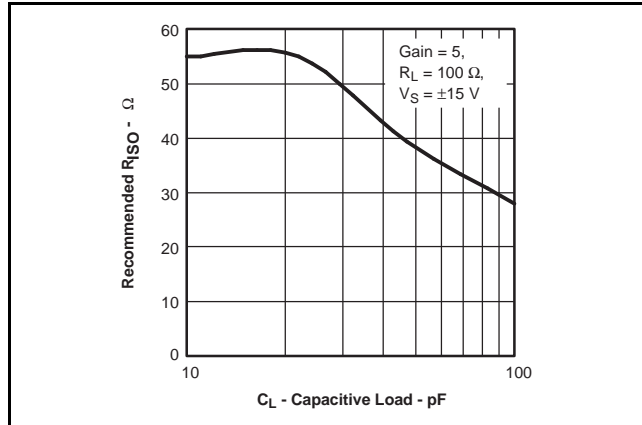


Figure 55. Recommended  $R_{ISO}$  vs Capacitive Load

Placing a small series resistor,  $R_{ISO}$ , between the amplifier output and the capacitive load, as shown in Figure 56, is an easy way of isolating the load capacitance.

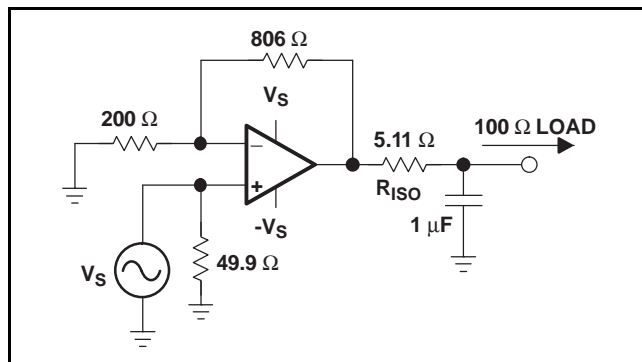


Figure 56. Resistor to Isolate Capacitive Load

Using a ferrite chip in place of  $R_{ISO}$ , as shown in Figure 57, is another approach of isolating the output of the amplifier. The ferrite impedance characteristic versus frequency is useful to maintain the low

frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. Use a ferrite chip with similar impedance to  $R_{ISO}$ , 20 ohms to 50 ohms, at 100 MHz and low impedance at dc.

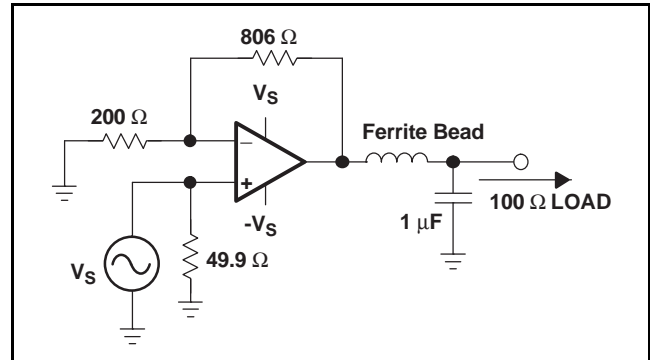


Figure 57. Ferrite Bead to Isolate Capacitive Load

Figure 58 shows another method used to maintain the low frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. At low frequency, feedback is mainly from the load side of  $R_{ISO}$ . At high frequency, the feedback is mainly via the 27-pF capacitor. The resistor  $R_{IN}$  in series with the negative input is used to stabilize the amplifier and should be equal to the recommended value of  $R_F$  at unity gain. Replacing  $R_{IN}$  with a ferrite of similar impedance at about 100 MHz as shown in Figure 59 gives similar results with reduced dc offset and low frequency noise. (See the *Additional Reference Material* section for expanding the usability of current-feedback amplifiers.)

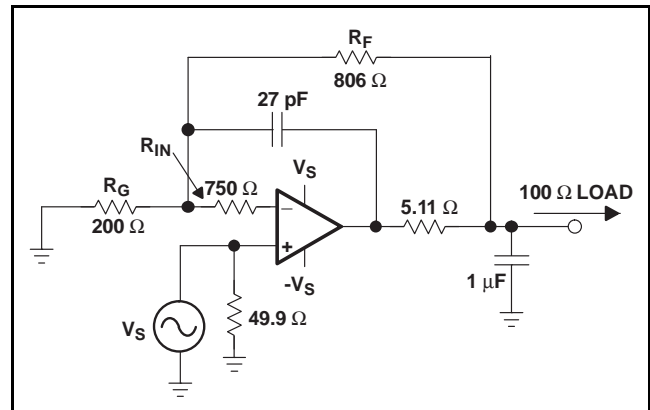
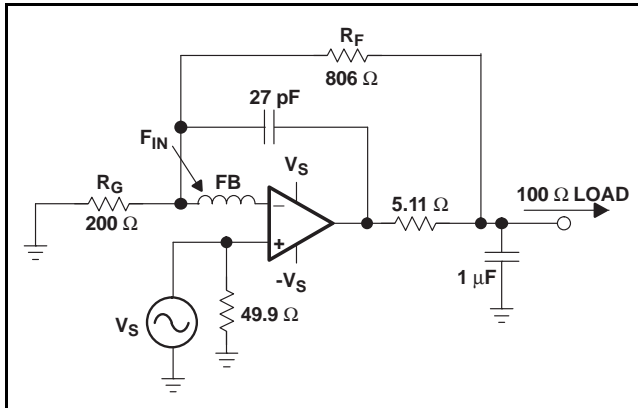
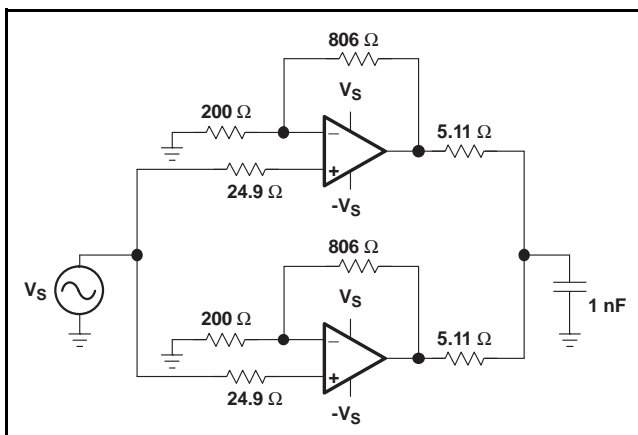


Figure 58. Feedback Technique with Input Resistor for Capacitive Load



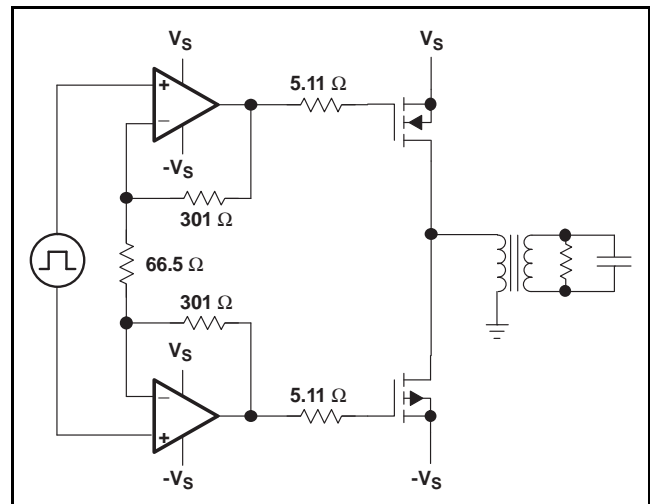
**Figure 59. Feedback Technique with Input Ferrite Bead for Capacitive Load**

Figure 60 shows how to use two amplifiers in parallel to double the output drive current to larger capacitive loads. This technique is used when more output current is needed to charge and discharge the load faster like when driving large FET transistors.



**Figure 60. Parallel Amplifiers for Higher Output Drive**

Figure 61 shows a push-pull FET driver circuit typical of ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.



**Figure 61. PowerFET Drive Circuit**

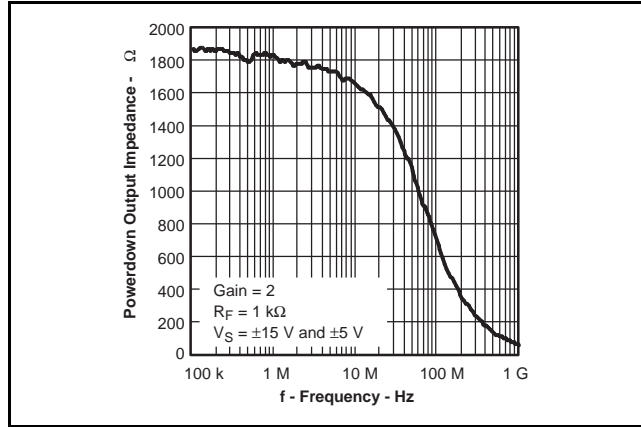
### SAVING POWER WITH POWER-DOWN FUNCTIONALITY AND SETTING THRESHOLD LEVELS WITH THE REFERENCE PIN

The THS3110 features a power-down pin (PD) which lowers the quiescent current from 4.8 mA down to 270  $\mu$ A, ideal for reducing system power.

The power-down pin of the amplifier defaults to the REF pin voltage in the absence of an applied voltage, putting the amplifier in the normal *on* mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the positive rail. The threshold voltages for power-on and power-down are relative to the supply rails and are given in the specification tables. Below the *Enable Threshold Voltage*, the device is on. Above the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

Figure 62 shows the total system output impedance which includes the amplifier output impedance in parallel with the feedback plus gain resistors, which cumulate to 1870 Ω. Figure 51 shows this circuit configuration for reference.



**Figure 62. Power-Down Output Impedance vs Frequency**

As with most current feedback amplifiers, the internal architecture places some limitations on the system when in power-down mode. Most notably is the fact that the amplifier actually turns *ON* if there is a ±0.7 V or greater difference between the two input nodes ( $V_+$  and  $V_-$ ) of the amplifier. If this difference exceeds ±0.7 V, the output of the amplifier creates an output voltage equal to approximately  $[(V_+ - V_-) - 0.7 \text{ V}] \times \text{Gain}$ . Also, if a voltage is applied to the output while in power-down mode, the  $V_-$  node voltage is equal to  $V_{O(\text{applied})} \times R_G / (R_F + R_G)$ . For low gain configurations and a large applied voltage at the output, the amplifier may actually turn *ON* due to the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach either 10% or 90% of the final output voltage. The time delays are in the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

## POWER-DOWN REFERENCE PIN OPERATION

In addition to the power-down pin, the THS3110 features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the PD pin. In most split-supply applications, the reference pin is connected to ground. In either case, the user needs to be aware of voltage-level thresholds that apply to the power-down pin. The tables below show examples and illustrate the relationship between the reference voltage and the power-down thresholds. In the table, the threshold levels are derived by the following equations:

$$\text{PD} \leq \text{REF} + 0.8 \text{ V for enable}$$

$$\text{PD} \geq \text{REF} + 2.0 \text{ V for disable}$$

where the usable range at the REF pin is

$$V_{S-} \leq V_{\text{REF}} \leq (V_{S+} - 4 \text{ V}).$$

The recommended mode of operation is to tie the REF pin to midrail, thus setting the enable/disable thresholds to  $V_{\text{midrail}} + 0.8 \text{ V}$  and  $V_{\text{midrail}} + 2 \text{ V}$  respectively.

POWER-DOWN THRESHOLD VOLTAGE LEVELS			
SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±15, ±5	0.0	0.8	2.0
±15	2.0	2.8	4
±15	-2.0	-1.2	0
±5	1.0	1.8	3
±5	-1.0	-0.2	1
+30	15	15.8	17
+10	5.0	5.8	7

Note that if the REF pin is left unterminated, it floats to the positive rail and falls outside of the recommended operating range given above ( $V_{S-} \leq V_{\text{REF}} \leq V_{S+} - 4 \text{ V}$ ). As a result, it no longer serves as a reliable reference for the PD pin and the enable/disable thresholds given above no longer apply. If the PD pin is also left unterminated, it also floats to the positive rail and the device is disabled. If balanced, split supplies are used ( $\pm V_S$ ) and the REF and PD pins are grounded, the device is enabled.

## PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with a high-frequency amplifier, such as the THS3110 and THS3111, requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

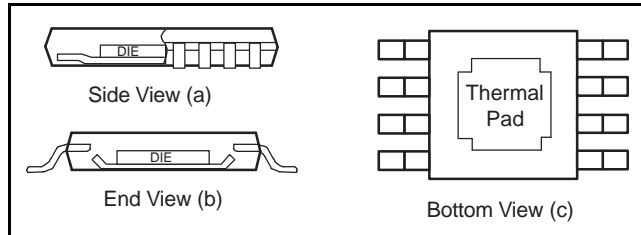
- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance [ $< 0.25$  inch (6,35 mm)] from the power-supply pins to high frequency 0.1- $\mu$ F and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (6.8  $\mu$ F or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
- Careful selection and placement of external components preserve the high-frequency performance of the THS3110 and THS3111. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wirewound-type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 2.0 k $\Omega$ , this parasitic capacitance can add a pole and/or a zero that can affect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces [0.05 inch (1,3 mm) to 0.1 inch (2,54 mm)] should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads ( $< 4$  pF) may not need an  $R_S$  since the THS3110 and THS3111 are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an  $R_S$  are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50- $\Omega$  environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3110/THS3111 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Socketing a high-speed part like the THS3110 and THS3111 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3110/THS3111 parts directly onto the board.

## PowerPAD DESIGN CONSIDERATIONS

The THS3110 and THS3111 are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted (see [Figure 63a](#) and [Figure 63b](#)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see [Figure 63c](#)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that devices such as the THS311x have no electrical connection between the PowerPAD and the die.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

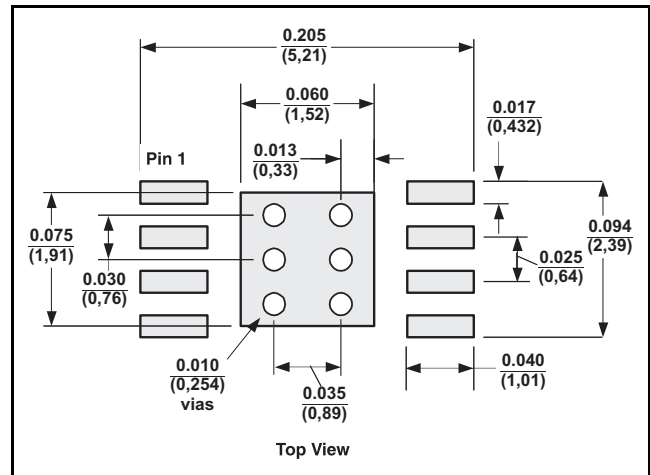


**Figure 63. Views of Thermal Enhanced Package**

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

## PowerPAD LAYOUT CONSIDERATIONS

1. PCB with a top side etch pattern as shown in [Figure 64](#). There should be etch for the leads as well as etch for the thermal pad.



Dimensions are in inches (mm).

**Figure 64. DGN PowerPAD PCB Etch and Via Pattern**

2. Place five holes in the area of the thermal pad. These holes should be 0.01 inch (0,254 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS3110/THS3111 IC. These additional vias may be larger than the 0.01-inch (0,254 mm) diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane. Note that the PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage such as  $V_{S-}$ , is acceptable as there is no electrical connection to the silicon.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3110/THS3111 PowerPAD package should make their connection to the internal ground plane with a complete connection around the

entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

## POWER DISSIPATION AND THERMAL CONSIDERATIONS

The THS3110 and THS3111 incorporate automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately +160°C. When the junction temperature reduces to approximately +140°C, the amplifier turns on again. But, for maximum performance and reliability, the designer must take care to ensure that the design does not exceed a junction temperature of +125°C. Between +125°C and +150°C, damage does not occur, but the performance of the amplifier begins to degrade and long term reliability suffers. The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

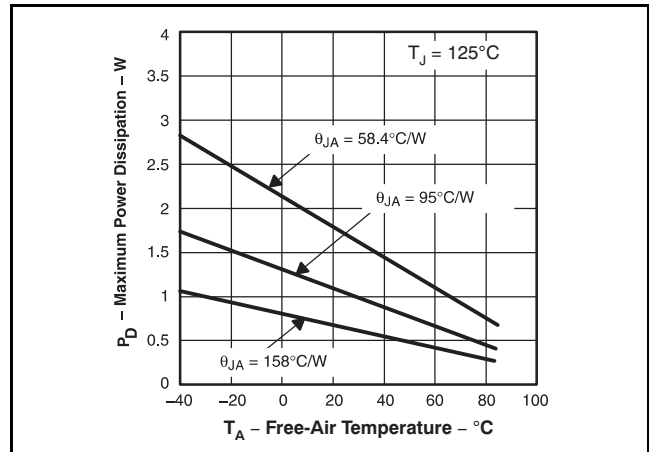
$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}} \quad (1)$$

Where:

- $P_{DMax}$  is the maximum power dissipation in the amplifier (W)
- $T_{Max}$  is the absolute maximum junction temperature (°C)
- $T_A$  is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $\theta_{JC}$  is the thermal coefficient from the silicon junctions to the case (°C/W)
- $\theta_{CA}$  is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the THS3110 and THS3111 are offered in an MSOP-8 with PowerPAD package offering even better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC.

Maximum power dissipation levels are depicted in [Figure 65](#) for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note (literature number [SLMA002](#)). [Figure 65](#) also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are with no airflow and PCB size = 3 in x 3 in (7,62 mm x 7,62 mm);  $\theta_{JA} = 58.4^\circ\text{C/W}$  for MSOP-8 with PowerPAD (DGN);  $\theta_{JA} = 95^\circ\text{C/W}$  for SOIC-8 High-K Test PCB (D);  $\theta_{JA} = 158^\circ\text{C/W}$  for MSOP-8 with PowerPAD, without solder.

**Figure 65. Maximum Power Distribution vs Ambient Temperature**

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

## DESIGN TOOLS

### Evaluation Fixtures, Spice Models, and Application Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal an evaluation board has been developed for the THS3110 and THS3111 operational amplifiers. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments web site, [www.ti.com](http://www.ti.com), or through your local Texas Instruments sales representative.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS3111 is available through the Texas Instruments web site ([www.ti.com](http://www.ti.com)). The product information center (PIC) is also available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

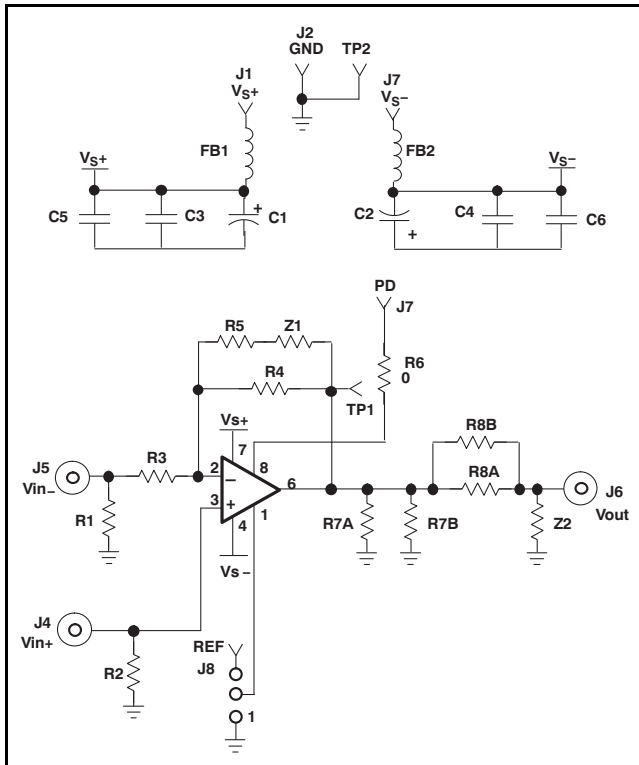


Figure 66. THS3110 EVM Circuit Configuration

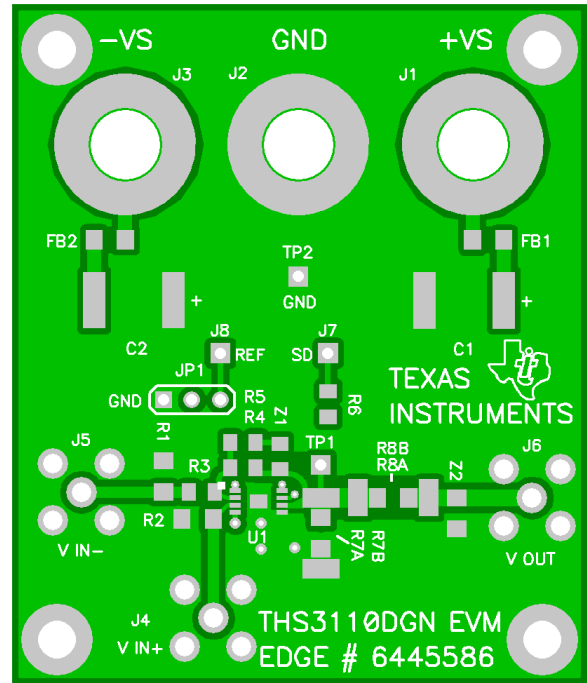


Figure 67. THS3110 EVM Board Layout (Top Layer)

NOTE: The Edge number for the THS3111 is 6445587.

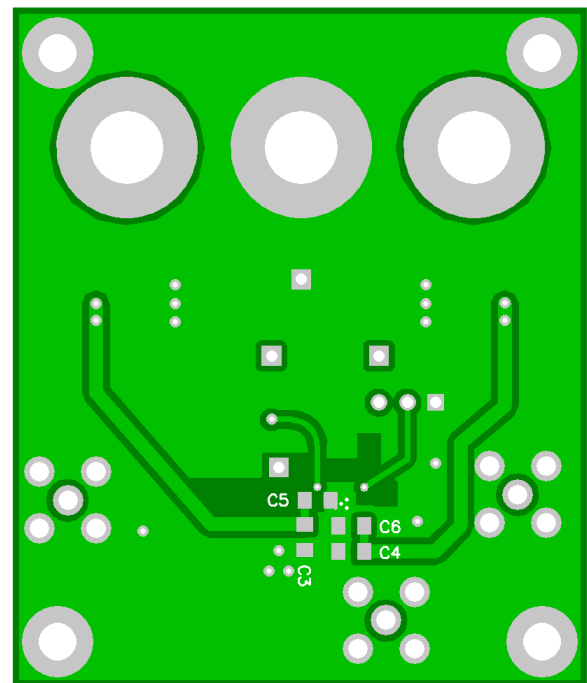


Figure 68. THS3110 EVM Board Layout (Bottom Layer)

**Table 2. Bill of Materials**

THS3110DGN and THS3111DGN EVM					
ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER <sup>(1)</sup>
1	Bead, ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00
2	Capacitor 6.8 μF, tantalum, 35 V, 10%	D	C1, C2	2	(AVX) TAJD685K035R
3	Open	0805	R5, Z1	2	
4	Capacitor 0.1 μF, ceramic, X7R, 50 V	0805	C3, C4	2	(AVX) 08055C104KAT2A
5	Capacitor 100 pF, ceramic, NPO, 100 V	0805	C5, C6	2	(AVX) 08051A101JAT2A
6	Resistor, 0 Ω, 1/8 W, 1%	0805	R6 <sup>(2)</sup>	1	(Phycomp) 9C08052A0R00JLHFT
7	Resistor, 750 Ω, 1/8 W, 1%	0805	R3, R4	2	(Phycomp) 9C08052A7500FKHFT
8	Open	1206	R7A, Z2	2	
9	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R2, R8A	2	(Phycomp) 9C12063A49R9FKRFT
10	Resistor, 53.6 Ω, 1/4 W, 1%	1206	R1	1	(Phycomp) 9C12063A53R6FKRFT
11	Open	2512	R7B, R8B	2	
12	Header, 0.1" (2.54 mm) CTRS, 0.025" (6.35 mm) SQ pins	3 Pos.	JP1 <sup>(2)</sup>	1	(Sullins) PZC36SAAN
13	Shunts		JP1 <sup>(2)</sup>	1	(Sullins) SSC02SYAN
14	Jack, banana receptance, 0.25" (6.35 mm) dia. hole		J1, J2, J3	3	(SPC) 813
15	Test point, red		J7 <sup>(2)</sup> , J8 <sup>(2)</sup> , TP1	3	(Keystone) 5000
16	Test point, black		TP2	1	(Keystone) 5001
17	Connector, SMA PCB jack		J4, J5, J6	3	(Amphenol) 901-144-8RFX
18	Standoff, 4-40 hex, 0.625" (15.875 mm) length			4	(Keystone) 1808
19	Screw, Phillips, 4-40, 0.250" (6.35 mm)			4	SHR-0440-016-SN
20	IC, THS3110		U1	1	(TI) THS3110DGN
21	Board, printed-circuit (THS3110)			1	(TI) EDGE # 6445586
22	IC, THS3111		U1	1	(TI) THS3111DGN
23	Board, printed-circuit (THS3111)			1	(TI) EDGE # 6445587

(1) Manufacturer part numbers are used for test purposes only.

(2) Applies to the THS3110DGN EVM only.

### ADDITIONAL REFERENCE MATERIAL

- PowerPAD Made Easy, application brief ([SLMA004](#))
- PowerPAD Thermally-Enhanced Package, technical brief ([SLMA002](#))
- Voltage Feedback vs Current Feedback Amplifiers, ([SLVA051](#))
- Current Feedback Analysis and Compensation ([SLOA021](#))
- Current Feedback Amplifiers: Review, Stability, and Application ([SBOA081](#))
- Effect of Parasitic Capacitance in Op Amp Circuits ([SLOA013](#))
- Expanding the Usability of Current-Feedback Amplifiers, by Randy Stephens, 3Q 2003 Analog Applications Journal [www.ti.com/sc/analogapps](http://www.ti.com/sc/analogapps)).

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (May 2008) to Revision E</b>	<b>Page</b>
• Changed Power-Down Characteristics, <i>Power-down quiescent current</i> test conditions of $V_S = \pm 15$ V Electrical Characteristics .....	5
• Changed Power-Down Characteristics, <i>PD pin bias current</i> parameter of $V_S = \pm 15$ V Electrical Characteristics .....	5
• Changed Power-Down Characteristics, <i>Power-down quiescent current</i> test conditions of $V_S = \pm 5$ V Electrical Characteristics .....	7
• Changed Power-Down Characteristics, <i>PD pin bias current</i> parameter of $V_S = \pm 5$ V Electrical Characteristics .....	7
• Added caption title to Figure 56 .....	18
• Added caption title to Figure 57 .....	18
• Added caption title to Figure 58 .....	18
• Added caption title to Figure 59 .....	19
• Added caption title to Figure 60 .....	19
• Changed the first sentence of the second paragraph of <i>Saving Power with Power-Down Functionality</i> section .....	19

<b>Changes from Revision C (February, 2007) to Revision D</b>	<b>Page</b>
• Changed $V_S = \pm 15$ V <i>Transimpedance</i> specifications from 1.5 M $\Omega$ (typ) to 1 M $\Omega$ (typ); 1 M $\Omega$ (at +25°C) to 0.75 M $\Omega$ ; 0.7 M $\Omega$ (over temperature) to 0.5 M $\Omega$ .....	4
• Changed $V_S = \pm 15$ V <i>Input offset voltage</i> specifications from 1.5 mV (typ) to 3 mV (typ); 6 mV (at +25°C) to 10 mV; 8 mV (over temperature) to 12 mV .....	4
• Changed $V_S = \pm 15$ V <i>+PSRR</i> specifications from 83 dB to 75 dB (typ); from 75 dB to 65 dB (at +25°C); from 70 dB (over temperature) to 60 dB .....	5
• Changed $V_S = \pm 15$ V <i>-PSRR</i> specifications from 78 dB to 69 dB (typ); from 70 dB to 60 dB (at +25°C); from 66 dB (over temperature) to 55 dB .....	5
• Changed $V_S = \pm 5$ V <i>Transimpedance</i> specifications from 1.6 M $\Omega$ (typ) to 1 M $\Omega$ (typ); 1 M $\Omega$ (at +25°C) to 0.75 M $\Omega$ ; 0.7 M $\Omega$ (over temperature) to 0.5 M $\Omega$ .....	6
• Changed $V_S = \pm 5$ V <i>Input offset voltage</i> specifications from 3 mV (typ) to 6 mV (typ); 6 mV (at +25°C) to 10 mV; 8 mV (over temperature) to 12 mV .....	6
• Changed $V_S = \pm 5$ V <i>+PSRR</i> specifications from 80 dB to 71 dB (typ); from 72 dB to 62 dB (at +25°C); from 67 dB (over temperature) to 57 dB .....	7
• Changed $V_S = \pm 5$ V <i>-PSRR</i> specifications from 75 dB to 66 dB (typ); from 67 dB to 57 dB (at +25°C); from 62 dB (over temperature) to 52 dB .....	7
• Corrected Typical Characteristic figure numbering errors from previous version .....	9
• Updated $\pm 15$ V <i>Transimpedance vs Frequency</i> characteristic graph .....	11

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3110ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3110I	<a href="#">Samples</a>
THS3110IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BIR	<a href="#">Samples</a>
THS3110IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BIR	<a href="#">Samples</a>
THS3110IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3110I	<a href="#">Samples</a>
THS3111CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3111C	<a href="#">Samples</a>
THS3111ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3111I	<a href="#">Samples</a>
THS3111IDG4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
THS3111IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BIS	<a href="#">Samples</a>
THS3111IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BIS	<a href="#">Samples</a>
THS3111IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3111I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3110IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3110IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3110IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3111IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3111IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3111IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3110IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS3110IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS3110IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS3111IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS3111IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS3111IDR	SOIC	D	8	2500	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
THS3110ID	D	SOIC	8	75	505.46	6.76	3810	4
THS3110IDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS3111CD	D	SOIC	8	75	505.46	6.76	3810	4
THS3111ID	D	SOIC	8	75	505.46	6.76	3810	4
THS3111IDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88

## GENERIC PACKAGE VIEW

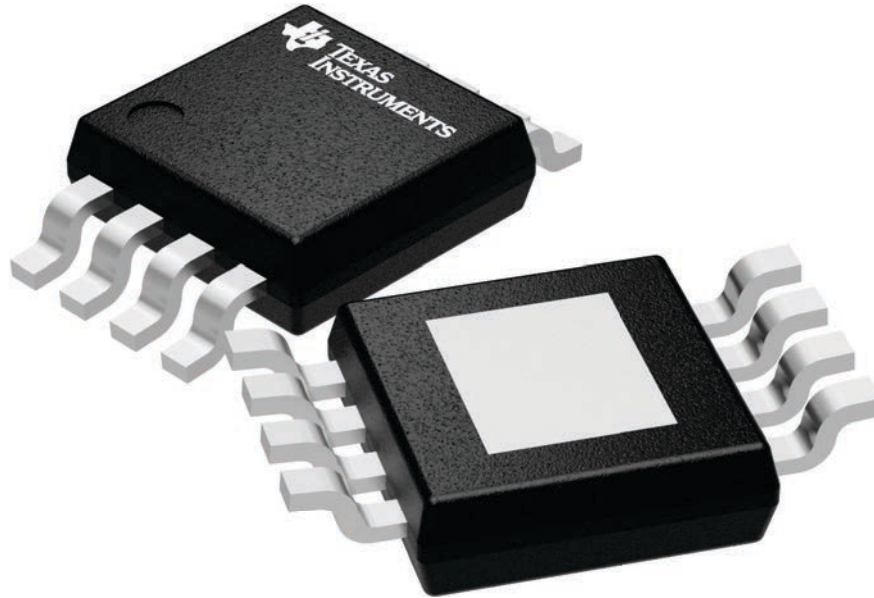
**DGN 8**

**PowerPAD VSSOP - 1.1 mm max height**

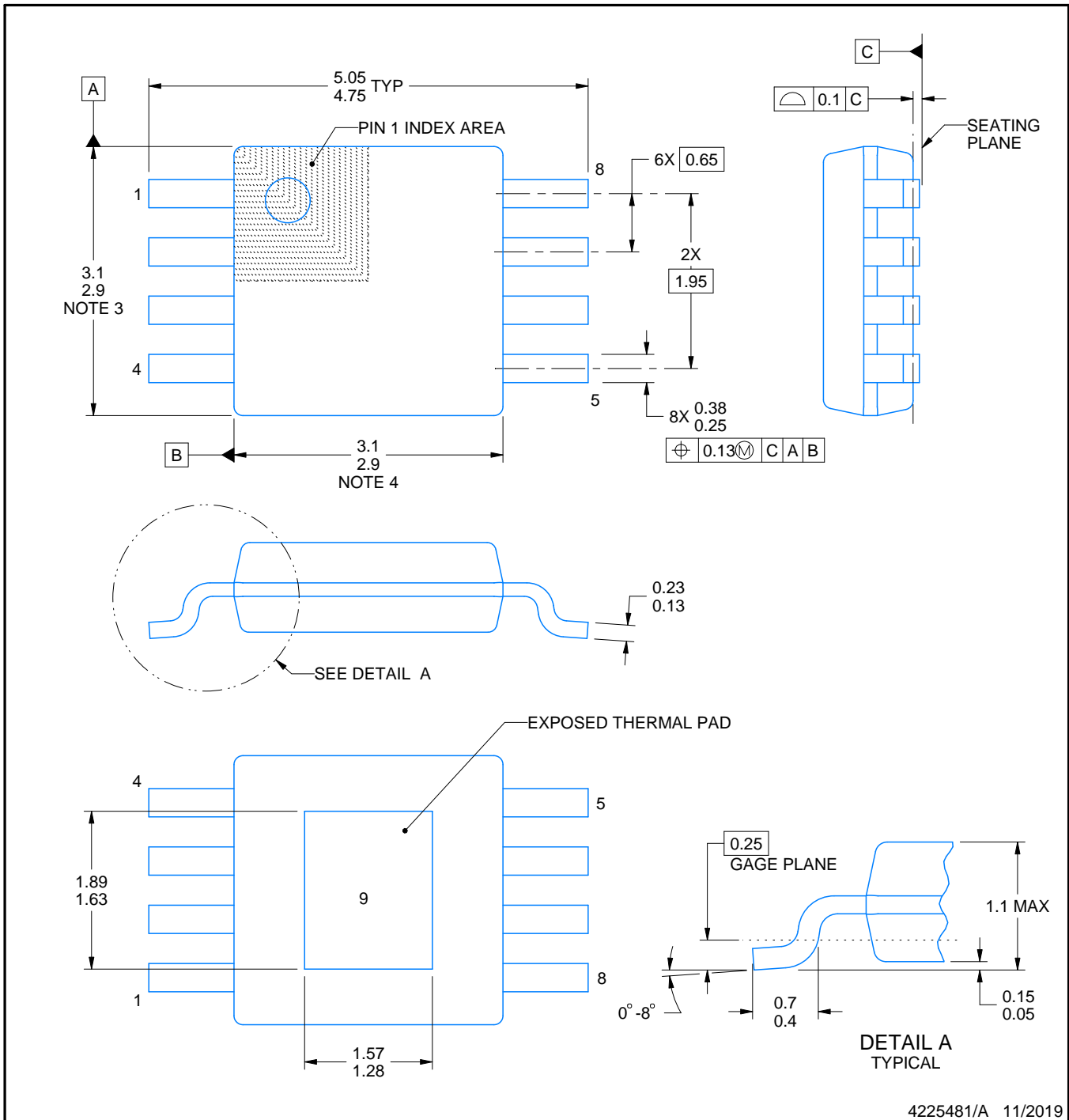
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/A



4225481/A 11/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

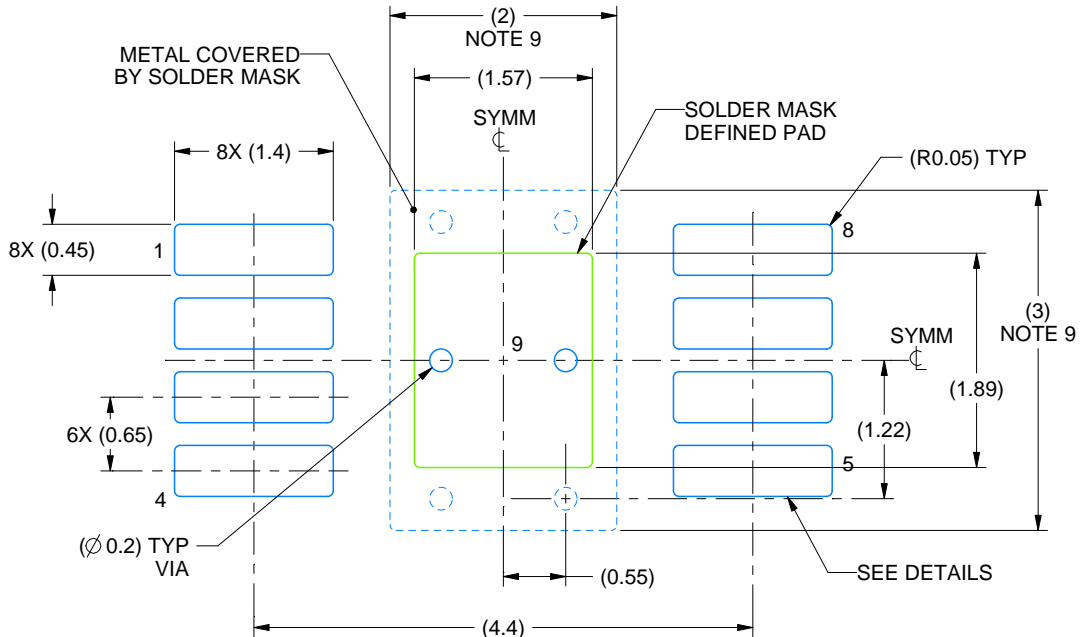
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

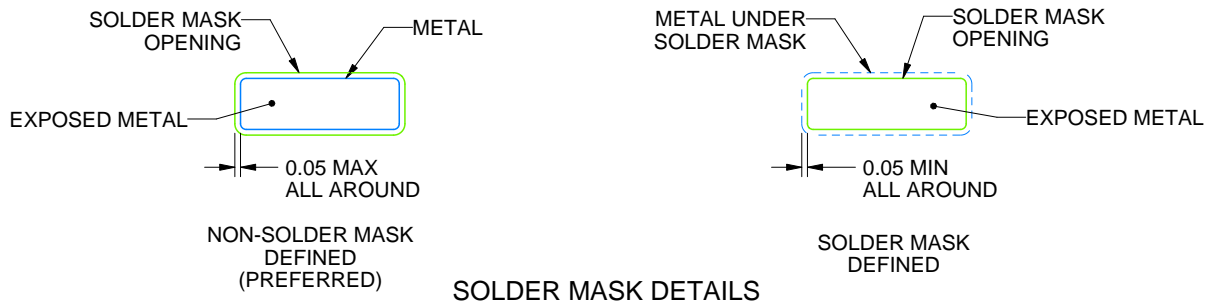
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4225481/A 11/2019

NOTES: (continued)

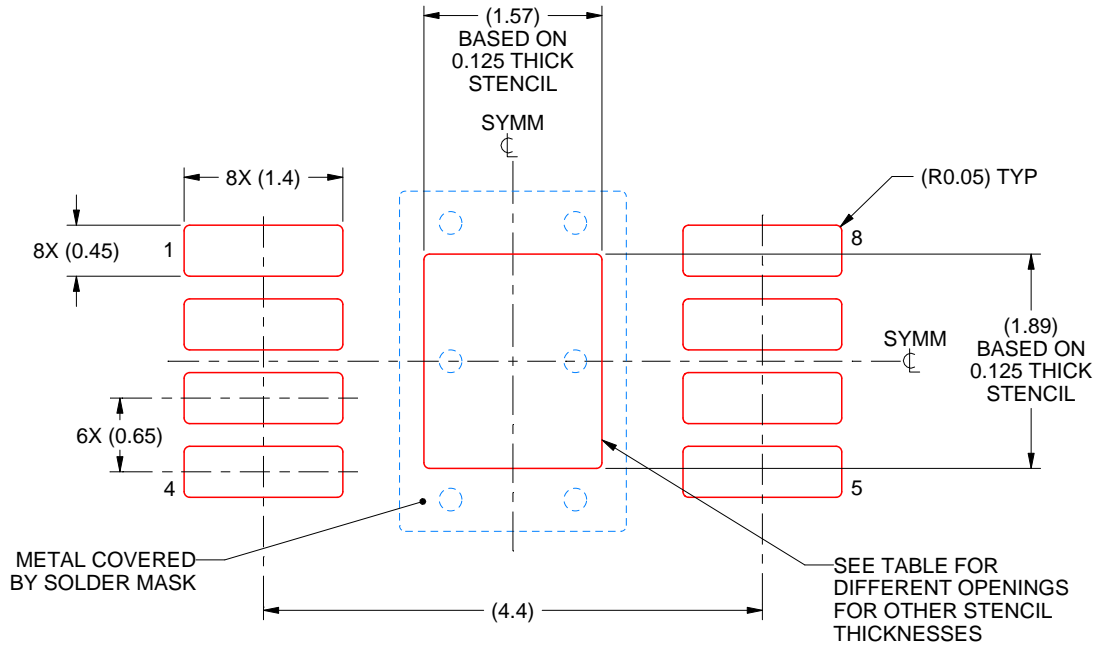
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



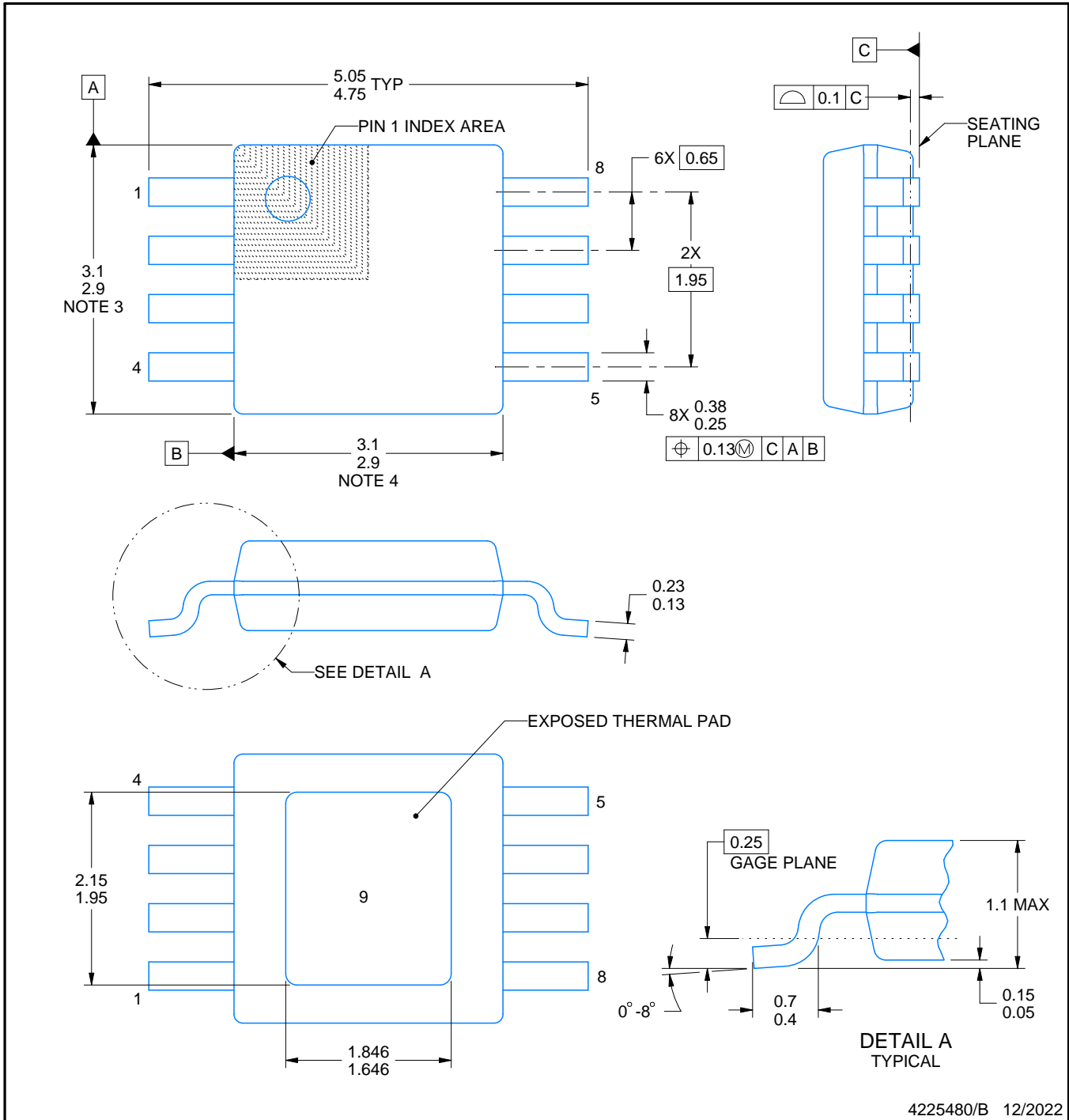
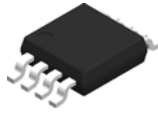
**SOLDER PASTE EXAMPLE**  
EXPOSED PAD 9:  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



4225480/B 12/2022

NOTES:

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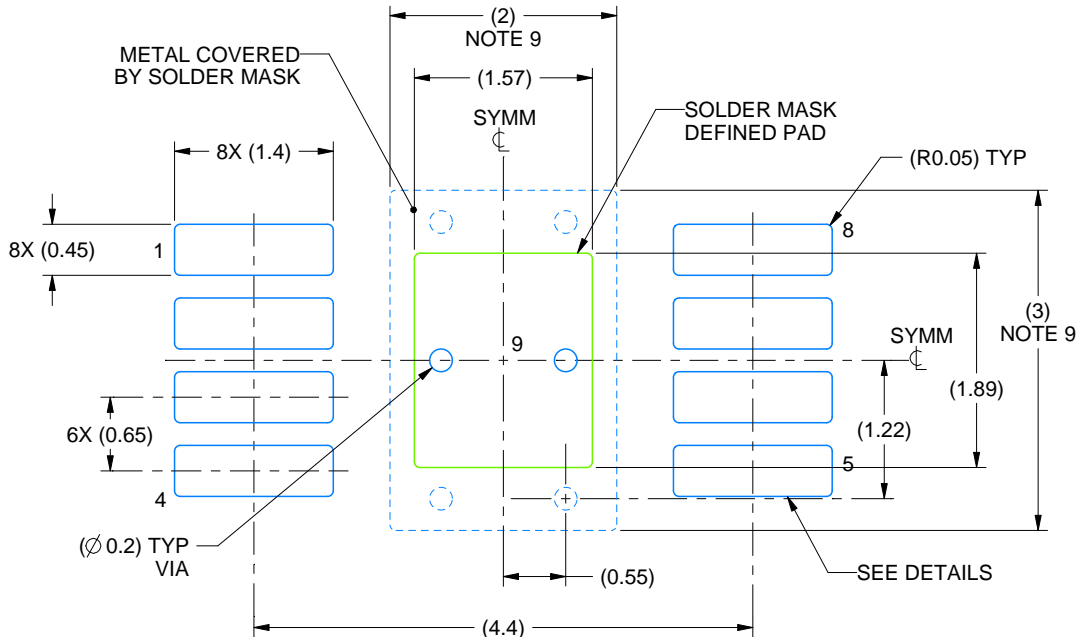
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

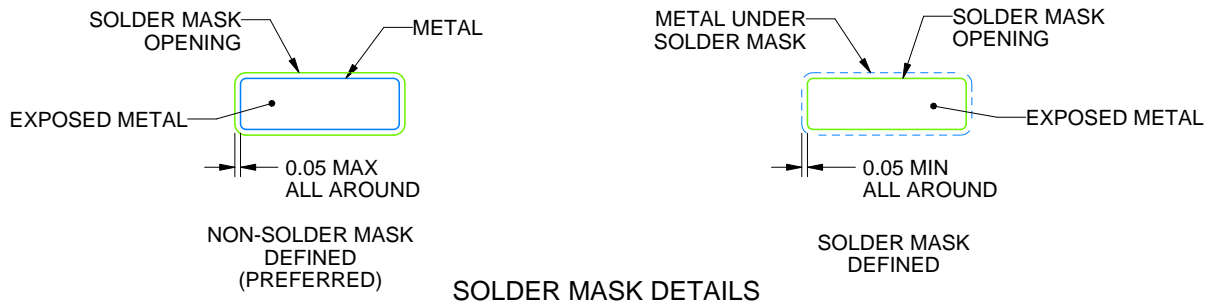
DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

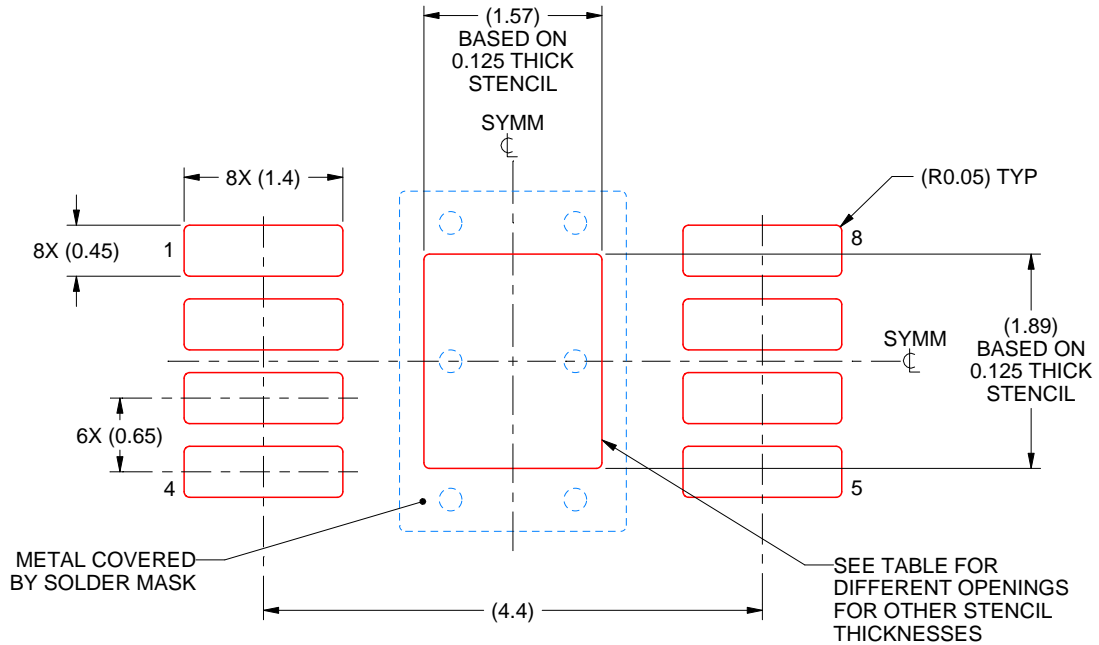
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 EXPOSED PAD 9:  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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