



**THE DATASHEET OF  
TPS3306-25D**



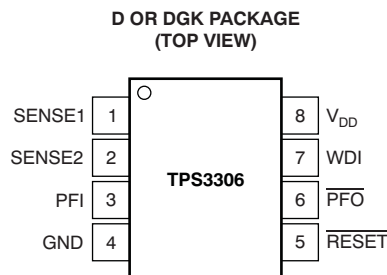
## DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL

### FEATURES

- Dual Supervisory Circuits With Power-Fail for DSP and Processor-Based Systems
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Watchdog Timer With 0.8 Second Time-Out
- Power-On Reset Generator With Integrated 100 ms Delay Time
- Open-Drain Reset and Power-Fail Output
- Supply Current of 15  $\mu$ A (Typ.)
- Supply Voltage Range: 7 V to 6 V
- Defined  $\overline{\text{RESET}}$  Output From  $V_{\text{DD}} \geq 1.1$  V
- MSOP-8 and SO-8 Packages
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### APPLICATIONS

- Multivoltage DSPs and Processors
- Portable Battery-Powered Equipment
- Embedded Control Systems
- Intelligent Instruments
- Automotive Systems

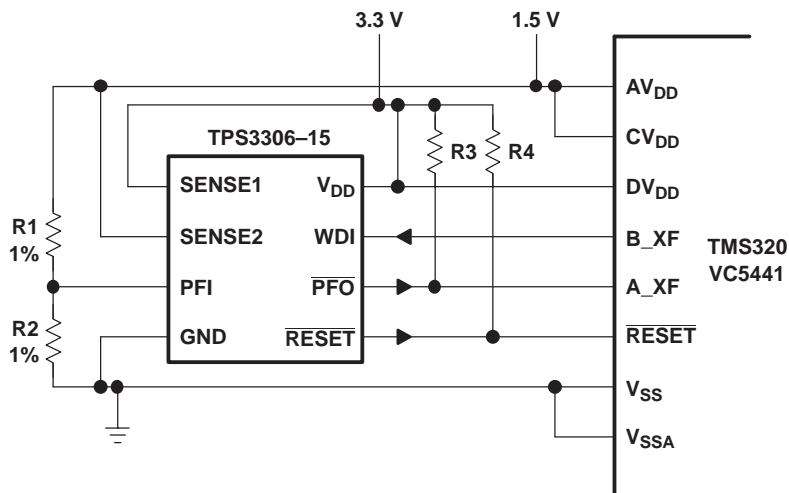


### DESCRIPTION

The TPS3306 family is a series of supervisory circuits designed for circuit initialization which require two supply voltages, primarily in DSP and processor-based systems.

The product spectrum of the TPS3306-xx is designed for monitoring two independent supply voltages of 3.3 V/1.5 V, 3.3 V/1.8 V, 3.3 V/2 V, 3.3 V/2.5 V, or 3.3 V/5 V.

TYPICAL OPERATING CIRCUIT



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## AVAILABLE OPTIONS

**Table 1. SUPPLY VOLTAGE MONITORING**

| DEVICE     | NOMINAL SUPERVISED VOLTAGE |        | THRESHOLD VOLTAGE (TYP) |        |
|------------|----------------------------|--------|-------------------------|--------|
|            | SENSE1                     | SENSE2 | SENSE1                  | SENSE2 |
| TPS3306-15 | 3.3 V                      | 1.5 V  | 2.93 V                  | 1.4 V  |
| TPS3306-18 | 3.3 V                      | 1.8 V  | 2.93 V                  | 1.68 V |
| TPS3306-20 | 3.3 V                      | 2 V    | 2.93 V                  | 1.85 V |
| TPS3306-25 | 3.3 V                      | 2.5 V  | 2.93 V                  | 2.25 V |
| TPS3306-33 | 5 V                        | 3.3 V  | 4.55 V                  | 2.93 V |

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## DESCRIPTION (CONTINUED)

The various supervisory circuits are designed to monitor the nominal supply voltage, as shown in the [Supply Voltage Monitoring](#) table.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{\text{DD}}$  becomes higher than 1.1 V. Thereafter, the supervisory circuits monitor the SENSEn inputs and keep  $\overline{\text{RESET}}$  active as long as SENSEn remains below the threshold voltage  $V_{\text{IT}}$ .

An internal timer delays the return of the  $\overline{\text{RESET}}$  output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{\text{d(typ)}} = 100$  ms, starts after SENSE1 and SENSE2 inputs have risen above the threshold voltage  $V_{\text{IT}}$ . When the voltage at SENSE1 or SENSE2 input drops below the threshold voltage  $V_{\text{IT}}$ , the output becomes active (low) again.

The integrated power-fail (PFI) comparator with separate open-drain ( $\overline{\text{PFO}}$ ) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3306-xx devices integrate a watchdog timer that is periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval,  $t_{\text{t(out)}} = 0.50$  s,  $\overline{\text{RESET}}$  becomes active for the time period  $t_{\text{d}}$ . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3306-xx devices are available in either 8-pin MSOP or standard 8-pin SO packages, and are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

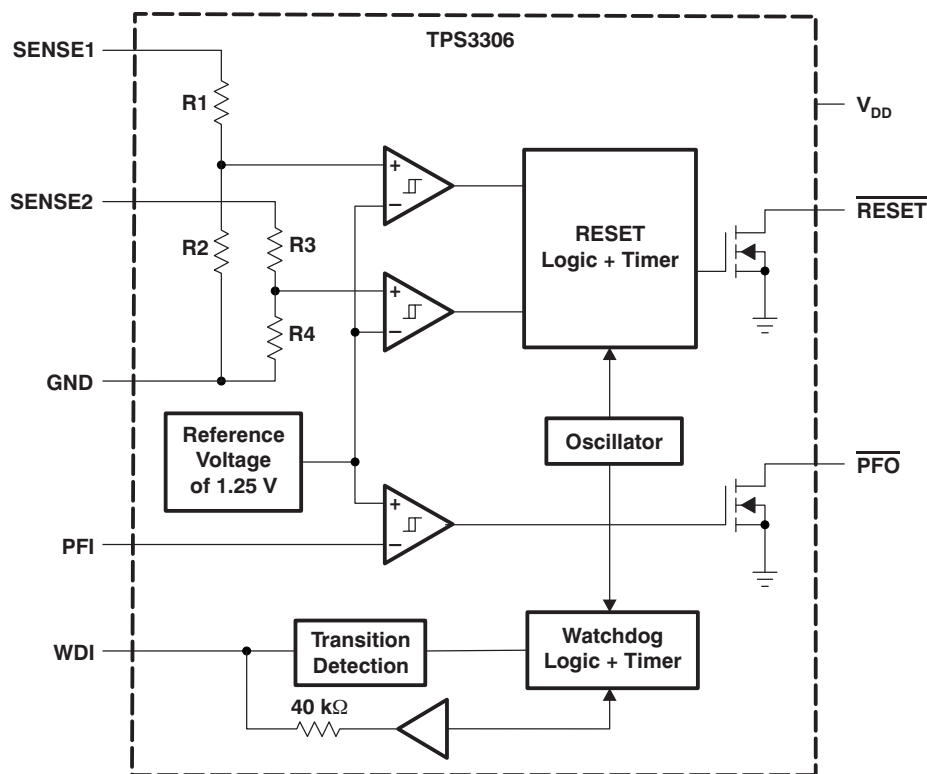
### FUNCTION/TRUTH TABLES

| SENSE1 > V <sub>IT1</sub> | SENSE2 > V <sub>IT2</sub> | RESET |
|---------------------------|---------------------------|-------|
| 0                         | 0                         | L     |
| 0                         | 1                         | L     |
| 1                         | 0                         | L     |
| 1                         | 1                         | H     |

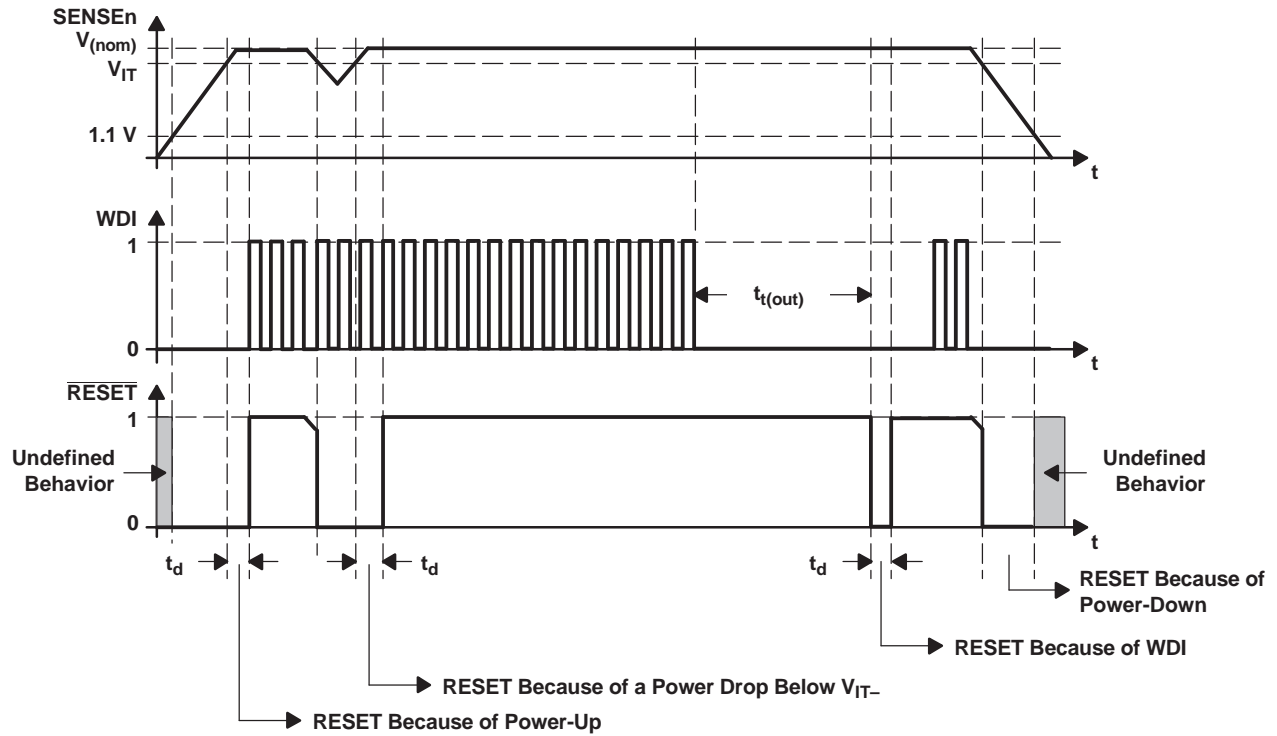
### FUNCTION/TRUTH TABLES

| PFI > V <sub>IT</sub> | PFO |
|-----------------------|-----|
| 0                     | L   |
| 1                     | H   |

### FUNCTIONAL BLOCK DIAGRAM



**TIMING DIAGRAM**



**Table 4. Terminal Functions**

| TERMINAL NAME      | NO. | I/O | DESCRIPTION                              |
|--------------------|-----|-----|--|
| GND                | 4   | I   | Ground                                   |
| PFI                | 3   | I   | Power-fail comparator input              |
| $\overline{PFO}$   | 6   | O   | Power-fail comparator output, open-drain |
| $\overline{RESET}$ | 5   | O   | Active-low reset output, open-drain      |
| SENSE1             | 1   | I   | Sense voltage input 1                    |
| SENSE2             | 2   | I   | Sense voltage input 2                    |
| WDI                | 7   | I   | Watchdog timer input                     |
| $V_{DD}$           | 8   | I   | Supply voltage                           |

**DETAILED DESCRIPTION**

**Watchdog**

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP typically has to toggle the watchdog input within 0.8 s to avoid a time-out occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected or tied with a high impedance driver, the watchdog is disabled and will be retriggered internally.

## DETAILED DESCRIPTION (continued)

### Saving Current While Using the Watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the time-out period, a current of  $5\text{ V}/40\text{ k}\Omega = 125\text{ }\mu\text{A}$  can flow into WDI.

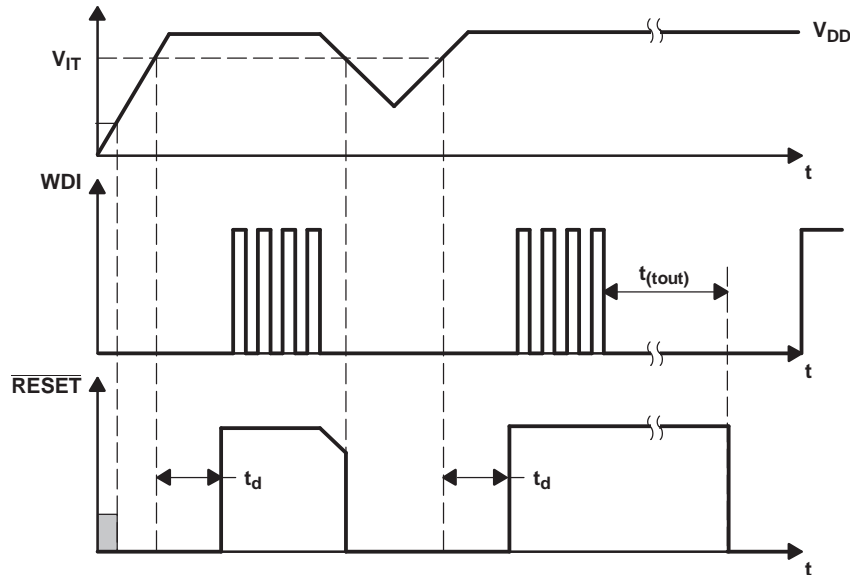
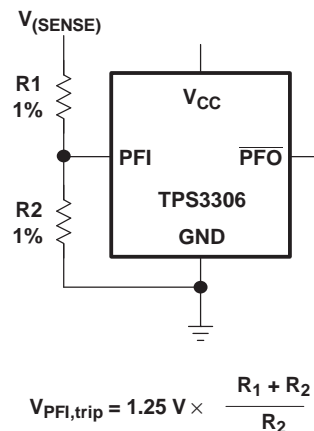


Figure 1. Watchdog Timing

### Power-Fail Comparator (PFI and $\overline{\text{PFO}}$ )

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) will be compared with an internal voltage reference of 1.25 V. If the input voltage falls below the power-fail threshold ( $V_{\text{PFI}}$ ) of typ. 1.25 V, the power-fail output ( $\overline{\text{PFO}}$ ) goes low. If it goes above 1.25 V plus about 10 mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above 1.25 V. The sum of both resistors should be about 1 M $\Omega$ , to minimize power consumption and also to assure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave  $\overline{\text{PFO}}$  unconnected.



$$V_{\text{PFI,trip}} = 1.25\text{ V} \times \frac{R_1 + R_2}{R_2}$$

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).<sup>(1)</sup>

|  | UNIT   |
|--|--|
| Supply voltage, $V_{DD}$ (see <sup>(2)</sup> )                 | 7 V  |
| PFI pin  | -0.3 V to $V_{DD} + 0.3$ V                   |
| All other pins (see <sup>(2)</sup> )                           | -0.3 V to 7 V                                |
| Maximum low output current, $I_{OL}$                           | 5 mA   |
| Maximum high output current, $I_{OH}$                          | -5 mA  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )  | $\pm 20$ mA                                  |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ ) | $\pm 20$ mA                                  |
| Continuous total power dissipation                             | See <a href="#">Dissipation Rating Table</a> |
| Operating free-air temperature range, $T_A$                    | -40°C to +85°C                               |
| Storage temperature range, $T_{stg}$                           | -65°C to +150°C                              |
| Soldering temperature  | 260°C  |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than  $t = 1000$  h continuously.

## DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq +25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = +25^\circ\text{C}$ | $T_A = +70^\circ\text{C}$<br>POWER RATING | $T_A = +85^\circ\text{C}$<br>POWER RATING |
|---------|--|--|---|---|
| DGK     | 424 mW                                       | 3.4 mW/°C  | 271 mW                                    | 220 mW                                    |
| D       | 725 mW                                       | 5.8 mW/°C  | 464 mW                                    | 377 mW                                    |

## RECOMMENDED OPERATING CONDITIONS

At specified temperature range.

|   | MIN                 | MAX                           | UNIT |
|---|---------------------|-------------------------------|------|
| Supply voltage, $V_{DD}$                    | 2.7                 | 6                             | V    |
| Input voltage at WDI and PFI, $V_I$         | 0                   | $V_{DD} + 0.3$                | V    |
| Input voltage at SENSE1 and SENSE2, $V_I$   | 0                   | $(V_{DD} + 0.3)V_{IT}/1.25$ V | V    |
| High-level input voltage at WDI, $V_{IH}$   | $0.7 \times V_{DD}$ |                               | V    |
| Low-level input voltage at WDI, $V_{IL}$    |                     | $0.3 \times V_{DD}$           | V    |
| Operating free-air temperature range, $T_A$ | -40                 | +85                           | °C   |

## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

| PARAMETER                                    |   | TEST CONDITIONS  | MIN   | TYP   | MAX                      | UNIT                        |   |     |
|--|---|--|---|---|--------------------------|-----------------------------|---|-----|
| V <sub>OL</sub>                              | Low-level output voltage  | RESET,<br>PFO  | V <sub>DD</sub> = 2.7 V to 6 V, I <sub>OL</sub> = 20 μA         |   | 0.2                      | V                           |   |     |
|  |   |  | V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA                 |   | 0.4                      |                             |   |     |
|  |   |  | V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 3 mA                   |   | 0.4                      |                             |   |     |
| Power-up reset voltage (see <sup>(1)</sup> ) |   | V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 20 μA             |   |   | 0.4                      | V                           |   |     |
| V <sub>IT</sub>                              | Negative-going input threshold voltage<br>(see <sup>(2)</sup> ) | V <sub>SENSE1</sub> ,<br>V <sub>SENSE2</sub>                 | V <sub>DD</sub> = 2.7 V to 6 V<br>T <sub>A</sub> = 0°C to +85°C | 1.37  | 1.40                     | 1.43                        | V   |     |
|  |   |  |   | 1.64  | 1.68                     | 1.72                        |   |     |
|  |   |  |   | 1.81  | 1.85                     | 1.89                        |   |     |
|  |   |  |   | 2.20  | 2.25                     | 2.30                        |   |     |
|  |   |  |   | 2.86  | 2.93                     | 3                           |   |     |
|  |   |  |   | 4.46  | 4.55                     | 4.64                        |   |     |
|  | Negative-going input threshold voltage<br>(see <sup>(2)</sup> ) | PFI  | V <sub>SENSE1</sub> ,<br>V <sub>SENSE2</sub>                    | V <sub>DD</sub> = 2.7 V to 6 V<br>T <sub>A</sub> = -40°C to +85°C | 1.22                     | 1.25                        | 1.28  | V   |
|  |   |  |   |   | 1.37                     | 1.40                        | 1.44  |     |
|  |   |  |   |   | 1.64                     | 1.68                        | 1.73  |     |
|  |   |  |   |   | 1.81                     | 1.85                        | 1.90  |     |
|  |   |  |   |   | 2.20                     | 2.25                        | 2.32  |     |
|  |   |  |   |   | 2.86                     | 2.93                        | 3.02  |     |
| V <sub>hys</sub>                             | Hysteresis  | PFI  | V <sub>IT</sub> = 1.25 V  |   | 10                       | mV                          |   |     |
|  |   |  |   | V <sub>SENSEn</sub>   | V <sub>IT</sub> = 1.40 V |                             | 15  |     |
|  |   |  |   |   | V <sub>IT</sub> = 1.68 V |                             | 15  |     |
|  |   |  |   |   | V <sub>IT</sub> = 1.86 V |                             | 20  |     |
|  |   |  |   |   | V <sub>IT</sub> = 2.25 V |                             | 20  |     |
|  |   |  |   |   | V <sub>IT</sub> = 2.93 V |                             | 30  |     |
|  |   |  |   |   | V <sub>IT</sub> = 4.55 V |                             | 40  |     |
|  |   |  |   |   | I <sub>H(AV)</sub>       |                             | Average high-level input current            | WDI |
| I <sub>L(AV)</sub>                           | Average low-level input current                                 | WDI = 0 V, V <sub>DD</sub> = 6 V, Time<br>average (dc = 12%) | -15   | -20   |                          |                             |   |     |
|  |   |  | I <sub>H</sub>  | High-level input current  | WDI                      | WDI = V <sub>DD</sub> = 6 V | 120   | 170 |
| SENSE1                                       | V <sub>SENSE1</sub> = V <sub>DD</sub> = 6 V                     | 5  |   |   |                          |                             | 8   |     |
|  |   | SENSE2   |   |   |                          |                             | V <sub>SENSE2</sub> = V <sub>DD</sub> = 6 V | 6   |
| I <sub>L</sub>                               | Low-level input current   |  | WDI   | WDI = 0 V, V <sub>DD</sub> = 6 V                                  | -120                     | -170                        |   | μA  |
| I <sub>I</sub>                               | Input current   | PFI  | V <sub>DD</sub> = 6 V, 0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub>   | -25   | 25                       | nA                          |   |     |
| I <sub>DD</sub>                              | Supply current  |  |   | 15  | 40                       | μA                          |   |     |
| C <sub>i</sub>                               | Input capacitance   |  | V <sub>I</sub> = 0 V to V <sub>DD</sub>                         | 10  |                          | pF                          |   |     |

(1) The lowest supply voltage at which RESET becomes active. t<sub>r</sub>, V<sub>DD</sub> ≥ 15 μs/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

## TIMING REQUIREMENTS

at  $V_{DD} = 2.7\text{ V to }6\text{ V}$ ,  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |             | TEST CONDITIONS | MIN   | TYP | MAX | UNIT          |
|-----------|-------------|-----------------|---|-----|-----|---------------|
| $t_w$     | Pulse width | SENSEn          | $V_{\text{SENSEnL}} = V_{IT} - 0.2\text{ V}$ , $V_{\text{SENSEnH}} = V_{IT} + 0.2\text{ V}$ |     | 6   | $\mu\text{s}$ |
|           |             | WDI             | $V_{IH} = 0.7 \times V_{DD}$ , $V_{IL} = 0.3 \times V_{DD}$                                 |     | 100 | ns            |

## SWITCHING CHARACTERISTICS

at  $V_{DD} = 2.7\text{ V to }6\text{ V}$ ,  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER           |   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT          |
|---------------------|---|---|-----|-----|-----|---------------|
| $t_{t(\text{out})}$ | Watchdog time-out                                     | $V_{I(\text{SENSEn})} \geq V_{IT} + 0.2\text{ V}$ ,<br>See <a href="#">Timing Diagram</a> | 0.5 | 0.8 | 1.2 | s             |
| $t_d$               | Delay time  | $V_{I(\text{SENSEn})} \geq V_{IT} + 0.2\text{ V}$ ,<br>See <a href="#">Timing Diagram</a> | 70  | 100 | 140 | ms            |
| $t_{PHL}$           | Propagation (delay) time,<br>high-to-low level output | SENSEn to $\overline{\text{RESET}}$   |     | 1   | 5   | $\mu\text{s}$ |
| $t_{PHL}$           | Propagation (delay) time,<br>high-to-low level output | PFI to $\overline{\text{PFO}}$  |     | 0.5 | 1   | $\mu\text{s}$ |
| $t_{PLH}$           | Propagation (delay) time,<br>low-to-high level output |   |     |     |     |               |

## TYPICAL CHARACTERISTICS

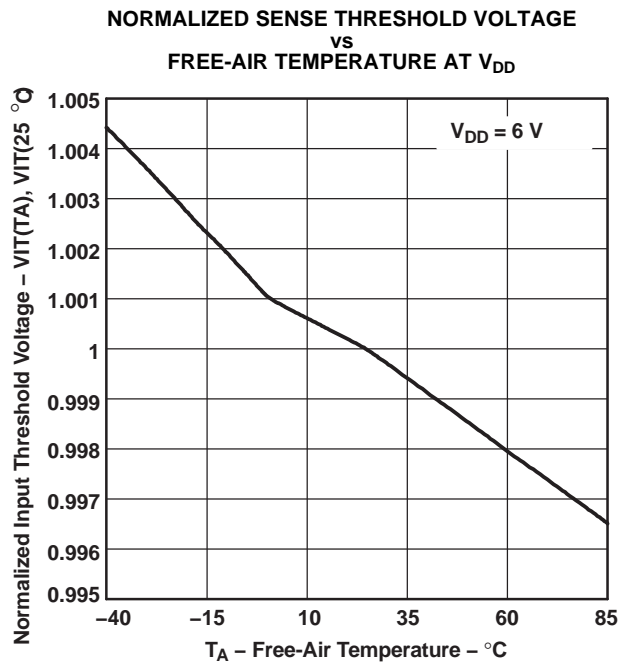


Figure 2.

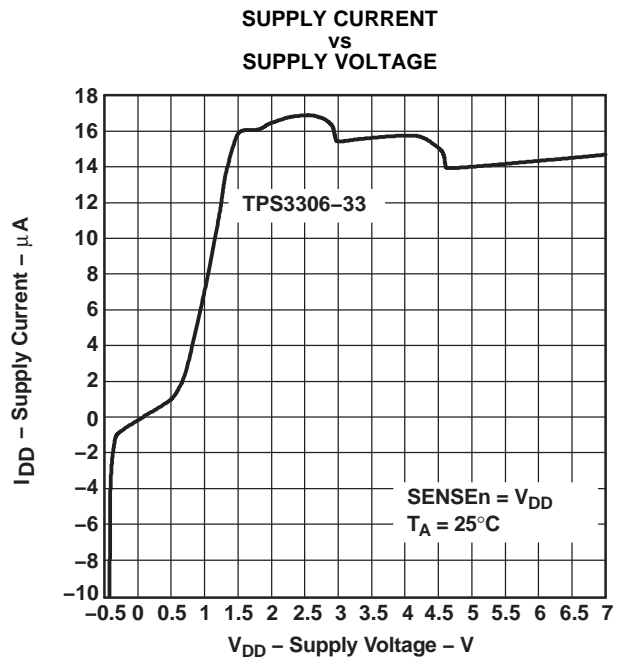


Figure 3.

**TYPICAL CHARACTERISTICS (continued)**

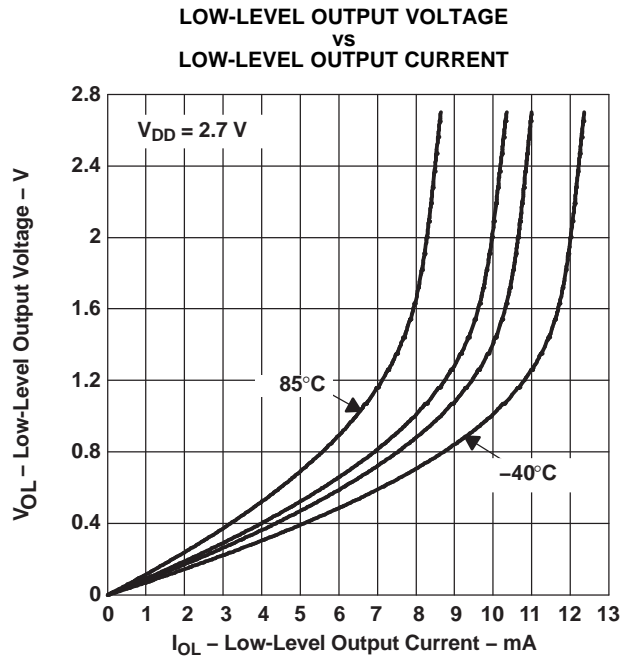


Figure 4.

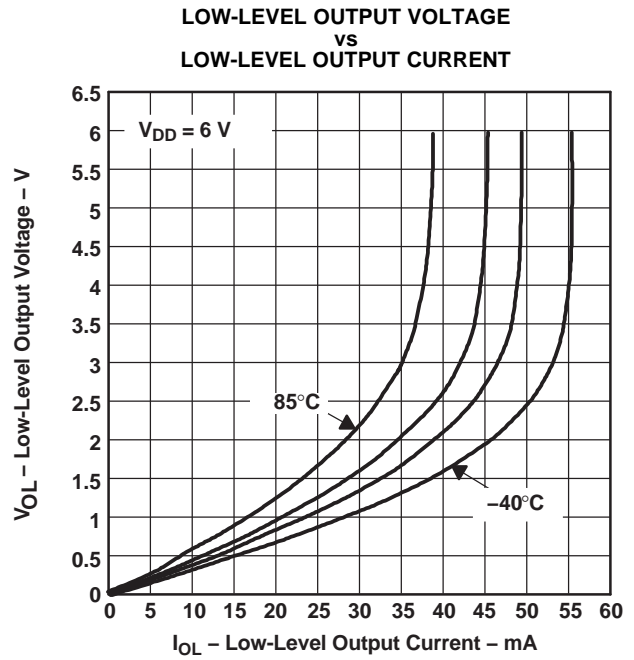


Figure 5.

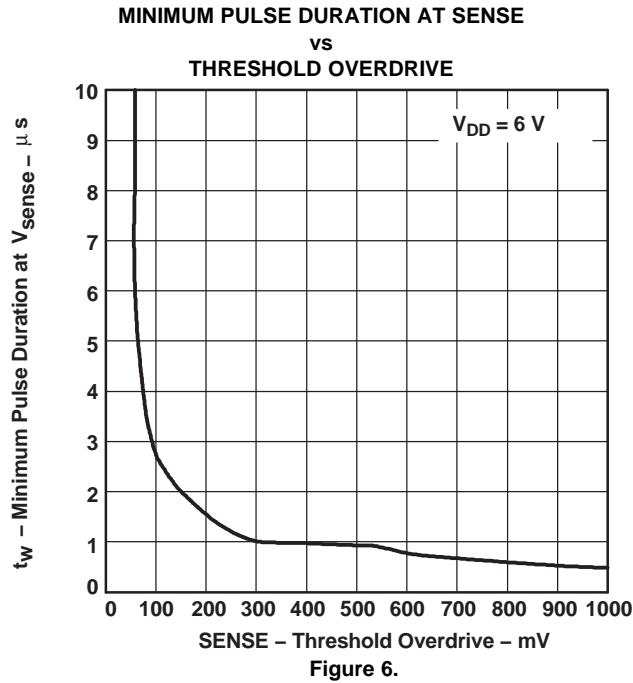


Figure 6.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS3306-15D      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30615                   | <a href="#">Samples</a> |
| TPS3306-15DGK    | ACTIVE        | VSSOP        | DGK             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AIC                     | <a href="#">Samples</a> |
| TPS3306-15DGKR   | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AIC                     | <a href="#">Samples</a> |
| TPS3306-15DR     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30615                   | <a href="#">Samples</a> |
| TPS3306-18D      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30618                   | <a href="#">Samples</a> |
| TPS3306-18DGK    | ACTIVE        | VSSOP        | DGK             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AID                     | <a href="#">Samples</a> |
| TPS3306-18DGKR   | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AID                     | <a href="#">Samples</a> |
| TPS3306-18DR     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30618                   | <a href="#">Samples</a> |
| TPS3306-20D      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30620                   | <a href="#">Samples</a> |
| TPS3306-25D      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30625                   | <a href="#">Samples</a> |
| TPS3306-25DGK    | ACTIVE        | VSSOP        | DGK             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AIF                     | <a href="#">Samples</a> |
| TPS3306-25DGKR   | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AIF                     | <a href="#">Samples</a> |
| TPS3306-25DR     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30625                   | <a href="#">Samples</a> |
| TPS3306-33D      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30633                   | <a href="#">Samples</a> |
| TPS3306-33DGK    | ACTIVE        | VSSOP        | DGK             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AIG                     | <a href="#">Samples</a> |
| TPS3306-33DGKR   | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AIG                     | <a href="#">Samples</a> |
| TPS3306-33DR     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 30633                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS3306 :**

- Automotive : [TPS3306-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS3306-15DGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TPS3306-15DR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS3306-18DGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TPS3306-18DR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS3306-25DGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TPS3306-25DR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS3306-33DGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TPS3306-33DR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS3306-15DGKR | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| TPS3306-15DR   | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| TPS3306-18DGKR | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| TPS3306-18DR   | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| TPS3306-25DGKR | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| TPS3306-25DR   | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| TPS3306-33DGKR | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| TPS3306-33DR   | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |

**TUBE**


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS3306-15D | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TPS3306-18D | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TPS3306-20D | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TPS3306-25D | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| TPS3306-33D | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



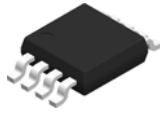
SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

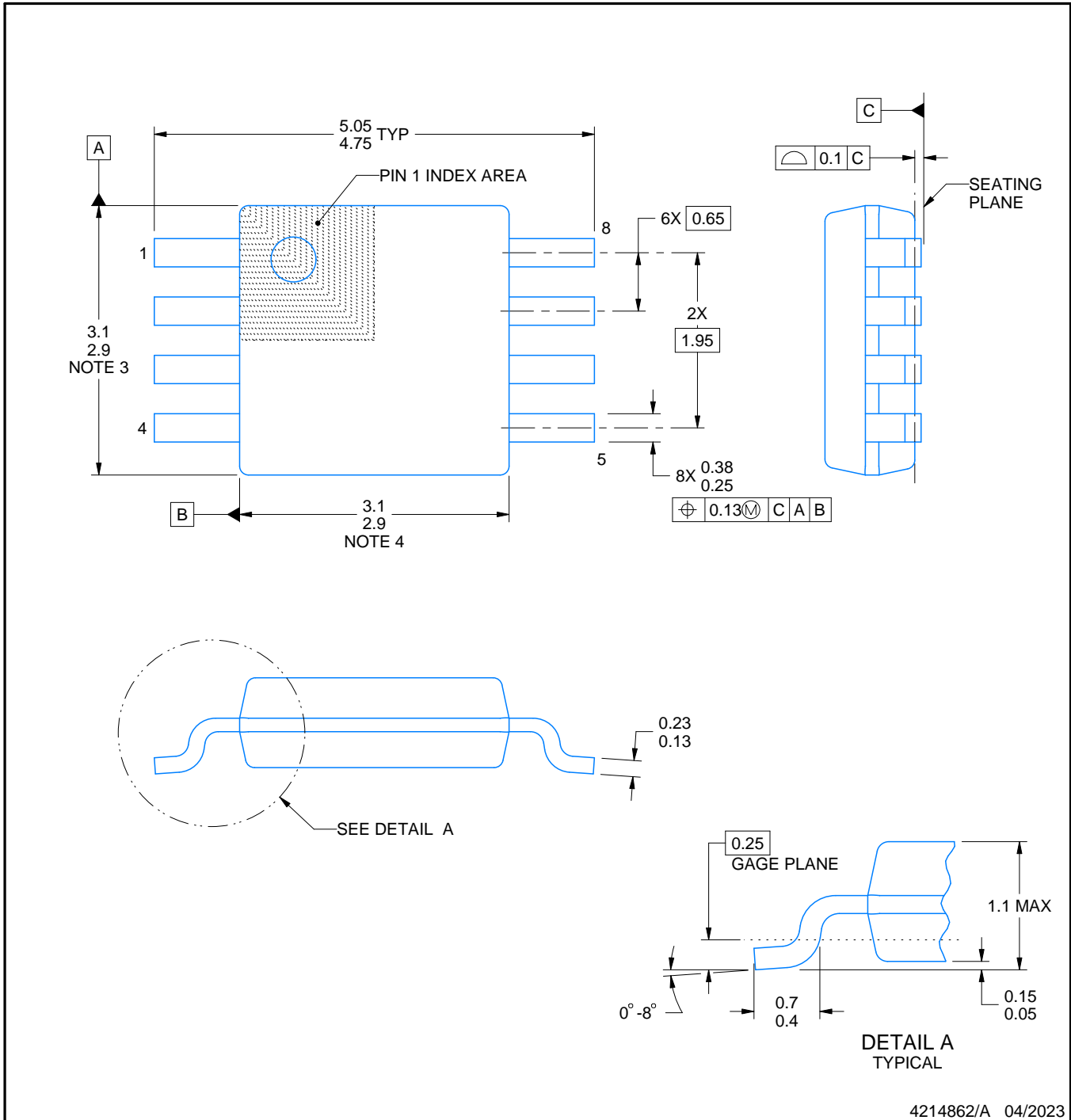
# DGK0008A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

### NOTES:

PowerPAD is a trademark of Texas Instruments.

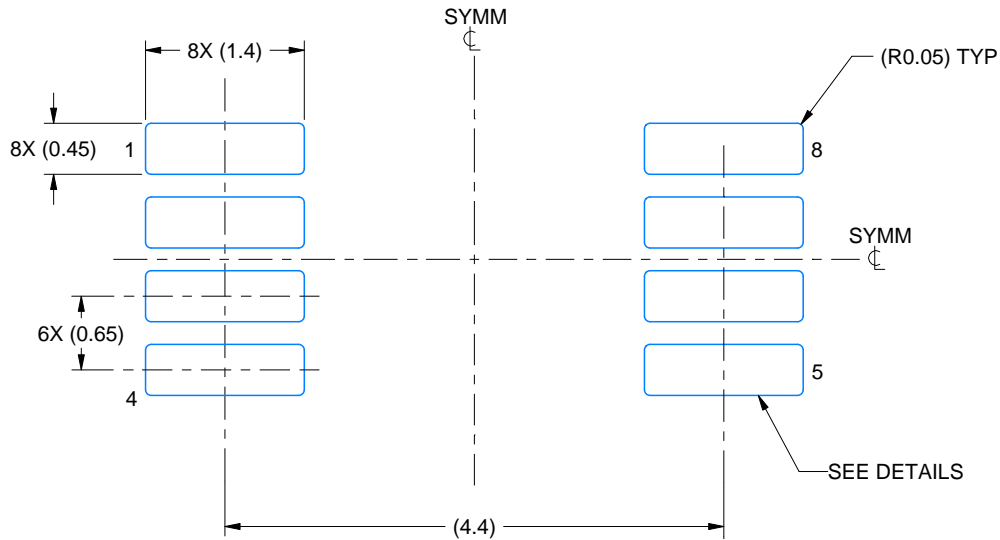
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

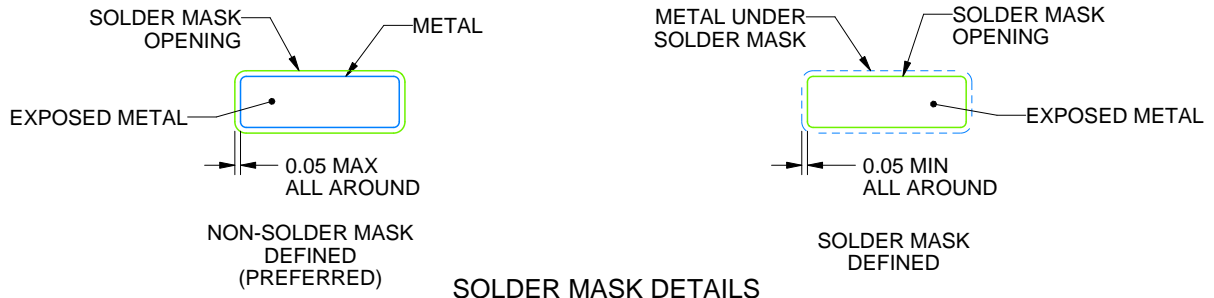
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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