



**THE DATASHEET OF  
DAC7821IPW**





## 12-Bit, Parallel Input, Multiplying Digital-to-Analog Converter

### FEATURES

- 2.5V to 5.5V Supply Operation
- Fast Parallel Interface:  
17ns Write Cycle
- Update Rate of 20.4MSPS
- 10MHz Multiplying Bandwidth
- $\pm 10V$  Reference Input
- Low Glitch Energy: 5nV-s
- Extended Temperature Range:  
 $-40^{\circ}C$  to  $+125^{\circ}C$
- 20-Lead TSSOP Packages
- 12-Bit Monotonic
- $\pm 1LSB$  INL
- 4-Quadrant Multiplication
- Power-On Reset with Brownout Detection
- Readback Function
- Industry-Standard Pin Configuration

### APPLICATIONS

- Portable Battery-Powered Instruments
- Waveform Generators
- Analog Processing
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Calibration
- Programmable Filters and Oscillators
- Composite Video
- Ultrasound

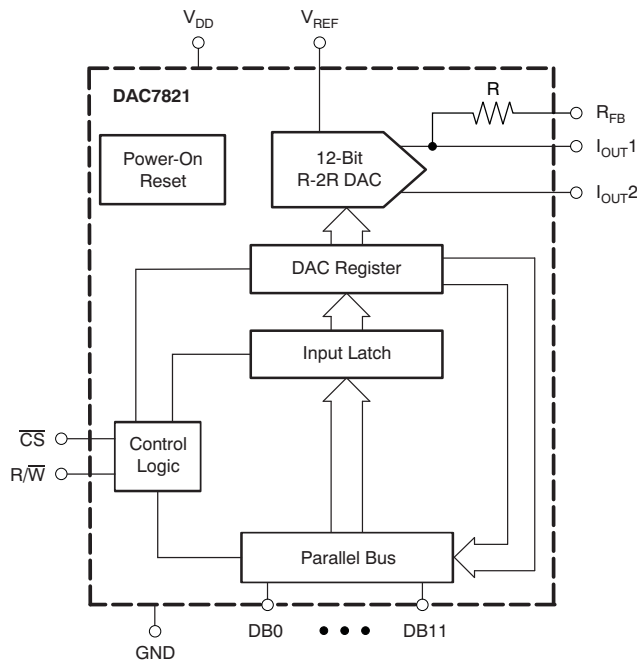
### DESCRIPTION

The DAC7821 is a CMOS 12-bit current output digital-to-analog converter (DAC). This device operates from a single 2.5V to 5.5V power supply, making it suitable for battery-powered and many other applications.

This DAC operates with a fast parallel interface. Data readback allows the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeroes and the DAC outputs are at zero scale.

The DAC7821 offers excellent 4-quadrant multiplication characteristics, with a large signal multiplying bandwidth of 10MHz. The applied external reference input voltage ( $V_{REF}$ ) determines the full-scale output current. An integrated feedback resistor ( $R_{FB}$ ) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier.

The DAC7821 is available in a 20-lead TSSOP package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	DAC7821	UNIT
$V_{DD}$ to GND	–0.3 to +7	V
Digital input voltage to GND	–0.3 to $V_{DD} + 0.3$	V
$V_{(I/O)}$ to GND	–0.3 to $V_{DD} + 0.3$	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature ( $T_J$ max)	+150	°C
ESD Rating, HBM	3000	V
ESD Rating, CDM	1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

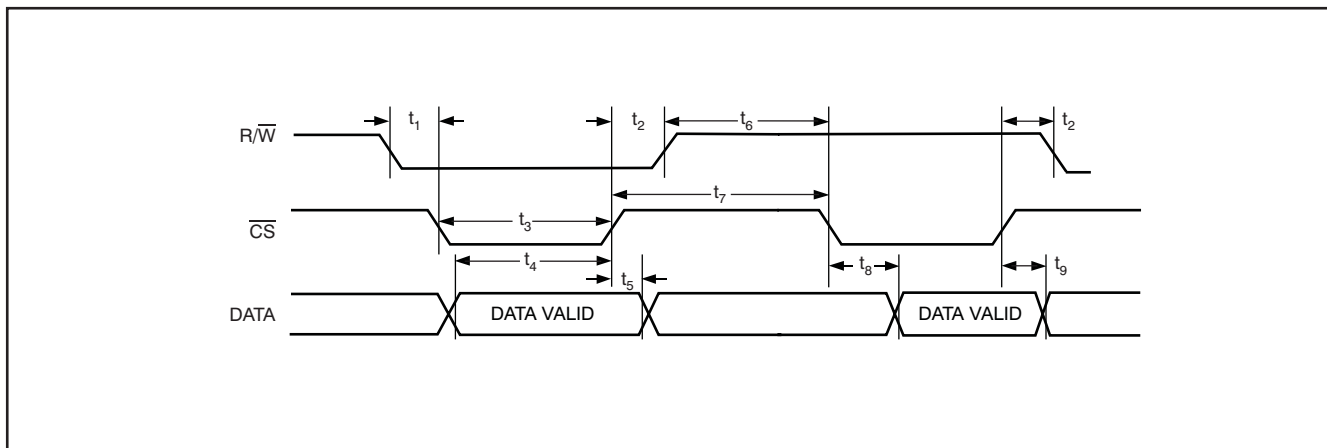
**ELECTRICAL CHARACTERISTICS**

$V_{DD} = +2.5V$  to  $+5.5V$ ;  $I_{OUT1} = \text{Virtual GND}$ ;  $I_{OUT2} = 0V$ ;  $V_{REF} = +10V$ ;  $T_A = \text{full operating temperature}$ . All specifications  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

PARAMETER	CONDITIONS	DAC7821			UNITS
		MIN	TYP	MAX	
<b>STATIC PERFORMANCE</b>					
Resolution		12			Bits
Relative accuracy				$\pm 1$	LSB
Differential nonlinearity				$\pm 1$	LSB
Output leakage current	Data = 000h, $T_A = +25^\circ\text{C}$			$\pm 10$	nA
Output leakage current	Data = 000h, $T_A = T_{MAX}$			$\pm 20$	nA
Full-scale gain error	All is loaded to DAC register		$\pm 5$	$\pm 10$	mV
Full-scale tempco			$\pm 5$		ppm/ $^\circ\text{C}$
Output capacitance	Code dependent		30		pF
<b>REFERENCE INPUT</b>					
$V_{REF}$ range		-15		15	V
Input resistance		8	10	12	k $\Omega$
$R_{FB}$ resistance		8	10	12	k $\Omega$
<b>LOGIC INPUTS AND OUTPUT<sup>(1)</sup></b>					
Input low voltage	$V_{IL}$ $V_{DD} = +2.7V$			0.6	V
	$V_{IL}$ $V_{DD} = +5V$			0.8	V
Input high voltage	$V_{IH}$ $V_{DD} = +2.7V$	2.1			V
	$V_{IH}$ $V_{DD} = +5V$	2.4			V
Input leakage current	$I_{IL}$			10	$\mu\text{A}$
Input capacitance	$C_{IL}$			10	pF
<b>POWER REQUIREMENTS</b>					
$V_{DD}$		2.7		5.5	V
$I_{DD}$ (normal operation)	Logic inputs = 0V			5	$\mu\text{A}$
$V_{DD} = +4.5V$ to $+5.5V$	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$		0.8	5	$\mu\text{A}$
$V_{DD} = +2.5V$ to $+3.6V$	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$		0.4	2.5	$\mu\text{A}$
<b>AC CHARACTERISTICS</b>					
Output voltage settling time				0.2	$\mu\text{s}$
Reference multiplying BW	$V_{REF} = 7V_{PP}$ , Data = FFFh		10		MHz
DAC glitch impulse	$V_{REF} = 0V$ to $10V$ , Data = 7FFh to 800h to 7FFh		5		nV-s
Feedthrough error $V_{OUT}/V_{REF}$	Data = 000h, $V_{REF} = 100\text{kHz}$		-70		dB
Digital feedthrough			2		nV-s
Total harmonic distortion			-105		dB
Output spot noise voltage			18		$\text{nV}/\sqrt{\text{Hz}}$

(1) Specified by design and characterization; not production tested.

TIMING INFORMATION



**TIMING REQUIREMENTS: 2.5 V to 4.5 V**

At  $t_r = t_f = 1\text{ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ ;  $V_{DD} = +2.5\text{V}$  to  $+4.5\text{V}$ ,  $V_{REF} = +10\text{V}$ ,  $I_{OUT2} = 0\text{V}$ . All specifications  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	DAC7821			UNIT
		MIN	TYP	MAX	
$t_1$	$R/\overline{W}$ to $\overline{CS}$ setup time	0			ns
$t_2$	$R/\overline{W}$ to $\overline{CS}$ hold time	0			ns
$t_3$	$\overline{CS}$ low time (write cycle)	10			ns
$t_4$	Data setup time	6			ns
$t_5$	Data hold time	0			ns
$t_6$	$R/\overline{W}$ high to $\overline{CS}$ low	5			ns
$t_7$	$\overline{CS}$ min high time	9			ns
$t_8$	Data access time		20	40	ns
$t_9$	Bus relinquish time		5	10	ns

(1) Ensured by design; not production tested.

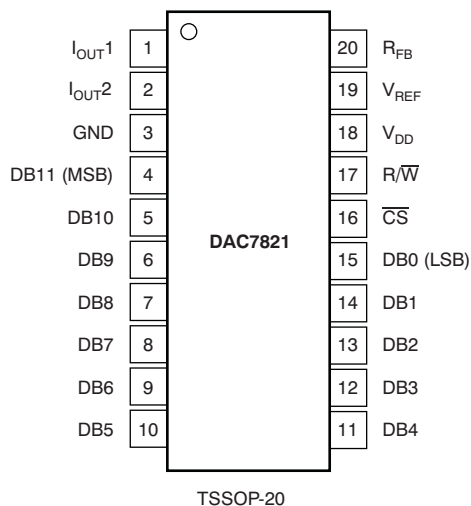
**TIMING REQUIREMENTS: 4.5 V to 5.5 V**

At  $t_r = t_f = 1\text{ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ ;  $V_{DD} = +4.5\text{V}$  to  $+5.5\text{V}$ ,  $V_{REF} = +10\text{V}$ ,  $I_{OUT2} = 0\text{V}$ . All specifications  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	DAC7821			UNIT
		MIN	TYP	MAX	
$t_1$	$R/\overline{W}$ to $\overline{CS}$ setup time	0			ns
$t_2$	$R/\overline{W}$ to $\overline{CS}$ hold time	0			ns
$t_3$	$\overline{CS}$ low time (write cycle)	10			ns
$t_4$	Data setup time	6			ns
$t_5$	Data hold time	0			ns
$t_6$	$R/\overline{W}$ high to $\overline{CS}$ low	5			ns
$t_7$	$\overline{CS}$ min high time	7			ns
$t_8$	Data access time		10	20	ns
$t_9$	Bus relinquish time		5	10	ns

(1) Ensured by design; not production tested.

## DEVICE INFORMATION

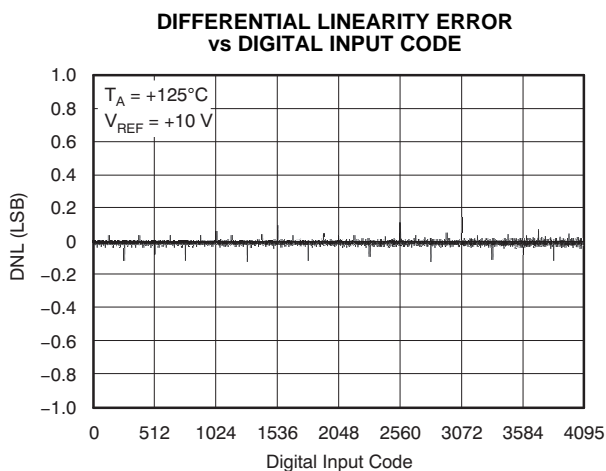
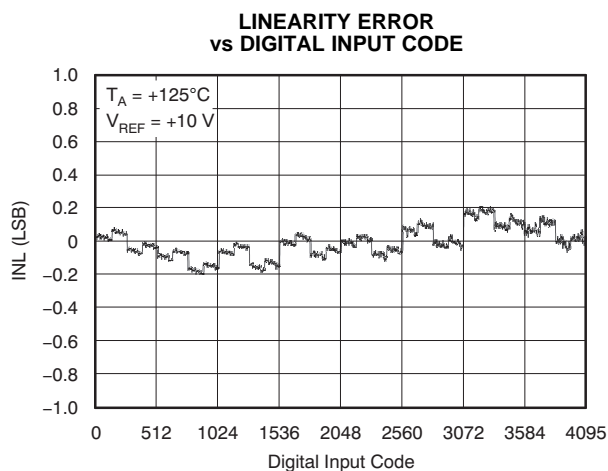
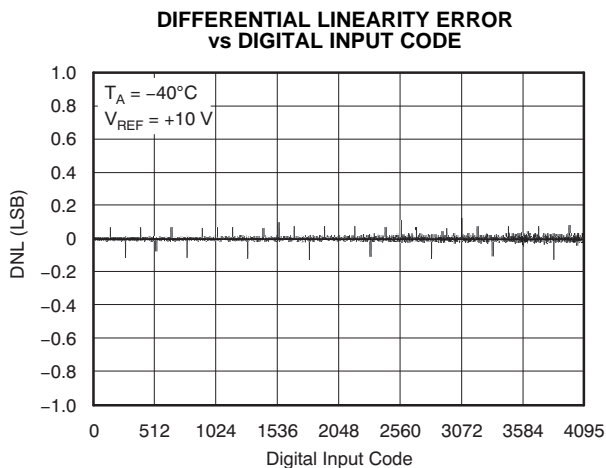
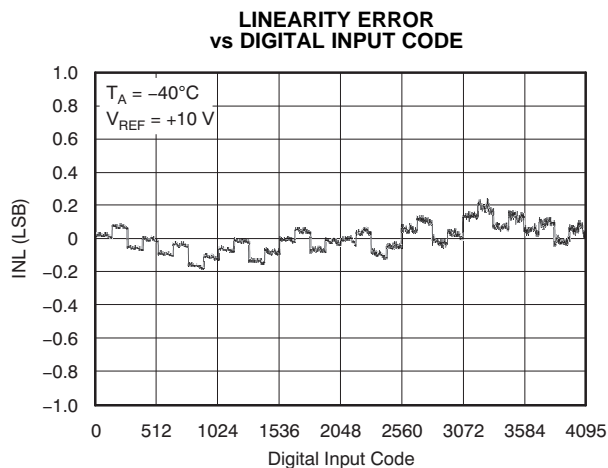
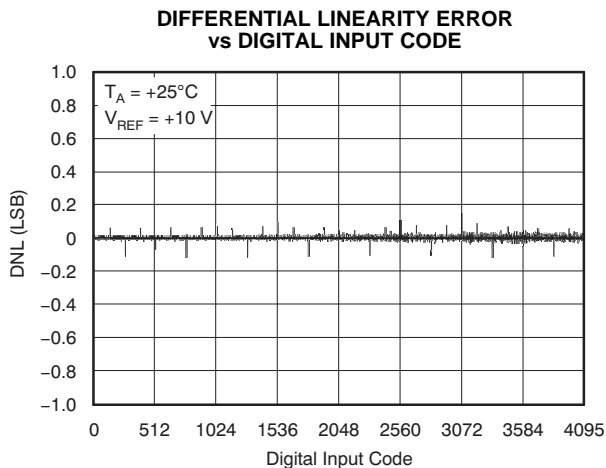
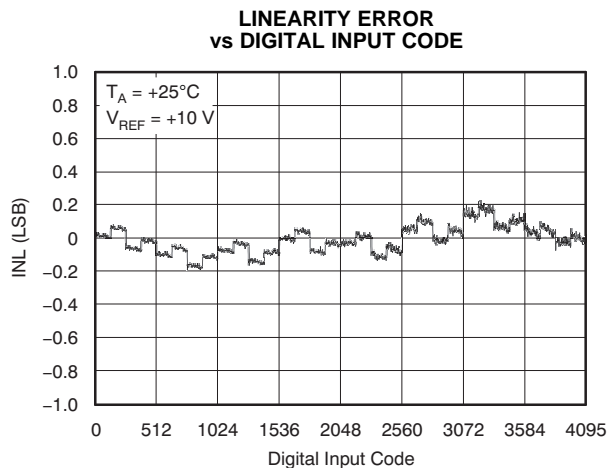


## TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
TSSOP NO.	NAME	
1	$I_{OUT1}$	DAC current output.
2	$I_{OUT2}$	DAC analog ground. This pin is normally tied to the analog ground of the system.
3	GND	Ground pin.
4–15	DB11 – DB0	Parallel data bits 11 to 0.
16	$\overline{CS}$	Chip select input. Active low. Used in conjunction with $R/\overline{W}$ to load parallel data to the input latch or read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
17	$R/\overline{W}$	Read/Write. When low, use in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
18	$V_{DD}$	Positive power supply input. These parts can be operated from a supply of 2.5V to 5.5V.
19	$V_{REF}$	DAC reference voltage input.
20	$R_{FB}$	DAC feedback resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5V$**

At  $T_A = +25^\circ C$ , unless otherwise noted.



TYPICAL CHARACTERISTICS:  $V_{DD} = +5V$  (continued)

At  $T_A = +25^\circ C$ , unless otherwise noted.

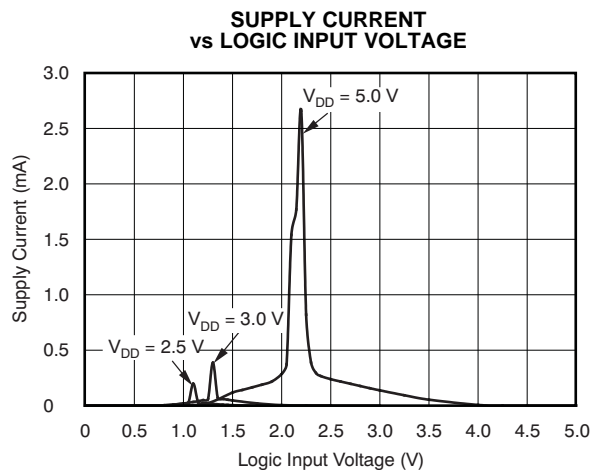


Figure 7.

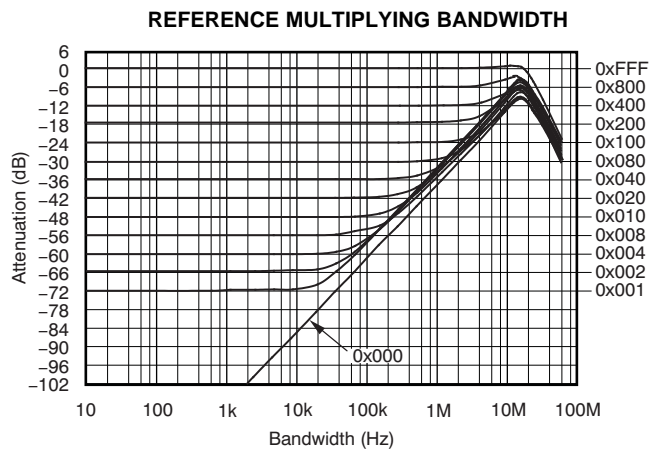


Figure 8.

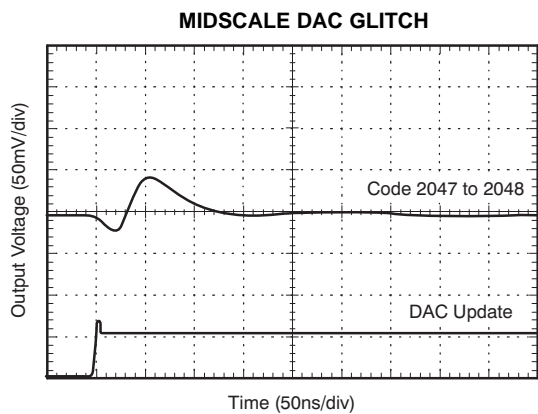


Figure 9.

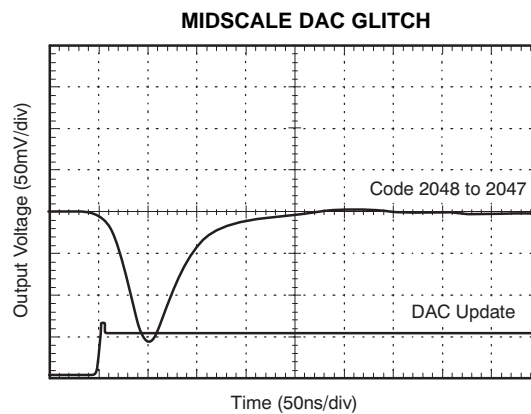


Figure 10.

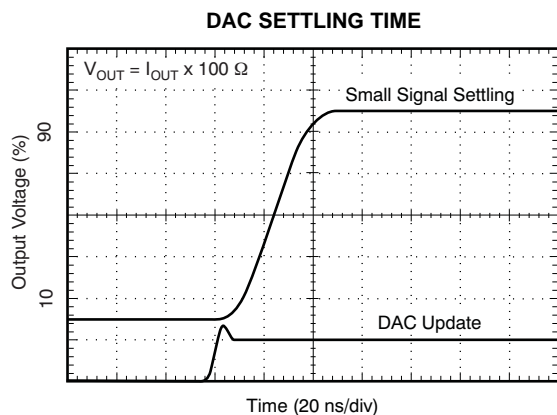


Figure 11.

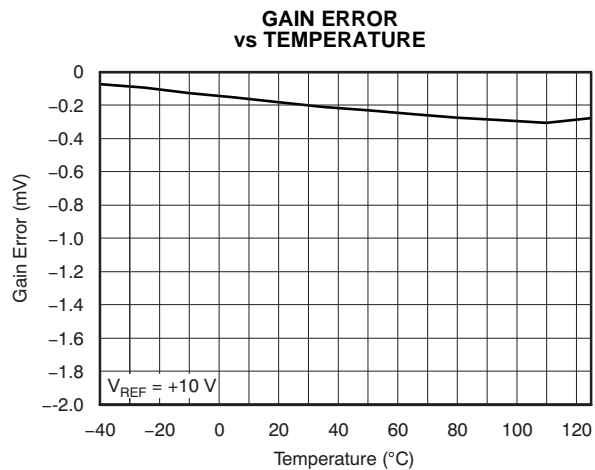
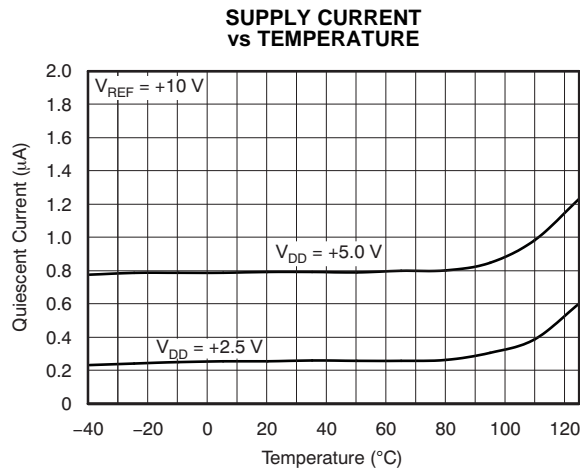


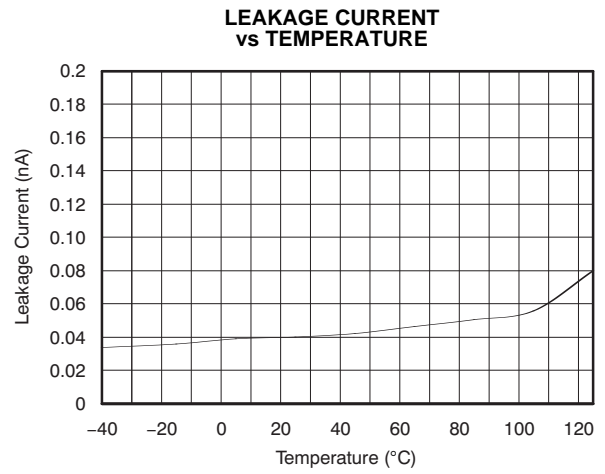
Figure 12.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5V$  (continued)**

At  $T_A = +25^\circ C$ , unless otherwise noted.



**Figure 13.**



**Figure 14.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.5V$**

At  $T_A = +25^\circ C$ , unless otherwise noted.

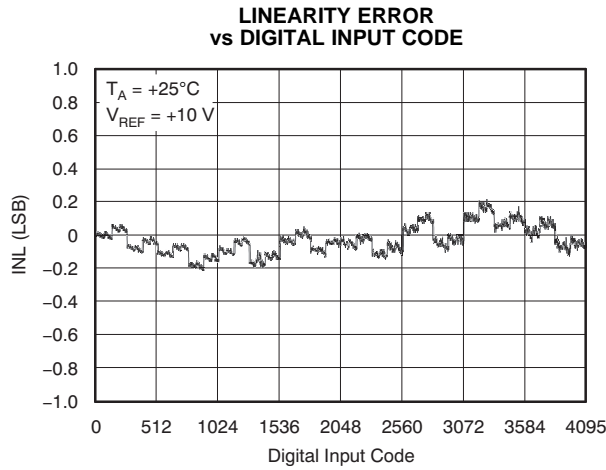


Figure 15.

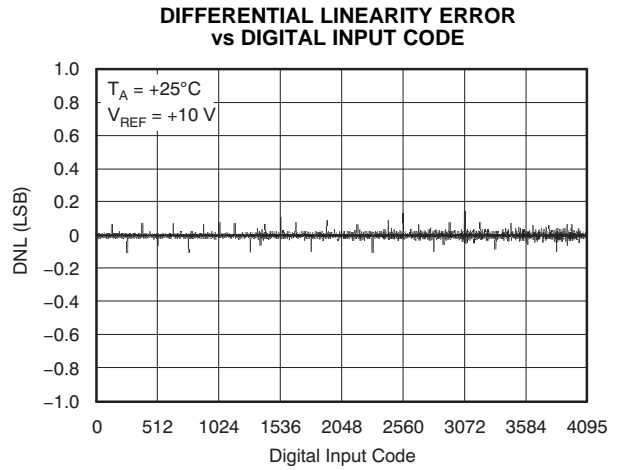


Figure 16.

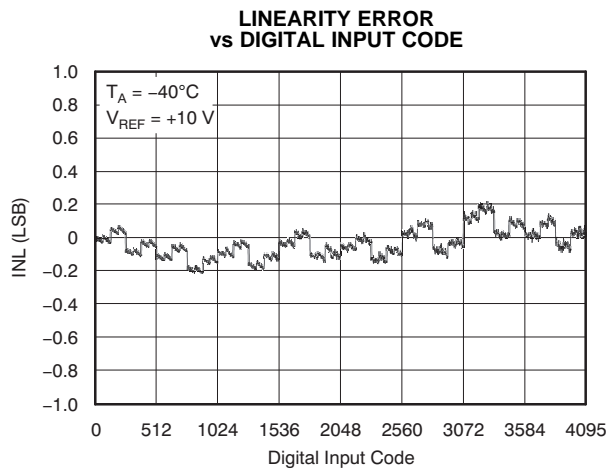


Figure 17.

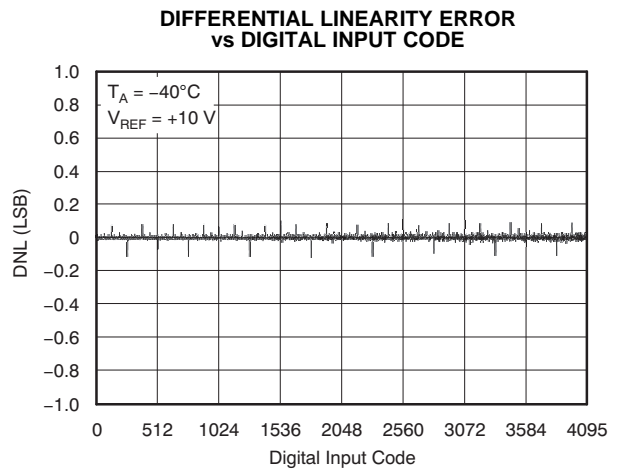


Figure 18.

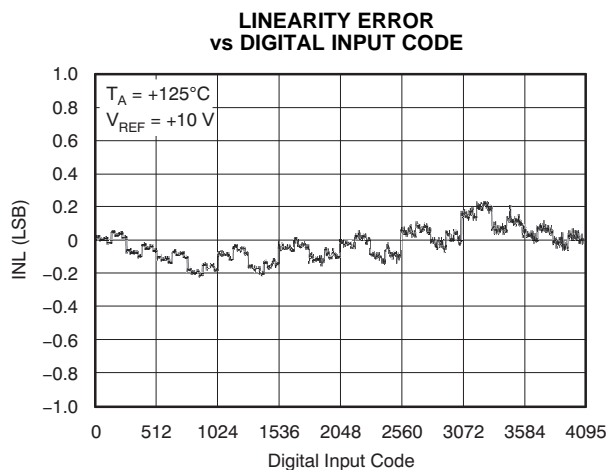


Figure 19.

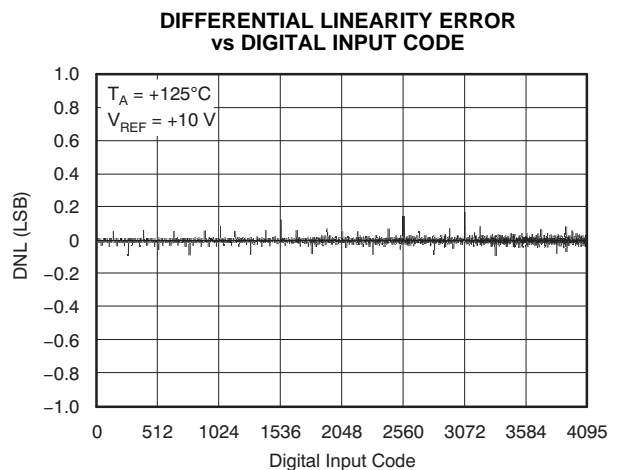
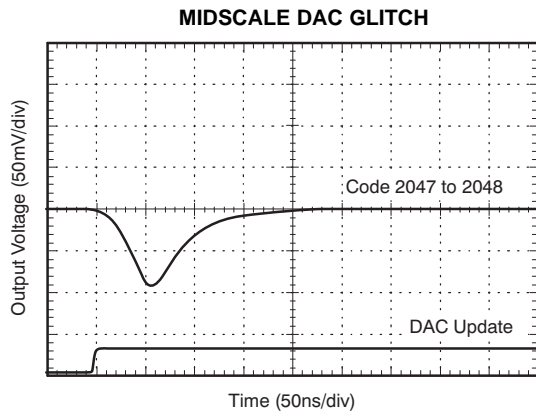


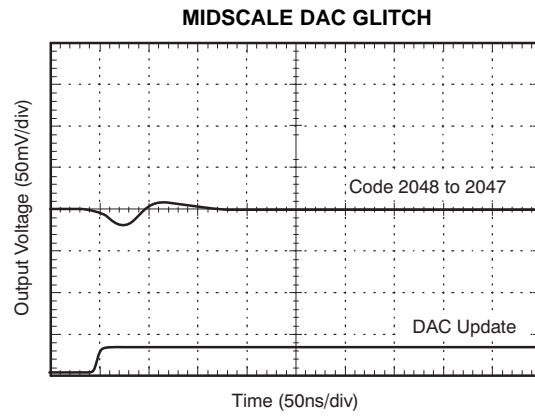
Figure 20.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.5V$  (continued)**

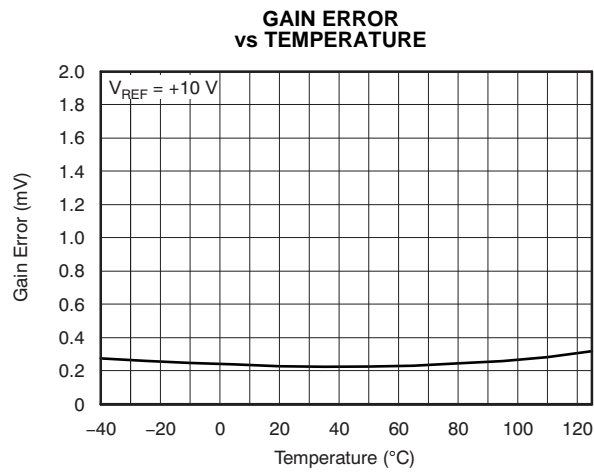
At  $T_A = +25^\circ C$ , unless otherwise noted.



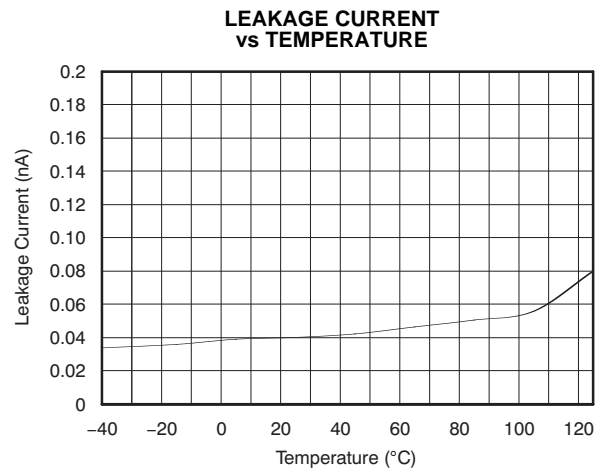
**Figure 21.**



**Figure 22.**



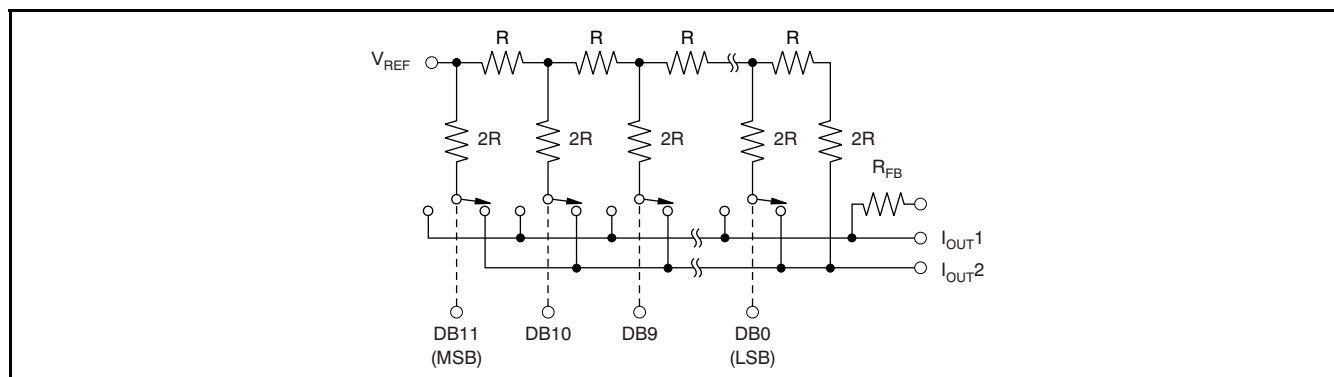
**Figure 23.**



**Figure 24.**

## THEORY OF OPERATION

The DAC7821 is a single channel, current output, 12-bit digital-to-analog converter (DAC). The architecture, illustrated in [Figure 25](#), is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to  $I_{OUT1}$  or the  $I_{OUT2}$  terminal. The  $I_{OUT1}$  terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input  $V_{REF}$  that determines the DAC full-scale current. The R-2R ladder presents a code-independent load impedance to the external reference of  $10k\Omega \pm 20\%$ . The external reference voltage can vary over a range of  $-15V$  to  $+15V$ , thus providing bipolar  $I_{OUT}$  current operation. By using an external I/V converter and the DAC7821  $R_{FB}$  resistor, output voltage ranges of  $-V_{REF}$  to  $V_{REF}$  can be generated.



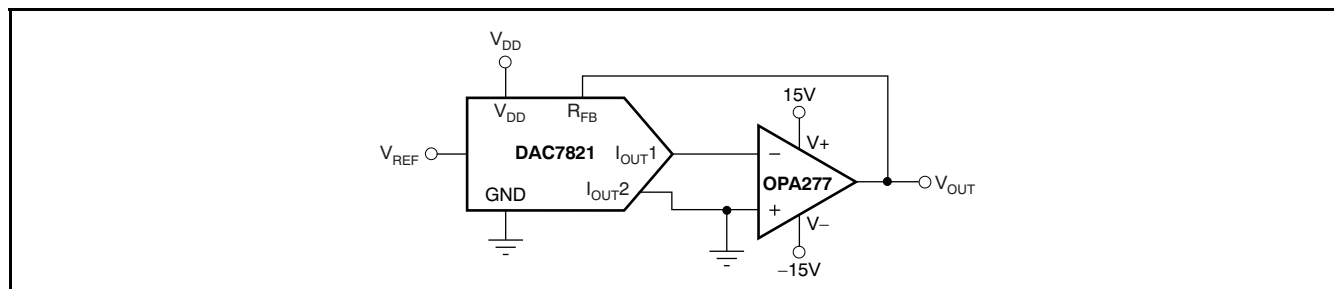
**Figure 25. Equivalent R-2R DAC Circuit**

When using an external I/V converter and the DAC7821  $R_{FB}$  resistor, the DAC output voltage is given by [Equation 1](#):

$$V_{OUT} = -V_{REF} \times \frac{CODE}{4096} \quad (1)$$

Each DAC code determines the 2R leg switch position to either GND or  $I_{OUT}$ . Because the DAC output impedance as seen looking into the  $I_{OUT1}$  terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC  $I_{OUT1}$  terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7821 as a result of offset modulation versus DAC code.

For best linearity performance of the DAC7821, an op amp with a low input offset voltage ([OPA277](#)) is recommended (see [Figure 26](#)). This circuit allows  $V_{REF}$  swinging from  $-10V$  to  $+10V$ .



**Figure 26. Voltage Output Configuration**

## APPLICATION INFORMATION

### Stability Circuit

For a current-to-voltage design (see Figure 27), the DAC7821 current output ( $I_{OUT}$ ) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design practices. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, compensation capacitor  $C_1$  (1pF to 5pF typ) can be added to the design, as shown in Figure 27.

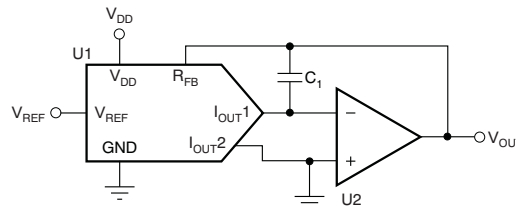


Figure 27. Gain Peaking Prevention Circuit with Compensation Capacitor

### Amplifier Selection

There are many choices and many differences in selecting the proper operational amplifier for a multiplying DAC (MDAC). Making the analog signal out of the MDAC is one critical aspect. However, there are also other issues to take into account such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy. Table 1 and Table 2 suggest some suitable operational amplifiers for low power, fast settling, and high-speed applications. A greater selection of operational amplifiers can be found at [www.ti.com/amplifier](http://www.ti.com/amplifier).

Table 1. Suitable Precision Operational Amplifiers from Texas Instruments

PRODUCT	TOTAL SUPPLY VOLTAGE (V) (min)	TOTAL SUPPLY VOLTAGE (V) (max)	$I_Q$ PER CHANNEL (max) (mA)	GBW (typ) (MHz)	SLEW RATE (typ) (V/ $\mu$ s)	OFFSET DRIFT (typ) ( $\mu$ V/ $^{\circ}$ C)	$I_{IB}$ (max) (pA)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
<b>Low Power</b>										
OPA703	4	12	0.2	1	0.6	4	10	70	SOT5-23, PDIP-8, SOIC-8	12V, CMOS, Rail-to-Rail I/O, Operational Amplifier
OPA735	2.7	12	0.75	1.6	1.5	0.01	200	115	SOT5-23, SOIC-8	0.05 $\mu$ V/ $^{\circ}$ C (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier
OPA344	2.7	5.5	0.25	1	1	2.5	10	80	SOT5-23, PDIP-8, SOIC-8	Low Power, Single-Supply, Rail-To-Rail Operational Amplifiers MicroAmplifier Series
OPA348	2.1	5.5	0.065	1	0.5	2	10	70	SC5-70, SOT5-23, SOIC-8	1MHz, 45 $\mu$ A, Rail-to-Rail I/O, Single Op Amp
OPA277	4	36	0.825	1	0.8	0.1	1000	130	PDIP-8, SOIC-8, SON-8	High Precision Operational Amplifiers
<b>Fast Settling</b>										
OPA350	2.7	5.5	7.5	38	22	4	10	76	MSOP-8, PDIP-8, SOIC-8	High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series
OPA727	4	12	6.5	20	30	0.6	500	86	MSOP-8, SON-8	e-trim 20MHz, High Precision CMOS Operational Amplifier
OPA227	5	36	3.8	8	2.3	0.1	10000	120	PDIP-8, SOIC-8	High Precision, Low Noise Operational Amplifiers

**Table 2. Suitable High Speed Operational Amplifiers from Texas Instruments (Multiple Channel Options)**

PRODUCT	SUPPLY VOLTAGE (V)	GBW PRODUCT (MHz)	VOLTAGE NOISE nV/ $\sqrt{\text{Hz}}$	GBW (typ) (MHz)	SLEW RATE (V/ $\mu\text{s}$ )	V <sub>os</sub> (typ) ( $\mu\text{V}$ )	V <sub>os</sub> (max) ( $\mu\text{V}$ )	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
<b>Single Channel</b>										
THS4281	$\pm 2.7$ to $\pm 15$	38	12.5	35	500	3500	500	1000	SOT5-23, MSOP-8, SOIC-8	Very Low-Power High Speed Rail-To-Rail Input/Output Voltage Feedback Operational Amplifier
THS4031	$\pm 4.5$ to $\pm 16.5$	200	1.6	100	500	3000	3000	8000	CDIP-8, MSOP-8, SOIC-8	100-MHz Low Noise Voltage-Feedback Amplifier
THS4631	$\pm 4.5$ to $\pm 16.5$	210	7	900	260	2000	50pA	2	SOIC-8, MSOP-8	High Speed FET-Input Operational Amplifier
OPA656	$\pm 4$ to $\pm 6$	230	7	290	250	2600	2pA	5pA	SOIC-8, SOT5-23	Wideband, Unity Gain Stable FET-Input Operational Amplifier
OPA820	$\pm 2.5$ to $\pm 6$	280	2.5	240	200	1200	900	23,000	SOIC-8, SOT5-23	Unity Gain Stable, Low Noise, Voltage Feedback Operational Amplifier
<b>Dual Channel</b>										
THS4032	$\pm 4.5$ to $\pm 16.5$	200	1.6	100	500	3000	3000	8000	SOIC-8, MSOP-8	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
OPA2822	$\pm 2$ to $\pm 6.3$	220	2	170	200	1200	9600	12000	SOIC-8, MSOP-8	SpeedPlus Dual Wideband, Low-Noise Operational Amplifier

### Positive Voltage Output Circuit

As Figure 28 illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC7821. This design is suggested instead of using an inverting amp to invert the output because of possible resistor tolerance errors. For a negative reference,  $V_{OUT}$  and GND of the reference are level-shifted to a virtual ground and a  $-2.5V$  input to the DAC7821 with an op amp.

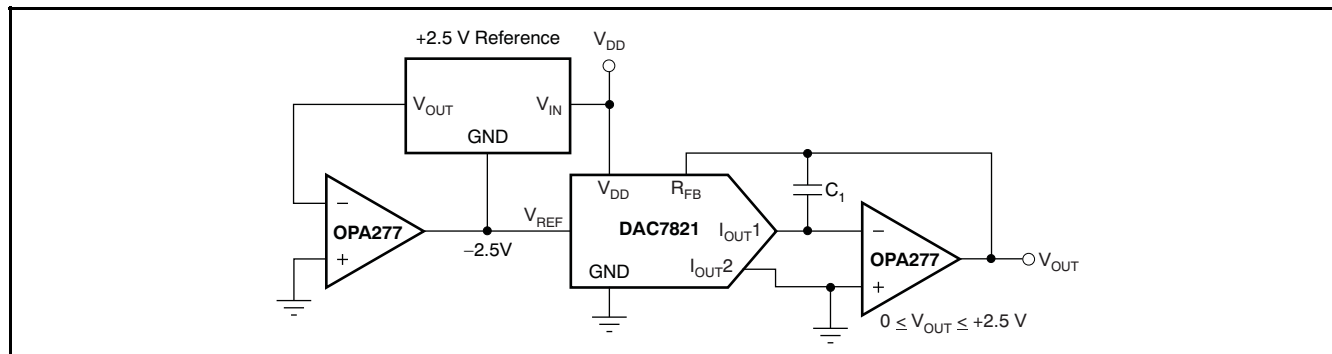


Figure 28. Positive Voltage Output Circuit

### Bipolar Output Section

The DAC7821, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output  $I_{OUT}$  is the inverse of the input reference voltage at  $V_{REF}$ .

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 29, external op amp U4 is added as a summing amp and has a gain of 2X that widens the output span to 5V. A 4-quadrant multiplying circuit is implemented by using a 2.5V offset of the reference voltage to bias U4. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full-scale produces output voltages of  $V_{OUT} = -2.5V$  to  $V_{OUT} = +2.5V$ .

$$V_{OUT} = \left( \frac{D}{0.5 \times 2^N} - 1 \right) \times V_{REF} \tag{2}$$

External resistance mismatching is the significant error in Figure 29.

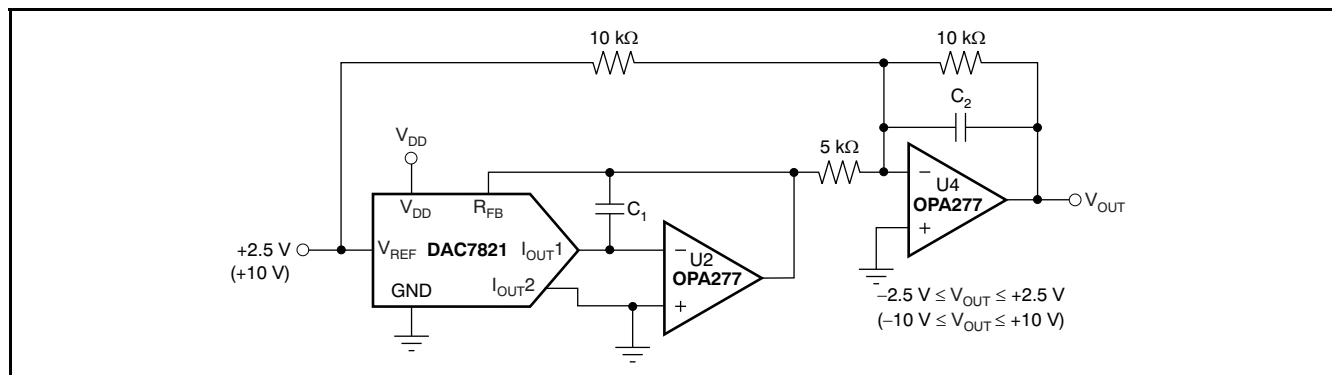


Figure 29. Bipolar Output Circuit

## Programmable Current Source Circuit

A DAC7821 can be integrated into the circuit in [Figure 30](#) to implement an improved Howland current pump for precise voltage-to-current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by [Equation 3](#):

$$I_L = \frac{(R_2 + R_3)/R_1}{R_3} \times V_{REF} \times D \quad (3)$$

The value of  $R_3$  in the previous equation can be reduced to increase the output current drive of  $U_3$ .  $U_3$  can drive  $\pm 20\text{mA}$  in both directions with voltage compliance limited up to  $15\text{V}$  by the  $U_3$  voltage supply. Elimination of the circuit compensation capacitor  $C_1$  in the circuit is not suggested as a result of the change in the output impedance  $Z_O$ , according to [Equation 4](#):

$$Z_O = \frac{R_1' R_3 (R_1 + R_2)}{R_1 (R_2' + R_3') - R_1' (R_2 + R_3)} \quad (4)$$

As shown in [Equation 4](#), with matched resistors,  $Z_O$  is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used,  $Z_O$  is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating  $C_1$  into the circuit, possible oscillation problems are eliminated. The value of  $C_1$  can be determined for critical applications; for most applications, however, a value of several pF is suggested.

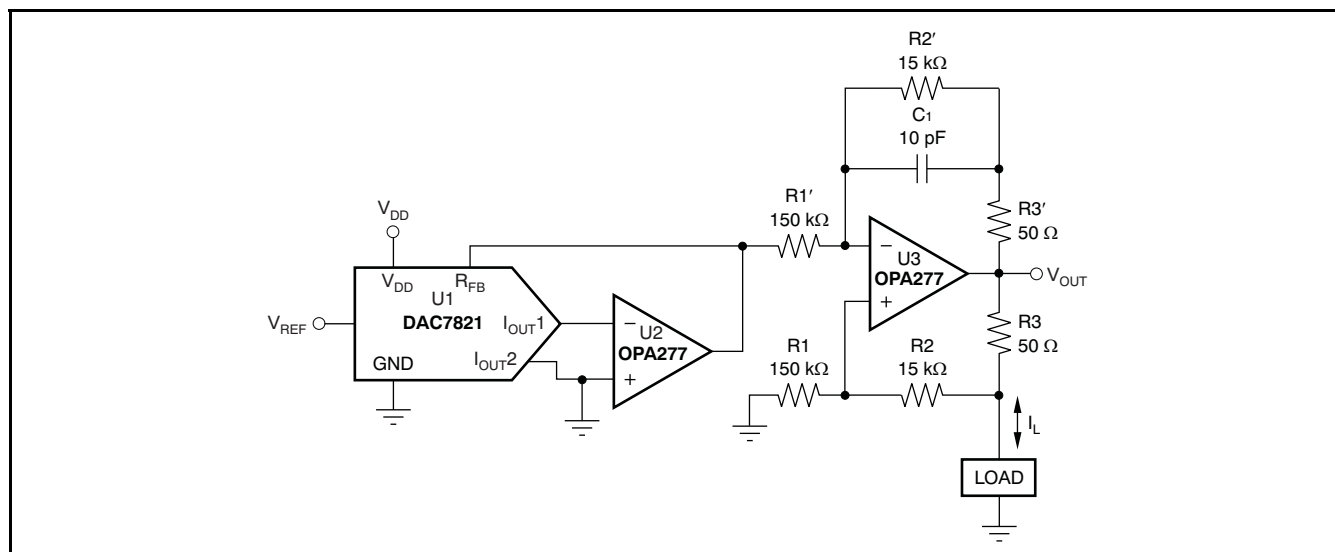


Figure 30. Programmable Bidirectional Current Source Circuit

## Parallel Interface

Data are loaded to the DAC7821 as a 12-bit parallel word. The bidirectional bus is controlled with  $\overline{CS}$  and  $R/\overline{W}$ , allowing data to be written to or read from the DAC register. To write to the device,  $\overline{CS}$  and  $R/\overline{W}$  are brought low, and data available on the data lines fill the input register. The rising edge of  $\overline{CS}$  latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent; therefore, a write sequence must consist of a falling and rising edge on  $\overline{CS}$  in order to ensure that data are loaded to the DAC register and its analog equivalent is reflected on the DAC output.

To read data stored in the device,  $R/\overline{W}$  is held high and  $\overline{CS}$  is brought low. Data are loaded from the DAC register back to the input register and out onto the data line, where it can be read back to the controller.

## Cross-Reference

The DAC7821 has an industry-standard pinout. [Table 3](#) provides the cross-reference information.

**Table 3. Cross-Reference**

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS- REFERENCE PART
DAC7821	±1	±1	–40°C to +125°C	20-Lead TSSOP	TSSOP-20	AD5445

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7821IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC7821	<a href="#">Samples</a>
DAC7821IPWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC7821	<a href="#">Samples</a>
DAC7821IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC7821	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

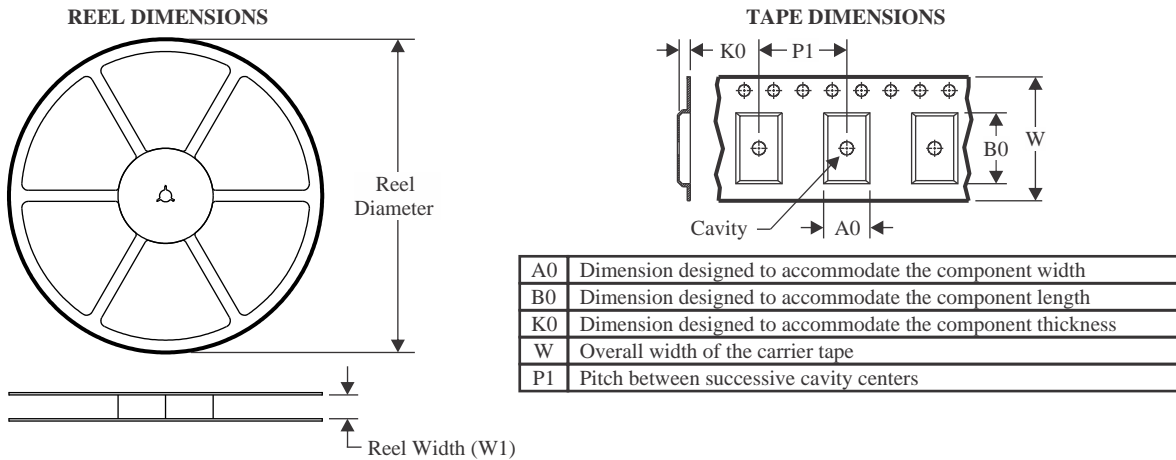
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

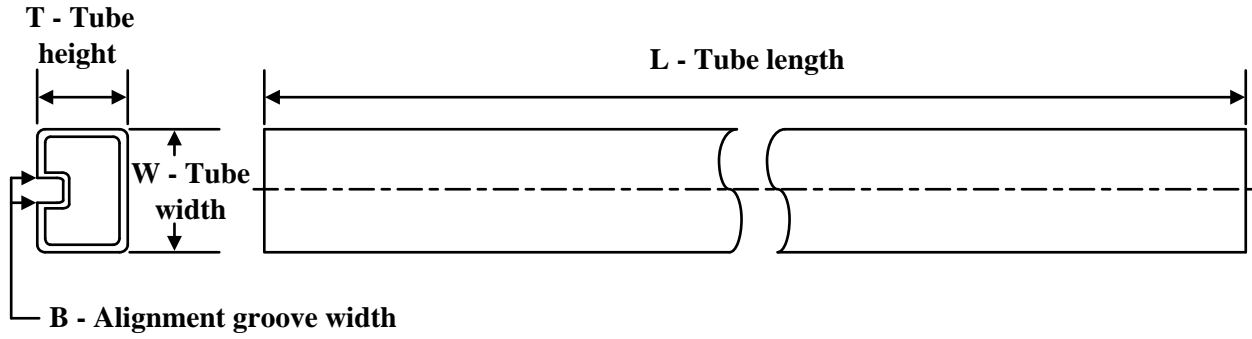

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7821IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

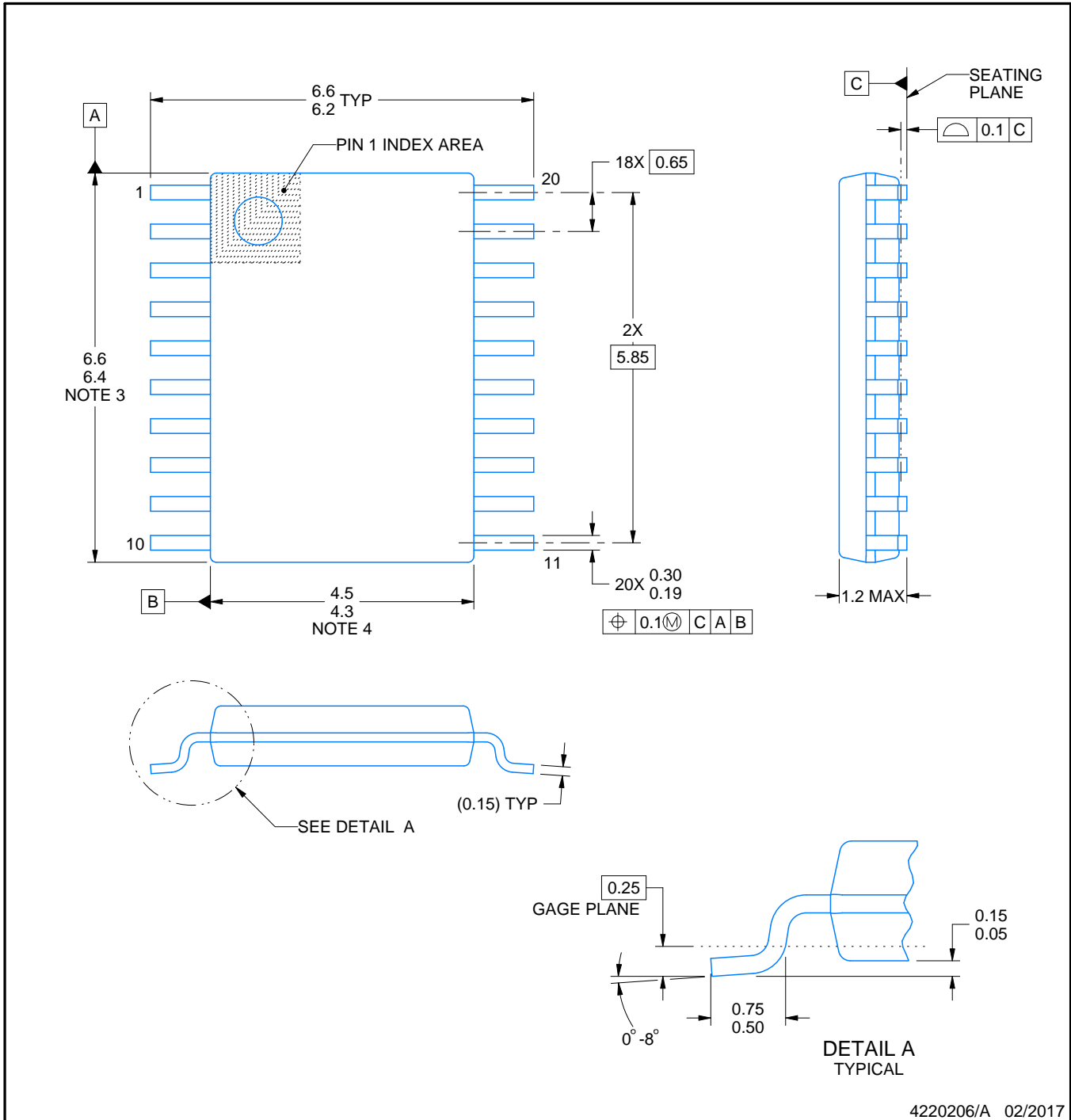

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7821PWR	TSSOP	PW	20	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC7821IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
DAC7821IPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

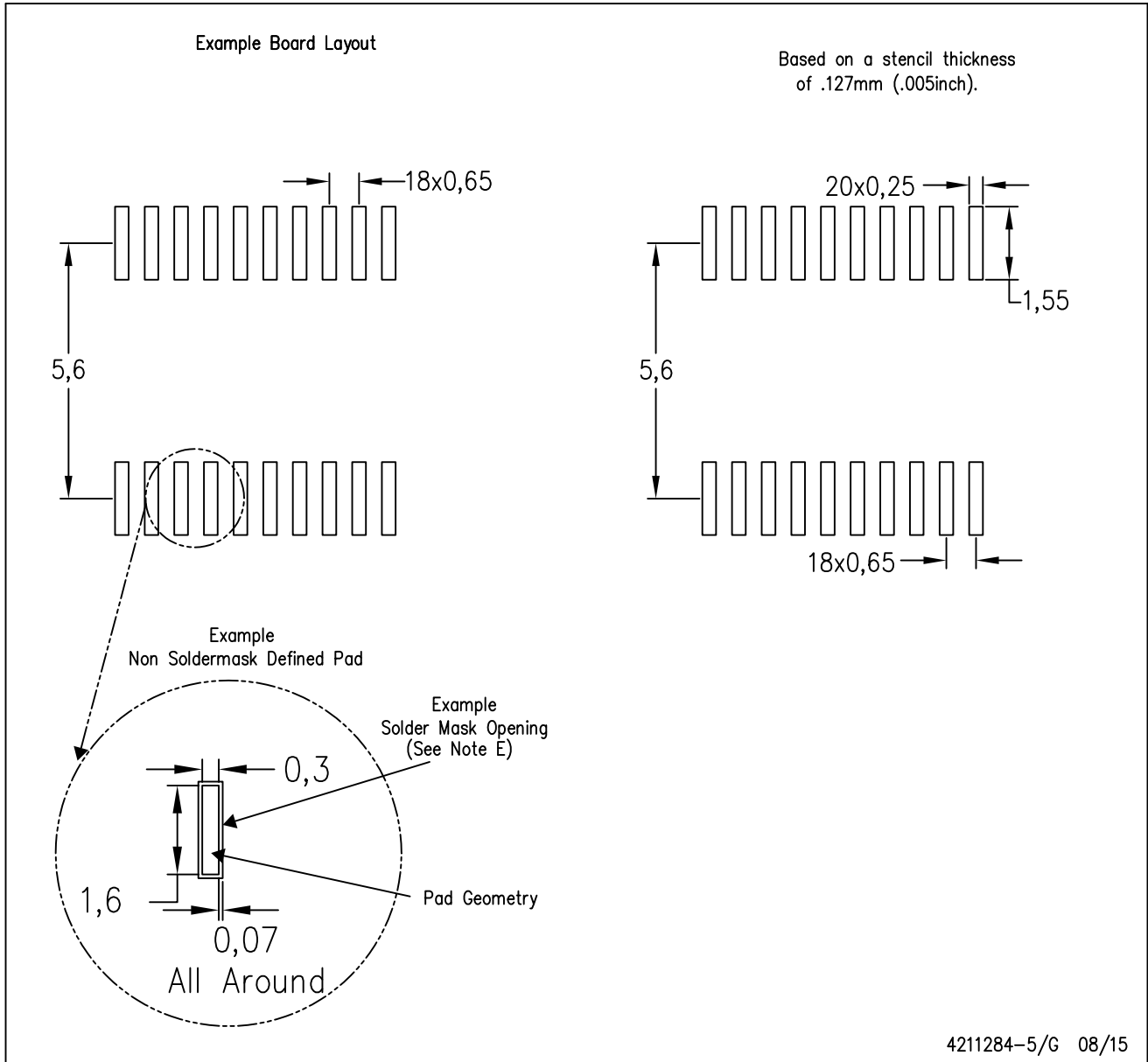
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View DAC7821PW](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management