



**THE DATASHEET OF  
AP2141DMPG-13**



## Description

The AP2141D and AP2151D are integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB 2.0 and is available with both polarities of Enable input. They offer current and thermal limiting and short circuit protection as well as controlled rise time and undervoltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

All devices are available in SOT25, SO-8, MSOP-8EP, and U-DFN2018-6 packages.

## Features

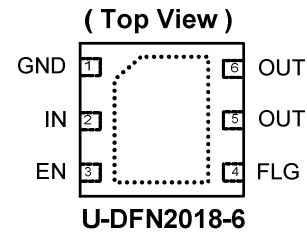
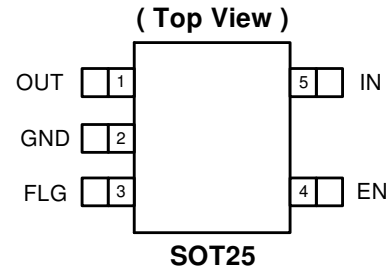
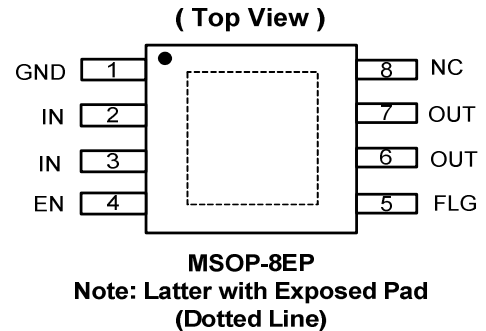
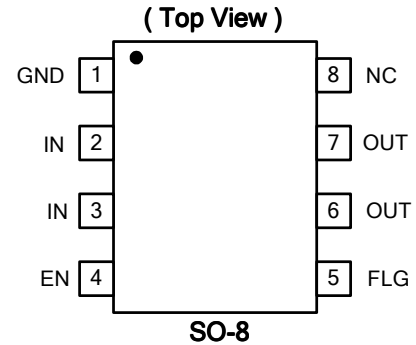
- Single USB Port Power Switches with Output Discharge
- Over-Current and Thermal Protection
- 0.8A Accurate Current Limiting
- Fast Transient Response
- Reverse Current Blocking
- 90mΩ On-Resistance
- Input Voltage Range: 2.7V - 5.5V
- 0.6ms Typical Rise Time
- Very Low Shutdown Current: 1μA (max)
- Fault Report (FLG) with Blanking Time (7ms typ)
- ESD Protection: 4kV HBM, 300V MM
- Active High (AP2151D) or Active Low (AP2141D) enable
- Ambient Temperature Range -40°C to +85°C
- SOT25, SO-8, MSOP-8EP (Exposed Pad), and U-DFN2018-6: Available in "Green" Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- 15kV ESD Protection per IEC 61000-4-2 (with external capacitance)
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

## Applications

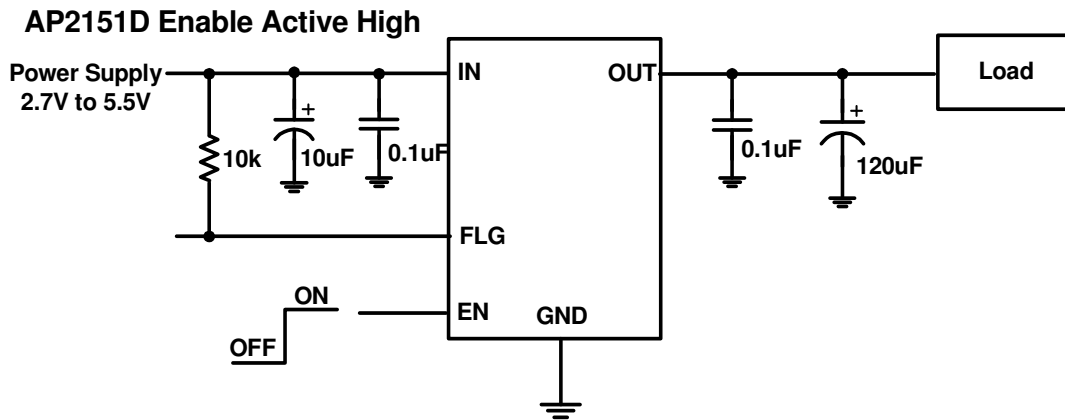
- Consumer Electronics – LCD TVs & Monitors, Game Machines
- Communications – Set-Top-Boxes, GPS, Smartphones
- Computing – Laptops, Desktops, Servers, Printers, Docking Stations, HUBs

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.  
 2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.  
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments



Typical Applications Circuit

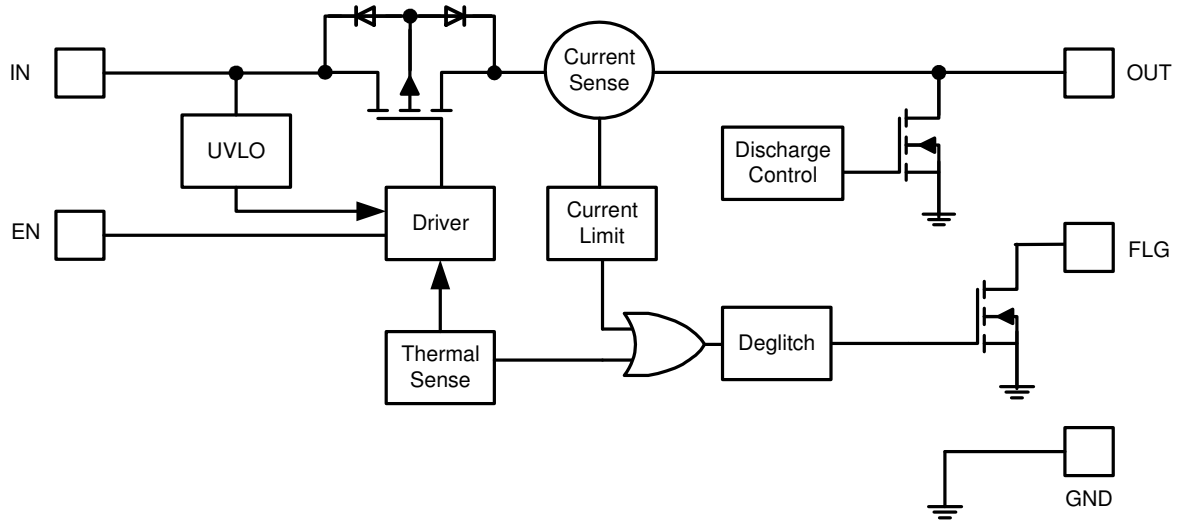


| Part Number | Channel | Enable Pin (EN) | Current Limit (Typical) | Recommended Maximum Continuous Load Current |
|-------------|---------|-----------------|-------------------------|---|
| AP2141D     | 1       | Active Low      | 0.8A                    | 0.5A  |
| AP2151D     | 1       | Active High     | 0.8A                    | 0.5A  |

Pin Descriptions

| Pin Name    | Pin Number |             |       |             | Descriptions  |
|-------------|------------|-------------|-------|-------------|---|
|             | SO-8       | MSOP-8EP    | SOT25 | U-DFN2018-6 |   |
| GND         | 1          | 1           | 2     | 1           | Ground  |
| IN          | 2, 3       | 2, 3        | 5     | 2           | Voltage Input Pin. (all IN pins must be tied together externally)   |
| EN          | 4          | 4           | 4     | 3           | Enable Input, active low (AP2141D) or active high (AP2151D).  |
| FLG         | 5          | 5           | 3     | 4           | Over-current and over-temperature fault report; open-drain flag is active low when triggered.   |
| OUT         | 6, 7       | 6, 7        | 1     | 5, 6        | Voltage Output Pin (all OUT pins must be tied together externally).   |
| NC          | 8          | 8           | N/A   | N/A         | No Internal Connection; recommend tie to OUT pins.  |
| Exposed tab | -          | Exposed tab | -     | Exposed tab | Exposed pad. Internally connected to GND. It should be externally connected to GND and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path. |

**Functional Block Diagram**



**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Symbol   | Parameter                          |  | Ratings              | Units |
|--|------------------------------------|--|----------------------|-------|
| ESD  | HBM                                | Human Body Model ESD Protection  | 4                    | kV    |
|  | MM                                 | Machine Model ESD Protection   | 300                  | V     |
|  | IEC System Level                   | Surges per EN61000-4-2. 1999 applied to output terminals of EVM (Note 5) | Air                  | 15    |
| Surges per EN61000-4-2. 1999 applied to output terminals of EVM (Note 5) |                                    | Contact  | 8                    | kV    |
| V <sub>IN</sub>  | Input Voltage                      |  | 6.5                  | V     |
| V <sub>OUT</sub>   | Output Voltage                     |  | V <sub>IN</sub> +0.3 | V     |
| V <sub>EN</sub> , V <sub>FLG</sub>                                       | Enable Voltage                     |  | 6.5                  | V     |
| I <sub>LOAD</sub>  | Maximum Continuous Load Current    |  | Internal Limited     | A     |
| T <sub>J(MAX)</sub>  | Maximum Junction Temperature       |  | +150                 | °C    |
| T <sub>ST</sub>  | Storage Temperature Range (Note 4) |  | -65 to +150          | °C    |

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices

- Notes:
4. UL Recognized Rating from -30°C to +70°C (Diodes qualified T<sub>ST</sub> from -65°C to +150°C)
  5. External capacitors need to be connected to the output, EVM board was tested with capacitor 2.2µF 50V 0805. This level is a pass test only and not a limit.

**Recommended Operating Conditions** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Symbol           | Parameter   | Min | Max             | Unit |
|------------------|---|-----|-----------------|------|
| V <sub>IN</sub>  | Input Voltage                                     | 2.7 | 5.5             | V    |
| I <sub>OUT</sub> | Output Current                                    | 0   | 500             | mA   |
| T <sub>A</sub>   | Operating Ambient Temperature                     | -40 | +85             | °C   |
| V <sub>IH</sub>  | High-Level Input Voltage on EN or $\overline{EN}$ | 2.0 | V <sub>IN</sub> | V    |
| V <sub>IL</sub>  | Low-Level Input Voltage on EN or $\overline{EN}$  | 0   | 0.8             | V    |

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{IN} = +5\text{V}$ , unless otherwise specified.)

| Symbol        | Parameter                              | Test Conditions   |   | Min                              | Typ  | Max | Unit               |            |
|---------------|--|---|---|----------------------------------|------|-----|--------------------|------------|
| $V_{UVLO}$    | Input UVLO                             | —   |   | 1.6                              | 1.9  | 2.5 | V                  |            |
| $I_{SHDN}$    | Input Shutdown Current                 | Disabled, $I_{OUT} = 0$   |   | —                                | 0.5  | 1   | $\mu\text{A}$      |            |
| $I_Q$         | Input Quiescent Current                | Enabled, $I_{OUT} = 0$  |   | —                                | 45   | 70  | $\mu\text{A}$      |            |
| $I_{LEAK}$    | Input Leakage Current                  | Disabled, OUT grounded  |   | —                                | 0.1  | 1   | $\mu\text{A}$      |            |
| $I_{REV}$     | Reverse Leakage Current                | Disabled, $V_{IN} = 0\text{V}$ , $V_{OUT} = 5\text{V}$ , $I_{REV}$ at $V_{IN}$  |   | —                                | 0.1  | 1   | $\mu\text{A}$      |            |
| $R_{DS(ON)}$  | Switch On-Resistance                   | $V_{IN} = 5\text{V}$ ,<br>$I_{OUT} = 0.5\text{A}$   | $T_A = +25^\circ\text{C}$                           | SOT25, MSOP-8,<br>MSOP-8EP, SO-8 | —    | 95  | 115                | m $\Omega$ |
|               |  |   | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | U-DFN2018-6                      | —    | 90  | 110                |            |
|               |  | $V_{IN} = 3.3\text{V}$ , $I_{OUT} = 0.5\text{A}$  | $T_A = +25^\circ\text{C}$                           | —                                | 120  | 140 |                    |            |
|               |  |   | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | —                                | —    | 170 |                    |            |
| $I_{SHORT}$   | Short-Circuit Current Limit            | Enabled into short circuit, $C_L = 22\mu\text{F}$   |   | —                                | 0.6  | —   | A                  |            |
| $I_{LIMIT}$   | Over-Load Current Limit                | $V_{IN} = 5\text{V}$ , $V_{OUT} = 4.0\text{V}$ , $C_L = 120\mu\text{F}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ |   | 0.6                              | 0.8  | 1.0 | A                  |            |
| $I_{TRIG}$    | Current Limiting Trigger Threshold     | Output Current Slew Rate (<100A/s) , $C_L = 22\mu\text{F}$  |   | —                                | 1.0  | —   | A                  |            |
| $I_{SINK}$    | EN Input Leakage                       | $V_{EN} = 5\text{V}$  |   | —                                | —    | 1   | $\mu\text{A}$      |            |
| $t_{D(ON)}$   | Output Turn-On Delay Time              | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$  |   | —                                | 0.05 | —   | ms                 |            |
| $t_R$         | Output Turn-On Rise Time               | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$  |   | —                                | 0.6  | 1.5 | ms                 |            |
| $t_{D(OFF)}$  | Output Turn-Off Delay Time             | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$  |   | —                                | 0.05 | —   | ms                 |            |
| $t_F$         | Output Turn-Off Fall Time              | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$  |   | —                                | 0.05 | 0.1 | ms                 |            |
| $R_{FLG}$     | FLG Output FET On-Resistance           | $I_{FLG} = 10\text{mA}$   |   | —                                | 20   | 40  | $\Omega$           |            |
| $t_{BLANK}$   | FLG Blanking Time                      | $C_{IN} = 10\mu\text{F}$ , $C_L = 22\mu\text{F}$  |   | 4                                | 7    | 15  | ms                 |            |
| $R_{DIS}$     | Discharge Resistance (Note 6)          | $V_{IN} = 5\text{V}$ , disabled, $I_{OUT} = 1\text{mA}$   |   | —                                | 100  | —   | $\Omega$           |            |
| $t_{DIS}$     | Discharge Time                         | $C_L = 1\mu\text{F}$ , $V_{IN} = 5\text{V}$ , disabled to $V_{OUT} < 0.5\text{V}$   |   | —                                | 0.6  | —   | ms                 |            |
| $T_{SHDN}$    | Thermal Shutdown Threshold             | Enabled, $R_{LOAD} = 1\text{k}\Omega$   |   | —                                | 140  | —   | $^\circ\text{C}$   |            |
| $T_{HYS}$     | Thermal Shutdown Hysteresis            | —   |   | —                                | 25   | —   | $^\circ\text{C}$   |            |
| $\theta_{JA}$ | Thermal Resistance Junction-to-Ambient | SOT25 (Note 7)  |   | —                                | 170  | —   | $^\circ\text{C/W}$ |            |
|               |  | SO-8 (Note 7)   |   | —                                | 127  | —   |                    |            |
|               |  | MSOP-8EP (Note 8)   |   | —                                | 67   | —   |                    |            |
|               |  | U-DFN2018-6 (Note 8)  |   | —                                | 70   | —   |                    |            |

- Notes:
6. The discharge function is active when the device is disabled (when enable is de-asserted). The discharge function offers a resistive discharge path for the external storage capacitor.
  7. Device mounted on FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
  8. Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Typical Performance Characteristics**

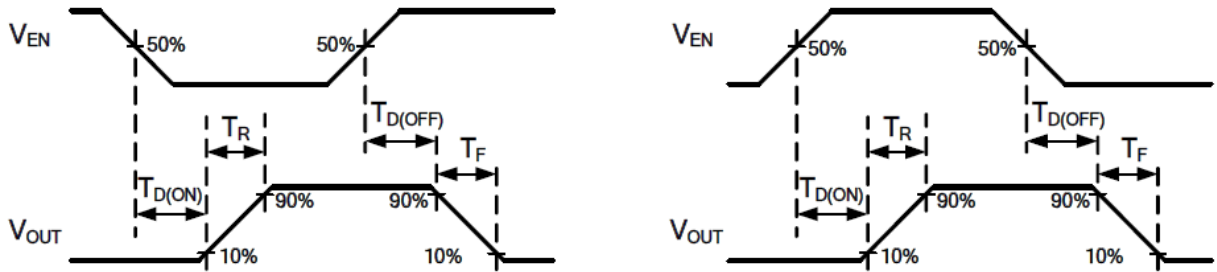
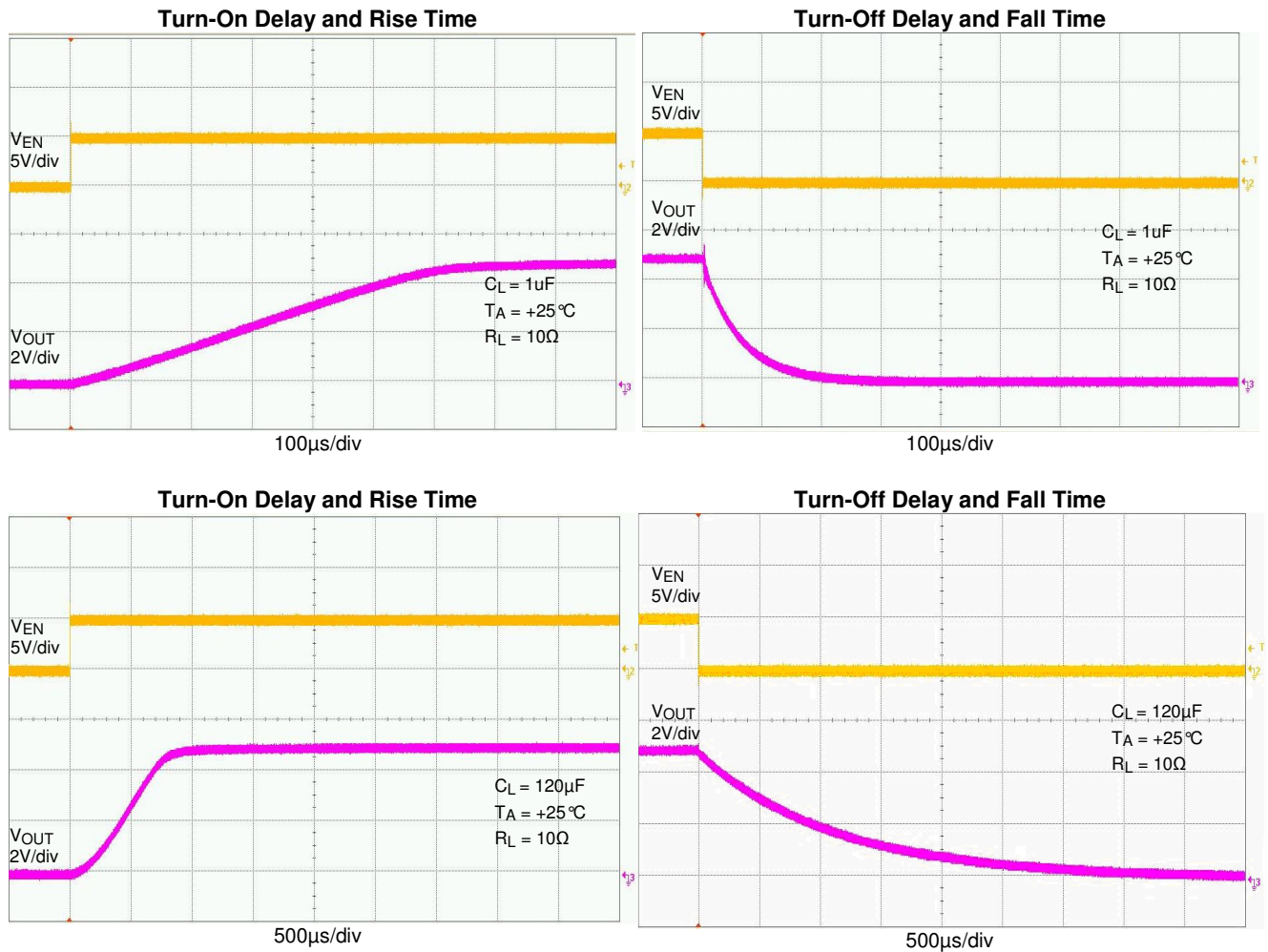


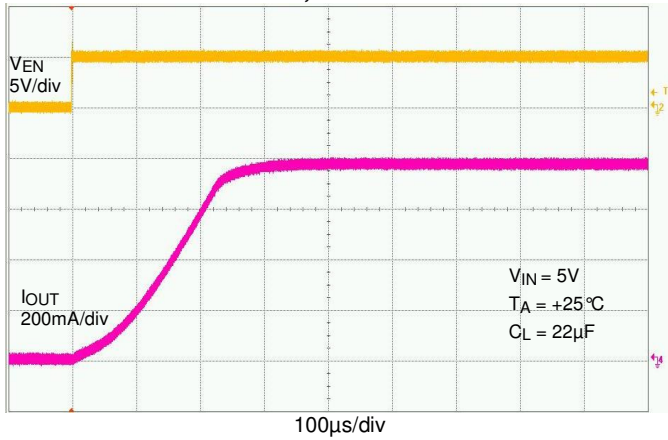
Figure 1 Voltage Waveforms: AP2141D (left), AP2151D (right)

All Enable Plots are for AP2151D Active High

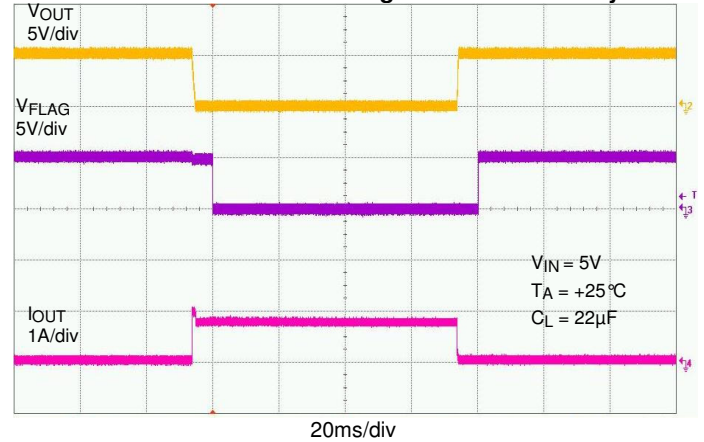


**Typical Performance Characteristics** (continued)

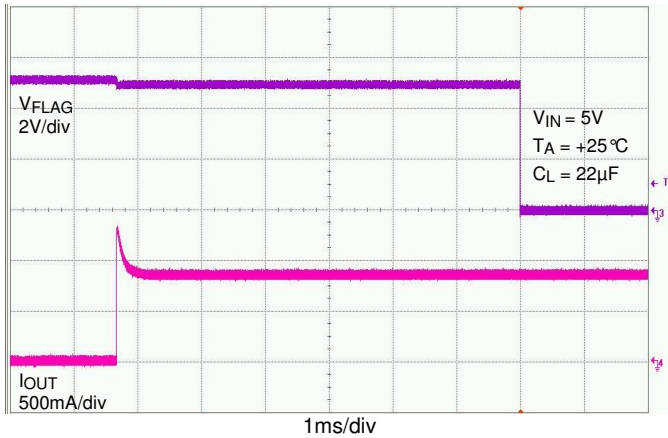
**Short Circuit Current, Device Enabled Into Short**



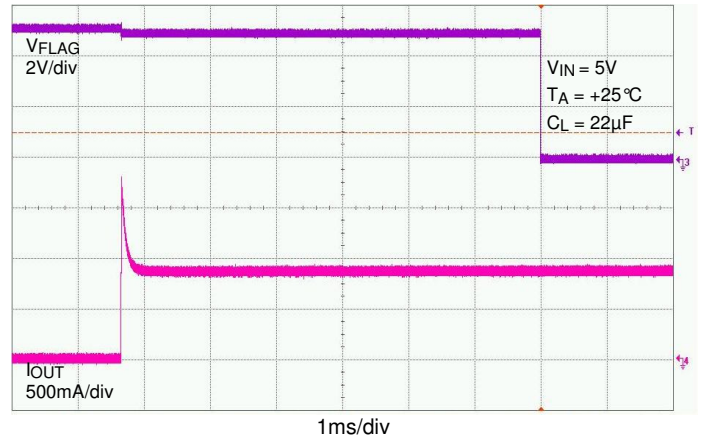
**Short Circuit with Blanking Time and Recovery**



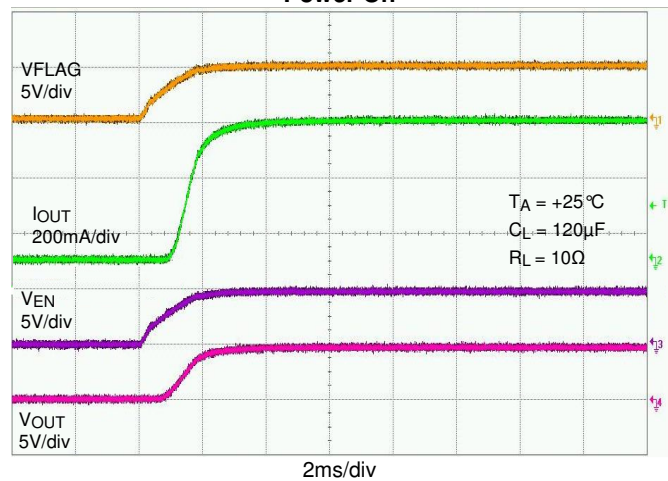
**3Ω Load Connected to Enabled Device**



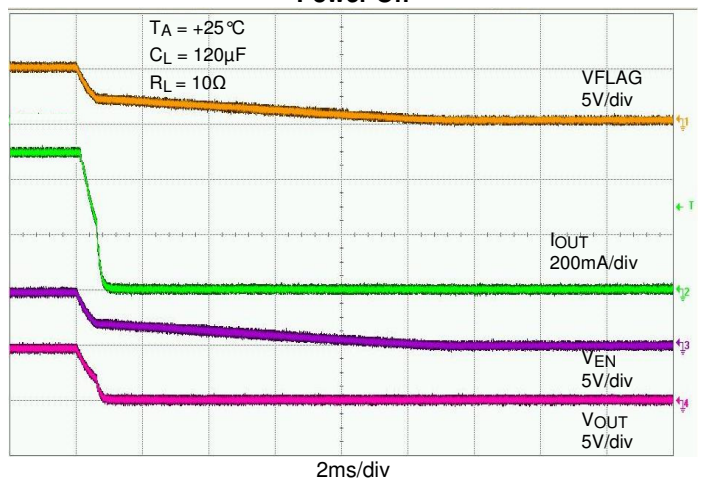
**2Ω Load Connected to Enabled Device**



**Power On**

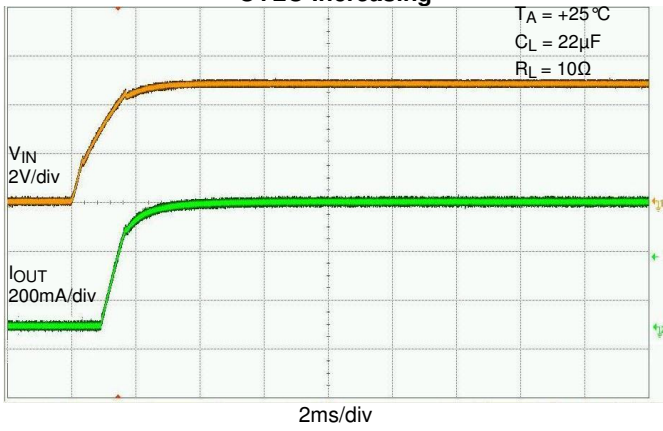


**Power Off**

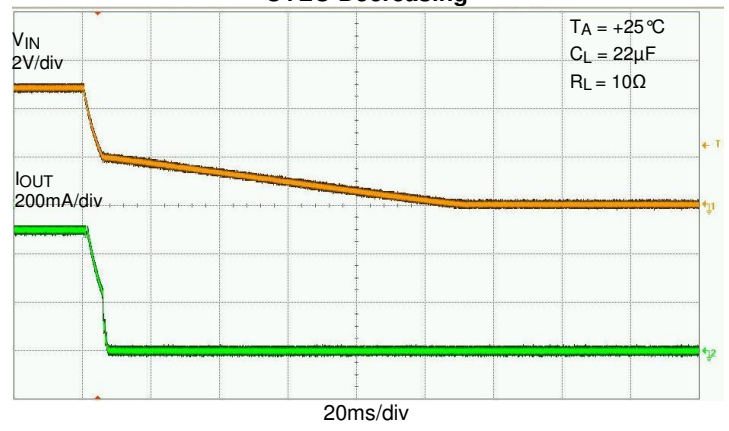


**Typical Performance Characteristics (cont.)**

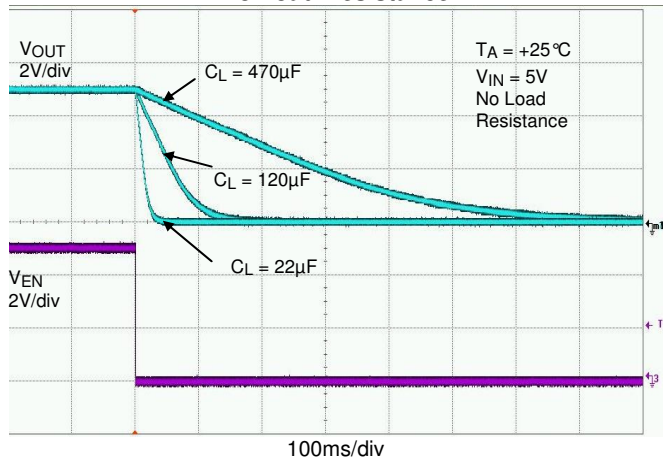
**UVLO Increasing**



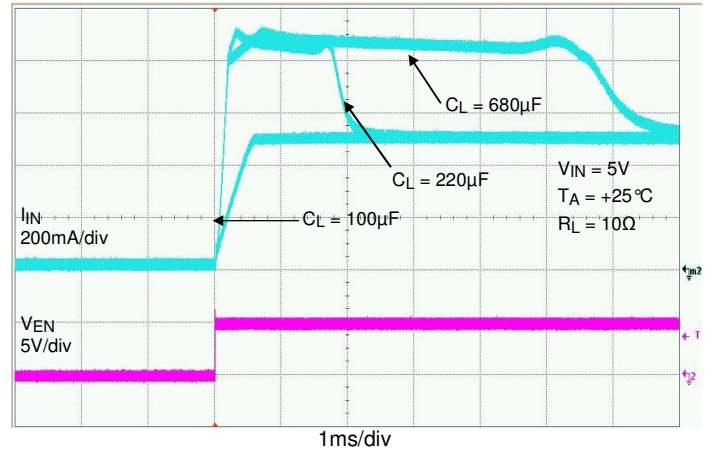
**UVLO Decreasing**



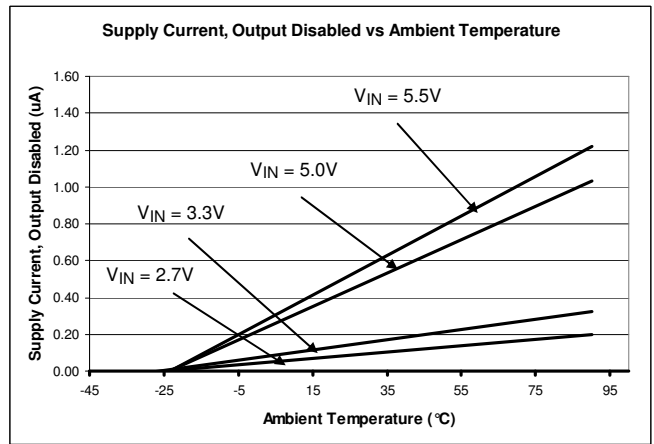
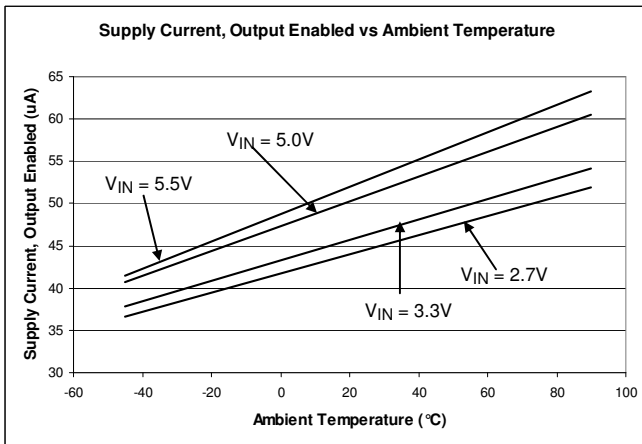
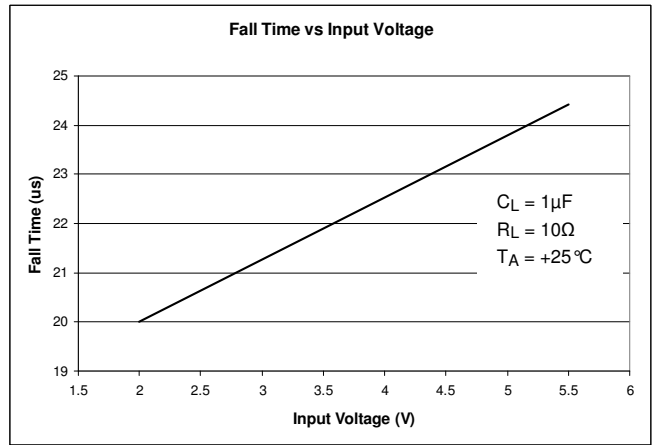
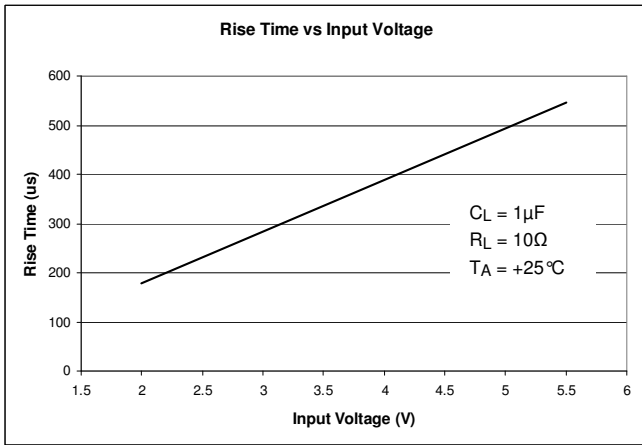
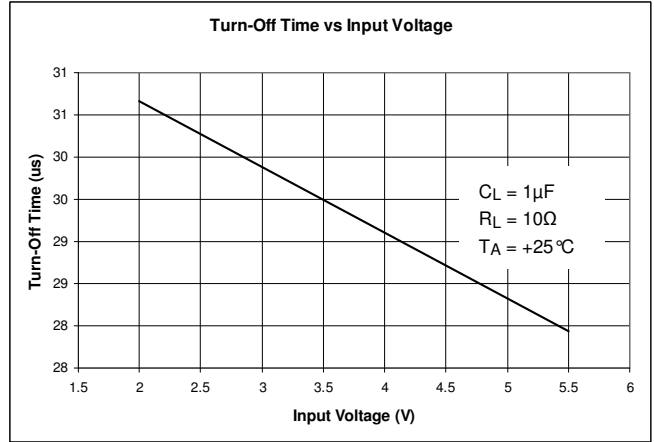
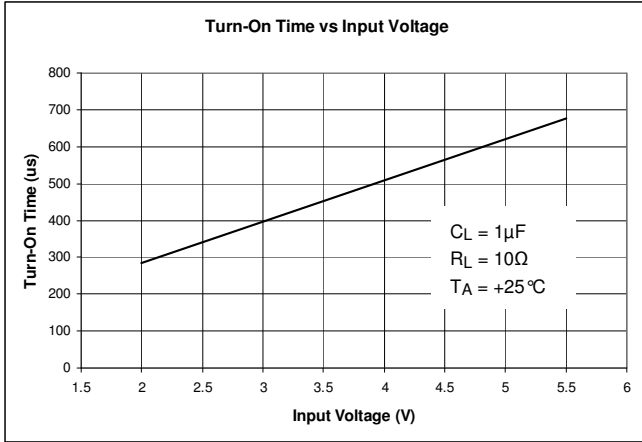
**Discharge Time  
No Load Resistance**



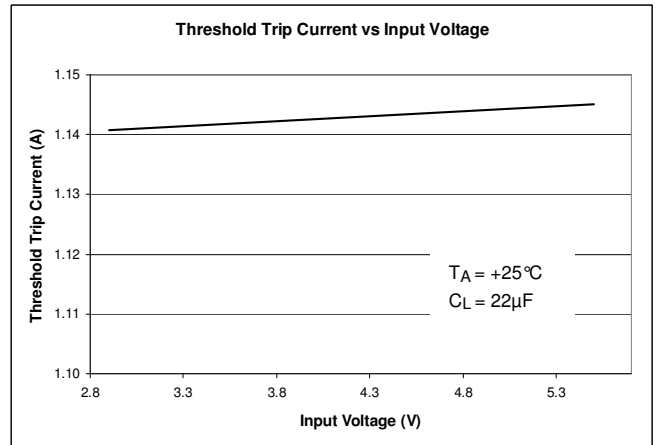
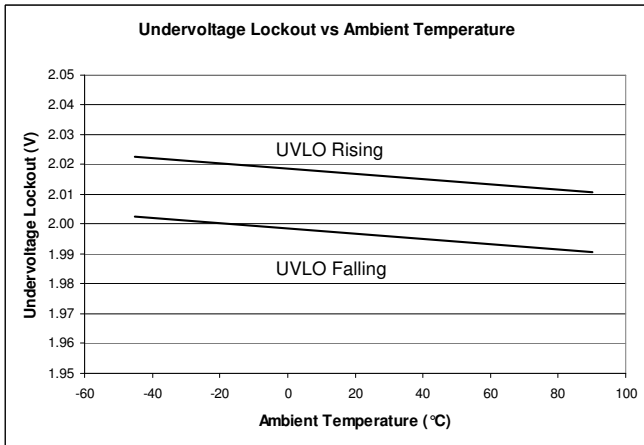
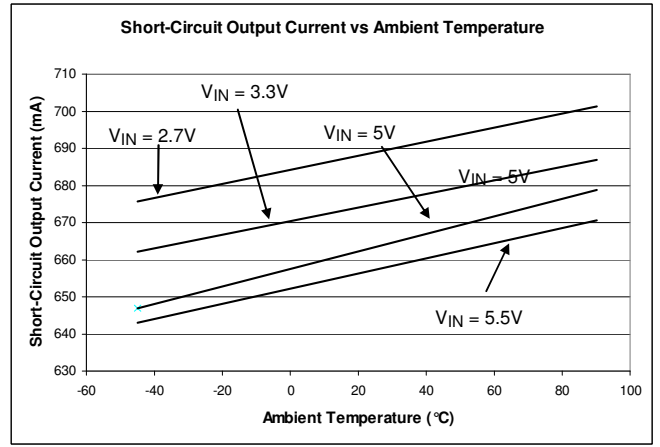
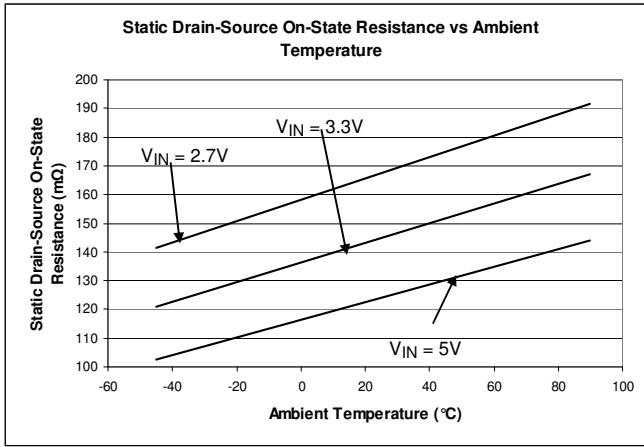
**Inrush Current**



**Typical Performance Characteristics (cont.)**



**Typical Performance Characteristics** (cont.)



## Application Information

The AP2141D and AP2151D are integrated high-side power switches optimized for Universal Serial Bus (USB) that require protection functions. The power switches are equipped with a driver that controls the gate voltage and incorporates slew-rate limitation. This, along with the various protection features and special functions, make these power switches ideal for hot-swap or hot-plug applications.

### Protection Features:

#### Undervoltage Lockout (UVLO)

Undervoltage lockout function (UVLO) guarantees that the internal power switch is initially off during start-up. The UVLO functions only when the switch is enabled. Even if the switch is enabled, the switch is not turned ON until the power supply has reached at least 1.9V. Whenever the input voltage falls below approximately 1.9V, the power switch is turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

#### Over-Current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

The different overload conditions and the corresponding response of the AP2141D/2151D are outlined below:

| S.NO | Conditions   | Explanation   | Behavior of the AP2141D/2151D   |
|------|--|---|---|
| 1    | Short circuit condition at start-up                            | Output is shorted before input voltage is applied or before the part is enabled | The IC senses the short circuit and immediately clamps output current to a certain safe level namely $I_{LIMIT}$ .  |
| 2    | Short-circuit or Overcurrent condition                         | Short-Circuit or Overload condition that occurs when the part is enabled.       | At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react.<br>After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at $I_{LIMIT}$ . |
| 3    | Gradual increase from nominal operating current to $I_{LIMIT}$ | Load increases gradually until the current-limit threshold. ( $I_{TRIG}$ )      | The current rises until $I_{TRIG}$ or thermal limit. Once the threshold has been reached, the device switches into its current limiting mode and is set at $I_{LIMIT}$ .  |

Note that when the output has been shorted to GND at extremely low temperatures ( $< -20^{\circ}\text{C}$ ), a minimum 120  $\mu\text{F}$  electrolytic capacitor on the output pin is recommended. A correct capacitor type with capacitor voltage rating and temperature characteristics must be properly chosen so that capacitance value does not drop too low at the extremely low temperature operation. A recommended capacitor should have temperature characteristics of less than a 10% variation of capacitance change when operated at extremely low temperatures. Our recommended aluminum electrolytic capacitor type is Panasonic FC series.

#### Thermal Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults are present for extended periods of time. The AP2141D/AP2151D implements thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately  $140^{\circ}\text{C}$ , the Thermal protection feature gets activated as follows: The internal thermal sense circuitry turns the power switch off and the FLG output is asserted thus preventing the power switch from damage. Hysteresis in the thermal sense circuit allows the device to cool down to approximately  $25^{\circ}\text{C}$  before the output is turned back on. The built-in thermal hysteresis feature avoids undesirable oscillations of the thermal protection circuit. The switch continues to cycle in this manner until the load fault is removed, resulting in a pulsed output. The FLG open-drain output is asserted when an over-current occurs with 7-ms deglitch.

#### Reverse Current Protection

In a normal MOSFET switch, current can flow in reverse direction (from the output side to the input side) when the output side voltage is higher than the input side, even when the switch is turned off. A reverse-current blocking feature is implemented in the AP21x1 series to prevent such back currents. This circuit is activated by the difference between the output voltage and the input voltage. When the switch is disabled, this feature blocks reverse current flow from the output back to the input.

## Application Information (continued)

### Special Functions:

#### Discharge Function

When enable is de-asserted, the discharge function is active. The output capacitor is discharged through an internal NMOS that has a discharge resistance of 100Ω. Hence, the output voltage drops down to zero. The time taken for discharge is dependent on the RC time constant of the resistance and the output capacitor.

#### FLG Response

The FLG open-drain output goes active low for any of the two conditions: Over-Current or Over-Temperature. The time from when a fault condition is encountered to when the FLG output goes low is 7-ms (typ). The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary Over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The 7-ms timeout is also applicable for Over-current recovery and Thermal recovery. The AP2141D/AP2151D are designed to eliminate erroneous Over-current reporting without the need for external components, such as an RC delay network.

#### Power Supply Considerations

A 0.01-μF to 0.1-μF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. This limits the input voltage drop during line transients. Placing a high-value electrolytic capacitor on the input (10-μF minimum) and output pin(s) is recommended when the output load is heavy. This precaution also reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients. This capacitor also prevents the output from going negative during turn-off due to inductive parasitics.

#### Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ( $T_A$ ) and  $R_{DS(ON)}$ , the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

The junction temperature can be calculated by:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

- $T_A$  = Ambient Temperature °C
- $R_{\theta JA}$  = Thermal Resistance
- $P_D$  = Total Power Dissipation

#### Generic Hot-Plug Applications

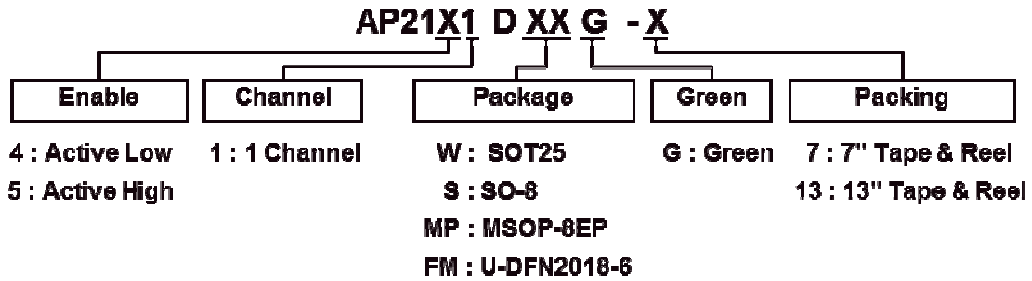
In many applications it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges as seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp up the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise and fall times of the AP2141D/AP2151D, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2141D/AP2151D also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2141D/AP2151D between the VCC input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls the system surge current and provides a hot-plugging mechanism for any device.

#### Dual-Purpose Port Applications

AP2141D/AP2151D is not recommended for use in dual-purpose port applications in which a single port is used for data communication between the host and peripheral devices while simultaneously maintaining a charge to the battery of the peripheral device. An example of such a non-recommended application is a shared HDMI/MHL (Mobile High-definition Link) port that allows streaming video between an HDTV or set-top box and a smartphone or tablet while maintaining a charge to the smartphone or tablet battery. Since the AP2141D/AP2151D includes an embedded discharge feature that discharges the output load of the device when the device is disabled, the batteries of the connected peripheral device will be subject to continual discharge whenever the AP2141D/AP2151D is disabled. An overstress condition to the device's discharge MOS transistor may result. In addition, if the output of the AP2141D/AP2151D is subjected to a constant voltage that would be present during a dual-purpose port application such as MHL, an overstress condition to the device may result.

**Ordering Information**

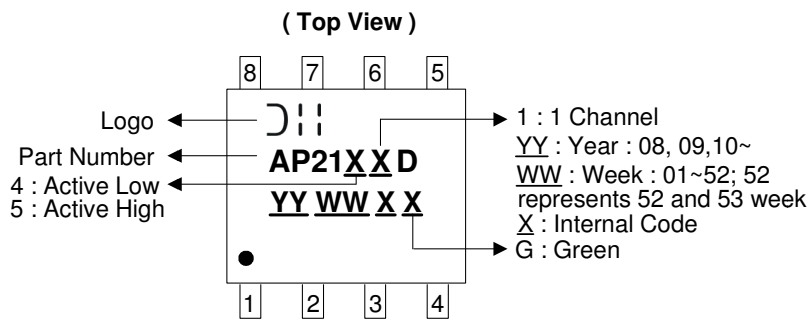


| Part Number   | Package Code | Packaging   | 7"/13" Tape and Reel |                    |
|---------------|--------------|-------------|----------------------|--------------------|
|               |              |             | Quantity             | Part Number Suffix |
| AP21X1DSG-13  | S            | SO-8        | 2,500/Tape & Reel    | -13                |
| AP21X1DMPG-13 | MP           | MSOP-8EP    | 2,500/Tape & Reel    | -13                |
| AP21X1DWG-7   | W            | SOT25       | 3,000/Tape & Reel    | -7                 |
| AP21X1DFMG-7  | FM           | U-DFN2018-6 | 3,000/Tape & Reel    | -7                 |

Note: 9. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

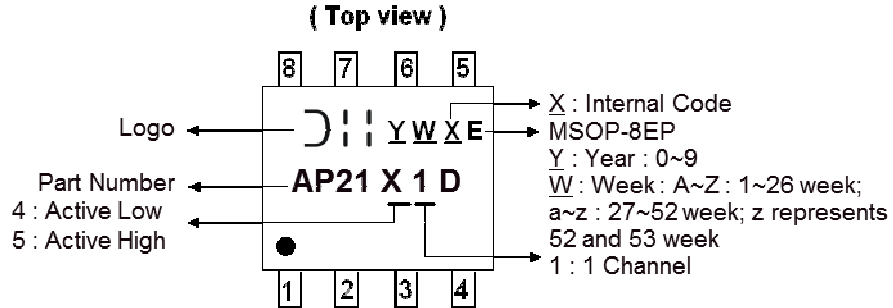
**Marking Information**

(1) SO-8

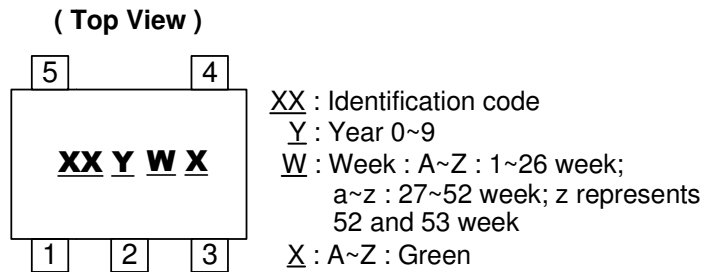


**Marking Information** (continued)

(2) MSOP-8EP



(3) SOT25



| Device   | Package Type | Identification Code |
|----------|--------------|---------------------|
| AP2141DW | SOT25        | JA                  |
| AP2151DW | SOT25        | JB                  |

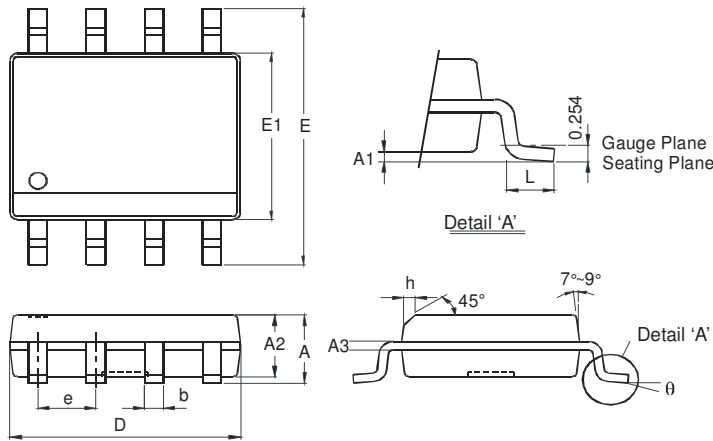
(4) U-DFN2018-6

| Device    | Package type | Identification Code |
|-----------|--------------|---------------------|
| AP2141DFM | U-DFN2018-6  | JA                  |
| AP2151DFM | U-DFN2018-6  | JB                  |

**Package Outline Dimensions** (All dimensions in mm.)

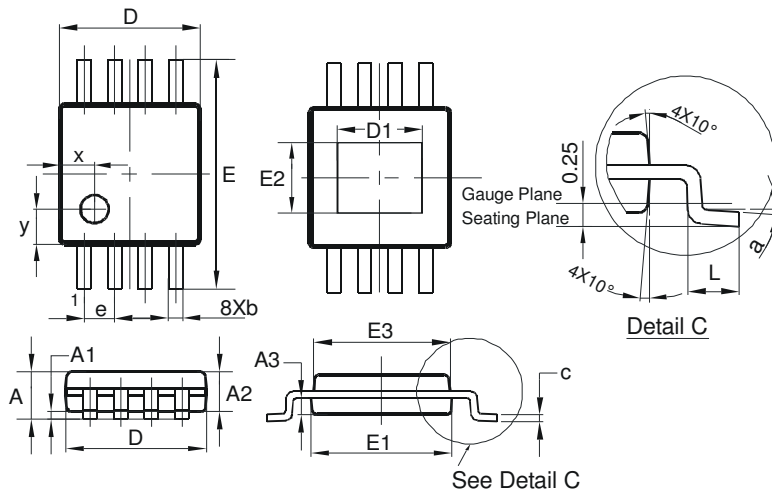
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.

(1) Package type: SO-8



| SO-8                 |          |      |
|----------------------|----------|------|
| Dim                  | Min      | Max  |
| A                    | -        | 1.75 |
| A1                   | 0.10     | 0.20 |
| A2                   | 1.30     | 1.50 |
| A3                   | 0.15     | 0.25 |
| b                    | 0.3      | 0.5  |
| D                    | 4.85     | 4.95 |
| E                    | 5.90     | 6.10 |
| E1                   | 3.85     | 3.95 |
| e                    | 1.27 Typ |      |
| h                    | -        | 0.35 |
| L                    | 0.62     | 0.82 |
| θ                    | 0°       | 8°   |
| All Dimensions in mm |          |      |

(2) Package Type: MSOP-8EP

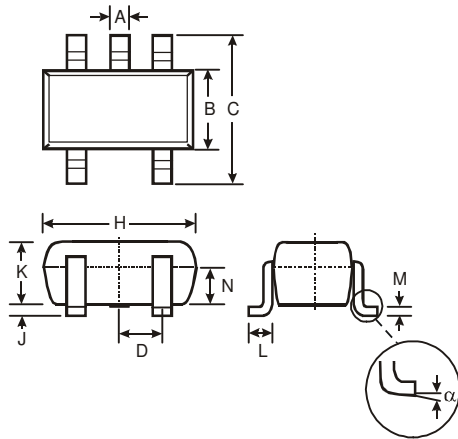


| MSOP-8EP             |      |      |       |
|----------------------|------|------|-------|
| Dim                  | Min  | Max  | Typ   |
| A                    | -    | 1.10 | -     |
| A1                   | 0.05 | 0.15 | 0.10  |
| A2                   | 0.75 | 0.95 | 0.86  |
| A3                   | 0.29 | 0.49 | 0.39  |
| b                    | 0.22 | 0.38 | 0.30  |
| c                    | 0.08 | 0.23 | 0.15  |
| D                    | 2.90 | 3.10 | 3.00  |
| D1                   | 1.60 | 2.00 | 1.80  |
| E                    | 4.70 | 5.10 | 4.90  |
| E1                   | 2.90 | 3.10 | 3.00  |
| E2                   | 1.30 | 1.70 | 1.50  |
| E3                   | 2.85 | 3.05 | 2.95  |
| e                    | -    | -    | 0.65  |
| L                    | 0.40 | 0.80 | 0.60  |
| a                    | 0°   | 8°   | 4°    |
| x                    | -    | -    | 0.750 |
| y                    | -    | -    | 0.750 |
| All Dimensions in mm |      |      |       |

**Package Outline Dimensions** (continued) (All dimensions in mm.)

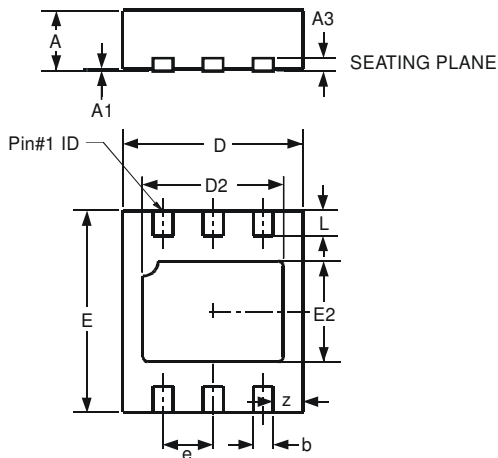
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.

(3) Package Type: SOT25



| SOT25                |       |      |      |
|----------------------|-------|------|------|
| Dim                  | Min   | Max  | Typ  |
| A                    | 0.35  | 0.50 | 0.38 |
| B                    | 1.50  | 1.70 | 1.60 |
| C                    | 2.70  | 3.00 | 2.80 |
| D                    | —     | —    | 0.95 |
| H                    | 2.90  | 3.10 | 3.00 |
| J                    | 0.013 | 0.10 | 0.05 |
| K                    | 1.00  | 1.30 | 1.10 |
| L                    | 0.35  | 0.55 | 0.40 |
| M                    | 0.10  | 0.20 | 0.15 |
| N                    | 0.70  | 0.80 | 0.75 |
| α                    | 0°    | 8°   | —    |
| All Dimensions in mm |       |      |      |

(4) Package Type: U-DFN2018-6

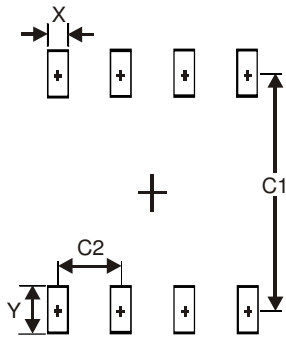


| U-DFN2018-6          |       |       |       |
|----------------------|-------|-------|-------|
| Dim                  | Min   | Max   | Typ   |
| A                    | 0.545 | 0.605 | 0.575 |
| A1                   | 0     | 0.05  | 0.02  |
| A3                   | —     | —     | 0.13  |
| b                    | 0.15  | 0.25  | 0.20  |
| D                    | 1.750 | 1.875 | 1.80  |
| D2                   | 1.30  | 1.50  | 1.40  |
| e                    | —     | —     | 0.50  |
| E                    | 1.95  | 2.075 | 2.00  |
| E2                   | 0.90  | 1.10  | 1.00  |
| L                    | 0.20  | 0.30  | 0.25  |
| z                    | —     | —     | 0.30  |
| All Dimensions in mm |       |       |       |

## Suggested Pad Layout

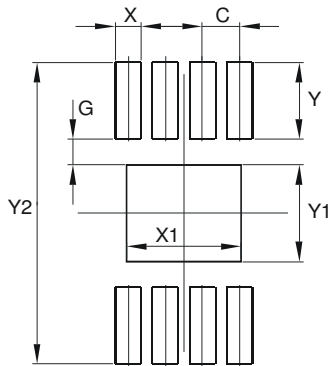
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

### (1) Package Type: SO-8



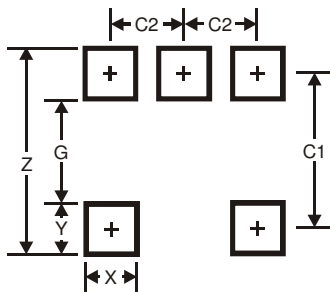
| Dimensions | Value (in mm) |
|------------|---------------|
| X          | 0.60          |
| Y          | 1.55          |
| C1         | 5.4           |
| C2         | 1.27          |

### (2) Package Type: MSOP-8EP



| Dimensions | Value (in mm) |
|------------|---------------|
| C          | 0.650         |
| G          | 0.450         |
| X          | 0.450         |
| X1         | 2.000         |
| Y          | 1.350         |
| Y1         | 1.700         |
| Y2         | 5.300         |

### (3) Package Type: SOT25

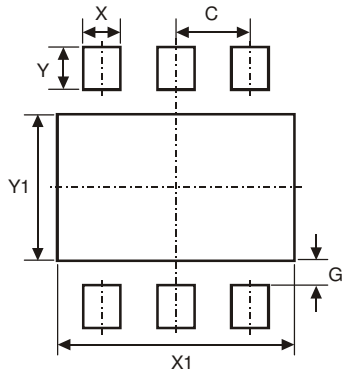


| Dimensions | Value (in mm) |
|------------|---------------|
| Z          | 3.20          |
| G          | 1.60          |
| X          | 0.55          |
| Y          | 0.80          |
| C1         | 2.40          |
| C2         | 0.95          |

**Suggested Pad Layout** (continued)

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

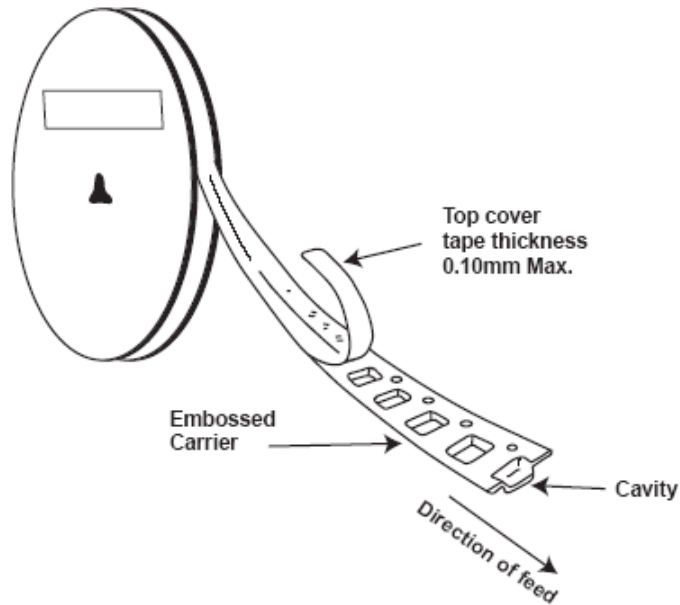
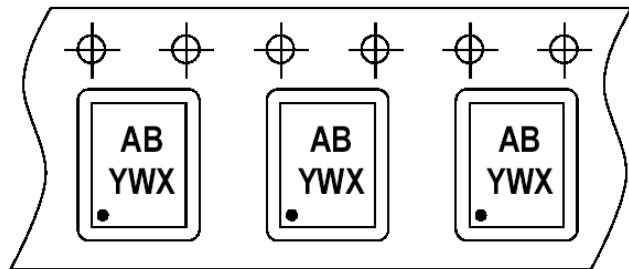
(4) Package type: U-DFN2018-6



| Dimensions | Value (in mm) |
|------------|---------------|
| C          | 0.50          |
| G          | 0.20          |
| X          | 0.25          |
| X1         | 1.60          |
| Y          | 0.35          |
| Y1         | 1.20          |

**Taping Orientation** (Note 10)

For U-DFN2018-6



Note: 10. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

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