



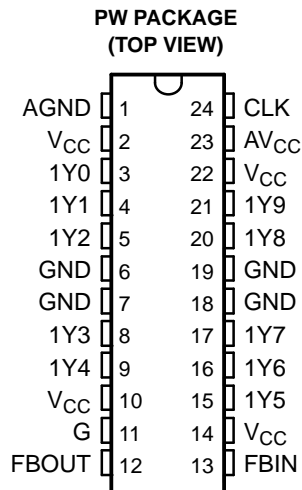
**THE DATASHEET OF
CDCVF2510PW**



3.3-V PHASE-LOCK LOOP CLOCK DRIVER

FEATURES

- Designed to Meet and Exceed PC133 SDRAM Registered DIMM Specification Rev. 1.1
- Spread Spectrum Clock Compatible
- Operating Frequency 50 MHz to 175 MHz
- Static Phase Error Distribution at 66 MHz to 166 MHz Is ± 125 ps
- Jitter (cyc - cyc) at 66 MHz to 166 MHz Is $|70|$ ps
- Advanced Deep Submicron Process Results in More Than 40% Lower Power Consumption Versus Current Generation PC133 Devices
- Available in Plastic 24-Pin TSSOP
- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes One Clock Input to One Bank of 10 Outputs
- External Feedback (FBIN) Terminal Is Used to Synchronize the Outputs to the Clock Input
- 25- Ω On-Chip Series Damping Resistors
- No External RC Network Required
- Operates at 3.3 V



**NOT RECOMMENDED
FOR NEW DESIGNS
USE CDCVF2510A AS
A REPLACEMENT**

DESCRIPTION

The CDCVF2510 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDCVF2510 operates at a 3.3-V V_{CC}. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of 10 outputs provides 10 low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK. Outputs are enabled or disabled via the control (G) input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDCVF2510 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDCVF2510 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, a fixed-phase signal at CLK, or following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

The CDCVF2510 is characterized for operation from 0°C to 85°C.

For application information see the application reports *High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516* (SLMA003) and *Using CDC2509A/2510A PLL With Spread Spectrum Clocking (SSC)* (SCAA039).

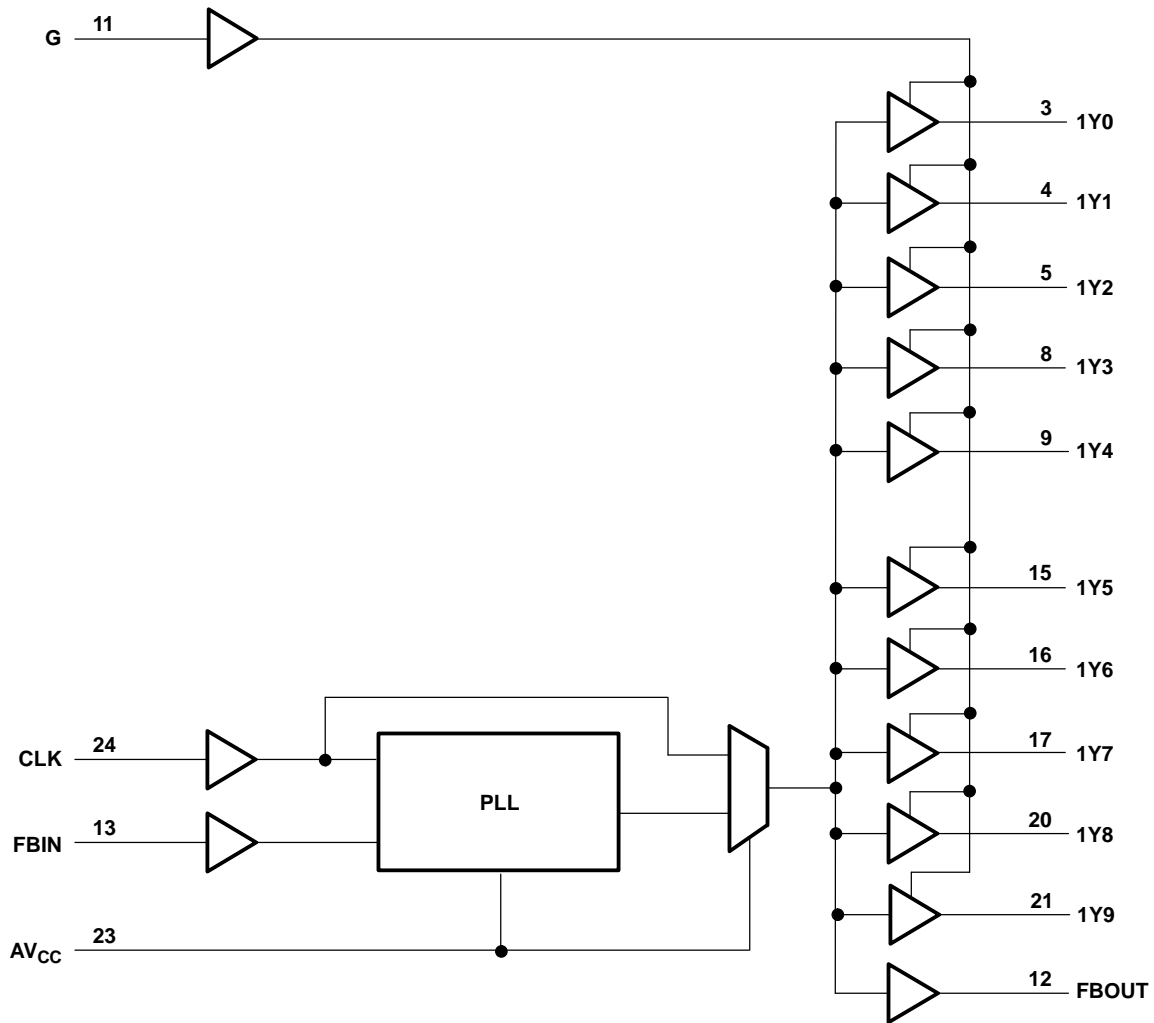


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE

INPUTS		OUTPUTS	
G	CLK	1Y (0:9)	FBOUT
X	L	L	L
L	H	L	H
H	H	H	H

FUNCTIONAL BLOCK DIAGRAM



AVAILABLE OPTIONS

T _A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 85°C	CDCVF2510PWR
	CDCVF2510PW

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDCVF2510 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs 1Y(0:9). When G is low, outputs 1Y(0:9) are disabled to a logic-low state. When G is high, all outputs 1Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25-Ω series-damping resistor.
1Y (0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by deasserting the G control input. Each output has an integrated 25-Ω series-damping resistor.
AV _{CC}	23	Power	Analog power supply. AV _{CC} provides the power reference for the analog circuitry. In addition, AV _{CC} can be used to bypass the PLL for test purposes. When AV _{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V _{CC}	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		UNIT
AV _{CC} ⁽²⁾	Supply voltage range	AV _{CC} < V _{CC} + 0.7 V
V _{CC}	Supply voltage range	-0.5 V to 4.3 V
V _I ⁽³⁾	Input voltage range	-0.5 V to 4.6 V
V _O ⁽⁴⁾	Voltage range applied to any output in the high or low state	-0.5 V to V _{CC} + 0.5 V
I _{IK} (V _I < 0)	Input clamp current	-50 mA
I _{OK} (V _O < 0 or V _O > V _{CC})	Output clamp current	±50 mA
I _O (V _O = 0 to V _{CC})	Continuous output current	±50 mA
V _{CC} or GND	Continuous current through each	±100 mA
T _A = 55°C (in still air) ⁽⁵⁾	Maximum power dissipation	0.7 W
T _{stg}	Storage temperature range	-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) AV_{CC} must not exceed V_{CC} + 0.7 V.

(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) This value is limited to 4.6 V maximum.

(5) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, see the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book* (SCBD002).

DISSIPATION RATING TABLE

PACKAGE	BOARD TYPE ⁽¹⁾	$R_{\theta JA}$	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽²⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PW	JEDEC low-K	114.5°C/W	920 mW	8.7 mW/°C	520 mW	390 mW
	JEDEC high-K	62.1°C/W	1690 mW	16.1 mW/°C	960 mW	720 mW

- (1) JEDEC high-K board has better thermal performance due to multiple internal copper planes.
(2) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).

RECOMMENDED OPERATING CONDITIONS ⁽¹⁾

		MIN	MAX	UNIT
V_{CC}, AV_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		-12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	85	°C

- (1) Unused inputs must be held high or low to prevent them from floating.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{clk}	Clock frequency ⁽¹⁾	50	175	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time ⁽²⁾		1	ms

- (1) To avoid any self oscillation of the PLL, a continuous clock signal has to be present at the clock input.
(2) Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the *Switching Characteristics* table are not applicable. This parameter does not apply for input modulation under SSC application.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}, AV_{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA	3 V		-1.2	V
V_{OH}	High-level output voltage	$I_{OH} = -100$ μ A	MIN to MAX	$V_{CC}-0.2$		V
		$I_{OH} = -12$ mA	3 V	2.1		
		$I_{OH} = -6$ mA	3 V	2.4		
V_{OL}	Low-level output voltage	$I_{OL} = 100$ μ A	MIN to MAX		0.2	V
		$I_{OL} = 12$ mA	3 V		0.8	
		$I_{OL} = 6$ mA	3 V		0.55	
I_{OH}	High-level output current	$V_O = 1$ V	3 V	-28		mA
		$V_O = 1.65$ V	3.3 V		-36	
		$V_O = 3.135$ V	3.6 V		-8	
I_{OL}	Low-level output current	$V_O = 1.95$ V	3 V	30		mA
		$V_O = 1.65$ V	3.3 V		40	
		$V_O = 0.4$ V	3.6 V		10	
I_I	Input current	$V_I = V_{CC}$ or GND	3.6 V		± 5	μ A

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} , AV _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{CC} ⁽²⁾	Supply current (static, output not switching) V _I = V _{CC} or GND, I _O = 0, Outputs: low or high	3.6 V, 0 V			40	μA
ΔI _{CC}	Change in supply current One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3.3 V to 3.6 V			500	μA
C _i	Input capacitance V _I = V _{CC} or GND	3.3 V		2.5		pF
C _o	Output capacitance V _O = V _{CC} or GND	3.3 V		2.8		pF

(2) For dynamic I_{CC} vs Frequency, see [Figure 8](#) and [Figure 9](#).

SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF, See ⁽¹⁾ and [Figure 1](#) and [Figure 2](#)

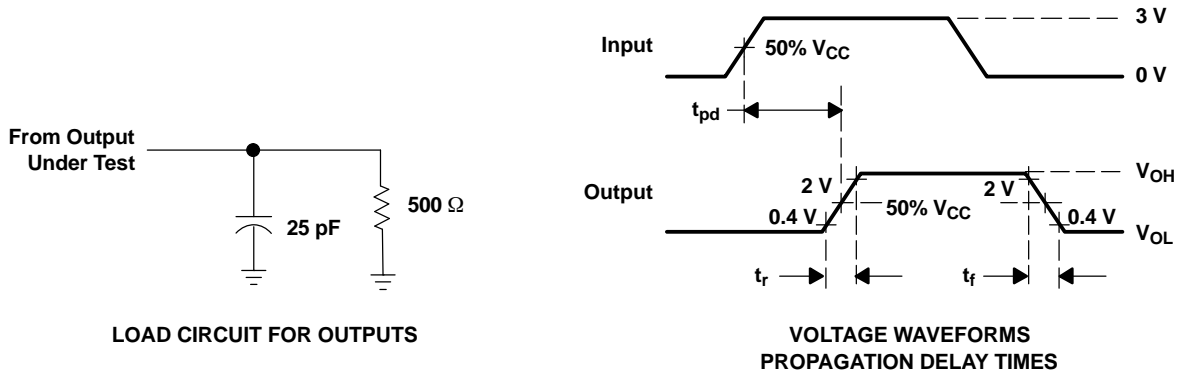
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} , AV _{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP	MAX	
Phase error time-static (normalized), See Figure 3 through Figure 6	CLK↑ = 66 MHz to 166 MHz	FBIN↑	-125		125	ps
t _{sk(o)}	Any Y	Any Y			100	ps
Phase error time-jitter ⁽³⁾	CLK = 66 MHz to 100 MHz	Any Y or FBOUT	-50		50	ps
Jitter _(cycle-cycle) : See Figure 7		Any Y or FBOUT		70		
	CLK = 100 MHz to 166 MHz	Any Y or FBOUT		65		ps
Duty cycle	f _(CLK) > 60 MHz	Any Y or FBOUT	45%		55%	
t _r	Rise time V _O = 0.4 V to 2 V	Any Y or FBOUT	0.3		1.1	ns/V
t _f	Fall time V _O = 2 V to 0.4 V	Any Y or FBOUT	0.3		1.1	ns/V
t _{PLH(bypass mode)}	Low-to-high propagation delay time, bypass mode CLK	Any Y or FBOUT	1.8		3.9	ns
t _{PHL(bypass mode)}	High-to-low propagation delay time, bypass mode CLK	Any Y or FBOUT	1.8		3.9	ns

(1) These parameters are not production tested.

(2) The t_{sk(o)} specification is only valid for equal loading of all outputs.

(3) Calculated per PC DRAM SPEC (t_{phase error, static} - jitter_(cycle-to-cycle)).

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 133$ MHz, $Z_O = 50 \Omega$, $t_r \leq 1.2$ ns, $t_f \leq 1.2$ ns.
 C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

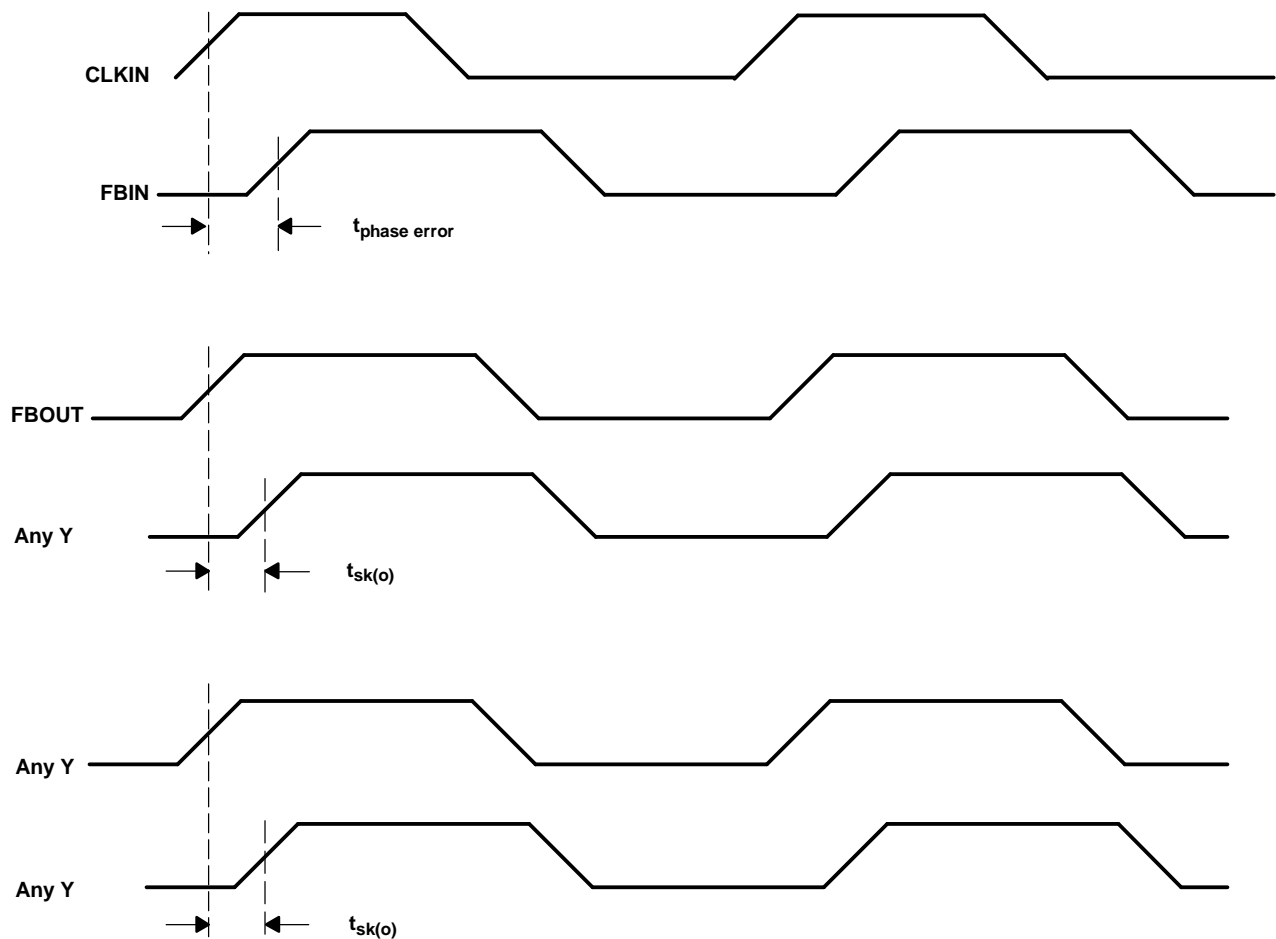


Figure 2. Phase Error and Skew Calculations

TYPICAL CHARACTERISTICS

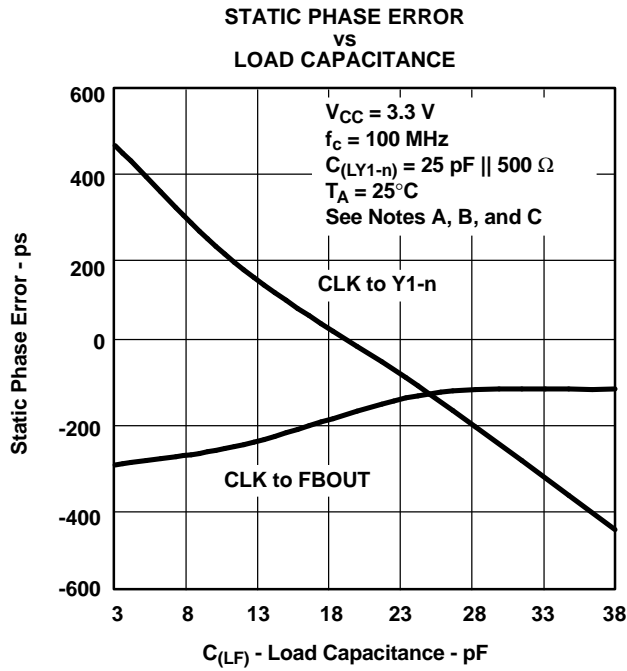


Figure 3.

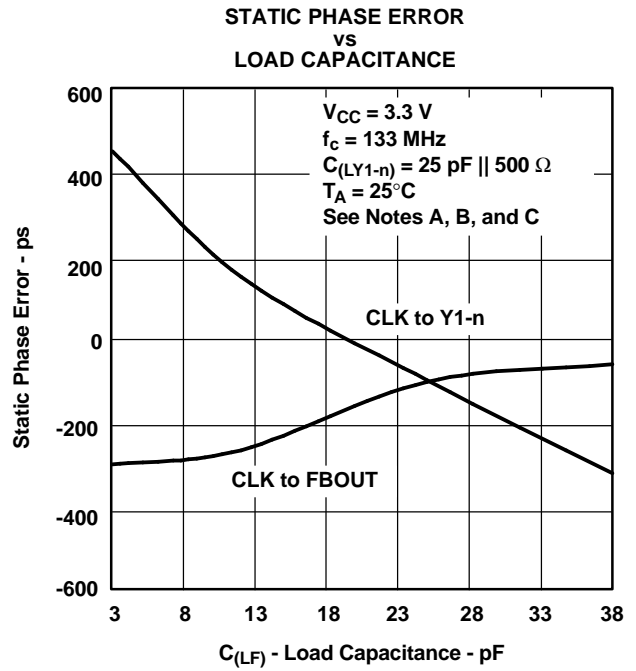


Figure 4.

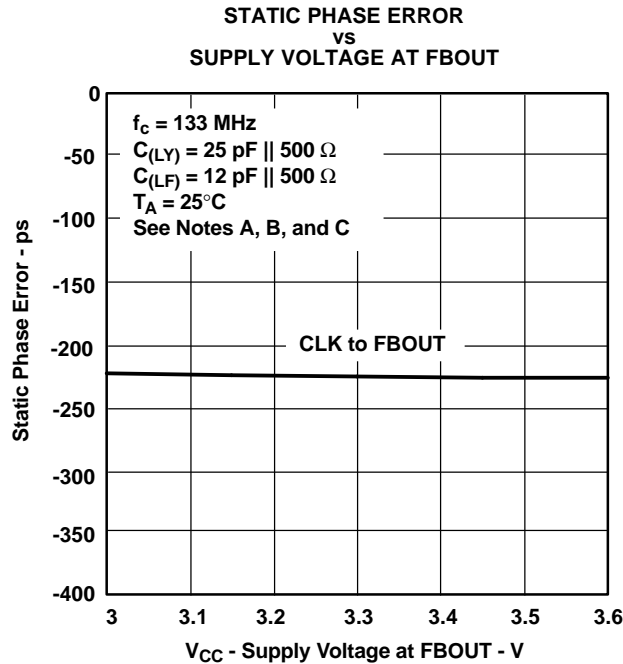
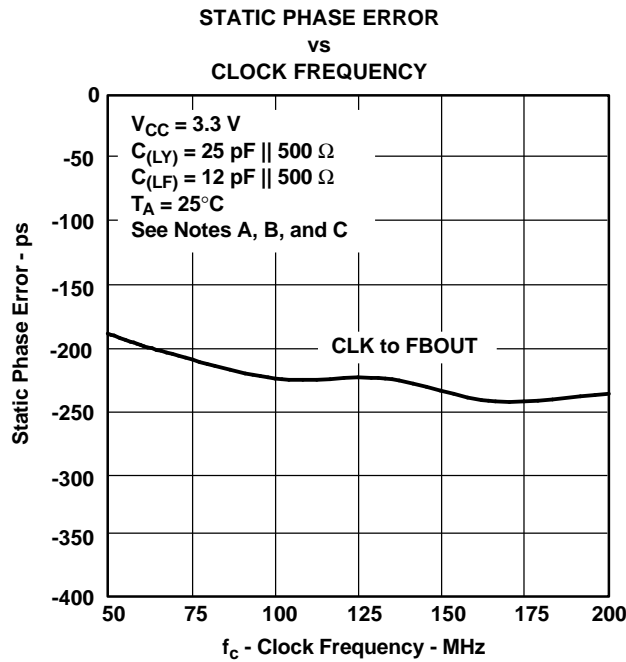


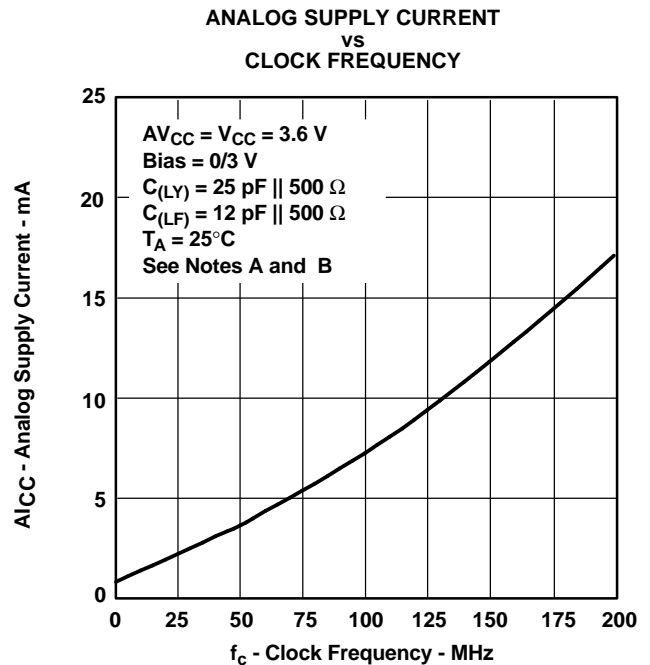
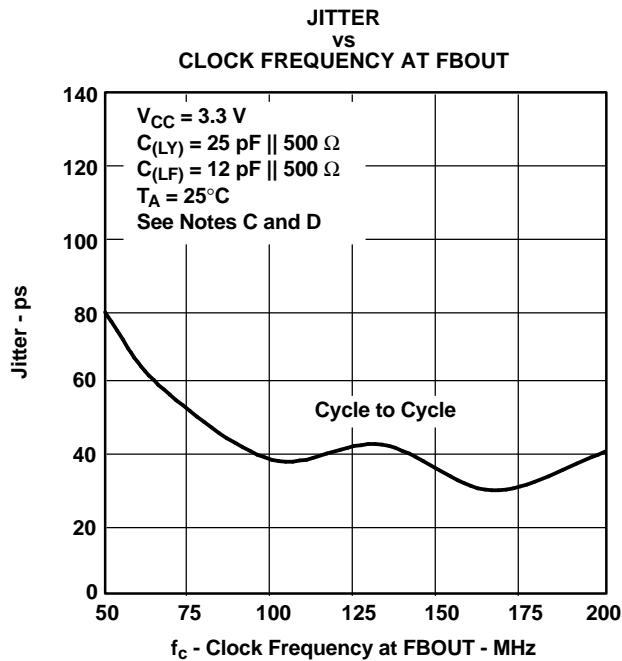
Figure 5.

TYPICAL CHARACTERISTICS (continued)

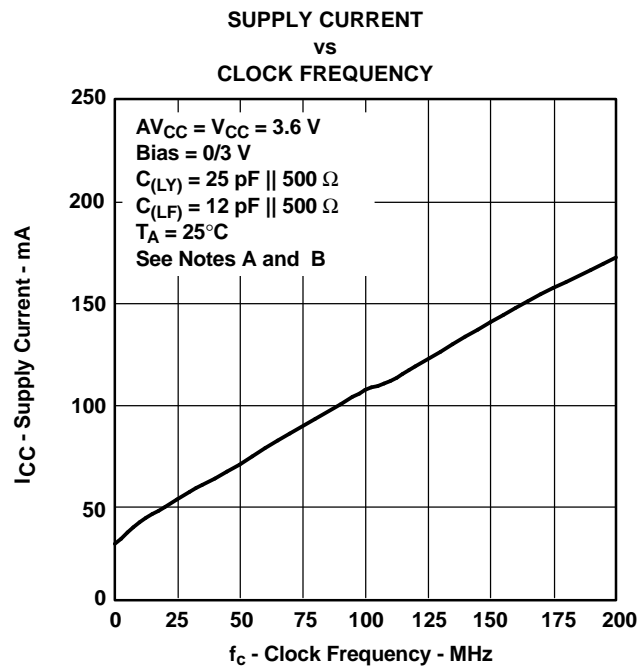


NOTE:

1. Trace length FBOUT to FBIN = 5 mm, $Z_O = 50 \Omega$
2. $C_{(LY)}$ = Lumped capacitive load Y_{1-n}
3. $C_{(LFX)}$ = Lumped feedback capacitance at FBOUT = FBIN



TYPICAL CHARACTERISTICS (continued)



NOTE:

1. Trace length FBOUT to FBIN = 5 mm, $Z_0 = 50 \Omega$
2. Total current = $I_{CC} + A I_{CC}$
3. $C_{(LY)}$ = Lumped capacitive load Y_{1-n}
4. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2510PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510	Samples
CDCVF2510PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510	Samples
CDCVF2510PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510	Samples
CDCVF2510PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510	Samples
HPA00015PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2510PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

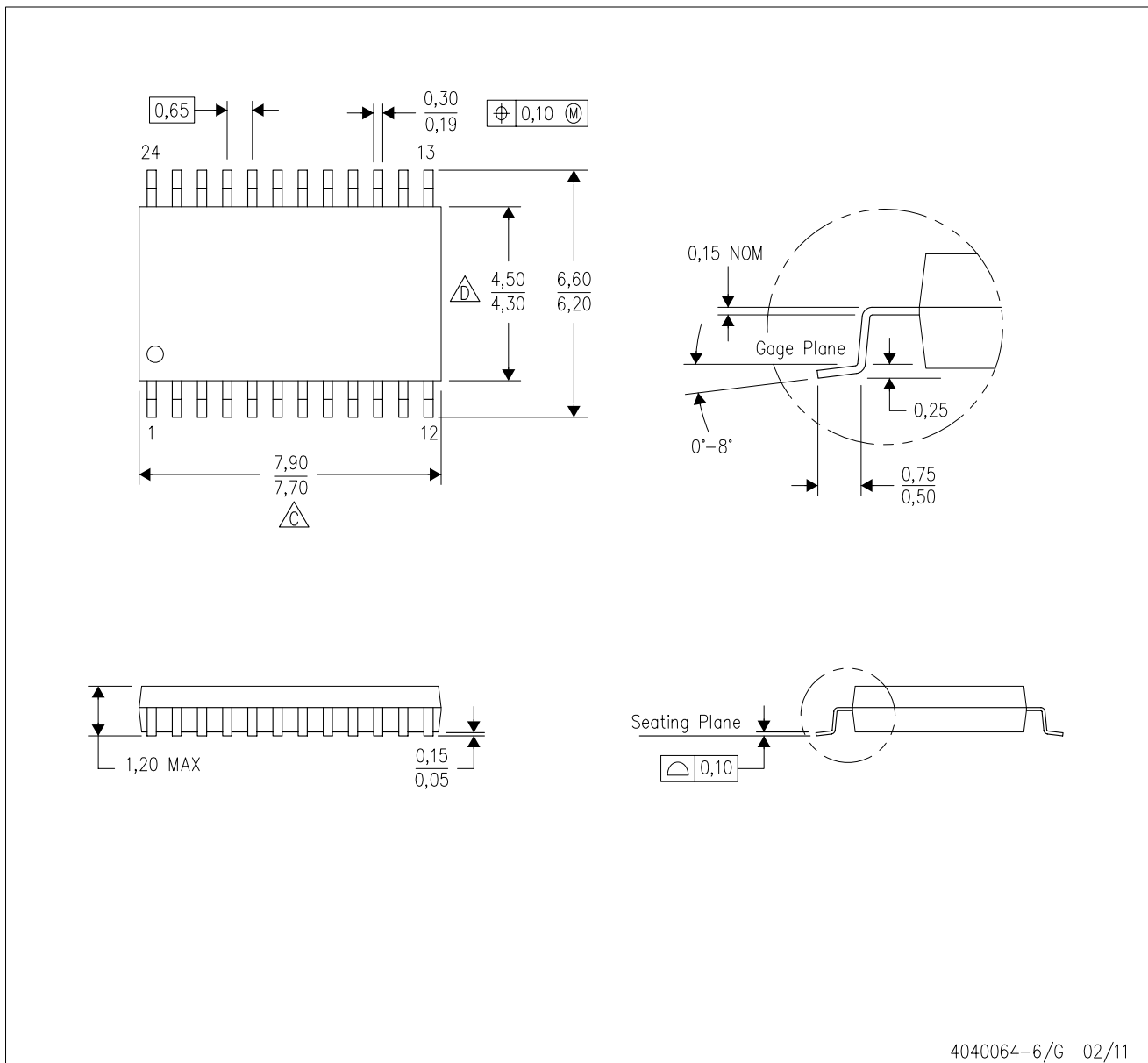


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2510PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

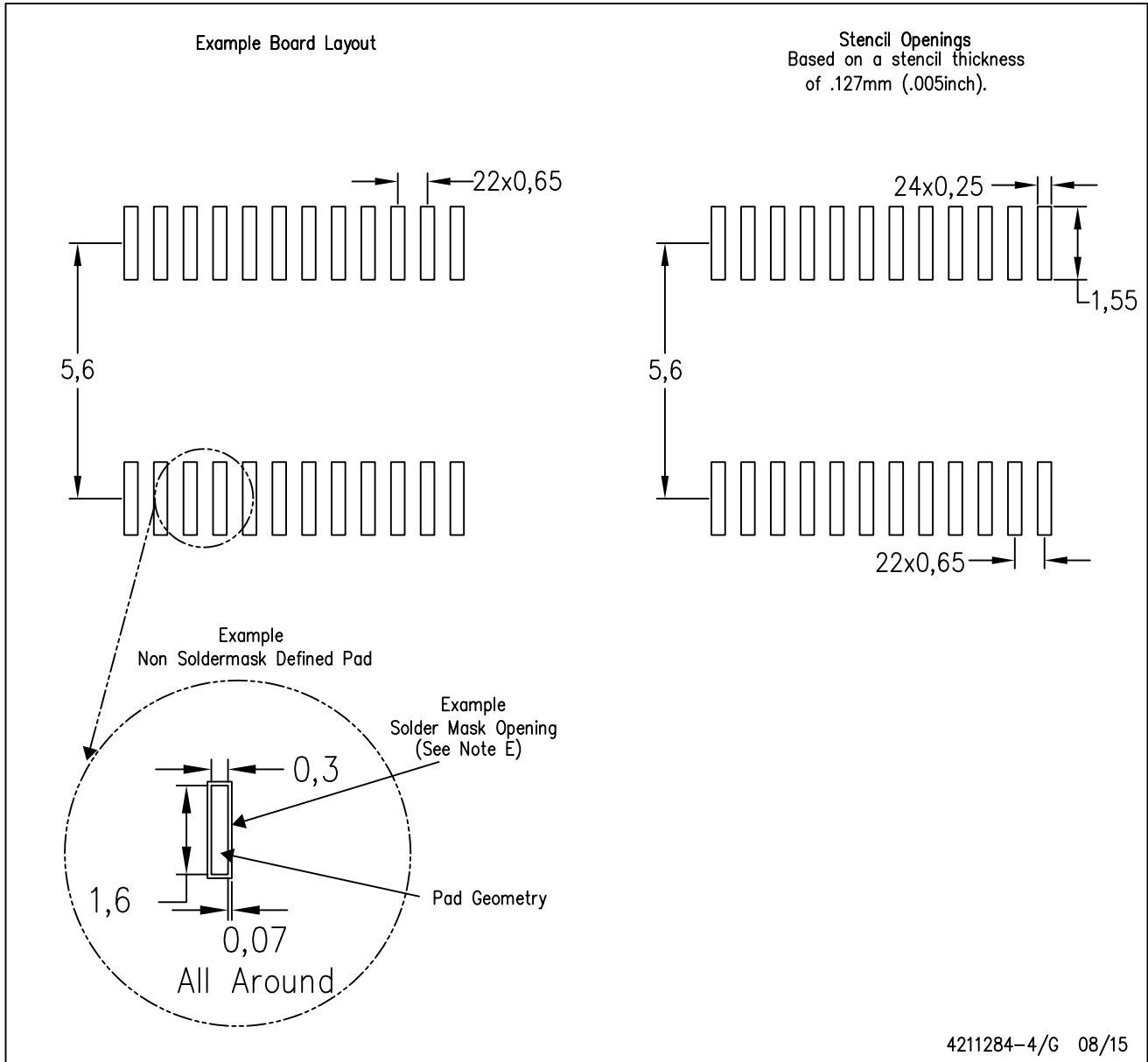


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View CDCVF2510PW](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management