# THE DATASHEET OF

# CY8C24423A-12PVXE

www.win-source.net 0086-755-83957316

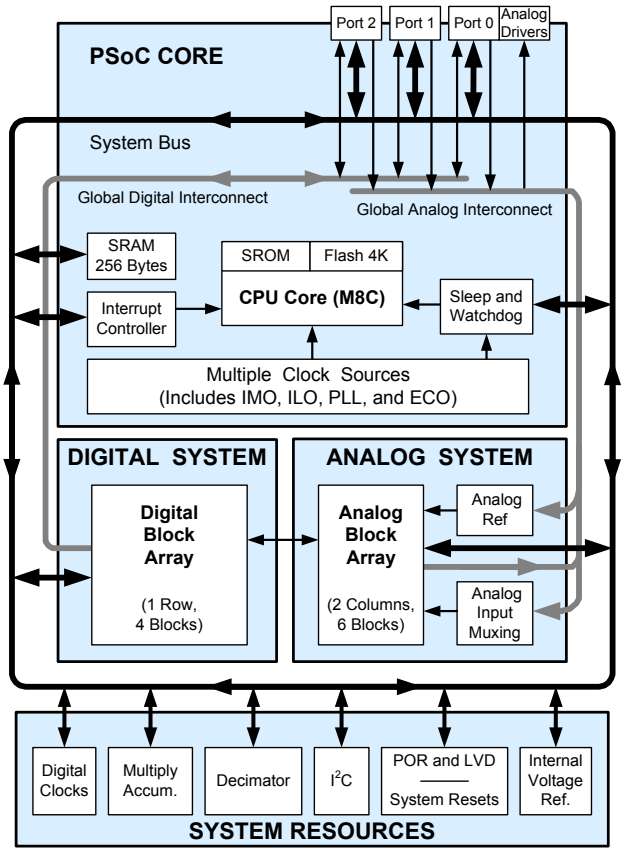
CY8C24223A, CY8C24423A

# Automotive - Extended Temperature PSoC® Programmable System-on-Chip

## Features

- AEC qualified
- Powerful Harvard architecture processor
  - M8C processor speeds up to 12 MHz
  - 8x8 multiply, 32-bit accumulate
  - Low power at high speed
  - 4.75V to 5.25V operating voltage
  - Automotive temperature range: -40°C to +125°C
- Advanced peripherals (PSoC® blocks)
  - Six rail-to-rail analog PSoC blocks provide:
    - Up to 14-Bit Analog-to-Digital Converters (ADCs)
    - Up to 9-Bit Digital-to-Analog Converters (DACs)
    - Programmable Gain Amplifiers (PGAs)
    - Programmable filters and comparators
  - Four digital PSoC blocks provide:
    - 8- to 32-bit timers and counters, 8- and 16-bit pulse-width modulators (PWMs)
    - CRC and PRS modules
    - Full- or Half-Duplex UART
    - SPI master or slave
    - Connectable to all General Purpose I/O (GPIO) pins
  - Complex peripherals by combining blocks
- Precision, programmable clocking
  - Internal ±4% 24 MHz oscillator
  - High accuracy 24 MHz with optional 32 kHz crystal and Phase Locked Loop (PLL)
  - Optional external oscillator, up to 24 MHz
  - Internal low speed, low power oscillator for Watchdog and Sleep functionality
- Flexible on-chip memory
  - 4K bytes Flash program storage, 100 erase/write cycles
  - 256 bytes SRAM data storage
  - In-System Serial Programming (ISSP)
  - Partial Flash updates
  - Flexible protection modes
  - EEPROM emulation in Flash
- Programmable pin configurations
  - 25 mA Sink, 10 mA Drive on all GPIO
  - Pull up, pull down, High Z, strong, or open drain drive modes on all GPIO
  - Up to 12 analog inputs on GPIO[1]
  - Two 30 mA analog outputs on GPIO
  - Configurable interrupt on all GPIO
- Additional system resources
  - I²C™ slave, master, or multi-master operation up to 400 kHz
  - Watchdog and Sleep timers
  - User-configurable Low Voltage Detection (LVD)
  - Integrated supervisory circuit
  - On-chip precision voltage reference
- Complete development tools
  - Free development software (PSoC Designer™)
  - Full Featured, In-Circuit Emulator (ICE) and Programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128K bytes trace memory

## Logic Block Diagram




**Note**
1. There are eight standard analog inputs on the GPIO. The other four analog inputs connect from the GPIO directly to specific switched-capacitor block inputs. See the *PSoC Technical Reference Manual* for more details

## Contents


**PSoC Functional Overview ..... 3**
PSoC Core ..... 3
Digital System ..... 3
Analog System ..... 4
Additional System Resources ..... 5
PSoC Device Characteristics ..... 5
**Getting Started ..... 5**
Application Notes ..... 5
Development Kits ..... 5
Training ..... 5
CYPros Consultants ..... 5
Solutions Library ..... 5
Technical Support ..... 5
**Development Tools ..... 6**
PSoC Designer Software Subsystems ..... 6
**Designing with PSoC Designer ..... 7**
Select User Modules ..... 7
Configure User Modules ..... 7
Organize and Connect ..... 7
Generate, Verify, and Debug ..... 7
**Document Conventions ..... 8**
Acronyms Used ..... 8
Units of Measure ..... 8
Numeric Naming ..... 8
**Pinouts ..... 9**
20-Pin Part Pinout ..... 9
28-Pin Part Pinout ..... 10
**Registers ..... 11**
Register Conventions ..... 11
Register Mapping Tables ..... 11
**Electrical Specifications ..... 14**
Absolute Maximum Ratings ..... 15
Operating Temperature ..... 15
DC Electrical Characteristics ..... 16
AC Electrical Characteristics ..... 21
**Packaging Information ..... 28**
Thermal Impedances ..... 29
Capacitance on Crystal Pins ..... 29
Solder Reflow Specifications ..... 29
**Development Tool Selection ..... 30**
Software ..... 30
Development Kits ..... 30
Evaluation Tools ..... 30
Device Programmers ..... 31
Accessories (Emulation and Programming) ..... 31
**Ordering Information ..... 32**
Ordering Code Definitions ..... 32
**Document History Page ..... 33**
**Sales, Solutions, and Legal Information ..... 34**
Worldwide Sales and Design Support ..... 34
Products ..... 34
PSoC® Solutions ..... 34
Cypress Developer Community ..... 34
Technical Support ..... 34

## PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip Controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the Logic Block Diagram on page 1, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global buses allow all the device resources to be combined into a complete custom system. Each CY8C24x23A PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, up to 24 GPIO are also included. The GPIO provide access to the global digital and analog interconnects.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO.

The M8C CPU core is a powerful processor with speeds up to 12 MHz, providing a two MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with multiple vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep Timer and Watchdog Timer (WDT).

Memory includes 4 KB of Flash for program storage and 256 bytes of SRAM for data storage. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

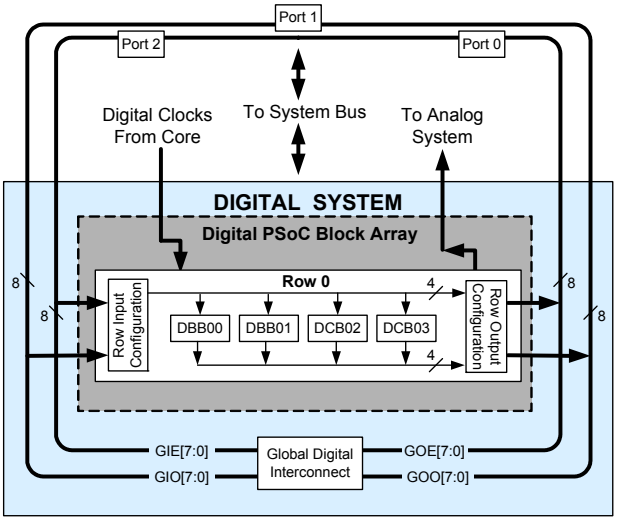
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to ±4% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the Sleep Timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt.

### Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user modules.

**Figure 1. Digital System Block Diagram**




Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with Dead Band (8- and 16-bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full or Half-Duplex 8-bit UART with selectable parity
- SPI master and slave
- $I^2C$ master, slave, or multi-master
- Cyclical Redundancy Checker/Generator (16 bit)
- IrDA
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 5.

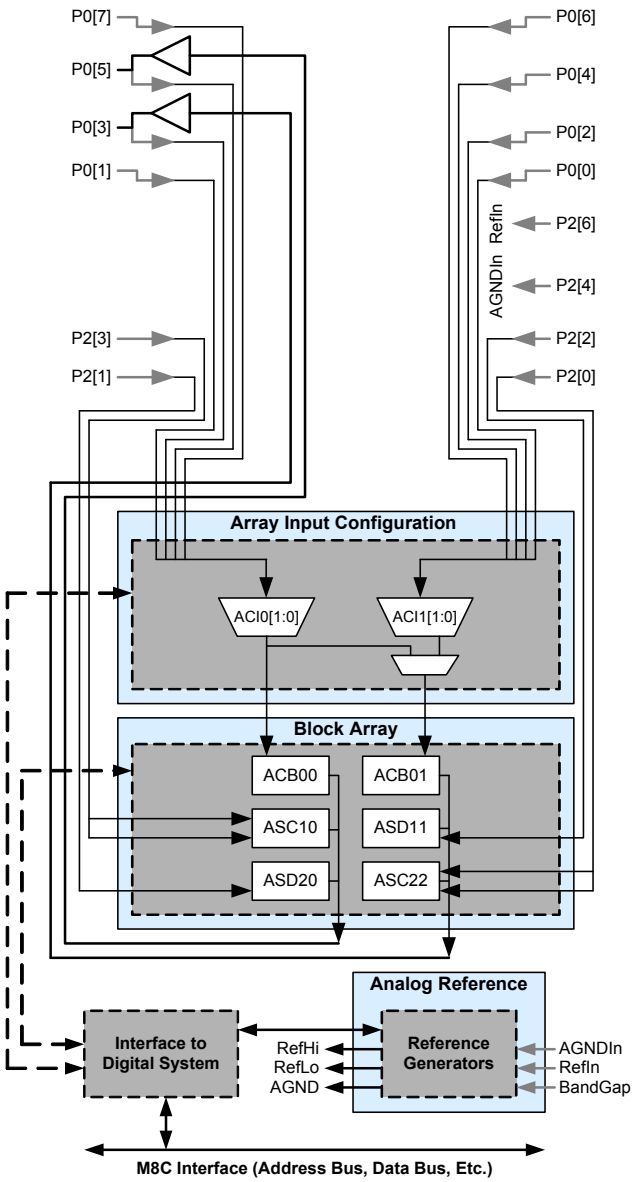
## Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- ADCs (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta-Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain up to 48x)
- Instrumentation amplifiers (one with selectable gain up to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one Continuous Time (CT) and two Switched Capacitor (SC) blocks, as shown in Figure 2.

**Figure 2. Analog System Block Diagram**



### Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful for complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The $I^2C$ module provides 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

## Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

### Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

### Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

### Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

### PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted in Table 1.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---|---|---|---|---|---|---|---|---|---|
| CY8C29x66[2] | up to 64 | 4 | 16 | 12 | 4 | 4 | 12 | 2K | 32K |
| CY8C27x43 | up to 44 | 2 | 8 | 12 | 4 | 4 | 12 | 256 Bytes | 16K |
| CY8C24x94 | 64 | 1 | 4 | 48 | 2 | 2 | 6 | 1K | 16K |
| CY8C24x23A[2] | up to 24 | 1 | 4 | 12 | 2 | 2 | 6 | 256 Bytes | 4K |
| CY8C23x33 | up to | 1 | 4 | 12 | 2 | 2 | 4 | 256 Bytes | 8K |
| CY8C21x34[2] | up to 28 | 1 | 4 | 28 | 0 | 2 | 4[3] | 512 Bytes | 8K |
| CY8C21x23 | 16 | 1 | 4 | 8 | 0 | 2 | 4[3] | 256 Bytes | 4K |
| CY8C20x34 | up to 28 | 0 | 0 | 28 | 0 | 0 | 3[3, 4] | 512 Bytes | 8K |

### CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

### Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

**Notes**
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense™ block.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software $I^2C$ slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

### PSoC Designer Software Subsystems

*Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

*Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers**. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

**C Language Compilers**. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

*Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

*In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

## Document Conventions

### Acronyms Used

The following table lists the acronyms that are used in this document.

**Table 2. Acronyms**

| Acronym | Description |
|---|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CPU | central processing unit |
| CT | continuous time |
| DAC | digital-to-analog converter |
| DC | direct current |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| FSR | full scale range |
| GPIO | general purpose I/O |
| GUI | graphical user interface |
| HBM | human body model |
| ICE | in-circuit emulator |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| I/O | input/output |
| IPOR | imprecise power on reset |
| LSb | least-significant bit |
| LVD | low voltage detect |
| MSb | most-significant bit |
| PC | program counter |
| PLL | phase-locked loop |
| POR | power on reset |
| PPOR | precision power on reset |
| PSoC® | Programmable System-on-Chip |
| PWM | pulse width modulator |
| SC | switched capacitor |
| SRAM | static random access memory |

### Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 8 on page 14 lists all the abbreviations used to measure the PSoC devices.

### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are decimal.

## Pinouts

The automotive CY8C24x23A PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

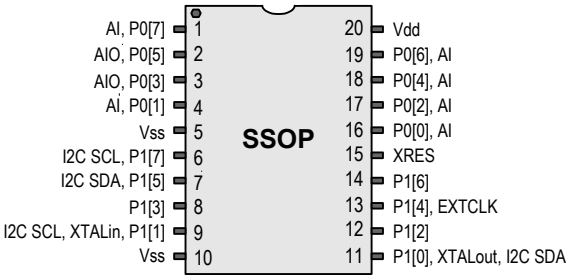
### 20-Pin Part Pinout

**Table 3. 20-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P0[7] | Analog column mux input |
| 2 | I/O | I/O | P0[5] | Analog column mux input and column output |
| 3 | I/O | I/O | P0[3] | Analog column mux input and column output |
| 4 | I/O | I | P0[1] | Analog column mux input |
| 5 | Power | | Vss | Ground connection |
| 6 | I/O | | P1[7] | $I^2C$ Serial Clock (SCL) |
| 7 | I/O | | P1[5] | $I^2C$ Serial Data (SDA) |
| 8 | I/O | | P1[3] | |
| 9 | I/O | | P1[1] | Crystal Input (XTALin), $I^2C$ Serial Clock (SCL), ISSP-SCLK[5] |
| 10 | Power | | Vss | Ground connection |
| 11 | I/O | | P1[0] | Crystal Output (XTALout), $I^2C$ Serial Data (SDA), ISSP-SDATA[5] |
| 12 | I/O | | P1[2] | |
| 13 | I/O | | P1[4] | Optional External Clock Input (EXTCLK) |
| 14 | I/O | | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull down |
| 16 | I/O | I | P0[0] | Analog column mux input |
| 17 | I/O | I | P0[2] | Analog column mux input |
| 18 | I/O | I | P0[4] | Analog column mux input |
| 19 | I/O | I | P0[6] | Analog column mux input |
| 20 | Power | | Vdd | Supply voltage |

**LEGEND**: A = Analog, I = Input, and O = Output.

**Figure 3. CY8C24223A 20-Pin PSoC Device**




**Note**
5. These are the ISSP pins, which are not High Z when coming out of POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.

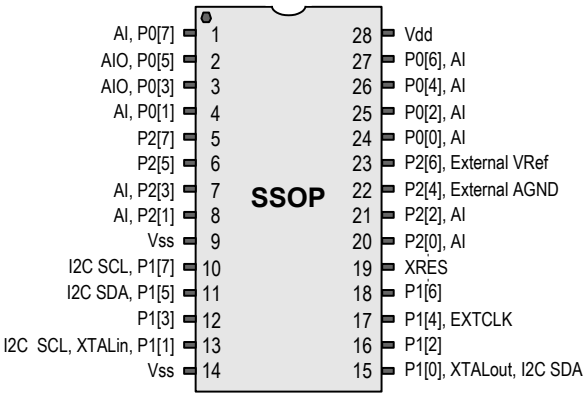
## 28-Pin Part Pinout

**Table 4. 28-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P0[7] | Analog column mux input |
| 2 | I/O | I/O | P0[5] | Analog column mux input and column output |
| 3 | I/O | I/O | P0[3] | Analog column mux input and column output |
| 4 | I/O | I | P0[1] | Analog column mux input |
| 5 | I/O | | P2[7] | |
| 6 | I/O | | P2[5] | |
| 7 | I/O | I | P2[3] | Direct switched capacitor block input |
| 8 | I/O | I | P2[1] | Direct switched capacitor block input |
| 9 | Power | | Vss | Ground connection |
| 10 | I/O | | P1[7] | $I^2C$ Serial Clock (SCL) |
| 11 | I/O | | P1[5] | $I^2C$ Serial Data (SDA) |
| 12 | I/O | | P1[3] | |
| 13 | I/O | | P1[1] | Crystal Input (XTALin), $I^2C$ Serial Clock (SCL), ISSP-SCLK[5] |
| 14 | Power | | Vss | Ground connection |
| 15 | I/O | | P1[0] | Crystal Output (XTALout), $I^2C$ Serial Data (SDA), ISSP-SDATA[5] |
| 16 | I/O | | P1[2] | |
| 17 | I/O | | P1[4] | Optional External Clock Input (EXTCLK) |
| 18 | I/O | | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull down |
| 20 | I/O | I | P2[0] | Direct switched capacitor block input |
| 21 | I/O | I | P2[2] | Direct switched capacitor block input |
| 22 | I/O | | P2[4] | External Analog Ground (AGND) |
| 23 | I/O | | P2[6] | External Voltage Reference (VRef) |
| 24 | I/O | I | P0[0] | Analog column mux input |
| 25 | I/O | I | P0[2] | Analog column mux input |
| 26 | I/O | I | P0[4] | Analog column mux input |
| 27 | I/O | I | P0[6] | Analog column mux input |
| 28 | Power | | Vdd | Supply voltage |

**LEGEND**: A = Analog, I = Input, and O = Output.

**Figure 4. CY8C24423A 28-Pin PSoC Device**



# Registers

## Register Conventions

This section lists the registers of the automotive CY8C24x23A PSoC device. For detailed register information, refer to the *PSoC Technical Reference Manual*.

The register conventions specific to this section are listed in the following table.

**Table 5. Abbreviations**

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.

**Table 6. Register Map Bank 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0GS | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | ASD20CR0 | 90 | RW | | D0 | |
| | 11 | | | 51 | | ASD20CR1 | 91 | RW | | D1 | |
| | 12 | | | 52 | | ASD20CR2 | 92 | RW | | D2 | |
| | 13 | | | 53 | | ASD20CR3 | 93 | RW | | D3 | |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | | A8 | | MUL_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | | A9 | | MUL_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | MUL_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | | AB | | MUL_DL | EB | R |
| DCB03DR0 | 2C | # | | 6C | | | AC | | ACC_DR1 | EC | RW |
| DCB03DR1 | 2D | W | | 6D | | | AD | | ACC_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | | 6E | | | AE | | ACC_DR3 | EE | RW |
| DCB03CR0 | 2F | # | | 6F | | | AF | | ACC_DR2 | EF | RW |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

**Blank fields are Reserved and must not be accessed.** # Access is bit specific.

**Table 7. Register Map Bank 1 Table: Configuration Space**

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | ASD20CR0 | 90 | RW | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | | D6 | |
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | | D7 | |
| | 18 | | | 58 | | | 98 | | | D8 | |
| | 19 | | | 59 | | | 99 | | | D9 | |
| | 1A | | | 5A | | | 9A | | | DA | |
| | 1B | | | 5B | | | 9B | | | DB | |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | | 64 | | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | | 6C | | | AC | | | EC | |
| DCB03IN | 2D | RW | | 6D | | | AD | | | ED | |
| DCB03OU | 2E | RW | | 6E | | | AE | | | EE | |
| | 2F | | | 6F | | | AF | | | EF | |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

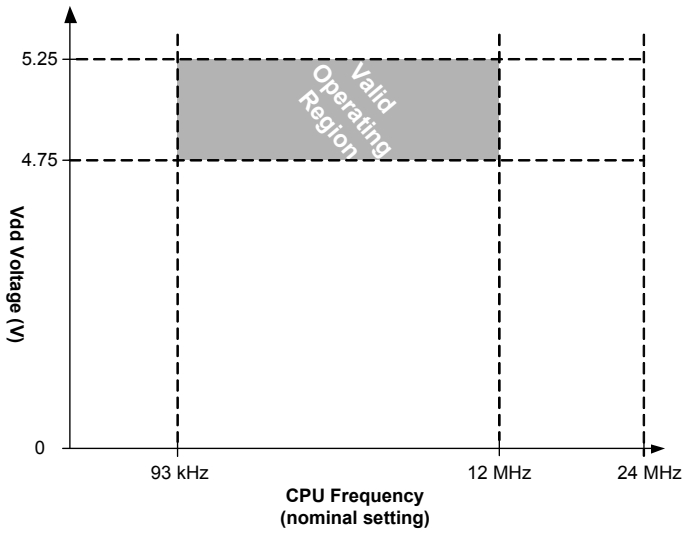
**Blank fields are Reserved and must not be accessed.** # Access is bit specific.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C24x23A PSoC device. For the latest electrical specifications, visit http://www.cypress.com.

Specifications are valid for -40°C ≤ $T_A$ ≤ 125°C and $T_J$ ≤ 135°C, except where noted.

**Figure 5. Voltage versus CPU Frequency**




The following table lists the units of measure that are used in this section.

**Table 8. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | µVrms | microvolts root-mean-square |
| dB | decibels | µW | microwatts |
| fF | femto farad | mA | milli-ampere |
| Hz | hertz | ms | milli-second |
| KB | 1024 bytes | mV | milli-volts |
| Kbit | 1024 bits | nA | nanoampere |
| kHz | kilohertz | ns | nanosecond |
| kΩ | kilohm | nV | nanovolts |
| Mbaud | megabaud | Ω | ohm |
| Mbps | megabits per second | pA | picoampere |
| MHz | megahertz | pF | picofarad |
| MΩ | megaohm | pp | peak-to-peak |
| µA | microampere | ppm | parts per million |
| µF | microfarad | ps | picosecond |
| µH | microhenry | sps | samples per second |
| µs | microsecond | σ | sigma: one standard deviation |
| µV | microvolts | V | volts |

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 9. Absolute Maximum Ratings**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -55 | +25 | +125 | °C | Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Storage temperatures above 65°C degrades reliability. Maximum combined storage and operational time at +125°C is 7000 hours. |
| $T_{BAKETEMP}$ | Bake Temperature | – | 125 | See package label | °C | |
| $T_{BAKETIME}$ | Bake Time | See package label | – | 72 | Hours | |
| $T_A$ | Ambient Temperature with Power Applied | -40 | – | +125 | °C | |
| Vdd | Supply Voltage on Vdd Relative to Vss | -0.5 | – | +6.0 | V | |
| $V_{IO}$ | DC Input Voltage | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $V_{IOZ}$ | DC Voltage Applied to Tri-state | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $I_{MIO}$ | Maximum Current into any Port Pin | -25 | – | +25 | mA | |
| ESD | Electro Static Discharge Voltage | 2000 | – | – | V | Human Body Model ESD. |
| LU | Latch up Current | – | – | 200 | mA | |

## Operating Temperature

**Table 10. Operating Temperature**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature | -40 | – | +125 | °C | |
| $T_J$ | Junction Temperature | -40 | – | +135 | °C | The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 29. The user must limit the power consumption to comply with this requirement. |

## DC Electrical Characteristics

*DC Chip-Level Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 11. DC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply Voltage | 4.75 | – | 5.25 | V | See table titled DC POR and LVD Specifications on page 20 |
| $I_{DD}$ | Supply Current | – | 5 | 8 | mA | Conditions are Vdd = 5.25V, -40°C ≤ $T_A$ ≤ 125°C, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog power = off. |
| $I_{SB}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[6] | – | 4 | 13 | µA | Conditions are with internal low speed oscillator active, Vdd = 5.25V, -40°C ≤ $T_A$ ≤ 55°C. Analog power = off. |
| $I_{SBH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[6] | – | 4 | 100 | µA | Conditions are with internal slow speed oscillator active, Vdd = 5.25V, 55°C < $T_A$ ≤ 125°C. Analog power = off. |
| $I_{SBXTL}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[6] | – | 6 | 15 | µA | Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 5.25V, -40°C ≤ $T_A$ ≤ 55°C. Analog power = off. |
| $I_{SBXTLH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[6] | – | 6 | 100 | µA | Conditions are with properly loaded, 1µW max, 32.768 kHz crystal. Vdd = 5.25V, 55°C < $T_A$ ≤ 125°C. Analog power = off. |
| $V_{REF}$ | Reference Voltage (Bandgap) | 1.25 | 1.3 | 1.35 | V | Trimmed for appropriate Vdd. |

*DC General Purpose I/O Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance.

**Table 12. DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull down Resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High Output Level | 3.5 | – | – | V | $I_{OH}$ = 10 mA, Vdd = 4.75 to 5.25V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined $I_{OH}$ budget. |
| $V_{OL}$ | Low Output Level | – | – | 0.75 | V | $I_{OL}$ = 25 mA, Vdd = 4.75 to 5.25V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined $I_{OL}$ budget. |
| $I_{OH}$ | High Level Source Current | 10 | – | – | mA | $V_{OH}$ ≥ Vdd-1.0V, see the limitations of the total current in the note for $V_{OH}$. |
| $I_{OL}$ | Low Level Sink Current | 25 | – | – | mA | $V_{OL}$ ≤ 0.75V, see the limitations of the total current in the note for $V_{OL}$. |
| $V_{IL}$ | Input Low Level | – | – | 0.8 | V | |

**Note**
6. Standby current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

**Table 12. DC GPIO Specifications** (continued)

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | 2.1 | – | | V | |
| $V_H$ | Input Hysterisis | – | 60 | – | mV | |
| $I_{IL}$ | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 μA |
| $C_{IN}$ | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C |
| $C_{OUT}$ | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C |

*DC Operational Amplifier Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time (CT) PSoC blocks and the Analog Switched Capacitor (SC) PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time (CT) PSoC blocks.

**Table 13. DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) Low Power<br>Input Offset Voltage (absolute value) Mid Power<br>Input Offset Voltage (absolute value) High Power | –<br>–<br>– | 1.6<br>1.3<br>1.2 | 11<br>9<br>9 | mV<br>mV<br>mV | |
| $TCV_{OSOA}$ | Input Offset Voltage Drift | – | 7.0 | 35.0 | μV/°C | |
| $I_{EBOA}$ | Input Leakage Current (Port 0 Analog Pins) | – | 200 | – | pA | Gross tested to 1 μA |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range<br>Common Mode Voltage Range (high power or high opamp bias) | 0.0<br>0.5 | –<br>– | Vdd<br>Vdd - 0.5 | V<br>– | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| $G_{OLOA}$ | Open Loop Gain<br>Power = Low<br>Power = Medium<br>Power = High | <br>–<br>–<br>– | <br>80<br>80<br>80 | <br>–<br>–<br>– | <br>dB<br>dB<br>dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| $V_{OHIGHOA}$ | High Output Voltage Swing (worst case internal load)<br>Power = Low<br>Power = Medium<br>Power = High | <br>Vdd - 0.2<br>Vdd - 0.2<br>Vdd - 0.5 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V<br>V<br>V | |
| $V_{OLOWOA}$ | Low Output Voltage Swing (worst case internal load)<br>Power = Low<br>Power = Medium<br>Power = High | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>0.2<br>0.2<br>0.5 | <br>V<br>V<br>V | |
| $I_{SOA}$ | Supply Current (including associated AGND buffer)<br>Power = Low, Opamp Bias = Low<br>Power = Low, Opamp Bias = High<br>Power = Medium, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = Low<br>Power = High, Opamp Bias = High | <br>–<br>–<br>–<br>–<br>–<br>– | <br>150<br>300<br>600<br>1200<br>2400<br>4600 | <br>200<br>400<br>800<br>1600<br>3200<br>6400 | <br>μA<br>μA<br>μA<br>μA<br>μA<br>μA | |
| $PSRR_{OA}$ | Supply Voltage Rejection Ratio | – | 80 | – | dB | Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd |

*DC Low Power Comparator Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 14. DC Low Power Comparator Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{REFLPC}$ | Low power comparator (LPC) reference voltage range | 0.2 | – | Vdd - 1 | V | |
| $I_{SLPC}$ | LPC supply current | – | 10 | 40 | µA | |
| $V_{OSLPC}$ | LPC voltage offset | – | 2.5 | 30 | mV | |

*DC Analog Output Buffer Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 15. DC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOB}$ | Input Offset Voltage (Absolute Value) | – | 3 | 18 | mV | |
| $TCV_{OSOB}$ | Input Offset Voltage Drift | – | +6 | – | µV/°C | |
| $V_{CMOB}$ | Common-Mode Input Voltage Range | 0.5 | – | Vdd - 1.0 | V | |
| $R_{OUTOB}$ | Output Resistance | – | 1 | – | Ω | |
| $V_{OHIGHOB}$ | High Output Voltage Swing (Load = 32Ω to Vdd/2) | 0.5 x Vdd + 1.1 | – | – | V | |
| $V_{OLOWOB}$ | Low Output Voltage Swing (Load = 32Ω to Vdd/2) | – | – | 0.5 x Vdd - 1.3 | V | |
| $I_{SOB}$ | Supply Current Including Bias Cell (No Load)<br>Power = Low<br>Power = High | <br>–<br>– | <br>1.1<br>2.6 | <br>5.1<br>8.8 | <br>mA<br>mA | |
| $PSRR_{OB}$ | Supply Voltage Rejection Ratio | – | 64 | – | dB | |

*DC Analog Reference Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block.

**Note** Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

**Table 16. DC Analog Reference Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| BG | Bandgap Voltage Reference | 1.25 | 1.30 | 1.35 | V |
| – | AGND = Vdd/2[7] | Vdd/2 - 0.02 | Vdd/2 | Vdd/2 + 0.02 | V |
| – | AGND = 2 x BandGap[7] | 2.4 | 2.6 | 2.8 | V |
| – | AGND = P2[4] (P2[4] = Vdd/2)[7] | P2[4] - 0.02 | P2[4] | P2[4] + 0.02 | V |
| – | AGND = BandGap[7] | 1.23 | 1.30 | 1.37 | V |
| – | AGND = 1.6 x BandGap[7] | 1.98 | 2.08 | 2.14 | V |
| – | AGND Column to Column Variation (AGND = Vdd/2)[7] | -0.035 | 0.000 | 0.035 | V |
| – | RefHi = Vdd/2 + BandGap[8] | Vdd/2 + 1.15 | Vdd/2 +1.30 | Vdd/2 +1.45 | V |
| – | RefHi = 3 x BandGap[8] | 3.65 | 3.9 | 4.15 | V |
| – | RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)[8] | P2[6] + 2.4 | P2[6] + 2.6 | P2[6] + 2.8 | V |
| – | RefHi = P2[4] + BandGap (P2[4] = Vdd/2)[8] | P2[4] + 1.24 | P2[4] +1.30 | P2[4] + 1.36 | V |
| – | RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)[8] | P2[4] + P2[6] - 0.1 | P2[4] + P2[6] | P2[4] + P2[6] + 0.1 | V |
| – | RefHi = 3.2 x BandGap[8] | 3.9 | 4.16 | 4.42 | V |
| – | RefLo = Vdd/2 – BandGap[8] | Vdd/2 - 1.45 | Vdd/2 - 1.3 | 1.15 | V |
| – | RefLo = BandGap[8] | 1.15 | 1.3 | 1.45 | V |
| – | RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)[8] | 2.4 - P2[6] | 2.6 - P2[6] | 2.8 - P2[6] | V |
| – | RefLo = P2[4] – BandGap (P2[4] = Vdd/2)[8] | P2[4] - 1.45 | 1.3 | P2[4] - 1.15 | V |
| – | RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)[8] | P2[4] - P2[6] - 0.1 | P2[4] - P2[6] | P2[4] - P2[6] + 0.1 | V |

**Notes**
7. This specification is only valid when CT Block Power = High. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.05V.
8. This specification is only valid when Ref Control Power = High.

*DC Analog PSoC Block Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 17. DC Analog PSoC Block Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{CT}$ | Resistor Unit Value (Continuous Time) | – | 12.24 | – | kΩ | |
| $C_{SC}$ | Capacitor Unit Value (Switch Cap) | – | 80 | – | fF | |

*DC POR and LVD Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Note** The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for more information on the VLT_CR register.

**Table 18. DC POR and LVD Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{PPOR2}$ | Vdd Value for PPOR Trip<br>PORLEV[1:0] = 10b | – | 4.55 | 4.70 | V | Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from watchdog. |
| | Vdd Value for LVD Trip | | | | | |
| $V_{LVD6}$ | VM[2:0] = 110b | 4.62 | 4.73 | 4.83 | V | |
| $V_{LVD7}$ | VM[2:0] = 111b | 4.710 | 4.814 | 4.950 | V | |

*DC Programming Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 19. DC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $Vdd_{IWRITE}$ | Supply Voltage for Flash Write Operations | 4.75 | – | – | V | |
| $I_{DDP}$ | Supply Current During Programming or Verify | – | 10 | 25 | mA | |
| $V_{ILP}$ | Input Low Voltage During Programming or Verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input High Voltage During Programming or Verify | 2.1 | – | – | V | |
| $I_{ILP}$ | Input Current when Applying $V_{ILP}$ to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull down resistor. |
| $I_{IHP}$ | Input Current when Applying $V_{IHP}$ to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull down resistor. |
| $V_{OLV}$ | Output Low Voltage During Programming or Verify | – | – | 0.75 | V | |
| $V_{OHV}$ | Output High Voltage During Programming or Verify | 3.5 | – | Vdd | V | |
| $Flash_{ENPB}$ | Flash Endurance (per block)[9] | 100 | – | – | – | Erase/write cycles per block. |
| $Flash_{ENT}$ | Flash Endurance (total)[9, 10] | 6,400 | – | – | – | Erase/write cycles. |
| $Flash_{DR}$ | Flash Data Retention[11] | 15 | – | – | Years | |

**Notes**

9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.
11. Flash data retention based on the use condition of ≤ 7000 hours at $T_A$ ≤ 125°C and the remaining time at $T_A$ ≤ 65°C.

## AC Electrical Characteristics

*AC Chip-Level Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 20. AC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO24}$ | Internal Main Oscillator Frequency for 24 MHz | 23.04[12] | 24 | 24.96[12] | MHz | Trimmed using factory trim values. |
| $F_{CPU1}$ | CPU Frequency (5V Vdd Nominal) | 0.09[12] | 12 | 12.48[12] | MHz | |
| $F_{24M}$ | Digital PSoC Block Frequency | 0 | 24 | 24.96[12, 13] | MHz | |
| $F_{32K1}$ | Internal Low Speed Oscillator Frequency | 15 | 32 | 64 | kHz | This specification applies when the ILO has been trimmed. |
| $F_{32KU}$ | Internal Low Speed Oscillator (ILO) Untrimmed Frequency | 5 | – | – | kHz | After a reset and before the M8C processor starts to execute, the ILO is not trimmed. |
| $F_{32K2}$ | External Crystal Oscillator | – | 32.768 | – | kHz | Accuracy is capacitor and crystal dependent. 50% duty cycle. |
| $F_{PLL}$ | PLL Frequency | – | 23.986 | – | MHz | A multiple (x732) of crystal frequency. |
| Jitter24M2 | 24 MHz Period Jitter (PLL) | – | – | 800 | ps | Refer to Figure 9 on page 22. |
| $T_{PLLSLEW}$ | PLL Lock Time | 0.5 | – | 10 | ms | Refer to Figure 6 on page 22. |
| $T_{PLLSLEWSLOW}$ | PLL Lock Time for Low Gain Setting | 0.5 | – | 50 | ms | Refer to Figure 7 on page 22. |
| $T_{OS}$ | External Crystal Oscillator Startup to 1% | – | 1700 | 2620 | ms | Refer to Figure 8 on page 22. |
| $T_{OSACC}$ | External Crystal Oscillator Startup to 100 ppm | – | 2800 | 3800 | ms | |
| Jitter32k | 32 kHz Period Jitter | – | 100 | – | ns | Refer to Figure 10 on page 22. |
| $T_{XRST}$ | External Reset Pulse Width | 10 | – | – | µs | |
| DC24M | 24 MHz Duty Cycle | 40 | 50 | 60 | % | |
| $DC_{ILO}$ | Internal Low Speed Oscillator (ILO) Duty Cycle | 20 | 50 | 80 | % | |
| Step24M | 24 MHz Trim Step Size | – | 50 | – | kHz | |
| Jitter24M1P | 24 MHz Period Jitter (IMO) Peak-to-Peak | – | 600 | – | ps | Refer to Figure 9 on page 22. |
| Jitter24M1R | 24 MHz Period Jitter (IMO) Root Mean Squared | – | – | 600 | ps | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.48[12] | MHz | |
| $SR_{POWERUP}$ | Power Supply Slew Rate | – | – | 250 | V/ms | Vdd slew rate during power up. |
| $T_{POWERUP}$ | Time between end of POR state and CPU code execution | – | 16 | 100 | ms | Power up from 0V. |

**Notes**
12. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
13. See the individual user module data sheets for information on maximum frequencies for user modules.

**Figure 6. PLL Lock Timing Diagram**

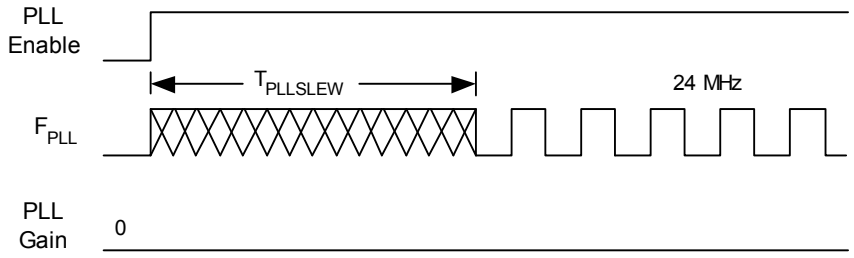



**Figure 7. PLL Lock for Low Gain Setting Timing Diagram**

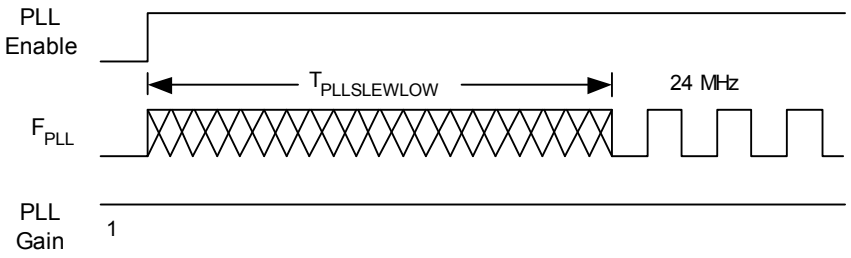



**Figure 8. External Crystal Oscillator Startup Timing Diagram**

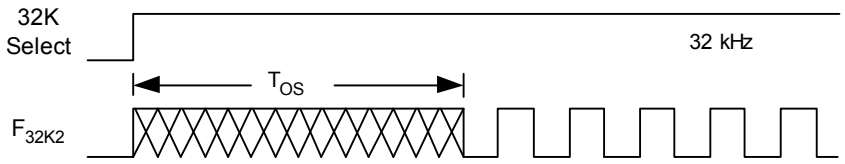



**Figure 9. 24 MHz Period Jitter (IMO) Timing Diagram**

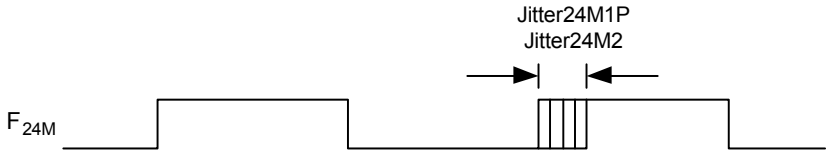
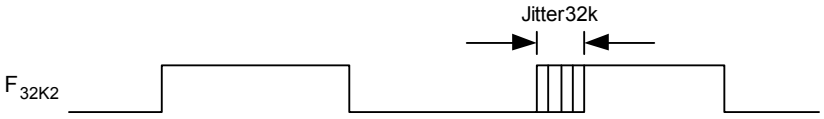



**Figure 10. 32 kHz Period Jitter (ECO) Timing Diagram**



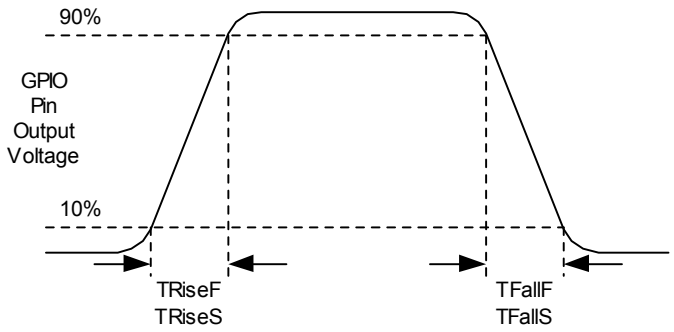
*AC General Purpose I/O Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 21. AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO Operating Frequency | 0 | – | 12.48[12] | MHz | Normal Strong Mode |
| TRiseF | Rise Time, Normal Strong Mode, Cload = 50 pF | 2 | – | 22 | ns | 10% - 90% |
| TFallF | Fall Time, Normal Strong Mode, Cload = 50 pF | 2 | – | 22 | ns | 10% - 90% |
| TRiseS | Rise Time, Slow Strong Mode, Cload = 50 pF | 9 | 27 | – | ns | 10% - 90% |
| TFallS | Fall Time, Slow Strong Mode, Cload = 50 pF | 9 | 22 | – | ns | 10% - 90% |

**Figure 11. GPIO Timing Diagram**




*AC Operational Amplifier Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Note** Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

**Table 22. AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $SR_{ROA}$ | Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) | | | | |
| | Power = Low, Opamp Bias = Low | 0.15 | – | – | V/µs |
| | Power = Low, Opamp Bias = High | 0.15 | – | – | V/µs |
| | Power = Medium, Opamp Bias = Low | 0.15 | – | – | V/µs |
| | Power = Medium, Opamp Bias = High | 1.7 | – | – | V/µs |
| | Power = High, Opamp Bias = Low | 1.7 | – | – | V/µs |
| | Power = High, Opamp Bias = High | 6.5 | – | – | V/µs |
| $SR_{FOA}$ | Falling Slew Rate (80% to 20%) (10 pF load, Unity Gain) | | | | |
| | Power = Low, Opamp Bias = Low | 0.01 | – | – | V/µs |
| | Power = Low, Opamp Bias = High | 0.01 | – | – | V/µs |
| | Power = Medium, Opamp Bias = Low | 0.01 | – | – | V/µs |
| | Power = Medium, Opamp Bias = High | 0.5 | – | – | V/µs |
| | Power = High, Opamp Bias = Low | 0.5 | – | – | V/µs |
| | Power = High, Opamp Bias = High | 4.0 | – | – | V/µs |
| $BW_{OA}$ | Gain Bandwidth Product | | | | |
| | Power = Low, Opamp Bias = Low | 0.75 | – | – | MHz |
| | Power = Low, Opamp Bias = High | 0.75 | – | – | MHz |
| | Power = Medium, Opamp Bias = Low | 0.75 | – | – | MHz |
| | Power = Medium, Opamp Bias = High | 3.1 | – | – | MHz |
| | Power = High, Opamp Bias = Low | 3.1 | – | – | MHz |
| | Power = High, Opamp Bias = High | 5.4 | – | – | MHz |

*AC Low Power Comparator Specifications*

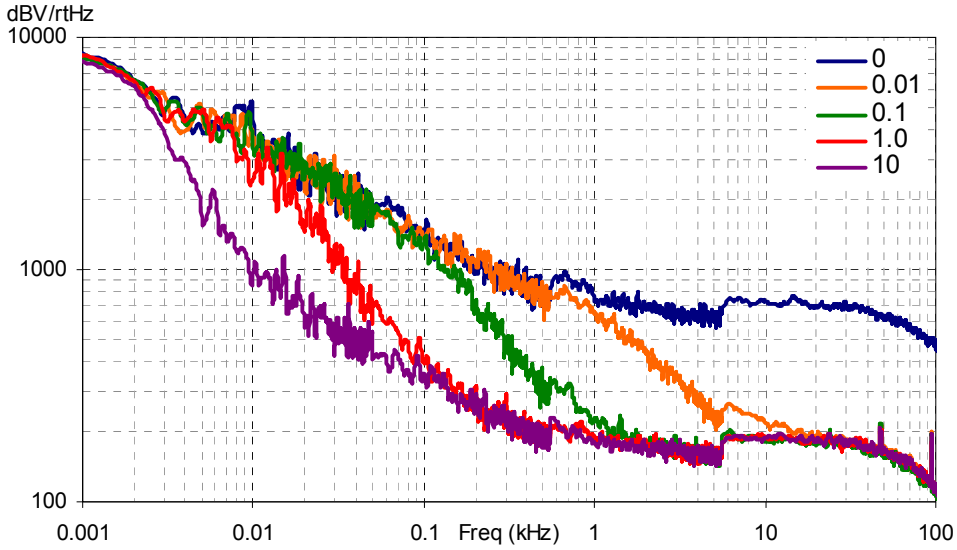
The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 23. AC Low Power Comparator Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{RLPC}$ | LPC response time | – | – | 50 | µs | ≥ 50 mV overdrive comparator reference set within $V_{REFLPC}$. |

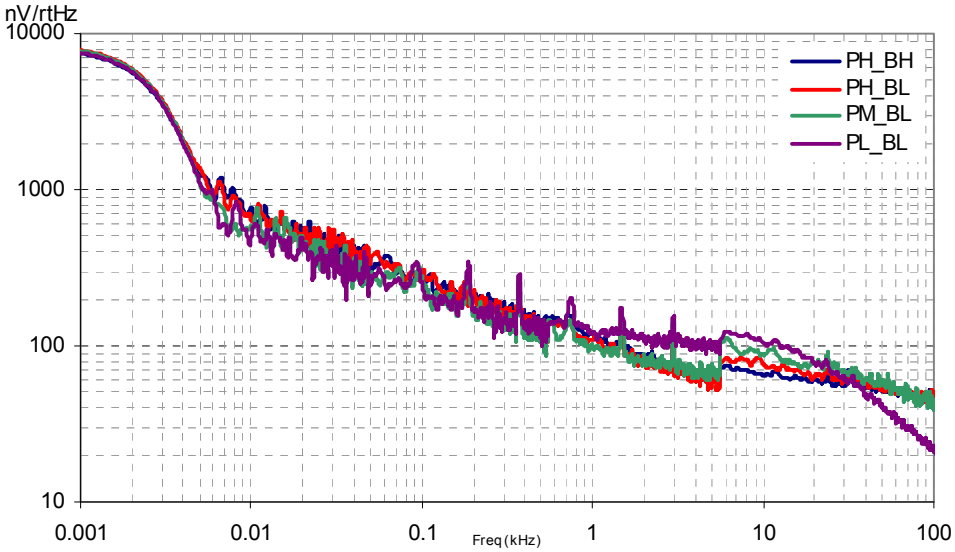
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

**Figure 12. Typical AGND Noise with P2[4] Bypass**




At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

**Figure 13. Typical Opamp Noise**



*AC Digital Block Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 24. AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| All Functions | Maximum Block Clocking Frequency | – | – | 24.96[12] | MHz | |
| Timer | Capture Pulse Width | 50[14] | – | – | ns | |
| | Maximum Frequency, No Capture | – | – | 24.96[12] | MHz | |
| | Maximum Frequency, With Capture | – | – | 24.96[12] | MHz | |
| Counter | Enable Pulse Width | 50[14] | – | – | ns | |
| | Maximum Frequency, No Enable Input | – | – | 24.96[12] | MHz | |
| | Maximum Frequency, Enable Input | – | – | 24.96[12] | MHz | |
| Dead Band | Kill Pulse Width: | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50[14] | – | – | ns | |
| | Disable Mode | 50[14] | – | – | ns | |
| | Maximum Frequency | – | – | 24.96[12] | MHz | |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency | – | – | 24.96[12] | MHz | |
| CRCPRS (CRC Mode) | Maximum Input Clock Frequency | – | – | 24.96[12] | MHz | |
| SPIM | Maximum Input Clock Frequency | – | – | 4.16[12] | MHz | Maximum data rate is 2.08 Mbps due to 2 x over clocking. |
| SPIS | Maximum Input Clock Frequency | – | – | 2.08[12] | MHz | |
| | Width of SS_ Negated Between Transmissions | 50[14] | – | – | ns | |
| Transmitter | Maximum Input Clock Frequency | – | – | 8.32[12] | MHz | Maximum baud rate is 1.04 Mbaud due to 8 x over clocking. |
| Receiver | Maximum Input Clock Frequency | – | – | 24.96[12] | MHz | Maximum baud rate is 3.12 Mbaud due to 8 x over clocking. |

**Note**
14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

*AC Analog Output Buffer Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 25. AC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{ROB}$ | Rising Settling Time to 0.1%, 1V Step, 100 pF Load<br>Power = Low<br>Power = High | <br>–<br>– | <br>–<br>– | <br>3<br>3 | <br>µs<br>µs |
| $T_{SOB}$ | Falling Settling Time to 0.1%, 1V Step, 100 pF Load<br>Power = Low<br>Power = High | <br>–<br>– | <br>–<br>– | <br>3<br>3 | <br>µs<br>µs |
| $SR_{ROB}$ | Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load<br>Power = Low<br>Power = High | <br>0.6<br>0.6 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $SR_{FOB}$ | Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load<br>Power = Low<br>Power = High | <br>0.6<br>0.6 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $BW_{OB}$ | Small Signal Bandwidth, 20m$V_{pp}$, 3dB BW, 100 pF Load<br>Power = Low<br>Power = High | <br>0.8<br>0.8 | <br>–<br>– | <br>–<br>– | <br>MHz<br>MHz |
| $BW_{OB}$ | Large Signal Bandwidth, 1$V_{pp}$, 3dB BW, 100 pF Load<br>Power = Low<br>Power = High | <br>300<br>300 | <br>–<br>– | <br>–<br>– | <br>kHz<br>kHz |

*AC External Clock Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 26. AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0.093 | – | 24.24 | MHz | |
| – | High Period | 20.6 | – | – | ns | |
| – | Low Period | 20.6 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | µs | |

*AC Programming Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 27. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{RSCLK}$ | Rise Time of SCLK | 1 | – | 20 | ns | |
| $T_{FSCLK}$ | Fall Time of SCLK | 1 | – | 20 | ns | |
| $T_{SSCLK}$ | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns | |
| $T_{HSCLK}$ | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $T_{ERASEB}$ | Flash Erase Time (Block) | – | 20 | 80[9] | ms | |
| $T_{WRITE}$ | Flash Block Write Time | – | 80 | 320[9] | ms | |
| $T_{DSCLK}$ | Data Out Delay from Falling Edge of SCLK | – | – | 50 | ns | |
| $T_{PRGH}$ | Total Flash Block Program Time ($T_{ERASEB}$ + $T_{WRITE}$), Hot | – | – | 200[9] | ms | $T_J \geq 0°C$ |
| $T_{PRGC}$ | Total Flash Block Program Time ($T_{ERASEB}$ + $T_{WRITE}$), Cold | – | – | 400[9] | ms | $T_J < 0°C$ |

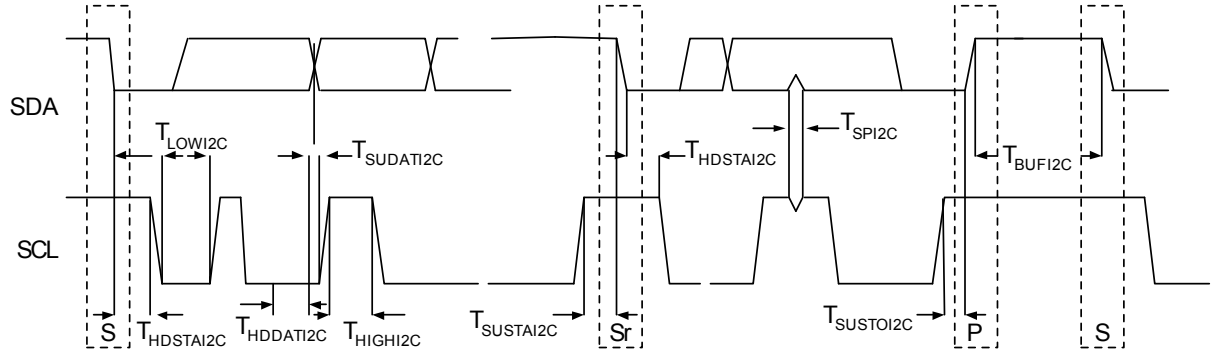
*AC I²C Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 28. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCLI2C}$ | SCL Clock Frequency | 0 | 100[15] | 0 | 400[15] | kHz |
| $T_{HDSTAI2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs |
| $T_{LOWI2C}$ | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | µs |
| $T_{HIGHI2C}$ | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | µs |
| $T_{SUSTAI2C}$ | Setup Time for a Repeated START Condition | 4.7 | – | 0.6 | – | µs |
| $T_{HDDATI2C}$ | Data Hold Time | 0 | – | 0 | – | µs |
| $T_{SUDATI2C}$ | Data Setup Time | 250 | – | 100[16] | – | ns |
| $T_{SUSTOI2C}$ | Setup Time for STOP Condition | 4.0 | – | 0.6 | – | µs |
| $T_{BUFI2C}$ | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | µs |
| $T_{SPI2C}$ | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns |

**Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus**




**Notes**

15. $F_{SCLI2C}$ is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the $F_{SCLI2C}$ specification adjusts accordingly.
16. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

## Packaging Information

This section illustrates the packaging specifications for the automotive CY8C24x23A PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

**Figure 15. 20-Pin (210-Mil) SSOP**

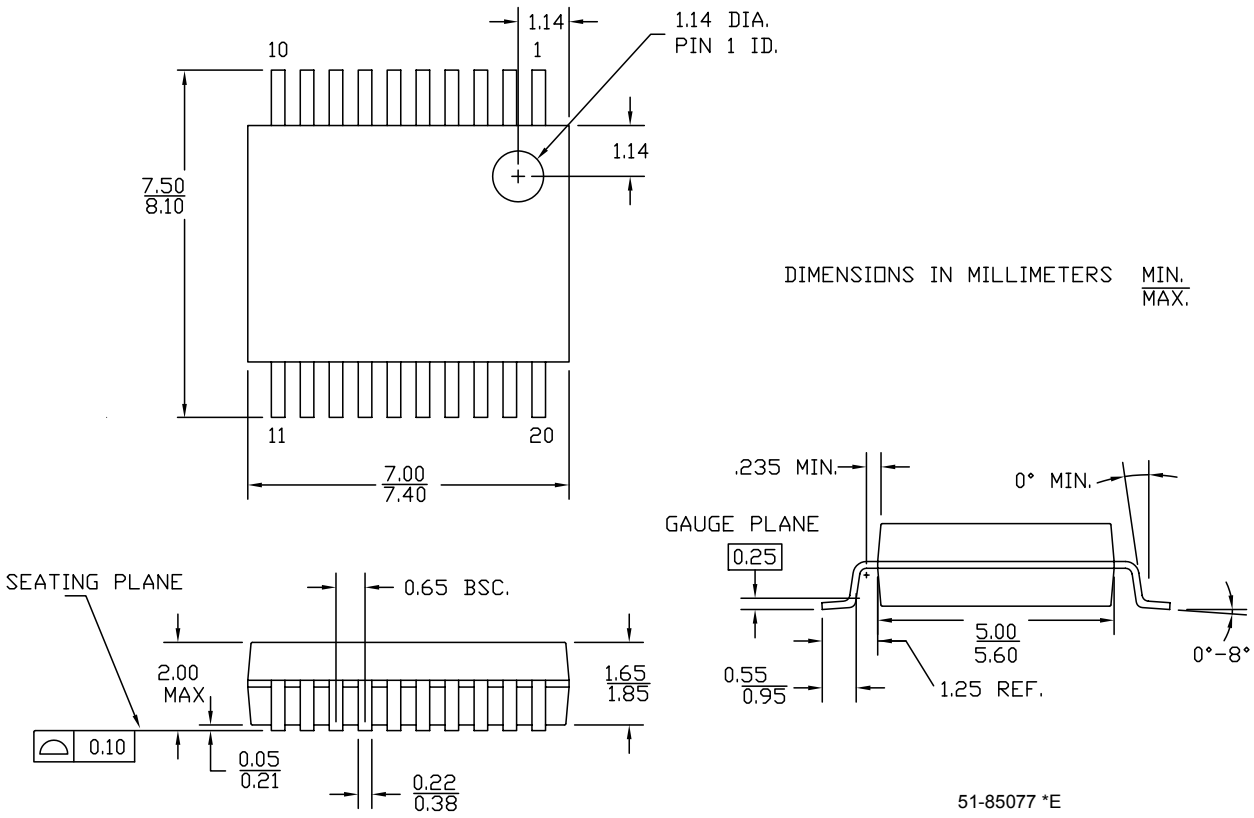
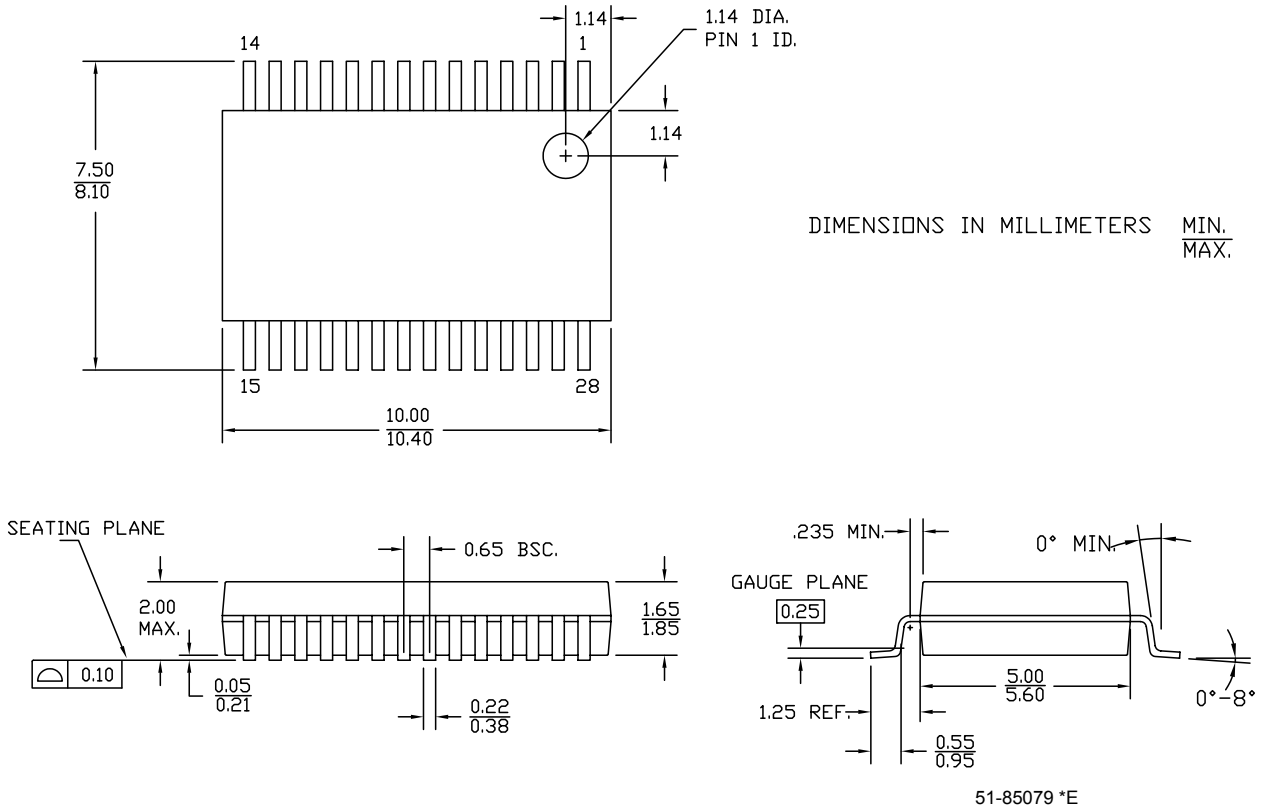


**Figure 16. 28-Pin (210-Mil) SSOP**




## Thermal Impedances

| Package | Typical $\theta_{JA}$ [17] |
|---|---|
| 20 SSOP | 117 °C/W |
| 28 SSOP | 101 °C/W |

## Capacitance on Crystal Pins

| Package | Package Capacitance |
|---|---|
| 20 SSOP | 2.6 pF |
| 28 SSOP | 2.8 pF |

## Solder Reflow Specifications

The following table shows the solder reflow temperature limits that must not be exceeded.

| Package | Maximum Time above $T_C$ – 5 °C | Maximum Peak Temperature |
|---|---|---|
| 20 SSOP | 30 seconds | 260°C |
| 28 SSOP | 30 seconds | 260°C |

**Note**
17. $T_J = T_A + POWER \times \theta_{JA}$

## Development Tool Selection

This section presents the development tools available for the CY8C24x23A family.

### Software

*PSoC Designer*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

*PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

### Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

*CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube Unit
- 28-Pin PDIP Emulation Pod for CY8C29466-24PXI
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Samples (two)
- PSoC Designer Software CD
- ISSP Cable
- MiniEval Socket Programming and Evaluation board
- Backward Compatibility Cable (for connecting to legacy Pods)
- Universal 110/220 Power Supply (12V)
- European Plug Adapter
- USB 2.0 Cable
- Getting Started Guide
- Development Kit Registration form

### Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3210-24X23 Evaluation Pod (EvalPod)*

PSoC EvalPods are pods that connect to the ICE In-Circuit Emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-24X23 provides evaluation of the CY8C24x23A PSoC device family.

## Device Programmers

All device programmers can be purchased from the Cypress Online Store.

*CY3210-MiniProg1*

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3207ISSP In-System Serial Programmer (ISSP)*

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

**Note**: CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

## Accessories (Emulation and Programming)

**Table 29. Emulation and Programming Accessories**

| Part Number | Pin Package | Pod Kit[18] | Foot Kit[19] | Adapter[20] |
|---|---|---|---|---|
| CY8C24223A-12PVXE | 20 SSOP | CY3250-24X23A | CY3250-20SSOP-FK | Adapters can be found at http://www.emulation.com. |
| CY8C24423A-12PVXE | 28 SSOP | CY3250-24X23A | CY3250-28SSOP-FK | |

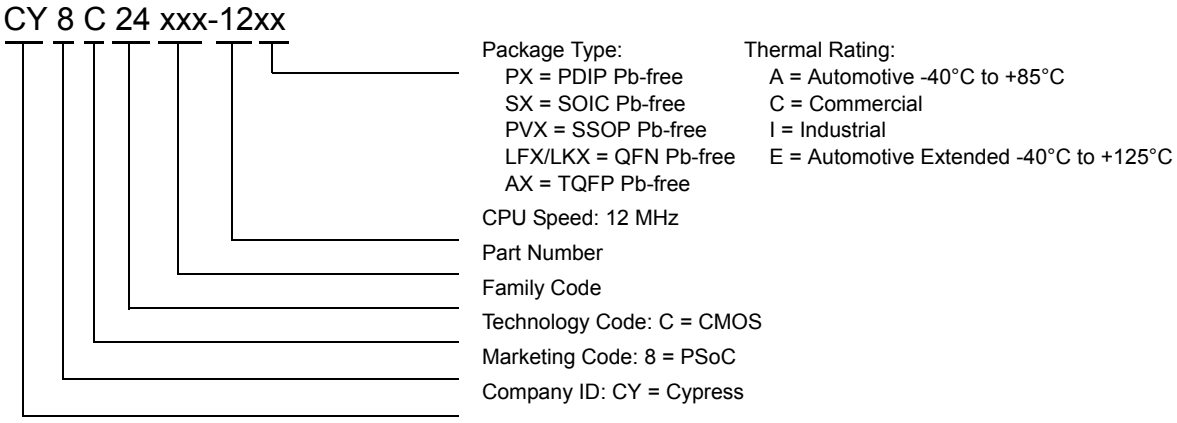
**Notes**
18. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
19. Foot kit includes surface mount feet that can be soldered to the target PCB.
20. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

## Ordering Information

The following table lists the automotive CY8C24x23A PSoC device group's key package features and ordering codes.

| Package | Ordering Code | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital Blocks | Analog Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 20 Pin (210 Mil) SSOP | CY8C24223A-12PVXE | 4K | 256 | No | -40°C to +125°C | 4 | 6 | 16 | 8 | 2 | Yes |
| 20 Pin (210 Mil) SSOP (Tape and Reel) | CY8C24223A-12PVXET | 4K | 256 | No | -40°C to +125°C | 4 | 6 | 16 | 8 | 2 | Yes |
| 28 Pin (210 Mil) SSOP | CY8C24423A-12PVXE | 4K | 256 | No | -40°C to +125°C | 4 | 6 | 24 | 12[1] | 2 | Yes |
| 28 Pin (210 Mil) SSOP (Tape and Reel) | CY8C24423A-12PVXET | 4K | 256 | No | -40°C to +125°C | 4 | 6 | 24 | 12[1] | 2 | Yes |

### Ordering Code Definitions



## Document History Page

| Document Title: CY8C24223A, CY8C24423A Automotive - Extended Temperature PSoC® Programmable System-on-Chip<br>Document Number: 38-12029 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 238268 | SFV | See ECN | First release of CY8C24x23A Automotive Preliminary Data Sheet. |
| *A | 271471 | HMT | See ECN | Update per SFV memo. Input MWR changes, including removing SMP. Change to Final. |
| *B | 286089 | HMT | See ECN | Update characterization data. Fine tune pinouts. Add Reflow Peak Temp. table. |
| *C | 512475 | HMT | See ECN | Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per extended temp. specs. Update CY branding and QFN convention. Update copyright and trademarks. |
| *D | 2101387 | AESA | See ECN | Post to www.cypress.com |
| *E | 2619935 | OGNE/AESA | 12/11/2008 | Changed title to “CY8C24223A, CY8C24423A PSoC® Programmable System-on-Chip™”<br>Added note on digital signaling in DC Analog Reference Specifications on page 19.<br>Added Die Sales information note to Ordering Information on page 32.<br>Updated data sheet template. |
| *F | 2659314 | PRKA/PYRS | 02/13/09 | Changed title to “Automotive - Extended Temperature CY8C24223A, CY8C24423A PSoC® Programmable System-on-Chip™”<br>Updated Development Tools and Designing with PSoC Designer sections on pages 5 and 6. |
| *G | 2719510 | BTK | 06/16/09 | Changed title. Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of the Register Reference section to “Registers”. Improved formatting of the register tables. Added clarifying comments to some electrical specifications. Changed $T_{RAMP}$ specification per MASJ input. Changed number of analog inputs for 28-pin package to 12 from 10. Fixed all AC specifications to conform to a ±4% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Added a footnote to clarify that 8 of the 12 analog inputs are regular and the other 4 are direct SC block connections. Added Development Tool Selection section. |
| *H | 2822792 | BTK/AESA | 12/07/2009 | Added $T_{PRGH}$, $T_{PRGC}$, $I_{OL}$, $I_{OH}$, $F_{32KU}$, $DC_{ILO}$, and $T_{POWERUP}$ electrical specifications. Updated the text of footnote 10. Added maximum values and updated typical values for $T_{ERASEB}$ and $T_{WRITE}$ electrical specifications. Replaced $T_{RAMP}$ electrical specification with $SR_{POWERUP}$ electrical specification. Added “Contents” on page 2. This revision fixes CDT 63984. |
| *I | 2888007 | NJF | 03/30/2010 | Updated Cypress website links.<br>Updated PSoC Designer Software Subsystems.<br>Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings.<br>Updated links in Sales, Solutions, and Legal Information.<br>Removed Third Party Tools and Build a PSoC Emulator into your Board. |
| *J | 3184892 | PRKA/VIVG | 03/01/2011 | No change. Sunset review spec. |
| *K | 3726340 | 08/28/2012 | tess_ukr/ LURE | Updated the following sections: Getting Started, Development Tools, and Designing with PSoC Designer as all the System level designs have been de-emphasized.<br>Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.<br>Updated package diagrams.<br>Updated solder reflow specifications. |
| *L | 4304787 | 03/11/2014 | JICG | Updated in new template.<br><br>Completing Sunset Review. |

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