



**THE DATASHEET OF
SN65LBC176AMDREP**



SN65LBC176A-EP DIFFERENTIAL BUS TRANSCEIVER

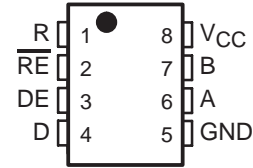
SGLS151C – DECEMBER 2002 – REVISED JULY 2004

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of -40°C to 125°C and -55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **High-Speed Low-Power LinBiCMOS™ Circuitry Designed for Signaling Rates‡ Up to 30 Mbps**
- **Bus-Pin ESD Protection Exceeds 12-kV HBM**
- **Compatible With ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E)**
- **Low Skew**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Disabled Supply Current Requirements . . . 700 μA Maximum**
- **Common-Mode Voltage Range of -7 V to 12 V**
- **Thermal-Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**
- **Receiver Input Sensitivity . . . $\pm 200\text{ mV}$ Max**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Glitch-Free Power-Up and Power-Down Protection**

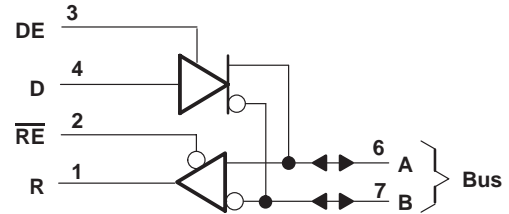
† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

‡ Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit length, and much higher signaling rates may be achieved without this requirement as displayed in the *TYPICAL CHARACTERISTICS* of this device.

D Package
(TOP VIEW)



logic diagram (positive logic)



Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS $V_A - V_B$	ENABLE $\overline{\text{RE}}$	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SN65LBC176A-EP DIFFERENTIAL BUS TRANSCEIVER

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description/ordering information

The SN65LBC176A-EP differential bus transceiver is a monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The SN65LBC176A-EP is designed for balanced transmission lines and is compatible with ANSI standard TIA/EIA-485-A and ISO 8482. The SN65LBC176A-EP offers improved switching performance over its predecessors without sacrificing significantly more power.

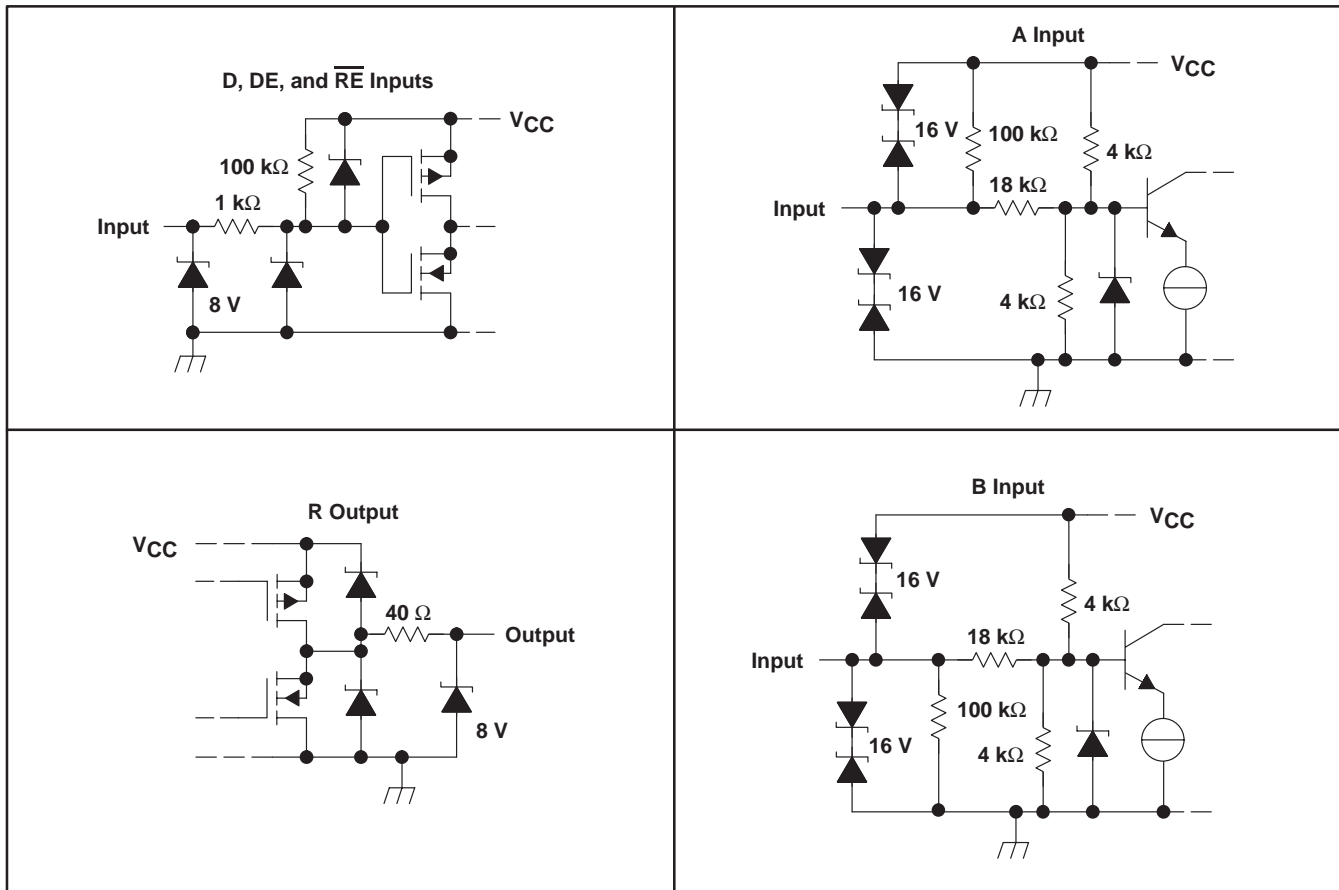
The SN65LBC176A-EP combines a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Low device supply current can be achieved by disabling the driver and the receiver.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Tape and Reel	SN65LBC176AQDREP	176AEP
-55°C to 125°C	SOIC – D	Tape and Reel	SN65LBC176AMDREP	176MEP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematics of inputs and outputs



absolute maximum ratings†

Supply voltage, V_{CC} (see Note 1)	–0.3 V to 6 V
Voltage range at any bus terminal (A or B)	–10 V to 15 V
Input voltage, V_I (D, DE, R, or \overline{RE})	–0.3 V to $V_{CC} + 0.5$ V
Electrostatic discharge: Bus terminals and GND, Class 3, A: (see Note 2)	12 kV
Bus terminals and GND, Class 3, B: (see Note 2)	400 V
All terminals, Class 3, A:	4 kV
All terminals, Class 3, B:	400 V
Continuous total power dissipation (see Note 3)	See Dissipation Rating Table
Storage temperature range, T_{stg} (see Note 4)	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

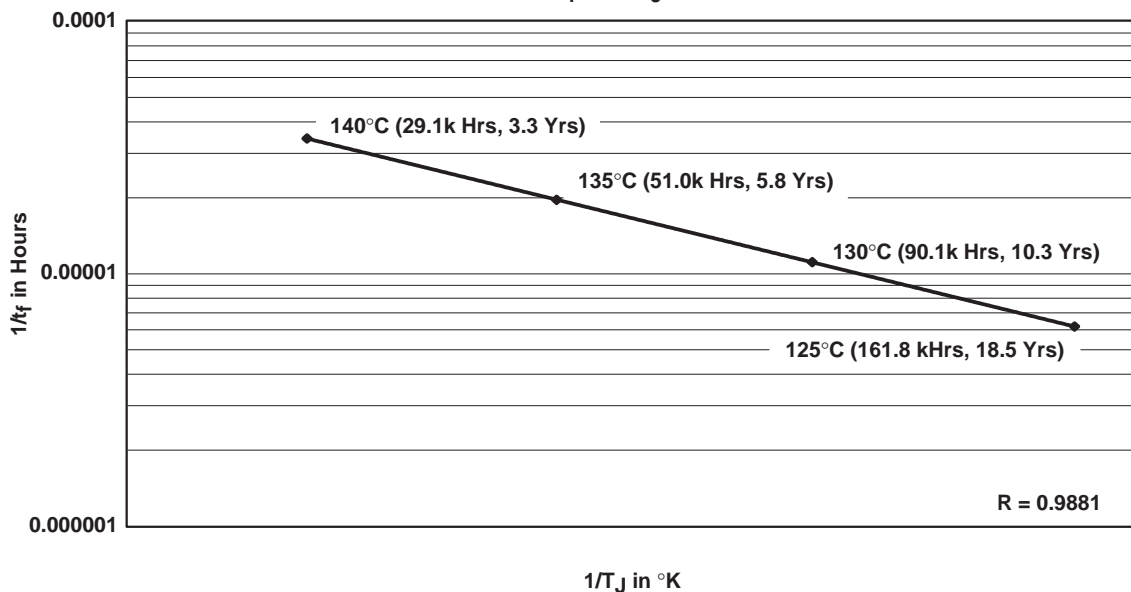
- NOTES:
1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
 2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
 3. Tested in accordance with MIL-STD-883C, Method 3015.7
 4. Long-term, high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when the board is mounted and with no air flow.

OPERATING LIFE DERATING TABLE – SN65LBC176AMDREP
 $1/t_f$ vs $1/T_J$ in °K



- NOTES:
- A. See the data sheet for absolute maximum and maximum recommended operating conditions.
 - B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
 - C. Attached enhanced plastic product disclaimer applies.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
		-7			
High-level input voltage, V_{IH} (output recessive)	D, DE, and \overline{RE}	2		V_{CC}	V
Low-level input voltage, V_{IL} (output dominant)	D, DE, and \overline{RE}	0		0.8	V
Differential input voltage, V_{ID} (see Note 5)		-12 [§]		12	V
High-level output current, I_{OH}	Driver	-60			mA
	Receiver	-8			
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65LBC176AQ-EP	-40		125	°C
	SN65LBC176AM-EP	-55		125	

[§] The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

NOTE 5: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT	
V_{IK}	Input clamp voltage $I_I = -18$ mA	-1.5	-0.8		V	
$ V_{OD} $	Differential output voltage $I_O = 0$ $R_L = 54 \Omega$, See Figure 1 $V_{test} = -7$ V to 12 V, See Figure 2	1.5	4	6	V	
		0.9	1.5	6		
		0.9	1.5	6		
$\Delta V_{OD} $	Change in magnitude of differential output voltage See Figure 1 and Figure 2	-0.2		0.2	V	
$V_{OC(SS)}$	Steady-state common-mode output voltage See Figure 1	1.8	2.4	3	V	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage [†] See Figure 1	-0.2		0.2	V	
I_{OZ}	High-impedance output current See receiver input currents					
I_{IH}	High-level enable input current $V_I = 2$ V	-100			μ A	
I_{IL}	Low-level enable input current $V_I = 0.8$ V	-100			μ A	
I_{OS}	Short-circuit output current -7 V $\leq V_O \leq 12$ V	-250	± 70	250	mA	
I_{CC}	Supply current $V_I = 0$ or V_{CC} , No load	Receiver disabled and driver enabled		5	9	mA
		Receiver disabled and driver disabled		0.4	0.7	
		Receiver enabled and driver enabled		8.5	15	

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ$ C.



driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high level output	R _L = 54 Ω, C _L = 50 pF, See Figure 3	2		12	ns
t _{PHL}	Propagation delay time, high-to-low level output		2		12	
t _{sk(p)}	Pulse skew (t _{PLH} – t _{PHL})				2	
t _r	Differential output signal rise time		1.2		11	
t _f	Differential output signal fall time		1.2		11	
t _{PZH}	Propagation delay time, high-impedance to high-level output	R _L = 110 Ω, See Figure 4			22	ns
t _{PZL}	Propagation delay time, high-impedance to low-level output	R _L = 110 Ω, See Figure 5			25	ns
t _{PHZ}	Propagation delay time, high-level to high-impedance output	R _L = 110 Ω, See Figure 4			22	ns
t _{PLZ}	Propagation delay time, low-level to high-impedance output	R _L = 110 Ω, See Figure 5			22	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	I _O = –8 mA			0.2	V
V _{IT–}	Negative-going input threshold voltage	I _O = 8 mA	–0.2			V
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT–})		50			mV
V _{IK}	Enable-input clamp voltage	I _I = –18 mA	–1.5	–0.8		V
V _{OH}	High-level output voltage	V _{ID} = 200 mV, I _{OH} = –8 mA, See Figure 6	4	4.9		V
V _{OL}	Low-level output voltage	V _{ID} = 200 mV, I _{OL} = 8 mA, See Figure 6		0.1	0.8	V
I _{OZ}	High-impedance-state output current	V _O = 0 to V _{CC}	–10		10	μA
I _I	Bus input current	V _{IH} = 12 V, V _{CC} = 5 V	Other input at 0 V	0.4	1	mA
		V _{IH} = 12 V, V _{CC} = 0		0.5	1	
		V _{IH} = –7 V, V _{CC} = 5 V		–0.8	–0.4	
		V _{IH} = –7 V, V _{CC} = 0		–0.8	–0.3	
I _{IH}	High-level enable-input current	V _{IH} = 2 V	–100			μA
I _{IL}	Low-level enable-input current	V _{IL} = 0.8 V	–100			μA
I _{CC}	Supply current	V _I = 0 or V _{CC} , No load	Receiver enabled and driver disabled	4	7	mA
			Receiver disabled and driver disabled	0.4	0.7	
			Receiver enabled and driver enabled	8.5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH} Propagation delay time, output↑	V _{ID} = -1.5 V to 1.5 V, See Figure 7	7		30	ns
t _{PHL} Propagation delay time, output↓		7		30	ns
t _{sk(p)} Pulse skew (t _{PHL} - t _{PLH})				6	ns
t _r Rise time, output	See Figure 7			5	ns
t _f Fall time, output				5	ns
t _{PZH} Output enable time to high level	C _L = 10 pF, See Figure 8			50	ns
t _{PZL} Output enable time to low level				50	ns
t _{PHZ} Output disable time from high level				60	ns
t _{PLZ} Output disable time from low level				40	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



PARAMETER MEASUREMENT INFORMATION

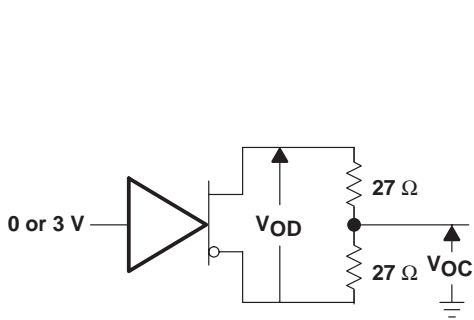


Figure 1. Driver V_{OD} and V_{OC}

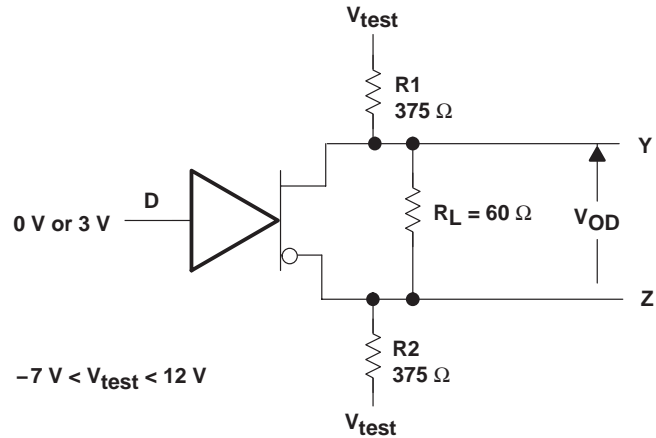
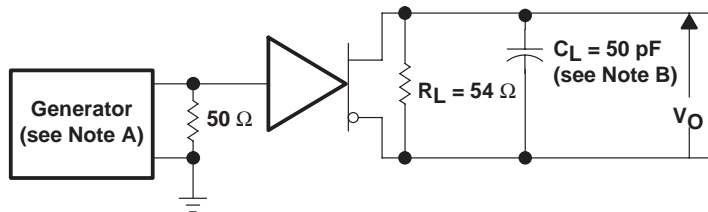
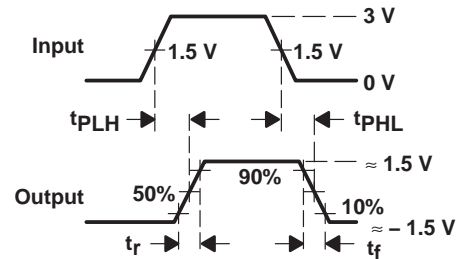


Figure 2. Driver V_{OD3}



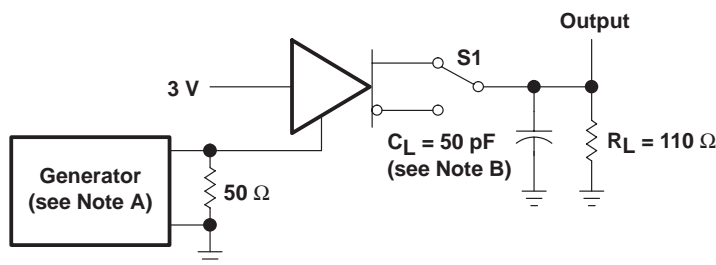
TEST CIRCUIT



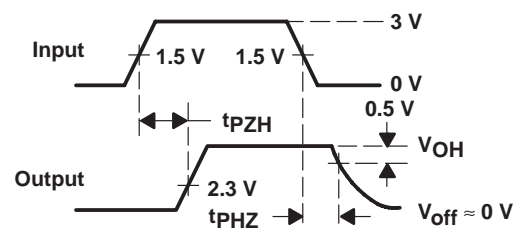
VOLTAGE WAVEFORMS

- NOTES: D. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
E. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

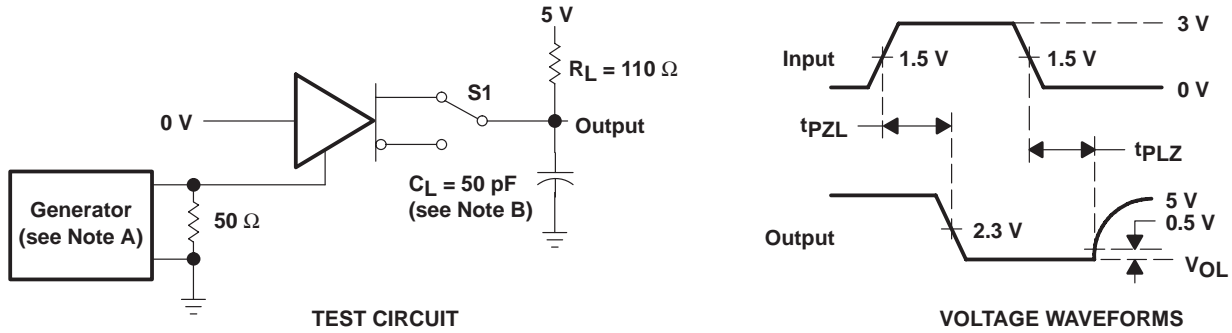
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

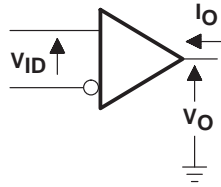
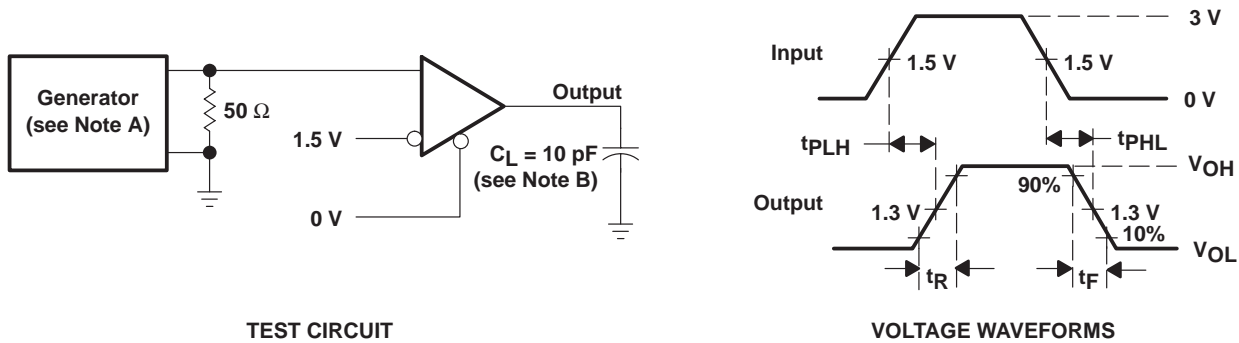


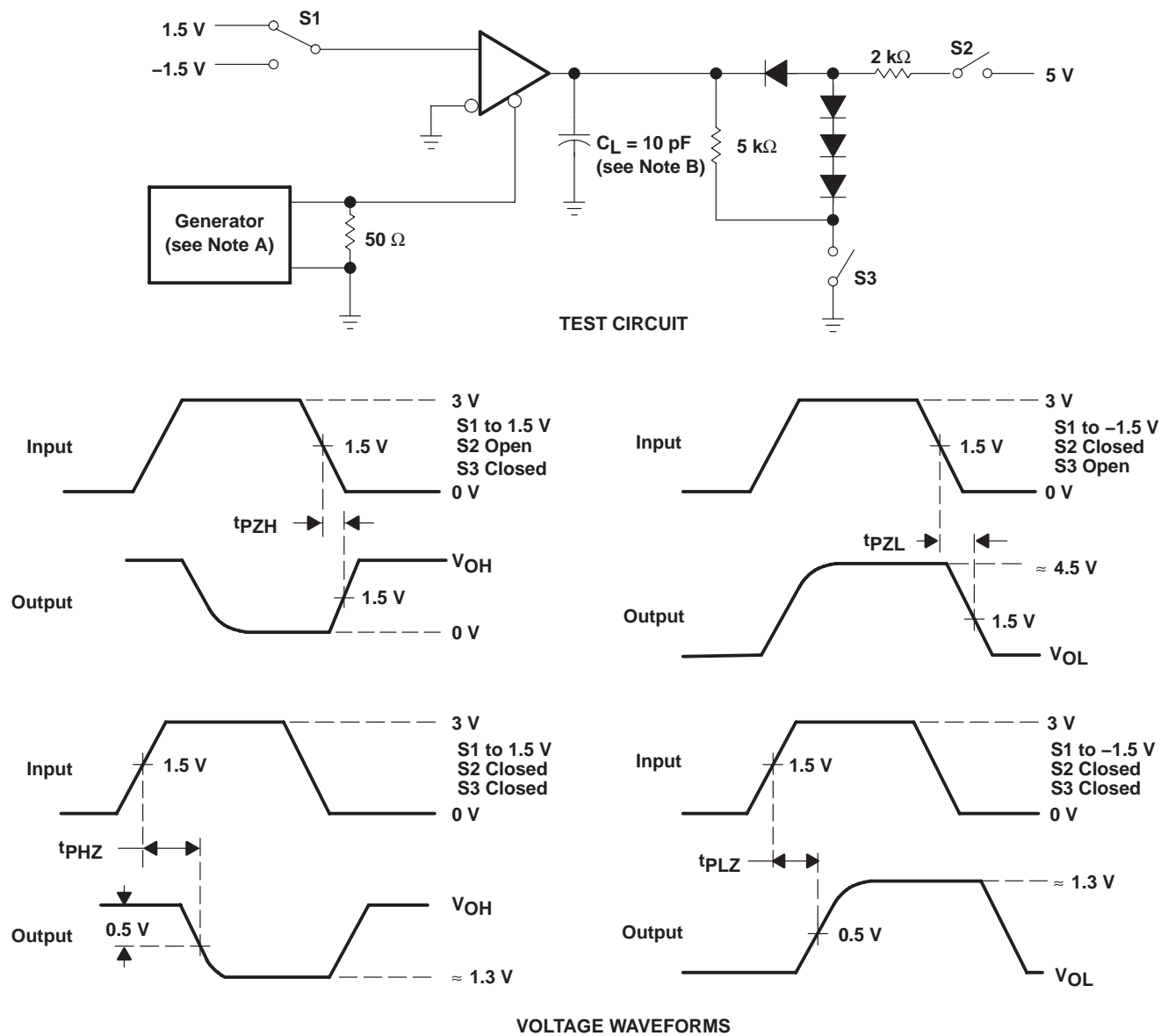
Figure 6. Receiver V_{OH} and V_{OL}



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

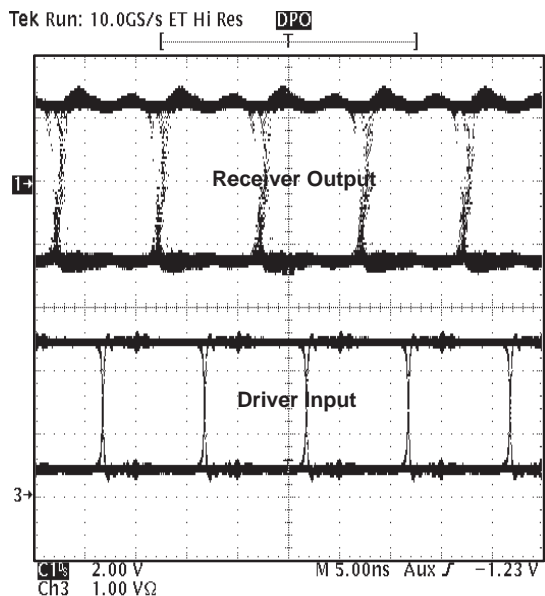


Figure 9. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well, even though they do not meet the standard by definition.

TYPICAL CHARACTERISTICS

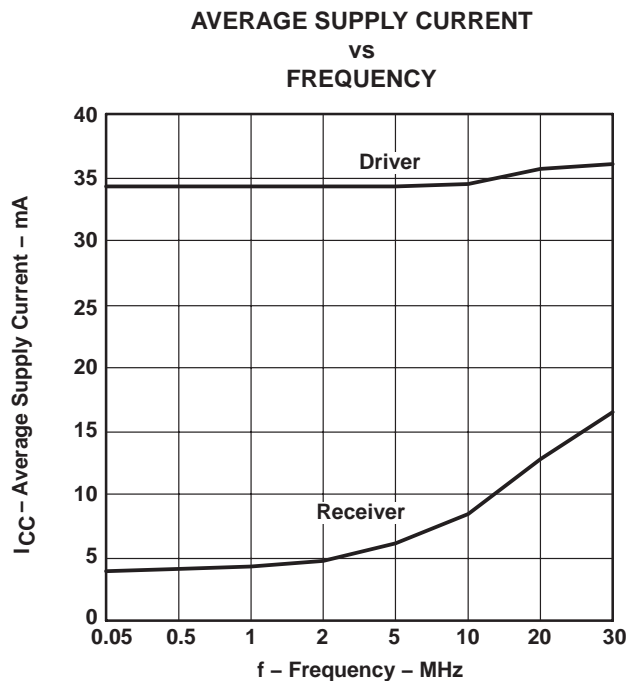


Figure 10

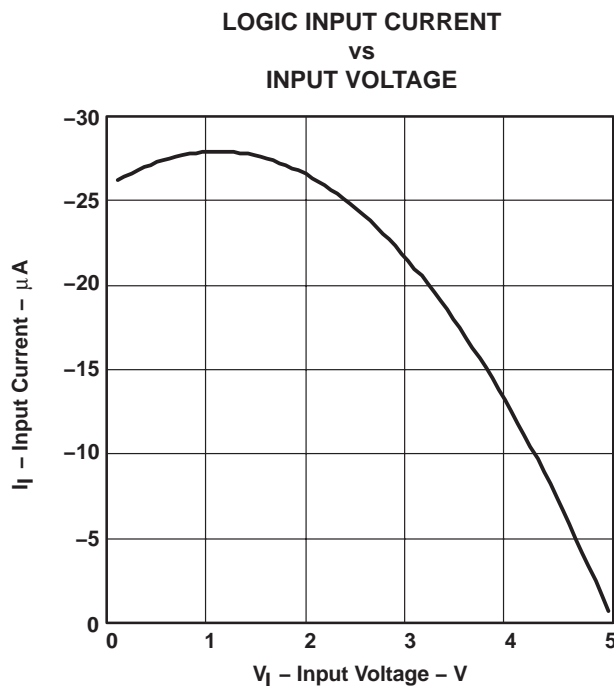


Figure 11

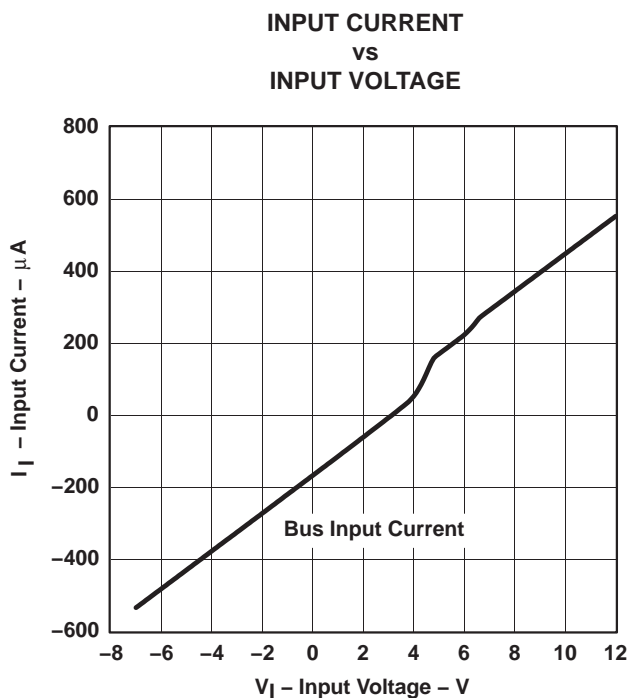


Figure 12

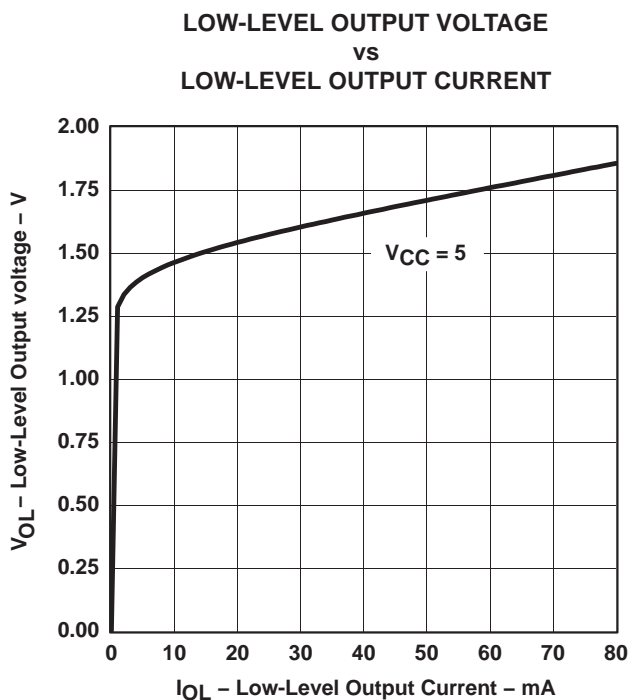


Figure 13

SN65LBC176A-EP DIFFERENTIAL BUS TRANSCEIVER

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TYPICAL CHARACTERISTICS

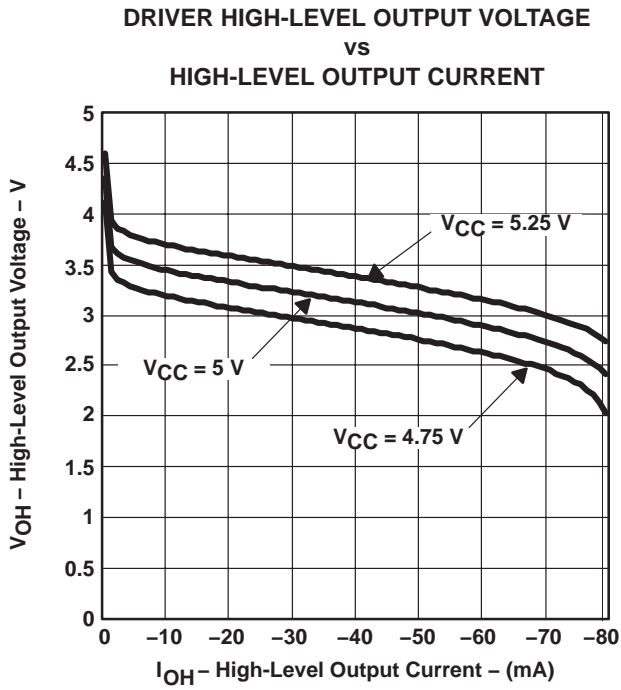


Figure 14

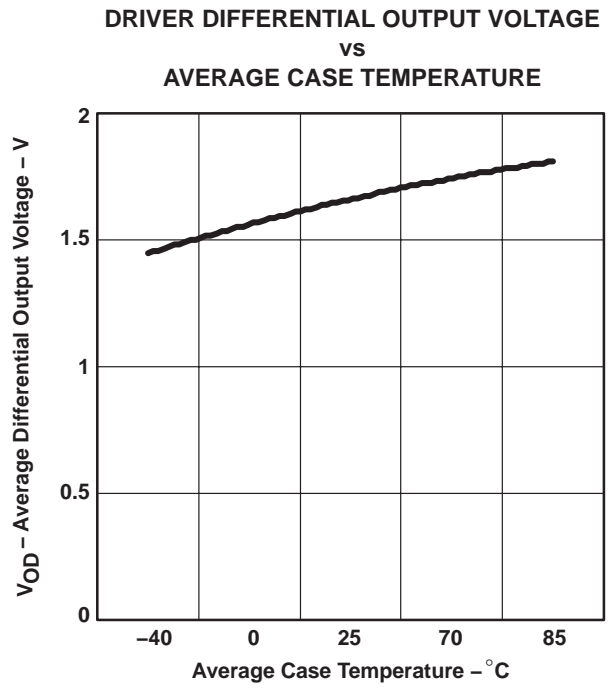


Figure 15

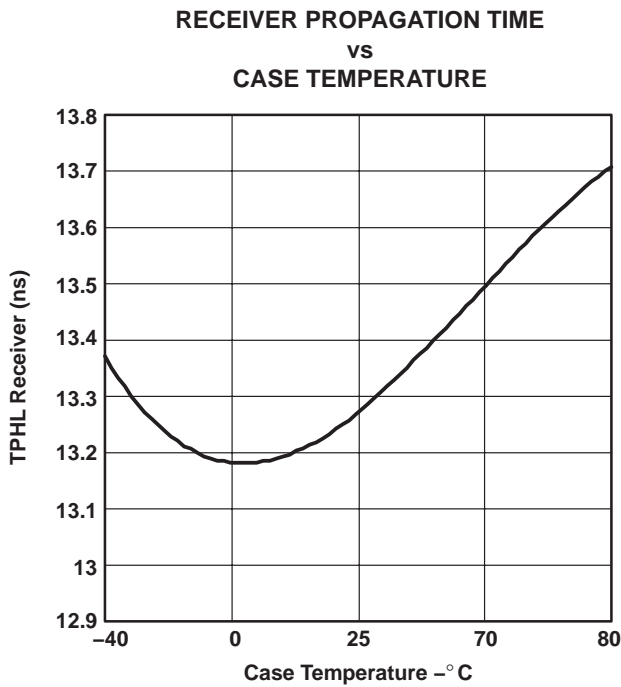


Figure 16

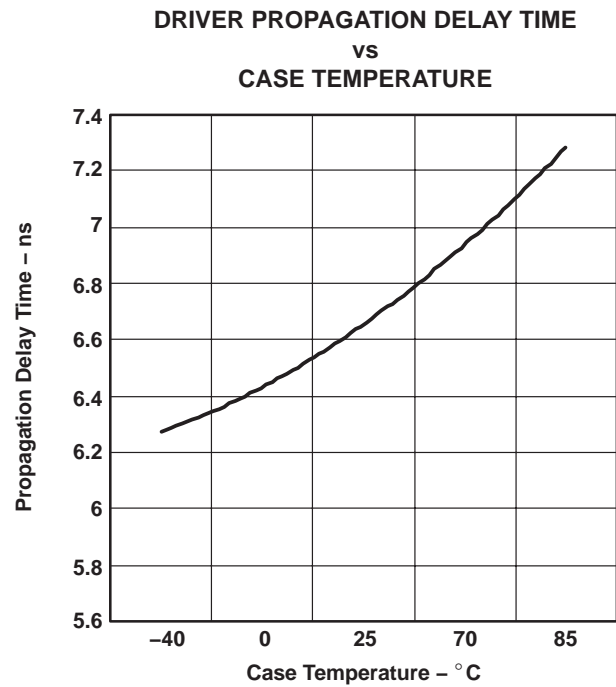


Figure 17

TYPICAL CHARACTERISTICS

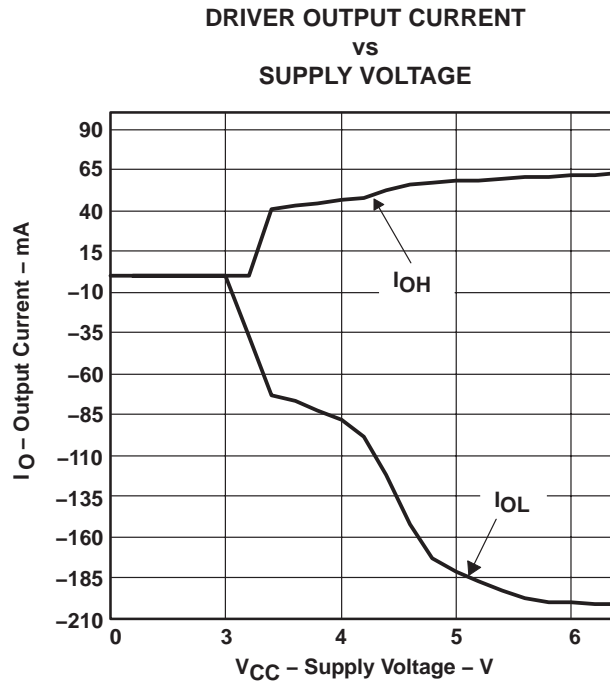


Figure 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC176AMDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	176MEP	Samples
SN65LBC176AQDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	176AEP	Samples
V62/03671-01XE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	176AEP	Samples
V62/03671-02XE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	176MEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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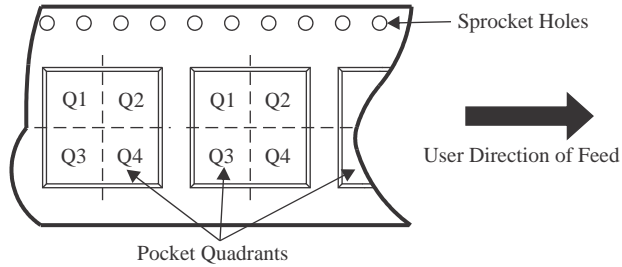
OTHER QUALIFIED VERSIONS OF SN65LBC176A-EP :

- Catalog: [SN65LBC176A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC176AQDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
SN65LBC176AQDREP	SOIC	D	8	2500	350.0	350.0	43.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

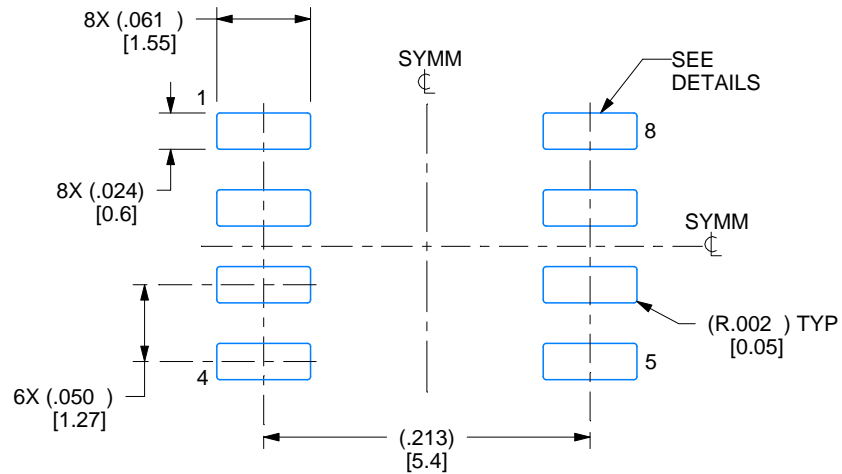
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

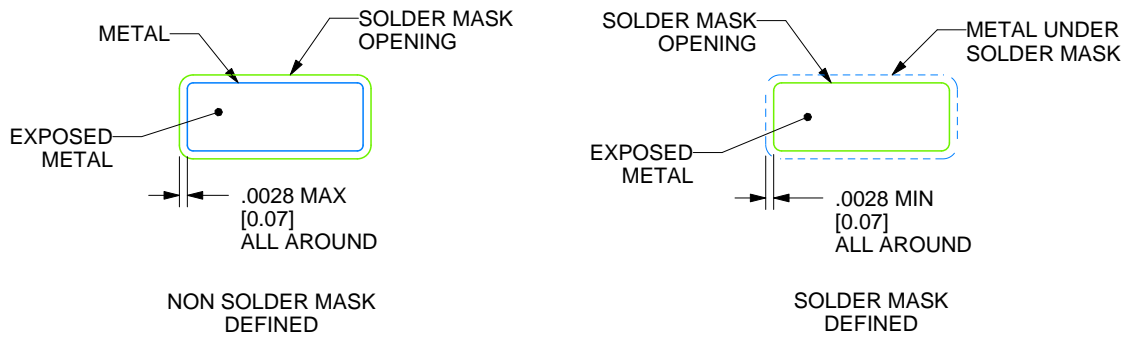
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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