



**THE DATASHEET OF  
CDCV857ADGGRG4**



- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 to 180 MHz
- Low Jitter (cyc–cyc):  $\pm 50$  ps
- Distributes One Differential Clock Input to Ten Differential Outputs
- Three-State Outputs When the Input Differential Clocks Are  $< 20$  MHz
- Operates From Dual 2.5-V Supplies
- Available in a 48-Pin TSSOP Package or 56-Ball MicroStar Junior™ BGA Package
- Consumes  $< 200$ - $\mu$ A Quiescent Current
- External Feedback PIN (FBIN,  $\overline{\text{FBIN}}$ ) Are Used to Synchronize the Outputs to the Input Clocks

## description

The CDCV857A is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to ten differential pairs of clock outputs (Y[0:9],  $\overline{\text{Y}}[0:9]$ ) and one differential pair of feedback clock output (FBO $\overline{\text{OUT}}$ ,  $\overline{\text{FBO}}\text{OUT}$ ). The clock outputs are controlled by the clock inputs (CLK,  $\overline{\text{CLK}}$ ), the feedback clocks (FBIN,  $\overline{\text{FBIN}}$ ), and the analog power input (AV $\overline{\text{DD}}$ ). When  $\overline{\text{PWRDWN}}$  is high, the outputs switch in phase and frequency with CLK. When  $\overline{\text{PWRDWN}}$  is low, all outputs are disabled to high impedance state (3-state), and the PLL is shut down (low power mode). The device also enters this low power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit will detect the low frequency condition and after applying a  $> 20$  MHz input signal this detection circuit turns on the PLL again and enables the outputs.

When AV $\overline{\text{DD}}$  is strapped low, the PLL is turned off and bypassed for test purposes. The CDCV857A is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV857A is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857A is characterized for operation from 0°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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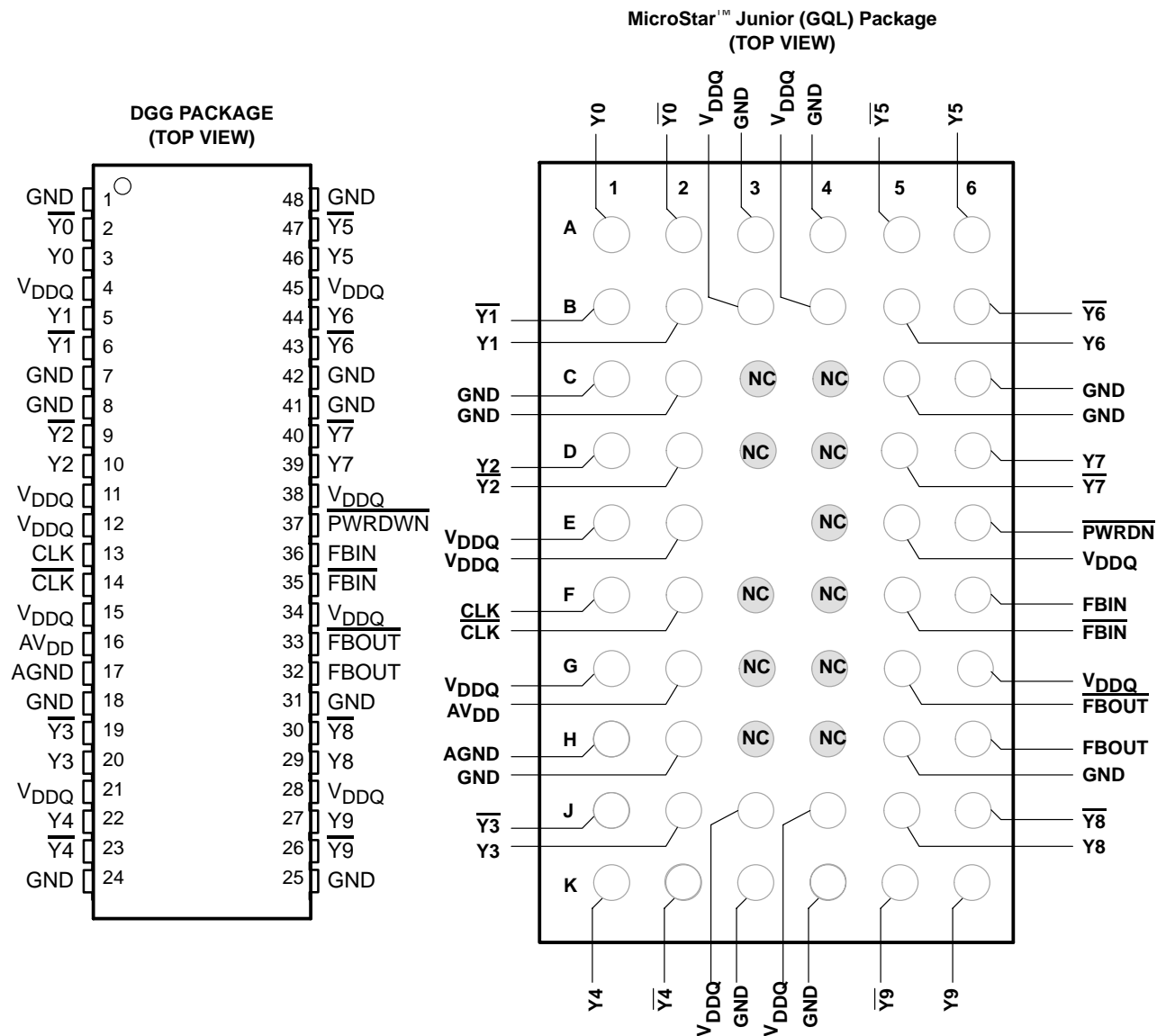
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# CDCV857A

## 2.5-V PHASE LOCK LOOP CLOCK DRIVER

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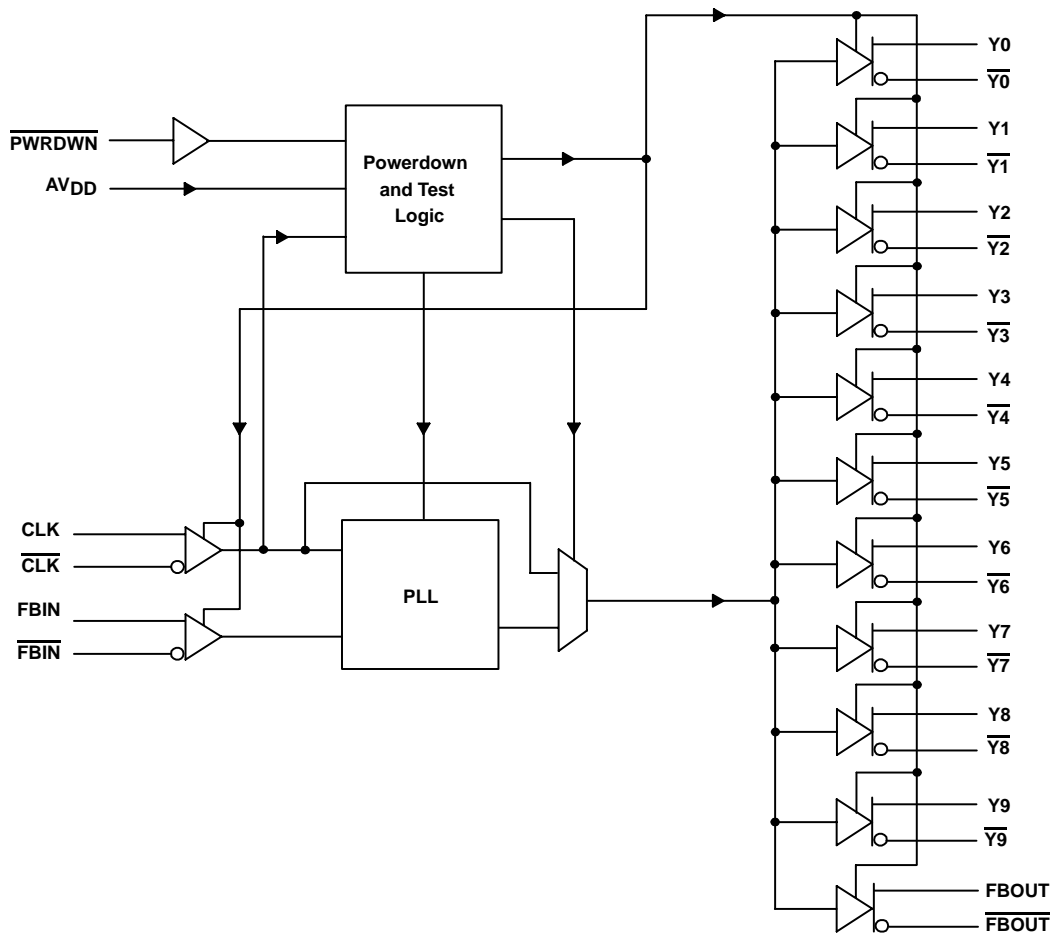


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**FUNCTION TABLE**  
(Select Functions)

INPUTS				OUTPUTS				PLL
AVDD	$\overline{\text{PWRDWN}}$	CLK	$\overline{\text{CLK}}$	Y[0:9]	$\overline{\text{Y[0:9]}}$	FBOU	$\overline{\text{FBOU}}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

**functional block diagram**



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### Terminal Functions

TERMINAL				DESCRIPTION
NAME	DGG	GQL		
AGND	17	H1		Ground for 2.5-V analog supply
AVDD	16	G2		2.5-V Analog supply
CLK, $\overline{\text{CLK}}$	13, 14	F1, F2	I	Differential clock input
$\overline{\text{FBIN}}$ , FBIN	35, 36	F5, F6	I	Feedback differential clock input
FBOU $\overline{\text{T}}$ , FBOU $\overline{\text{T}}$	32, 33	H6, G5	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4		Ground
$\overline{\text{PWRDWN}}$	37	E6	I	Output enable for Y and $\overline{\text{Y}}$
VDDQ	4, 11, 12, 15, 21, 28, 34, 38, 45	B3, B4, E1, E2, E5, G1, G6, J3, J4		2.5-V Supply
Y[0:9]	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	A1, B2, D1, J2, K1, A6, B5, D6, J5, K6	O	Buffered output copies of input clock, CLK
$\overline{\text{Y}}[0:9]$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	A2, B1, D2, J1, K2, A5, B6, D5, J6, K5	O	Buffered output copies of input clock, $\overline{\text{CLK}}$

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>DDQ</sub> , AV <sub>DD</sub>	0.5 V to 3.6 V
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub> )	±50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub> )	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DDQ</sub> )	±50 mA
Continuous current to GND or V <sub>DDQ</sub>	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package	89°C/W
GQL package	137.6°C/W
Storage temperature range T <sub>stg</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This value is limited to 3.6 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51.



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### recommended operating conditions (see Note 4)

		MIN	TYP	MAX	UNIT
Supply voltage, $V_{DDQ}$ , $AV_{DD}$		2.3		2.7	V
Low level input voltage, $V_{IL}$	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$			$V_{DDQ}/2 - 0.18$	V
	$\overline{\text{PWRDWN}}$	-0.3		0.7	
High level input voltage, $V_{IH}$	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$	$V_{DDQ}/2 + 0.18$			V
	$\overline{\text{PWRDWN}}$	1.7		$V_{DDQ} + 0.3$	
DC input signal voltage (see Note 5)		-0.3		$V_{DDQ}$	V
Differential input signal voltage, $V_{ID}$ (see Note 6)	DC   CLK, FBIN	0.36		$V_{DDQ} + 0.6$	V
	AC   CLK, FBIN	0.7		$V_{DDQ} + 0.6$	
Output differential cross-voltage, $V_{OX}$ (see Note 7)		$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V
Input differential pair cross-voltage, $V_{IX}$ (see Note 7)		$V_{DDQ}/2 - 0.2$		$V_{DDQ}/2 + 0.2$	V
High-level output current, $I_{OH}$				-12	mA
Low-level output current, $I_{OL}$				12	mA
Input slew rate, SR		1		4	V/ns
Operating free-air temperature, $T_A$		0		85	°C

- NOTES:
4. Unused inputs must be held high or low to prevent them from floating.
  5. DC input signal voltage specifies the allowable dc execution of differential input.
  6. Differential input signal voltage specifies the differential voltage  $|V_{TR} - V_{CP}|$  required for switching, where  $V_{TR}$  is the true input level and  $V_{CP}$  is the complementary input level.
  7. Differential cross-point voltage is expected to track variations of  $V_{CC}$  and is the voltage at which the differential signals must be crossing.

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## 2.5-V PHASE LOCK LOOP CLOCK DRIVER

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input voltage	All inputs V <sub>DDQ</sub> = 2.3 V, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>DDQ</sub> = min to max, I <sub>OH</sub> = -1 mA	V <sub>DDQ</sub> - 0.1			V
		V <sub>DDQ</sub> = 2.3 V, I <sub>OH</sub> = -12 mA	1.7			
V <sub>OL</sub>	Low-level output voltage	V <sub>DDQ</sub> = min to max, I <sub>OL</sub> = 1 mA			0.1	V
		V <sub>DDQ</sub> = 2.3 V, I <sub>OL</sub> = 12 mA			0.6	
I <sub>OH</sub>	High-level output current	V <sub>DDQ</sub> = 2.3 V, V <sub>O</sub> = 1 V	-18	-32		mA
I <sub>OL</sub>	Low-level output current	V <sub>DDQ</sub> = 2.3 V, V <sub>O</sub> = 1.2 V	26	35		mA
V <sub>O</sub>	Output voltage swing	Differential outputs are terminated with 120 Ω	1.1		V <sub>DDQ</sub> - 0.4	V
V <sub>OX</sub>	Output differential cross-voltage§		V <sub>DDQ</sub> /2 - 0.2	V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 + 0.2	
I <sub>I</sub>	Input current	V <sub>DDQ</sub> = 2.7 V, V <sub>I</sub> = 0 V to 2.7 V			±10	μA
I <sub>OZ</sub>	High-impedance-state output current	V <sub>DDQ</sub> = 2.7 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND			±10	μA
I <sub>DDPD</sub>	Power down current on V <sub>DDQ</sub> + AV <sub>DD</sub>	CLK and $\overline{\text{CLK}}$ = 0 MHz; $\overline{\text{PWRDWN}}$ = Low; Σ of I <sub>DD</sub> and A <sub>IDD</sub>		100	200	μA
I <sub>DD</sub>	Dynamic current on V <sub>DDQ</sub>	Differential outputs terminated with 120 Ω/CL = 14 pF	f <sub>O</sub> = 180 MHz	275	330	mA
			f <sub>O</sub> = 167 MHz	250	300	
		Differential outputs terminated with 120 Ω/CL = 0 pF	f <sub>O</sub> = 180 MHz	225	275	
			f <sub>O</sub> = 167 MHz	210	250	
A <sub>IDD</sub>	Supply current on AV <sub>DD</sub>	f <sub>O</sub> = 180 MHz		10	12	mA
		f <sub>O</sub> = 167 MHz		8	10	
C <sub>I</sub>	Input capacitance	V <sub>CC</sub> = 2.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	2	2.5	3	pF
C <sub>O</sub>	Output capacitance	V <sub>CC</sub> = 2.5 V, V <sub>O</sub> = V <sub>CC</sub> or GND	2.5	3	3.5	pF

† All typical values are at respective nominal V<sub>DDQ</sub>.

‡ The value of V<sub>OC</sub> is expected to be |V<sub>TR</sub> + V<sub>CP</sub>]/2. In case of each clock directly terminated by a 120-Ω resistor, where V<sub>TR</sub> is the true input signal voltage and V<sub>CP</sub> is the complementary input signal voltage.

§ Differential cross-point voltage is expected to track variations of V<sub>DDQ</sub> and is the voltage at which the differential signals must be crossing.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f <sub>CLK</sub>	Operating clock frequency	60	180	MHz
	Application clock frequency			
Input clock duty cycle		40%	60%	
Stabilization time¶ (PLL mode)			10	μs
Stabilization time¶ (Bypass mode)			30	ns

¶ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.



**switching characteristics**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT	
t <sub>PLH</sub> <sup>‡</sup>	Low to high level propagation delay time	Test mode/CLK to any output		4.5		ns	
t <sub>PHL</sub> <sup>‡</sup>	High-to low level propagation delay time	Test mode/CLK to any output		4.5		ns	
t <sub>jit(per)</sub> <sup>§</sup>	Jitter (period), See Figure 6	66 MHz	-55		55	ps	
		100/133/167/180 MHz	-35		35	ps	
t <sub>jit(cc)</sub> <sup>§</sup>	Jitter (cycle-to-cycle), See Figure 3	66 MHz	-60		60	ps	
		100/133/167/180 MHz	-50		50	ps	
t <sub>jit(hper)</sub> <sup>§</sup>	Half-period jitter, See Figure 7	66 MHz	-100		100	ps	
		100/133/167/180 MHz	-75		75	ps	
t <sub>slr(i)</sub>	Input clock slew rate, See Figure 8		1		4	V/ns	
t <sub>slr(o)</sub>	Output clock slew rate, See Figure 8		1		2	V/ns	
t <sub>d(∅)</sub> <sup>§</sup>	Dynamic phase offset (this includes jitter), See Figure 4(b)	SSC off	66 MHz	-180		180	ps
			100/133 MHz	-130		130	
			167/180 MHz	-90		90	
		SSC on	66 MHz	-230		230	
			100/133 MHz	-170		170	
			167/180 MHz	-100		100	
t <sub>(∅)</sub>	Static phase offset, See Figure 4(a)	66 MHz	-150		150	ps	
		100/133/167/180 MHz	-100		100		
t <sub>sk(o)</sub> <sup>¶</sup>	Output skew, See Figure 5				75	ps	
t <sub>r</sub> , t <sub>f</sub>	Output rise and fall times (20% – 80%)	Load: 120 Ω/14 pF	650		900	ps	

<sup>†</sup> All typical values are at a respective nominal V<sub>DDQ</sub>.

<sup>‡</sup> Refers to transition of noninverting output.

<sup>§</sup> This parameter is assured by design but can not be 100% production tested.

<sup>¶</sup> All differential output pins are terminated with 120 Ω/14 pF.

# CDCV857A 2.5-V PHASE LOCK LOOP CLOCK DRIVER

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## PARAMETER MEASUREMENT INFORMATION

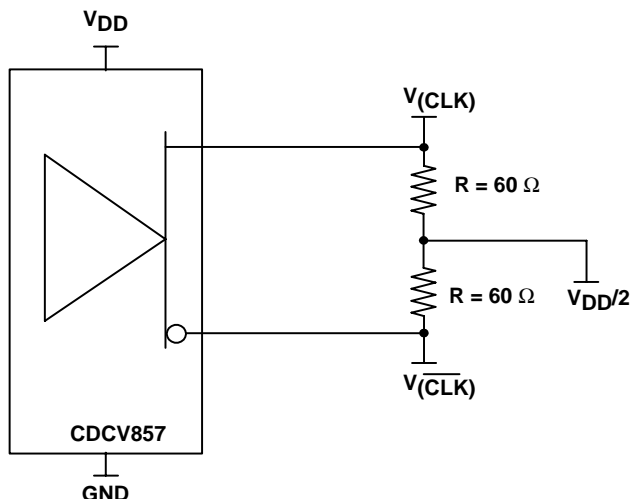
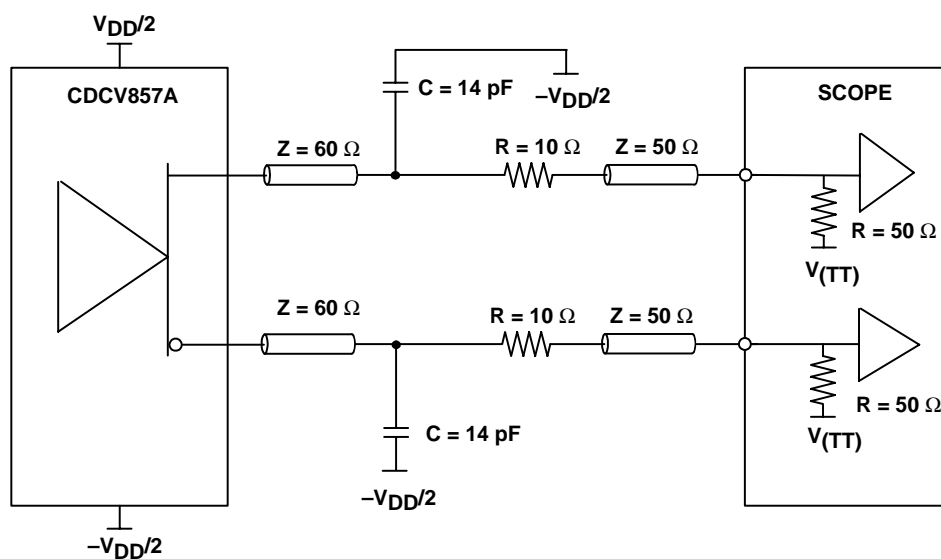


Figure 1. IBIS Model Output Load (used for slew rate measurement)



NOTE:  $V_{(TT)} = \text{GND}$

Figure 2. Output Load Test Circuit

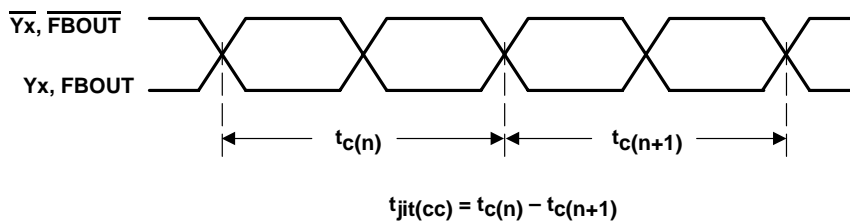


Figure 3. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION

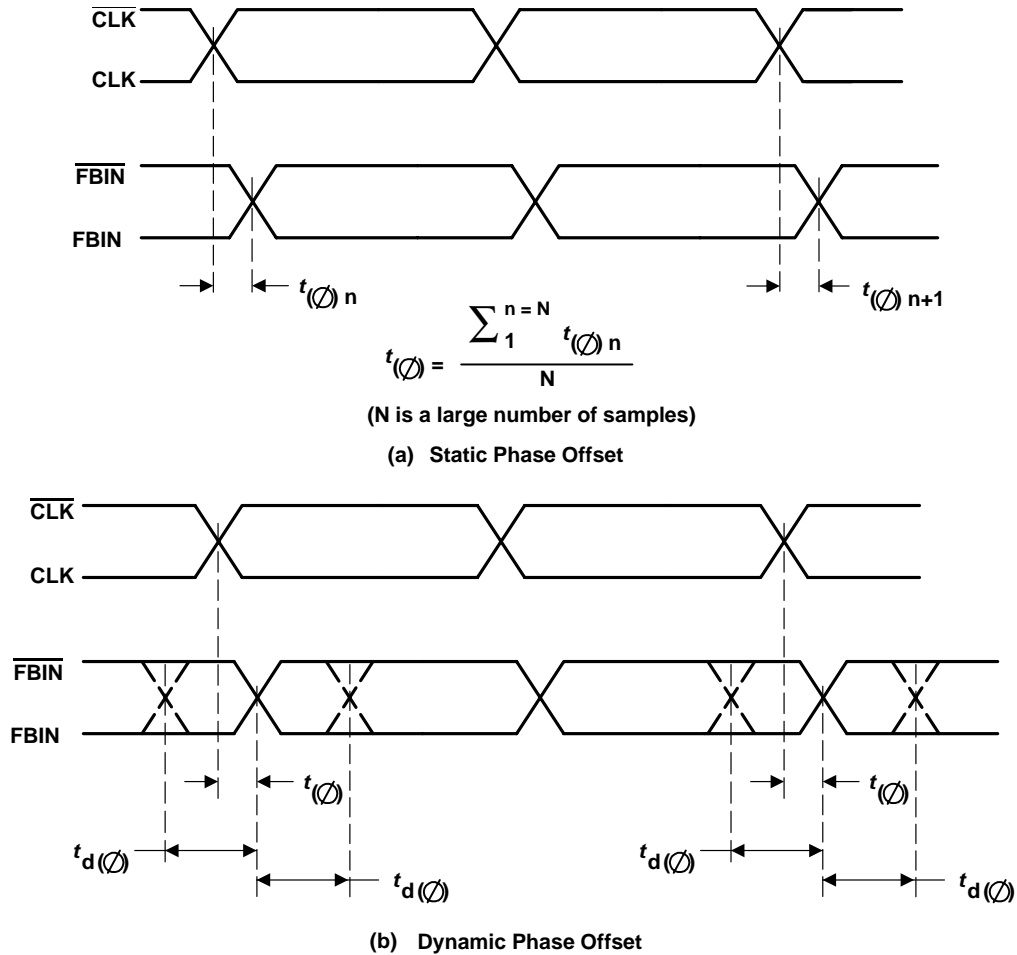


Figure 4. Phase Offset

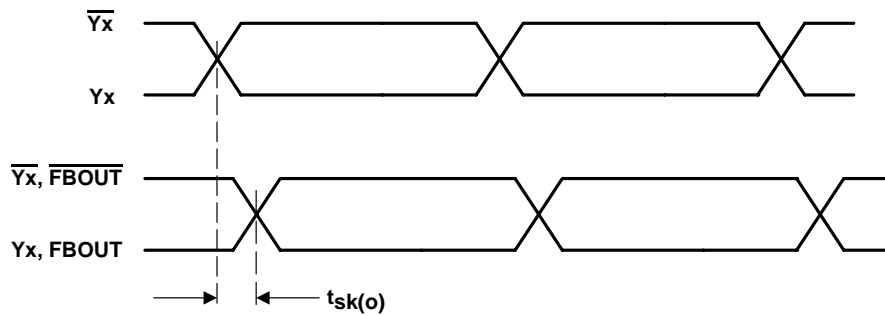


Figure 5. Output Skew

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### PARAMETER MEASUREMENT INFORMATION

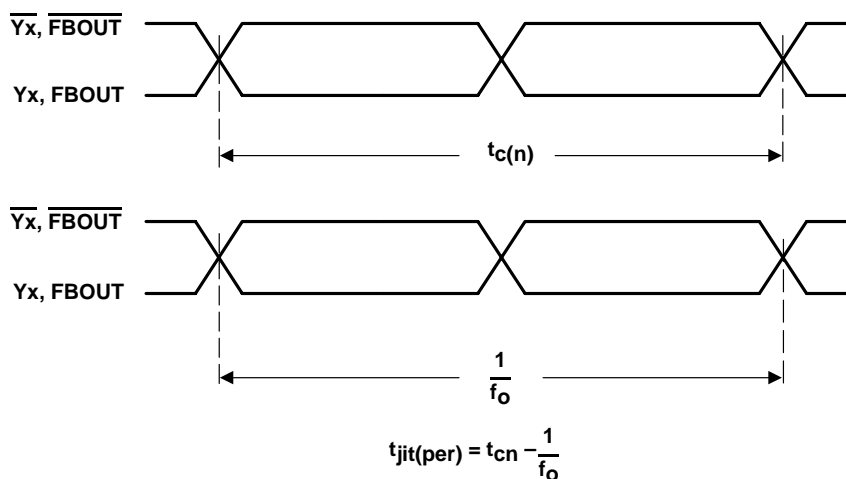


Figure 6. Period Jitter

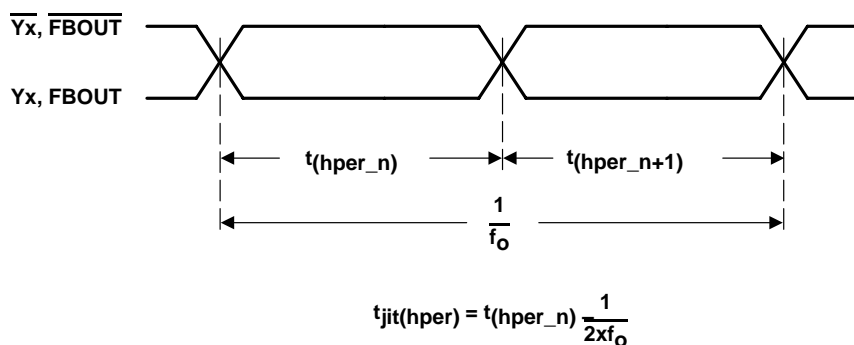


Figure 7. Half-Period Jitter



Figure 8. Input and Output Slew Rates

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCV857ADGG	NRND	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	CDCV857A	
CDCV857ADGGG4	NRND	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	CDCV857A	
CDCV857ADGGR	NRND	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	CDCV857A	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCV857ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCV857ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDCV857ADGG	DGG	TSSOP	48	40	530	11.89	3600	4.9
CDCV857ADGGG4	DGG	TSSOP	48	40	530	11.89	3600	4.9

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