# THE DATASHEET OF

# SN65LBC175N

# SN65LBC175, SN75LBC175 Quadruple Low-Power Differential Line Receivers

## 1 Features

- Meets or exceeds the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT recommendation V.11
- Designed to operate with pulse durations as short as 20 ns
- Designed for multipoint transmission on long bus lines in noisy environments
- Input sensitivity: ±200 mV
- Low-power consumption: 20 mA maximum
- Open-circuit fail-safe design
- Common-mode input voltage range of −7 V to 12 V
- Pin compatible with SN75175 and LTC489

## 2 Applications

- Factory automation
- ATM and cash counters
- Smart grid
- AC and servo motor drives

## 3 Description

The SN65LBC175 and SN75LBC175 are monolithic, quadruple, differential line receivers with 3-state outputs designed to meet the requirements of the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT Recommendation V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The receivers are enabled in pairs, with an active-high enable input. Each differential receiver input features high impedance, hysteresis for increased noise immunity, and sensitivity of ±200 mV over a common-mode input voltage range of 12 V to −7 V. The fail-safe design ensures that when the inputs are open-circuited, the outputs are always high. Both devices are designed using the TI proprietary LinBiCMOS™ technology allowing low power consumption, high switching speeds, and robustness.

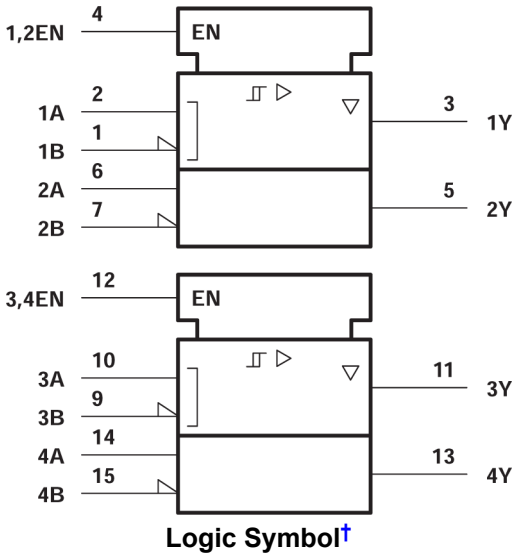
These devices offer optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC175 is available in the 16-pin DIP (N), small-outline package (D), and the wide small-outline package (DW). The SN75LBC175 is available in the 16-pin DIP (N) and the small-outline package (D).

The SN65LBC175 is characterized over the industrial temperature range of −40°C to 85°C. The SN75LBC175 is characterized for operation over the commercial temperature range of 0°C to 70°C.

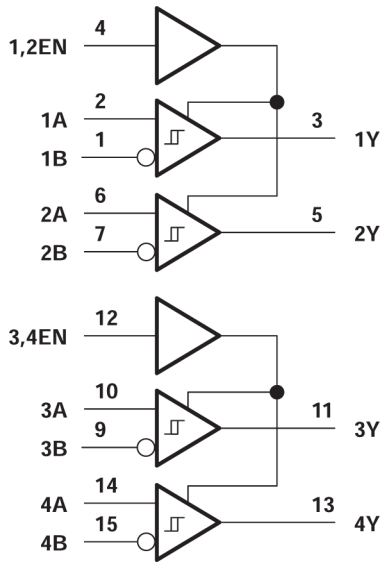
**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| SN65LBC175<br>SN75LBC175 | D (SOIC, 16) | 9.9 mm × 6 mm |
| | DW (SOIC, 16) | 10.3 mm × 10.3 mm |
| | N (PDIP, 16) | 19.3 mm × 9.4 mm |

(1) For more information see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Logic Symbol†**




**Logic Diagram (Positive Logic)**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# Table of Contents

# 4 Pin Configuration and Functions

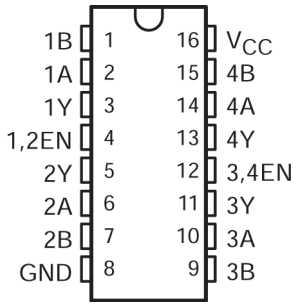



**Figure 4-1. D, DW, or N Package (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1B | 1 | I | Channel 1 Inverting Differential Input |
| 1A | 2 | I | Channel 1 Non-Inverting Differential Input |
| 1Y | 3 | O | Channel 1 Output |
| 1,2 EN | 4 | I | Channel 1 and 2 Active High Enable |
| 2Y | 5 | O | Channel 2 Output |
| 2A | 6 | I | Channel 2 Non-Inverting Differential Input |
| 2B | 7 | I | Channel 2 Inverting Differential Input |
| GND | 8 | GND | Device Ground |
| 3B | 9 | I | Channel 3 Inverting Differential Input |
| 3A | 10 | I | Channel 3 Non-Inverting Differential Input |
| 3Y | 11 | O | Channel 3 Output |
| 3,4 EN | 12 | I | Channel 3 and 4 Active High Enable |
| 4Y | 13 | O | Channel 4 Output |
| 4A | 14 | I | Channel 4 Non-Inverting Differential Input |
| 4B | 15 | I | Channel 4 Inverting Differential Input |
| $V_{CC}$ | 16 | POW | Device Supply |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ (see (2)) | Supply voltage range | | −0.3 | 7 | V |
| $V_I$ | Input voltage | (A or B inputs) | | ±25 | V |
| $V_{ID}$ (see (3)) | Differential input voltage | | | ±25 | V |
| | Voltage range at Y, 1/2EN, 3/4EN | | −0.3 | $V_{CC}$ + 0.5 | V |
| | Continuous total dissipation | | See Dissipation Rating Table | | |
| $T_A$ | Operating free-air temperature range: | SN65LBC175 | −40 | 85 | °C |
| | | SN75LBC175 | 0 | 70 | °C |
| $T_{stg}$ | Storage temperature range | | −65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1500 | |
| | | Machine Model (MM) | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

over operating free-air temperature range (unless otherwise noted)

## 5.3 Dissipation Rating Table

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D | 1100 mW | 8.7 mW/°C | 709 mW | 578 mW |
| DW | 1200 mW | 9.6 mW/°C | 770 mW | 625 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

## 5.4 Thermal Information

| THERMAL METRIC[1] | | SOIC (D) | SOIC (DW) | PDIP (N) | UNIT |
|---|---|---|---|---|---|
| | | 16 Pins | 16 Pins | 16 Pins | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 84.6 | 71.1 | 60.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 43.5 | 37.4 | 48.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 43.2 | 36.8 | 40.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.4 | 13.3 | 27.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 42.8 | 36.4 | 40.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 5.5 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, $V_{IC}$ | | −7 | | 12 | V |
| Differential input voltage, $V_{ID}$ | | | | ±6 | V |
| High-level input voltage, $V_{IH}$ | EN inputs | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | EN inputs | | | 0.8 | V |
| High-level output current, $I_{OH}$ | | | | −8 | mA |
| Low-level output current, $I_{OL}$ | | | | 8 | mA |
| Operating free-air temperature, $T_A$ | SN65LBC175 | −40 | | 85 | °C |
| | SN75LBC175 | 0 | | 70 | |

## 5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IT}+$ | Positive-going input threshold voltage | | $I_O$ = −8 mA | | | 0.2 | | | V |
| $V_{IT}-$ | Negative-going input threshold voltage | | $I_O$ = 8 mA | | | −0.2 | | | V |
| $V_{hys}$ | Hysteresis voltage ($V_{IT}+ - V_{IT}-$) | | | | | | 45 | | mV |
| $V_{IK}$ | Enable input clamp voltage | | $I_I$ = −18 mA | | | | −0.9 | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 200 mV, | $I_{OH}$ = −8 mA | | 3.5 | 4.5 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = −200 mV, | $I_{OL}$ = 8 mA | | | 0.3 | 0.5 | V |
| $I_{OZ}$ | High-impedance-state output current | | $V_O$ = 0 V to $V_{CC}$ | | | | | ±20 | µA |
| $I_I$ | Bus input current | A or B inputs | $V_{IH}$ = 12 V, | $V_{CC}$ = 5 V, | Other inputs at 0 V | 0.7 | | 1 | mA |
| | | | $V_{IH}$ = 12 V, | $V_{CC}$ = 0 V, | Other inputs at 0 V | 0.8 | | 1 | |
| | | | $V_{IH}$ = −7 V, | $V_{CC}$ = 5 V, | Other inputs at 0 V | −0.5 | | −0.8 | |
| | | | $V_{IH}$ = −7 V, | $V_{CC}$ = 0 V, | Other inputs at 0 V | −0.4 | | −0.8 | |
| $I_{IH}$ | High-level enable input current | | $V_{IH}$ = 5 V | | | | | ±20 | µA |
| $I_{IL}$ | Low-level enable input current | | $V_{IL}$ = 0 V | | | | | −20 | µA |
| $I_{OS}$ | Short-circuit output current | | $V_O$ = 0 | | | −80 | | −120 | mA |
| $I_{CC}$ | Supply current | | Outputs enabled, | $I_O$ = 0, | $V_{ID}$ = 5 V | | 11 | 20 | mA |
| | | | Outputs disabled | | | | 0.9 | 1.4 | |

(1) All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.

## 5.7 Switching Characteristics

$V_{CC}$ = 5 V, $C_L$ = 15 pF, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation delay time, high- to low-level output | $V_{ID}$ = −1.5 V to 1.5 V, See Figure 6-1 | 11 | 22 | 30 | ns |
| $t_{PLH}$ | Propagation delay time, low- to high-level output | | 11 | 22 | 30 | ns |
| $t_{PZH}$ | Output enable time to high level | See Figure 6-2 | | 17 | 30 | ns |
| $t_{PZL}$ | Output enable time to low level | See Figure 6-3 | | 18 | 30 | ns |
| $t_{PHZ}$ | Output disable time from high level | See Figure 6-2 | | 30 | 40 | ns |
| $t_{PLZ}$ | Output disable time from low level | See Figure 6-3 | | 23 | 30 | ns |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | See Figure 6-2 | | 4 | 6 | ns |
| $t_t$ | Transition time | See Figure 6-1 | | 3 | 10 | ns |

## 5.8 Typical Characteristics

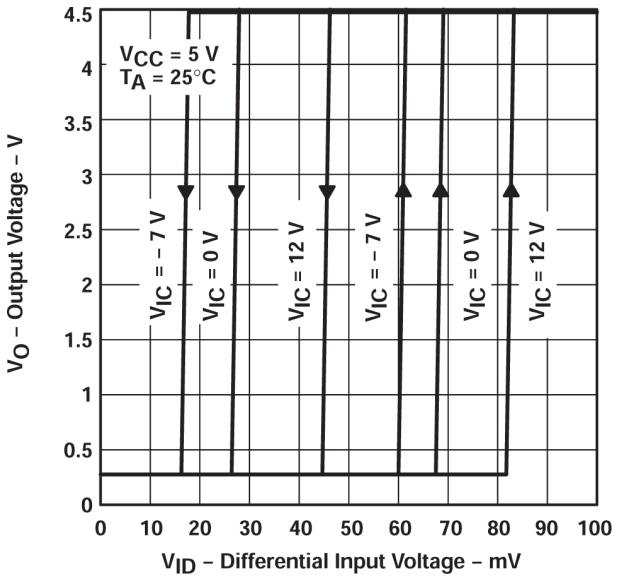



**Figure 5-1. Output Voltage vs Differential Input Voltage**

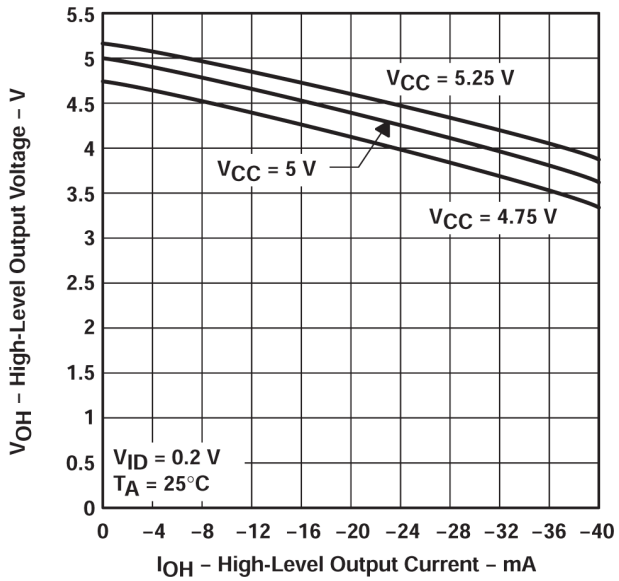



**Figure 5-2. High-level Output Voltage vs High-level Output Current**

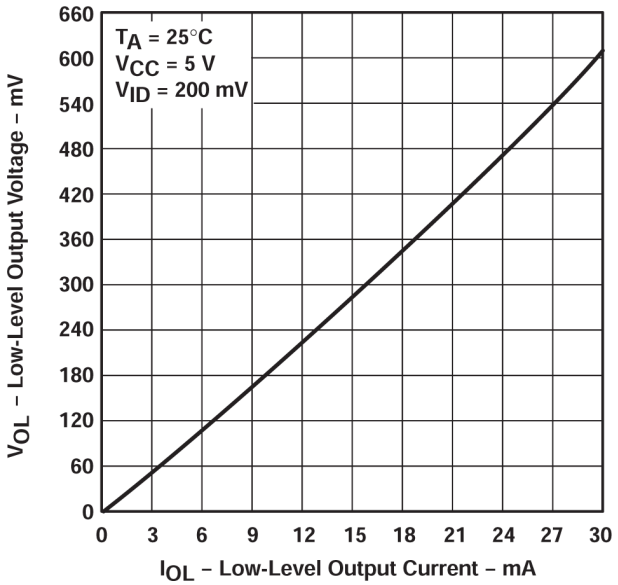



**Figure 5-3. Low-level Output Voltage vs Low-level Output Current**

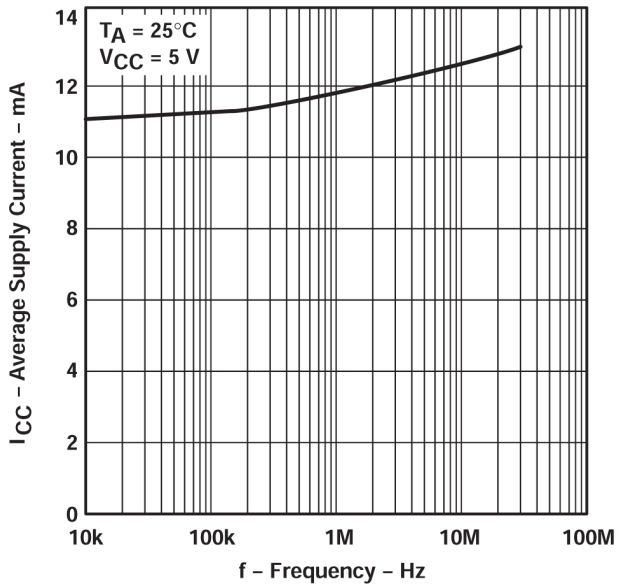



**Figure 5-4. Average Supply Current vs Frequency**

## 5.8 Typical Characteristics (continued)

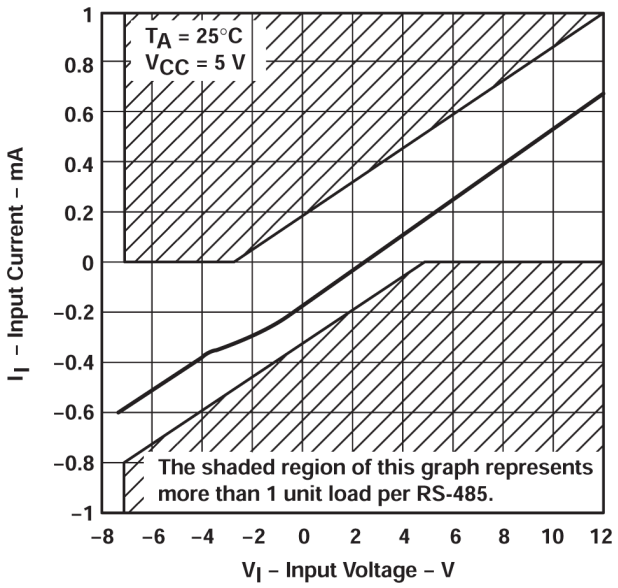



**Figure 5-5. Input Current vs Input Voltage (Complementary Input at 0 v)**

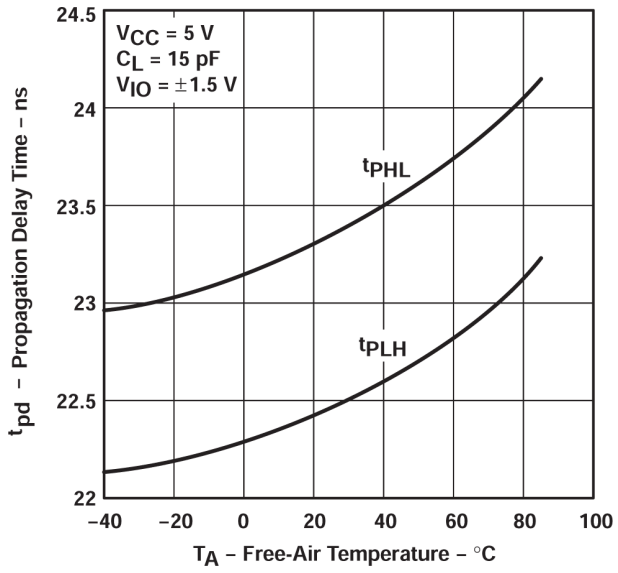



**Figure 5-6. Propagation Delay Time vs Free-air Temperature**

## 6 Parameter Measurement Information

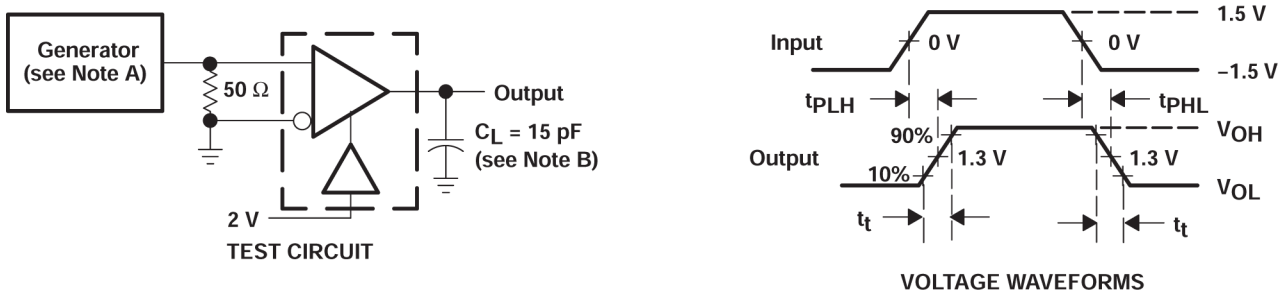
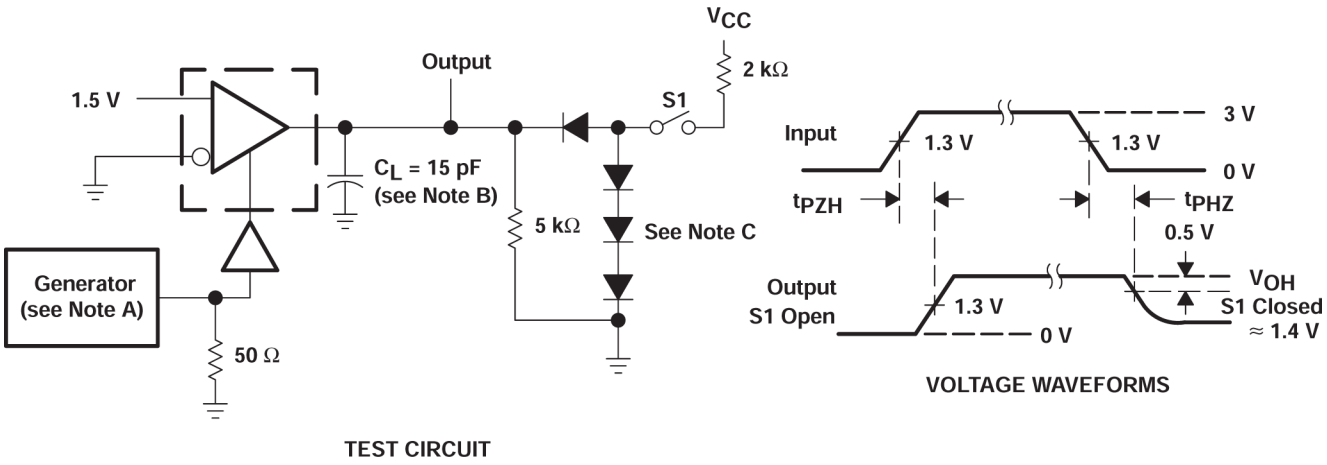
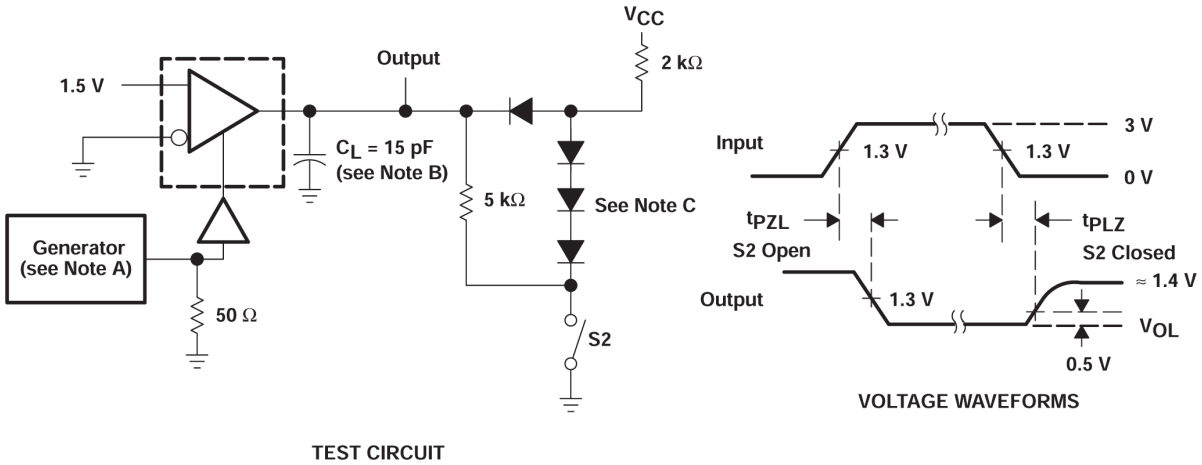



**Figure 6-1. $t_{PLH}$ and $t_{PHL}$ Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

**Figure 6-2. $t_{PHZ}$ and $t_{PZH}$ Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

**Figure 6-3. $t_{PZL}$ and $t_{PLZ}$ Test Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Device Functional Modes

**Table 7-1. Function Table (Each Receiver)**

| DIFFERENTIAL INPUTS | ENABLE[1] | OUTPUT |
|---|---|---|
| A−B | | Y |
| $V_{ID} \geq 0.2$ V | H | H |
| −0.2 V < $V_{ID}$ < 0.2 V | H | ? |
| $V_{ID} \leq -0.2$ V | H | L |
| X | L | Z |
| Open circuit | H | H |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

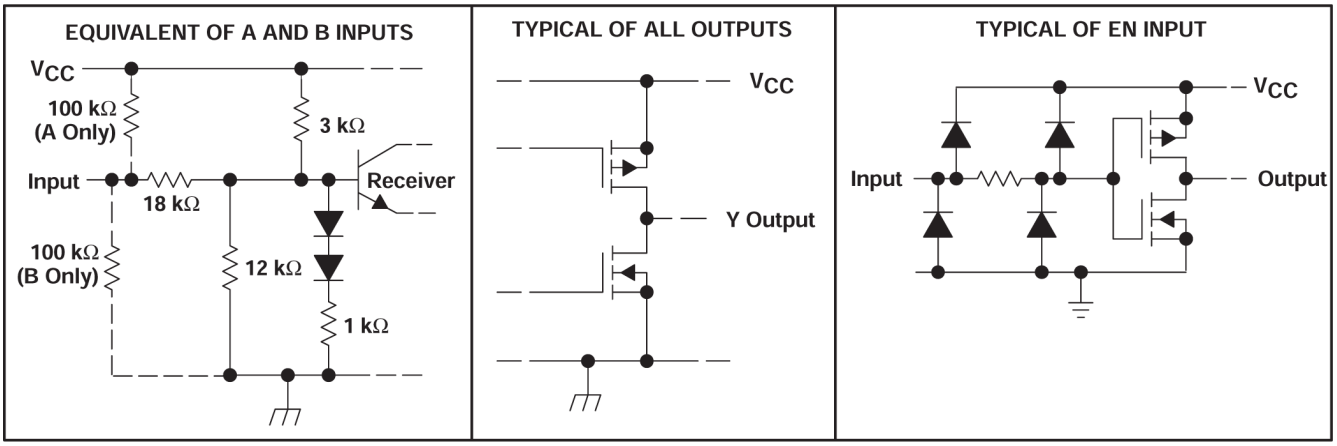



**Figure 7-1. Schematics of Inputs and Outputs**

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (March 2009) to Revision H (November 2023) | Page |
|---|---|
| • Changed the numbering format for tables, figures, and cross-references throughout the document | 1 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC175D | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65LBC175 | |
| SN65LBC175DG4 | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65LBC175 | |
| SN65LBC175DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65LBC175 | Samples |
| SN65LBC175DW | LIFEBUY | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65LBC175 | |
| SN65LBC175DWG4 | LIFEBUY | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65LBC175 | |
| SN65LBC175DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65LBC175 | Samples |
| SN65LBC175N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN65LBC175N | Samples |
| SN75LBC175D | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75LBC175 | |
| SN75LBC175DR | LIFEBUY | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75LBC175 | |
| SN75LBC175N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75LBC175N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN75LBC175 :**

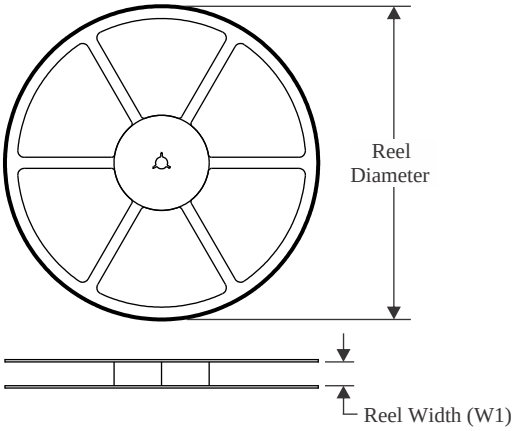
- Military : SN55LBC175

NOTE: Qualified Version Definitions:

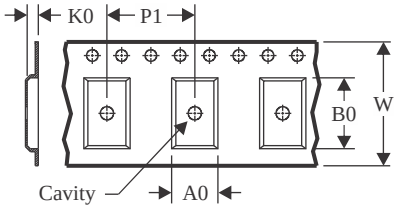
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

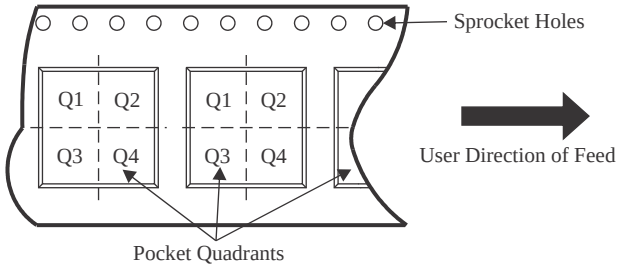



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

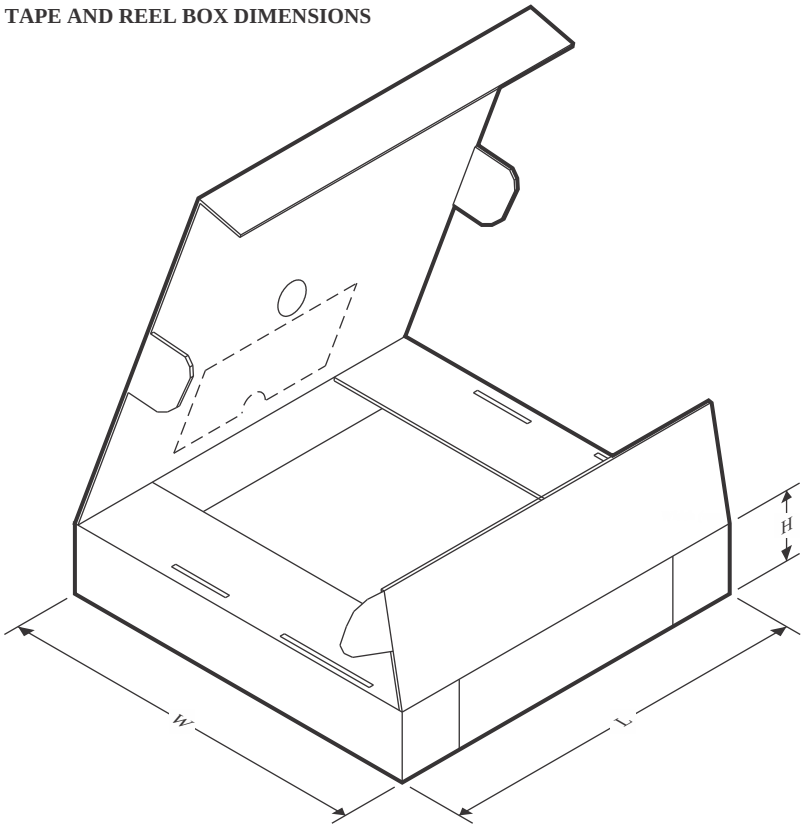
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65LBC175DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| SN75LBC175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75LBC175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

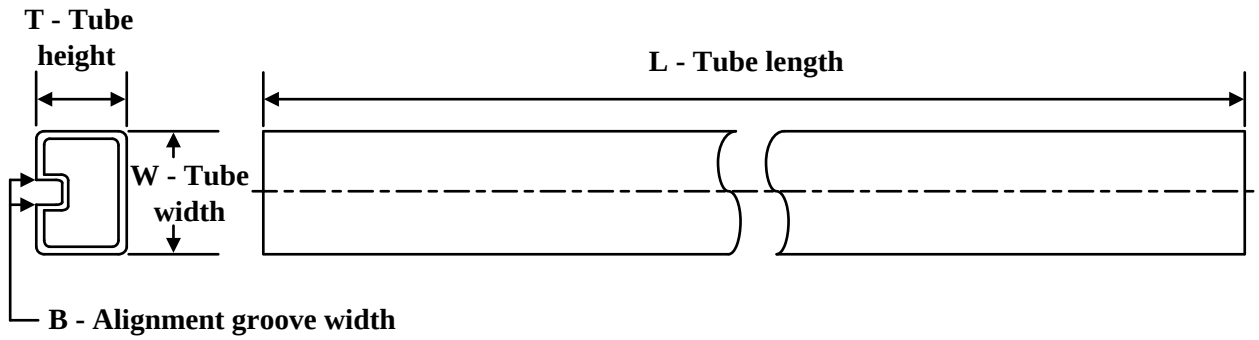
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LBC175DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65LBC175DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| SN75LBC175DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN75LBC175DR | SOIC | D | 16 | 2500 | 350.0 | 350.0 | 43.0 |

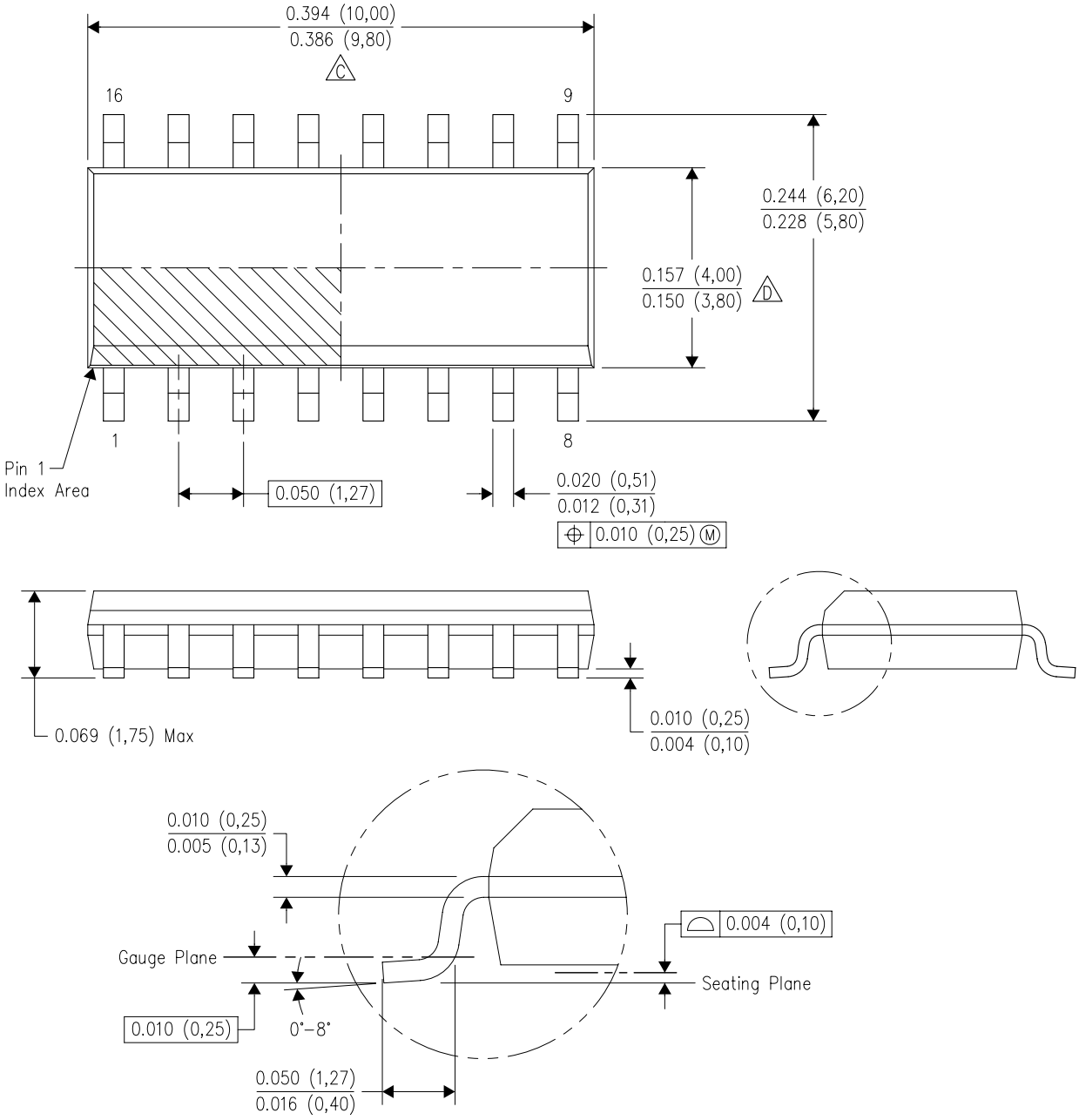
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN65LBC175D | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN65LBC175D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN65LBC175DG4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN65LBC175DG4 | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN65LBC175DW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| SN65LBC175DWG4 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| SN65LBC175N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75LBC175D | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN75LBC175D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN75LBC175N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# GENERIC PACKAGE VIEW

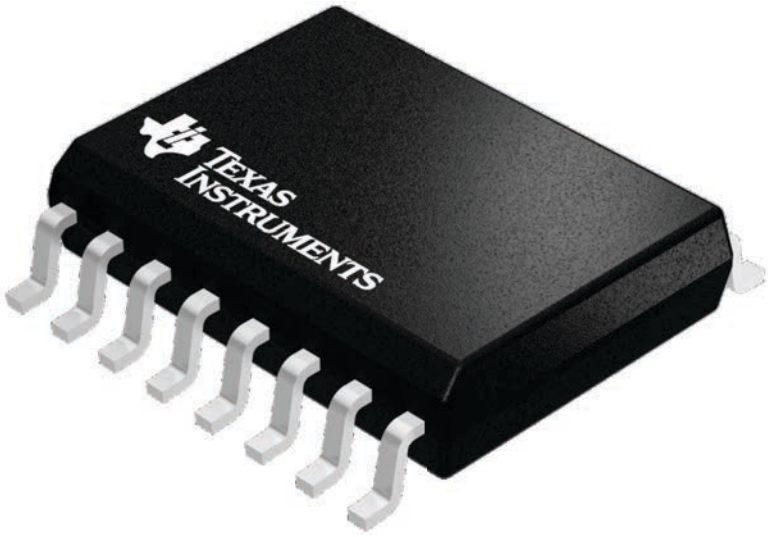
## DW 16

## SOIC - 2.65 mm max height

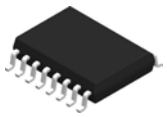
**7.5 x 10.3, 1.27 mm pitch**

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224780/A

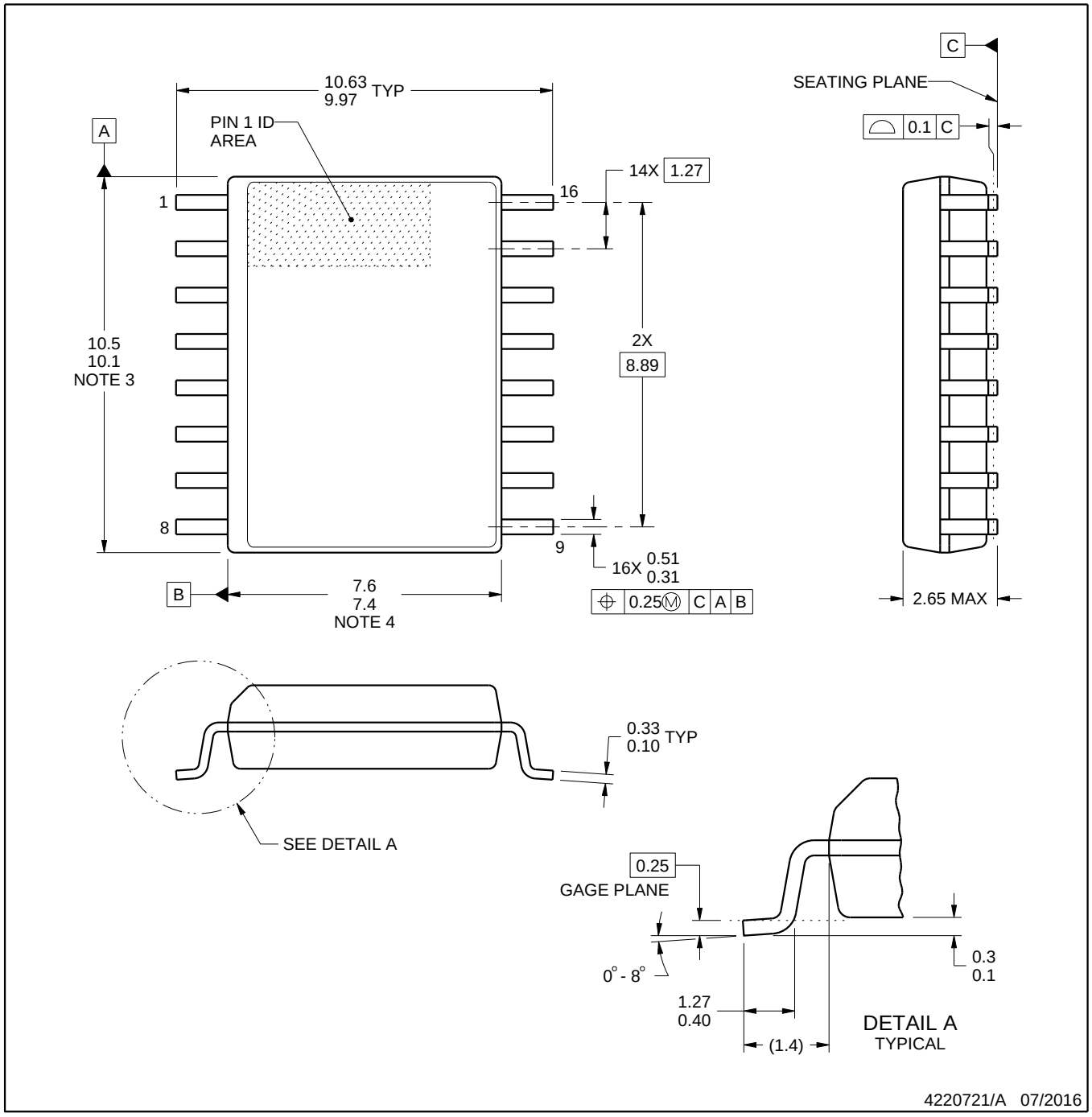


# PACKAGE OUTLINE

## DW0016A

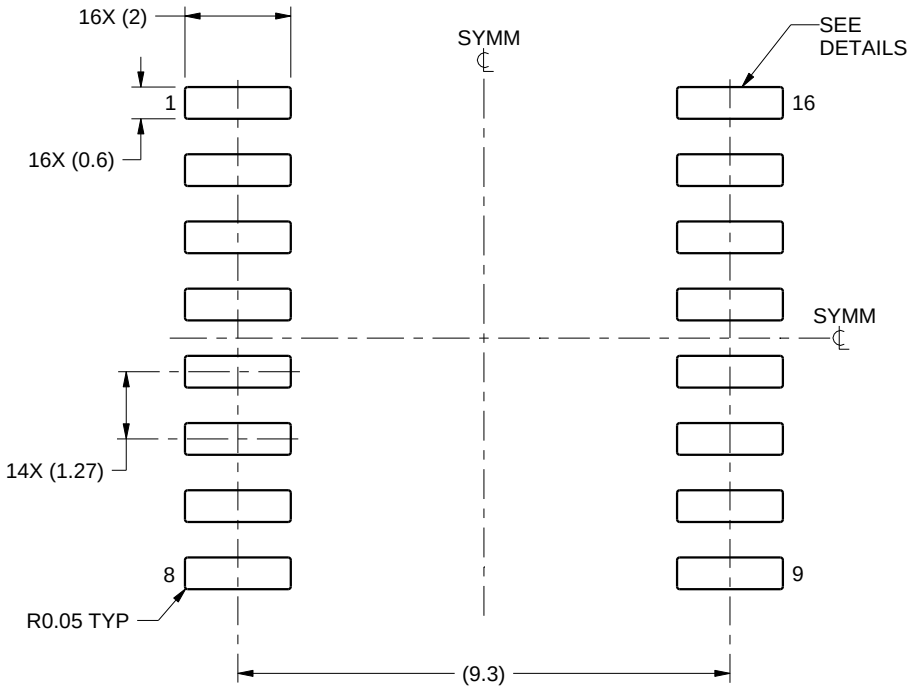
## SOIC - 2.65 mm max height

SOIC

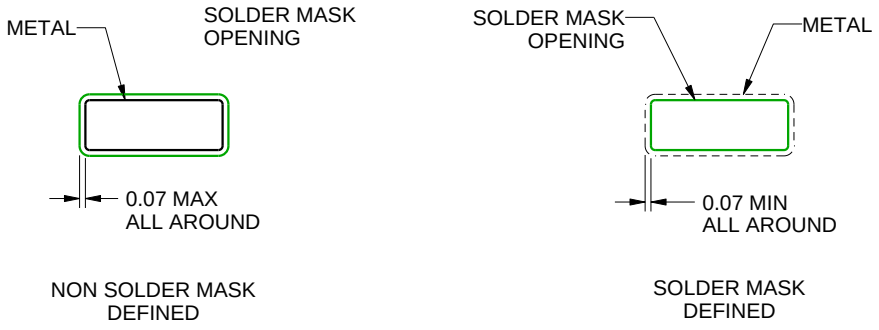



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:7X

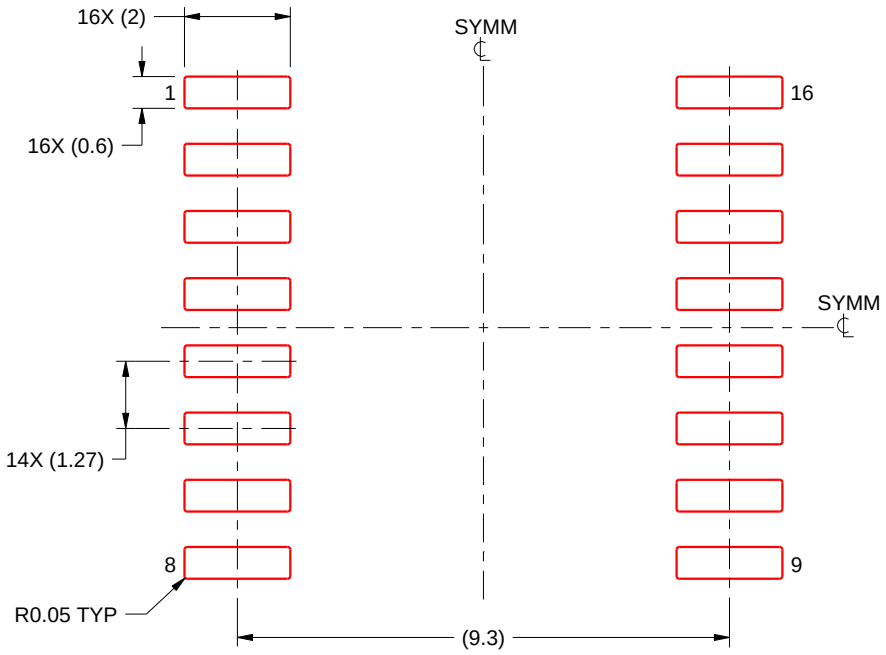



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

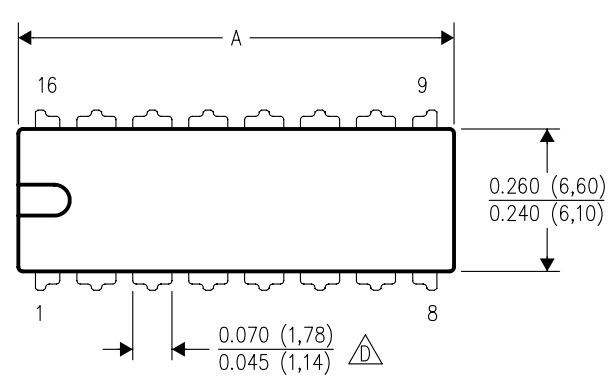
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

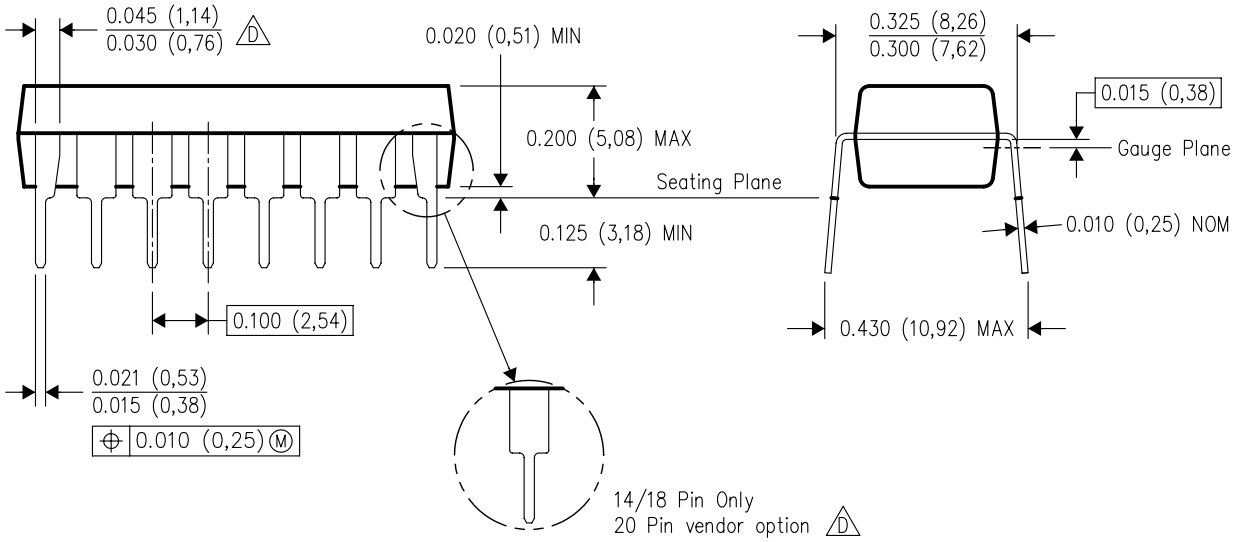
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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