THE DATASHEET OF

HMC861LP3E

HMC861LP3E

v01.0112

13 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1, 3)

Typical Applications

The HMC861LP3E is ideal for:

- Satellite Communication Systems
- Point-to-Point & Point-to-Multi-Point Radios
- Military Applications
- Test Equipment

Features

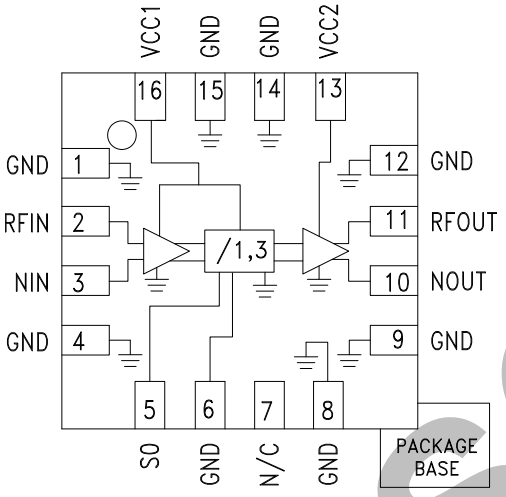
Low Noise Floor: -152 dBc/Hz at 100 kHz offset

Programmable Frequency Divider, N = 1 or 3

Wide Bandwidth 100 MHz to 13 GHz

16 Lead 3X3 mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC861LP3E is a low noise programmable frequency divider in a 3 x 3 mm leadless surface mount package. The divider can be programmed to divide from N = 1,3 in the 100 MHz to 13 GHz input frequency range. The low phase noise and wide frequency range make this device ideal for high performance and wide band communication systems.

Electrical Specifications, T_A = +25 °C, Vcc1 = Vcc2 = +5V

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Input Characteristics					
Max RF Input Frequency	Sine Wave or Square Wave Input	13			GHz
Min RF Input Frequency [1]	Sine Wave or Square Wave Input			0.1	GHz
RF Input Power Range		-10	0	10	dBm
Divider Output Characteristics					
Output Power	(see the Pout plots for each division ratio)		2		dBm
Divider Ratio N		1		3	
SSB Phase Noise @ 100 kHz Offset	Fin = 6 GHz, Pin = 0 dBm, N = 1		-152		dBc/Hz
SSB Phase Noise @ 100 kHz Offset	Fin = 6 GHz, Pin = 0 dBm, N = 3		-153		dBc/Hz
Logic Inputs					
VIH Input High Voltage		3		5	V
VIL Input Low Voltage		0		0.4	V
Power Supplies					
Vcc1, Vcc2	Analog Supply (See pin description table)	4.75	5	5.25	V
Current Consumption					
Icc	N = 1, S0 = L		125		mA
	N = 3, S0 = H		180		mA
Control Bits			1		Bit

[1] Square wave input waveform is recommended below 400 MHz for best phase noise performance. If sine wave input waveform is used below 400 MHz, it is recommended that power input is > +5 dBm for best operation including phase noise performance.

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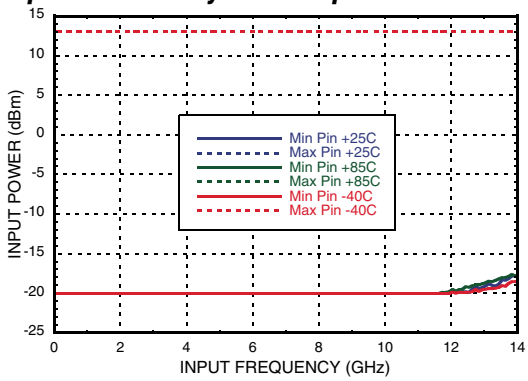
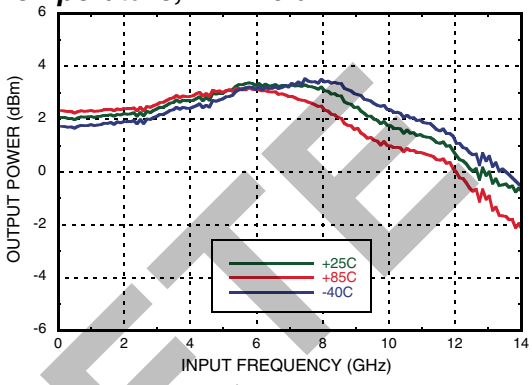
Divide-by-1

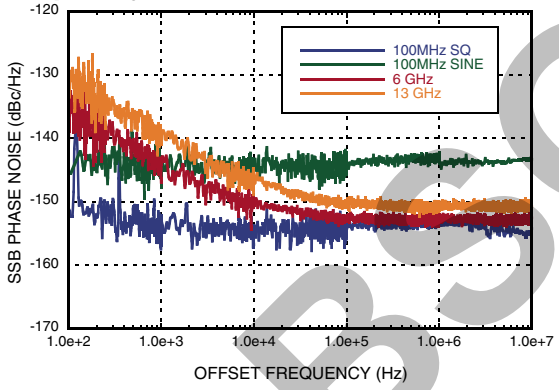
Input Sensitivity vs. Temperature



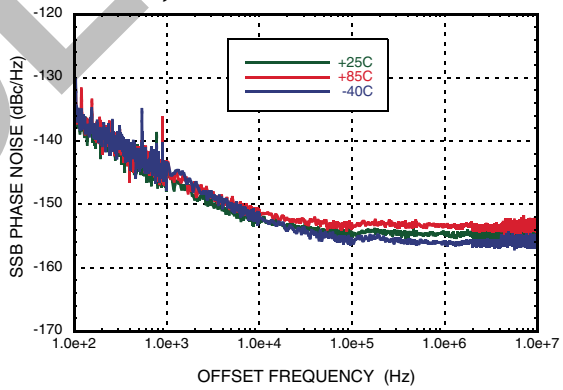
Output Power vs. Temperature, Pin = 0 dBm



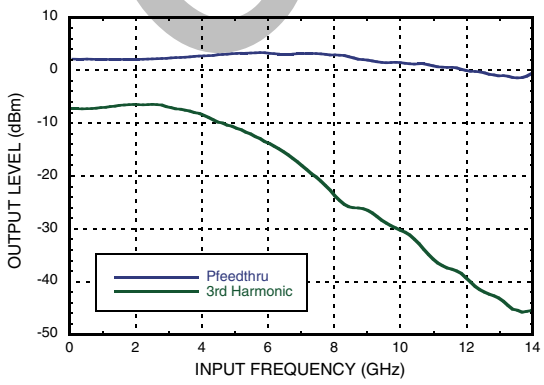
Phase Noise vs. Frequency, Pin = 0 dBm



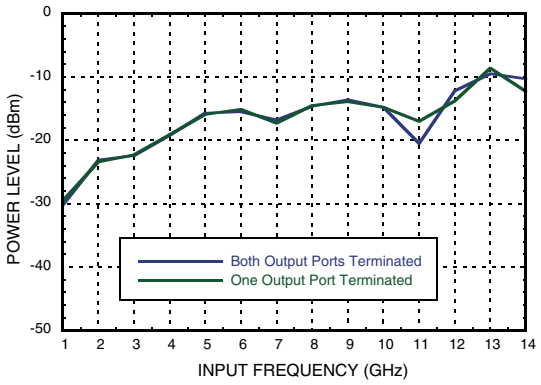
Phase Noise vs. Temperature, Fin = 6 GHz, Pin = 0 dBm



Output Harmonics, Pin = 0 dBm



Reverse Leakage, Pin = 0 dBm



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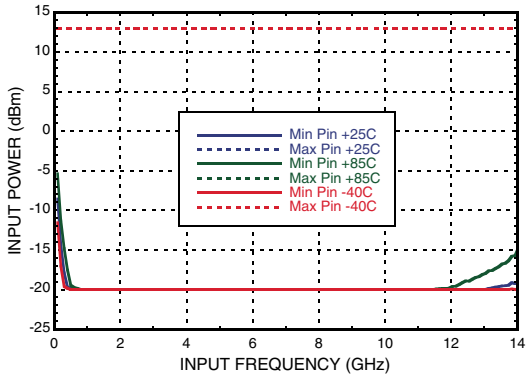
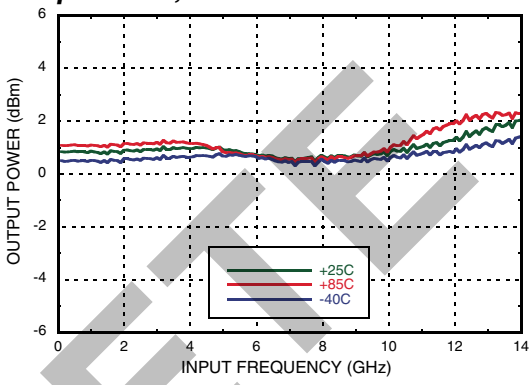
Divide-by-3

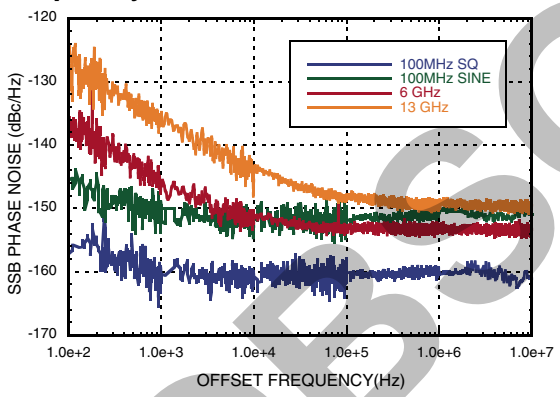
Input Sensitivity vs. Temperature



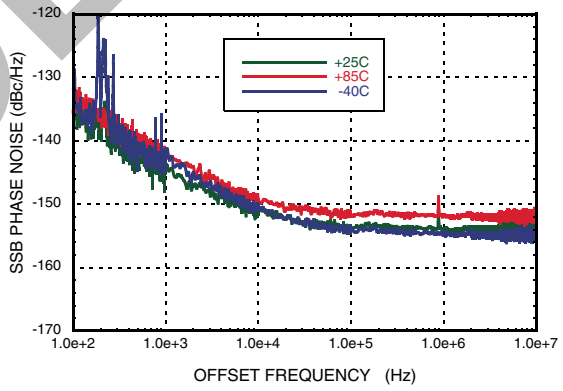
Output Power vs. Temperature, Pin = 0 dBm



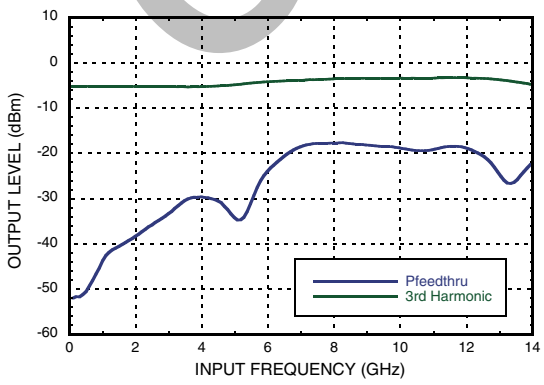
Phase Noise vs. Frequency, Pin = 0 dBm



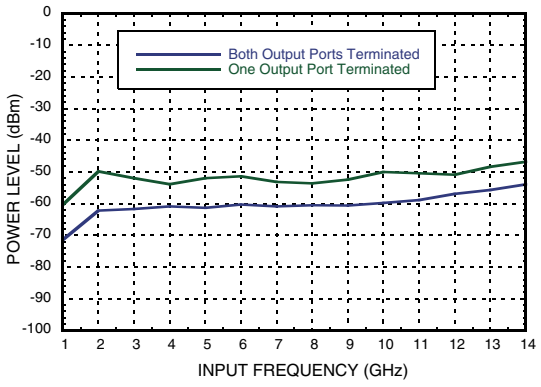
Phase Noise vs. Temperature, Fin = 6 GHz, Pin = 0 dBm



Output Harmonics, Pin = 0 dBm



Reverse Leakage, Pin = 0 dBm



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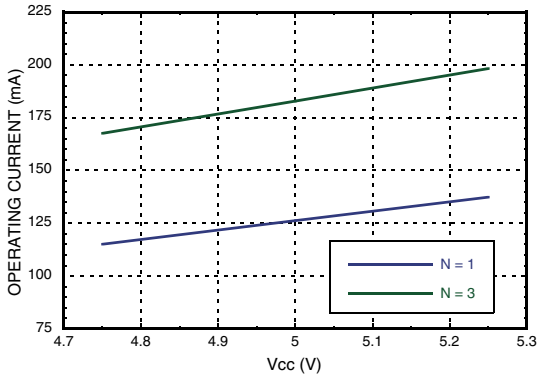
Icc vs. Vcc



Absolute Maximum Ratings

RF Input Power	13 dBm
Supply Voltage (Vcc)	5.5V
Control Inputs (S0)	5.5V
Storage Temperature	-65 to +125 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Reliability Information

Junction Temperature to Maintain 1 Million Hour MTTF	150 °C
Nominal Junction Temperature (T = 85 °C and Pin = 10 dBm))	108 °C
Thermal Resistance (Junction to GND Paddle, 5V Supply)	25 °C/W
Operating Temperature	-40 to +85 °C

Digital Control Input Voltages

State	S0
Low	0 to 0.4V
High	3V to 5V

Programming Truth Table for Frequency Division Ratios

S0	Divider Ratio (N)
0	1
1	3

0 = Logic Low 1 = Logic High
Note: Vcc1, Vcc2 must be applied before logic.

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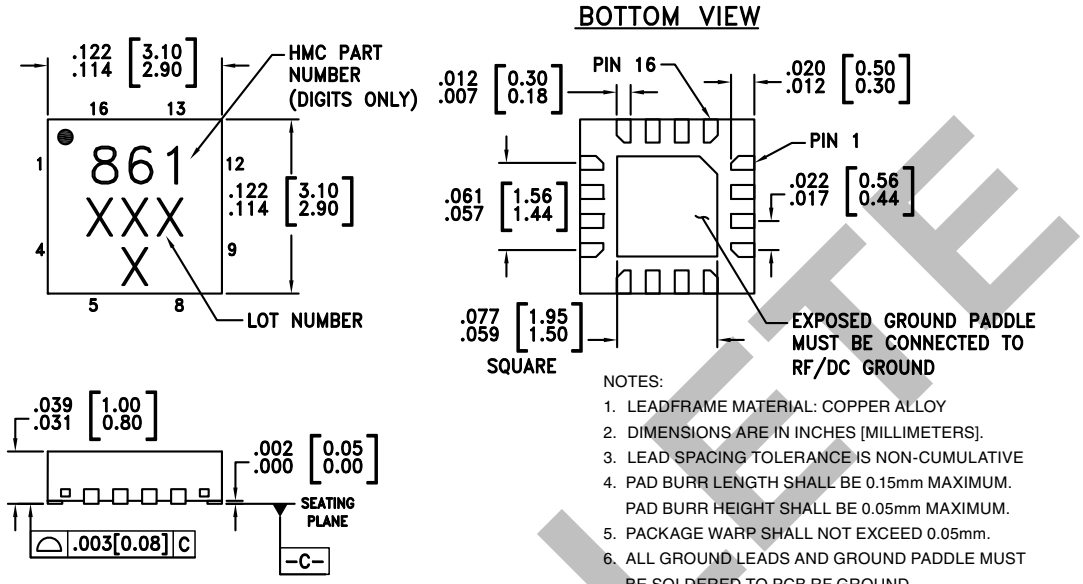
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC861LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	861 XXX X

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

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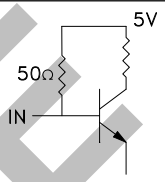
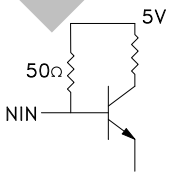
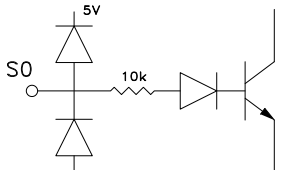
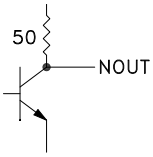
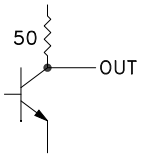
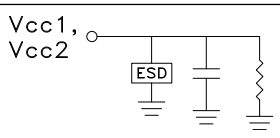
Pin Description

Pin Number	Function	Description	Interface Schematic
1, 4, 8, 9, 12, 14, 15	GND	Ground: Backside of package has exposed metal ground slug which must be connected to RF/DC ground.	
2	IN	RF Input must be DC blocked.	
3	$\overline{\text{NIN}}$	RF Input 180° out of phase with pin 2 for differential operation. AC ground for single ended operation.	
5	S0	CMOS compatible division ratio control bit. See programming truth table.	
6	GND	Internally connected to circuitry, must be connected to RF/DC ground for proper operation.	
7	NC	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
10	$\overline{\text{NOUT}}$	Divider output 180° out of phase with pin 11. RF output must be DC blocked.	
11	OUT	Divided Output. RF output must be DC blocked.	
13, 16	Vcc1, Vcc2	Supply voltage 5V. Connect both pins to +5V supply.	

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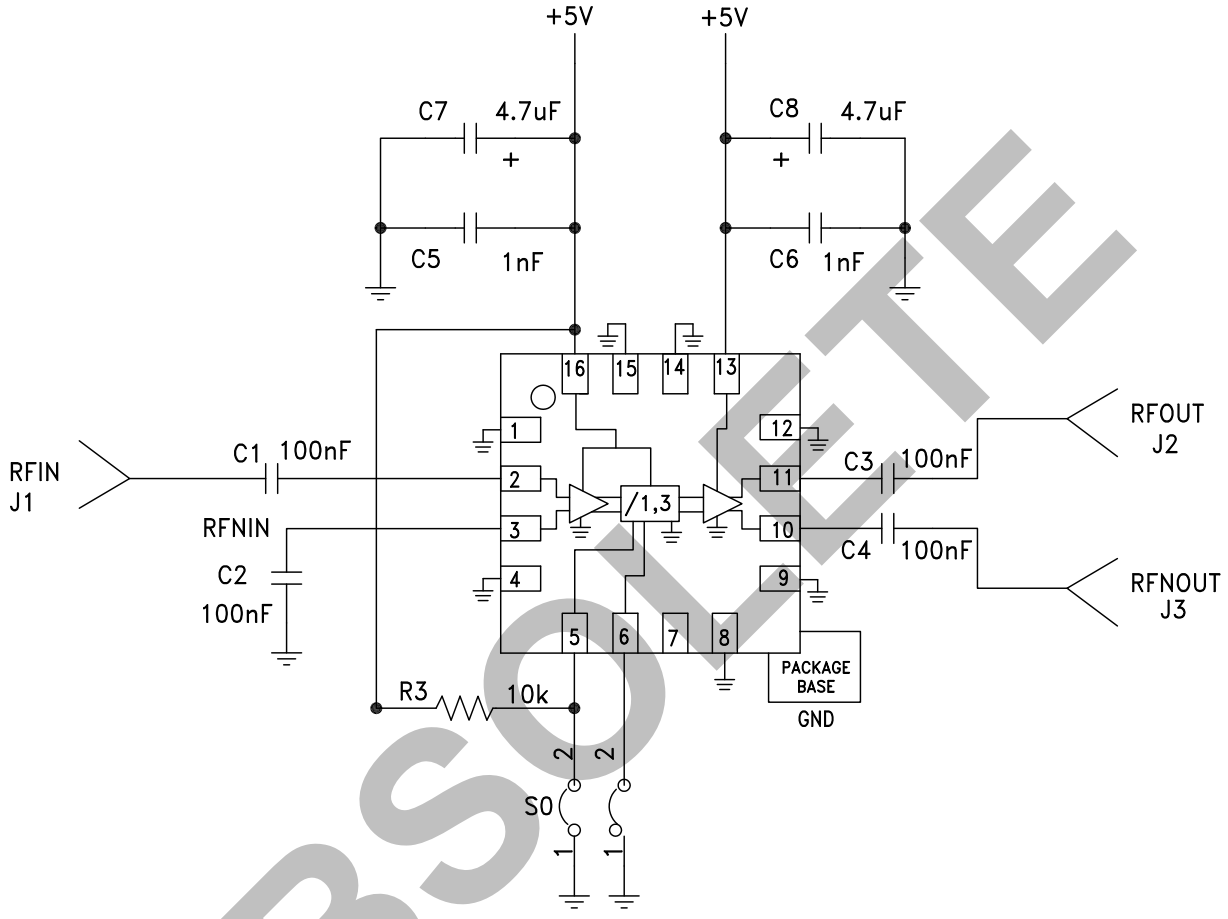
Evaluation PCB Schematic



NOTES:
1. The shorting link from PCB ground to pin 6 must be installed for proper operation.
2. Capacitors C1, C2, C3, and C4 are broadband multilayer capacitors, American Technical Ceramics part number ATC530L. The 100 nF capacitance value is per ATC datasheet.

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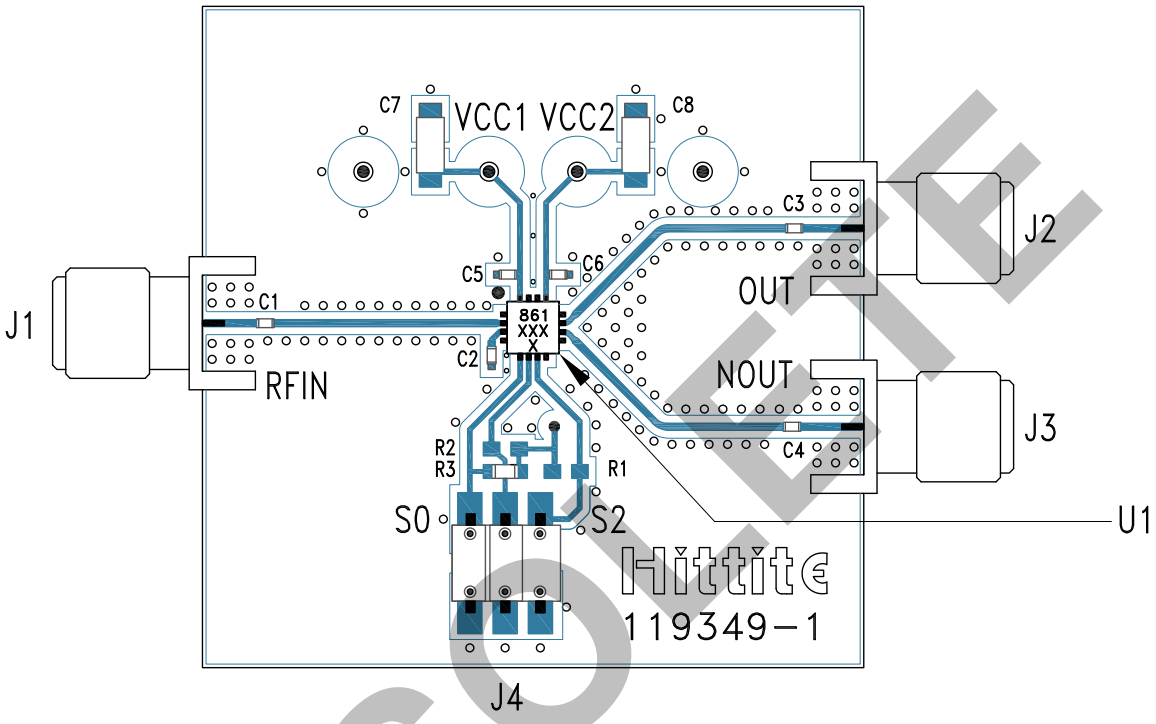
Evaluation PCB



List of Materials for Evaluation PCB Eval01-HMC861LP3E [1]

Item	Description
J1 - J3	Connector, SMA, Female
J4	DC Connector Header, Molex 2mm
C1 - C4	100 nF Capacitor, Broadband, 0402
C5, C6	1000 pF Capacitor, 0402 Pkg.
C7, C8	4.7 uF Capacitor, 1206
R3	10 k Ohm Resistor, 0402
Vcc1, Vcc2	DC Pin, 0.040" Dia.
U1	HMC861LP3E, Programmable Divider
PCB [2]	119349 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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