



# THE DATASHEET OF ADM698AR



## ADM698/ADM699

### FEATURES

- Superior Upgrade for MAX698/MAX699
- Guaranteed  $\overline{\text{RESET}}$  Assertion with  $V_{CC} = 1 \text{ V}$
- Low 0.6 mA Supply Current
- Precision 4.65 V Voltage Monitor
- Power OK/Reset Time Delay
- Watchdog Timer
- Minimum Component Count
- Performance Specified over Temperature

### APPLICATIONS

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical  $\mu\text{P}$  Power Monitoring

### GENERAL DESCRIPTION

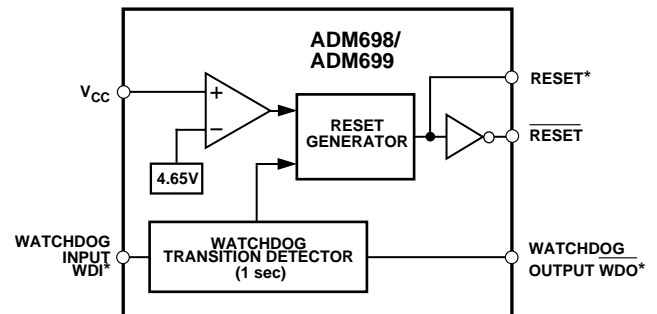
The ADM698/ADM699 supervisory circuits provide power supply monitoring and watchdog timing for microprocessor systems.

The ADM698 monitors the 5 V  $V_{CC}$  power supply and generates a  $\overline{\text{RESET}}$  pulse during power up, power down and during low voltage "Brown Out" conditions. The  $\overline{\text{RESET}}$  output is guaranteed to be functional (logic low) with  $V_{CC}$  as low as 1 V.

The ADM699 features an identical monitoring circuit as in the ADM698 plus an additional watchdog timer input to monitor microprocessor activity. The  $\overline{\text{RESET}}$  output is forced low if the watchdog input is not toggled within the 1 second watchdog timeout period.

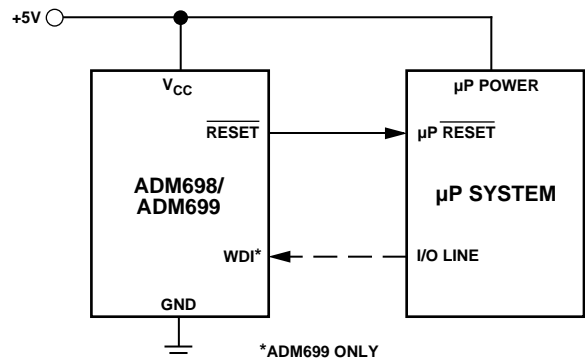
Both parts are available in 8-pin plastic DIP and 16-lead SOIC packages. The 16-lead SOIC contains additional outputs  $\overline{\text{RESET}}$  (without inversion) and Watchdog Output  $\overline{\text{WDO}}$  (ADM699 only).

### FUNCTIONAL BLOCK DIAGRAM



\*WDI (ADM699 ONLY)  
 $\overline{\text{RESET}}$  (SOIC ONLY)  
 $\overline{\text{WDO}}$  (ADM699 SOIC ONLY)

### TYPICAL APPLICATION CIRCUIT



\*ADM699 ONLY

### REV. 0

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# ADM698/ADM699—SPECIFICATIONS (V<sub>CC</sub> = +5 V ± 10%, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub> unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V <sub>CC</sub> Operating Voltage Range	3.0		5.5	V	
Supply Current		0.6	1.95	mA	
Power-Down Reset Assertion	4.5	4.65	4.73	V	
Power-Up Reset Deassertion			4.73	V	
Reset Threshold Hysteresis		40		mV	
Reset Active Time	140	200	280	ms	T <sub>A</sub> = +25°C, V <sub>CC</sub> = +5 V
Watchdog Timeout Period (ADM699)	1.0	1.6	2.25	s	T <sub>A</sub> = +25°C, V <sub>CC</sub> = +5 V
Minimum WDI Input Pulse Width	50			ns	V <sub>IL</sub> = 0.4, V <sub>IH</sub> = 3.5 V
$\overline{\text{RESET}}$ Output Voltage			0.4	V	I <sub>SINK</sub> = 1.6 mA, V <sub>CC</sub> = 4.4 V
$\overline{\text{RESET}}$ Output Voltage (V <sub>CC</sub> = 1 V)		4	200	mV	I <sub>SINK</sub> = 10 μA, V <sub>CC</sub> = 1.0 V
RESET and $\overline{\text{WDO}}$ Output Voltage	3.5		0.4	V	I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 5 V
	3.5			V	I <sub>SINK</sub> = 1.6 mA, V <sub>CC</sub> = 5 V
$\overline{\text{RESET}}$ Output Short Circuit Current		25		mA	I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 4.4 V Output Sink Current
WDI Input Threshold (ADM699)					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	μA	WDI = V <sub>CC</sub> , T <sub>A</sub> = +25°C
	-50	-20		μA	WDI = 0 V, T <sub>A</sub> = +25°C

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>CC</sub> . . . . .	-0.3 V to +6 V
All Other Inputs . . . . .	-0.3 V to V <sub>CC</sub> + 0.3 V
Power Dissipation 8-Pin DIP . . . . .	500 mW
θ <sub>JA</sub> , Thermal Impedance . . . . .	+120°C/W
Power Dissipation 16-Pin SOIC . . . . .	375 mW
θ <sub>JA</sub> , Thermal Impedance . . . . .	+110°C/W
Power Dissipation 8-Pin Cerdip . . . . .	500 mW
θ <sub>JA</sub> , Thermal Impedance . . . . .	+125°C/W
Operating Temperature Range	
Industrial (A Version) . . . . .	-40°C to +85°C
Extended (S Version) . . . . .	-55°C to +125°C
Storage Temperature Range . . . . .	-65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . .	+300°C
Vapor Phase (60 secs) . . . . .	+215°C
Infrared (15 secs) . . . . .	+220°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM698/ADM699 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## ORDERING GUIDE

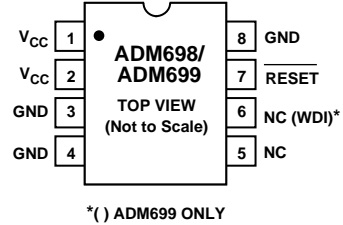
Model	Temperature Range	Package Option
ADM698AN	-40°C to +85°C	N-8
ADM698AR	-40°C to +85°C	R-16
ADM698AQ	-40°C to +85°C	Q-8
ADM698SQ	-55°C to +125°C	Q-8
ADM699AN	-40°C to +85°C	N-8
ADM699AR	-40°C to +85°C	R-16
ADM699AQ	-40°C to +85°C	Q-8
ADM699SQ	-55°C to +125°C	Q-8



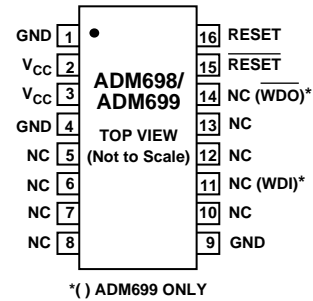
## PIN FUNCTION DESCRIPTION

Mnemonic	Function
$V_{CC}$	+5 V Power Supply Input.
GND	0 V. Ground reference for all signals.
$\overline{RESET}$	Logic Output. $\overline{RESET}$ goes low whenever $V_{CC}$ falls below the reset voltage threshold (4.65 V typ). $\overline{RESET}$ remains low for a minimum of 140 ms after $V_{CC}$ returns to 5 V. $\overline{RESET}$ also goes low for a minimum of 140 ms if the watchdog timer is enabled but not serviced within its time-out period.
WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is driven to midsupply.
RESET	(SOIC packages only) Logic Output. RESET is an active high output. It is the inverse of $\overline{RESET}$ .
$\overline{WDO}$	(SOIC ADM699 only) Logic Output. The Watchdog Output, $\overline{WDO}$ , goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, the watchdog timer is disabled and $\overline{WDO}$ remains high.

### PIN CONFIGURATION (DIP)



### PIN CONFIGURATION (SOIC)



## TYPICAL PERFORMANCE CURVES

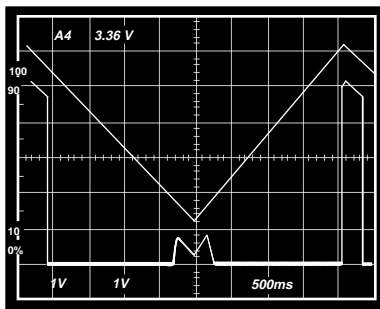


Figure 1. RESET Output Voltage vs.  $V_{CC}$

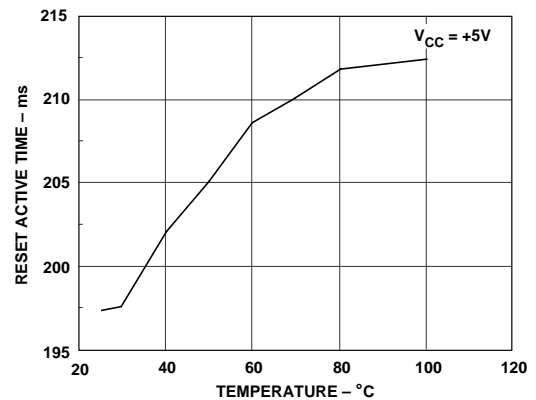


Figure 2. RESET Active Time vs. Temperature

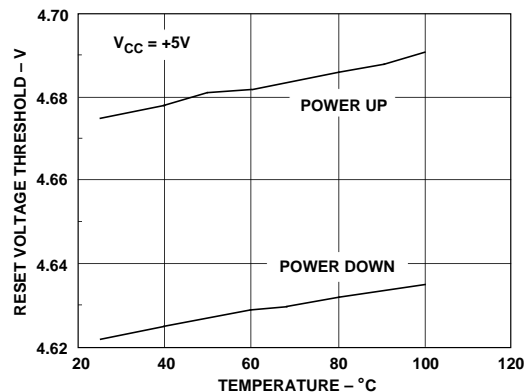


Figure 3. RESET Voltage Threshold vs. Temperature

# ADM698/ADM699

## CIRCUIT INFORMATION

### Power Fail RESET

A precision voltage detector monitors  $V_{CC}$  and generates a  $\overline{\text{RESET}}$  output to hold the microprocessor's Reset line low when  $V_{CC}$  falls below the reset threshold (4.65 V) (see Figure 4). The reset voltage threshold is set to accommodate a 5% variation on  $V_{CC}$ . The voltage detector has 40 mV hysteresis to ensure that glitches on  $V_{CC}$  do not activate the  $\overline{\text{RESET}}$  output.

On power up, an internal monostable holds  $\overline{\text{RESET}}$  low for 140 ms after  $V_{CC}$  rises above the reset threshold. This allows the power supply to stabilize on power up and also prevents repeated toggling of  $\overline{\text{RESET}}$  even if the 5 V power drops out and recovers with each power line cycle. In order to prevent mistripping due to transient voltage spikes, it is recommended that a 0.1  $\mu\text{F}$  capacitor be connected at the  $V_{CC}$  pin.

The  $\overline{\text{RESET}}$  output is guaranteed to remain low with  $V_{CC}$  as low as 1 V. This holds the microprocessor in a stable shutdown condition as the power supply comes up.

On the 16-lead SOIC package, an active high RESET output is also provided. This is the complement of  $\overline{\text{RESET}}$  and is intended for microprocessors requiring an active high signal.

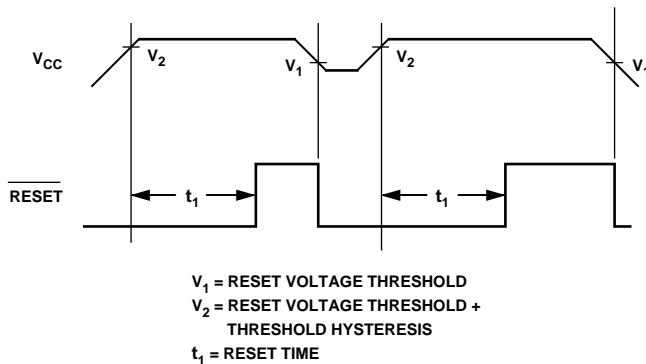


Figure 4. Watchdog Timeout Period vs. Temperature

### Watchdog Timer (ADM699 Only)

The watchdog timer input (WDI) monitors an I/O line from the  $\mu\text{P}$  system. The  $\mu\text{P}$  must toggle this input once every 1.6 seconds to verify correct software execution. Failure to toggle the line indicates that the  $\mu\text{P}$  system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the processor.

The WDI input is a three level input and will recognize a low-to-high or a high-to-low transition on its input. The watchdog timer is reset by each WDI transition and then begins its timeout period. If the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. If the watchdog timer is not needed, the WDI input should be left floating.

The Watchdog Output ( $\overline{\text{WDO}}$ ) (SOIC package Only) provides watchdog status information. It is driven low if WDI is not toggled within the watchdog timeout period. It goes high at the next WDI transition. It is also set high when  $V_{CC}$  falls below the reset threshold.

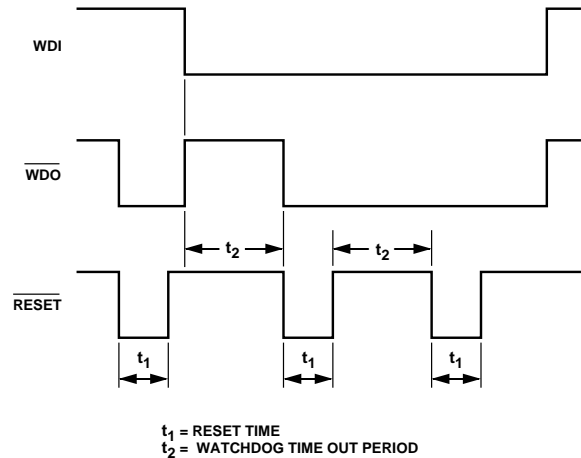
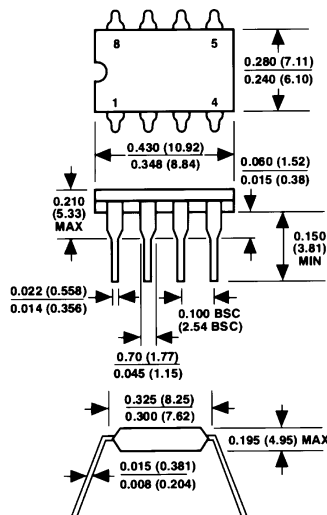


Figure 5. Watchdog Timeout Period and Reset Active Time

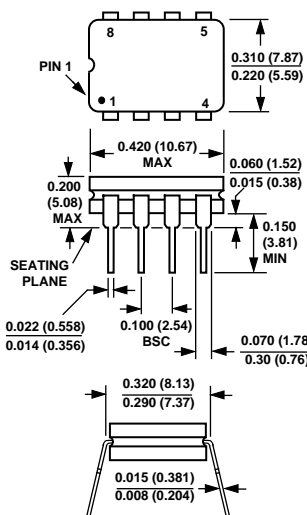
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

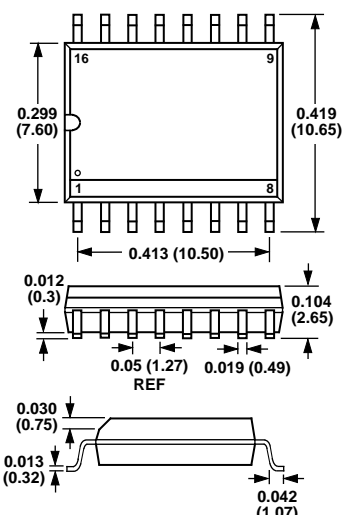
### 8-Pin Plastic DIP (N-8)



### 8-Pin Cerdip (Q-8)



### 16-Lead SOIC (R-16)



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