



**THE DATASHEET OF  
MC100ELT25DTG**



# MC10ELT25, MC100ELT25

## -5 V Differential ECL to TTL Translator

### Description

The MC10ELT/100ELT25 is a differential ECL to TTL translator. Because ECL levels are used, a +5 V, -5.2 V (or -4.5 V) and ground are required. The small outline 8-lead package and the single gate of the ELT25 makes it ideal for those applications where space, performance and low power are at a premium.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The 100 Series contains temperature compensation.

### Features

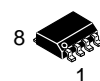
- 2.6 ns Typical Propagation Delay
- 100 MHz  $F_{MAX}$  CLK
- 24 mA TTL Outputs
- Flow Through Pinouts
- Operating Range:  $V_{CC} = 4.5$  V to 5.5 V with  $GND = 0$  V;  
 $V_{EE} = -4.2$  V to -5.7 V with  $GND = 0$  V
- Internal Input 50 K $\Omega$  Pulldown Resistors
- Q Output will default HIGH with inputs open or < 1.3 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



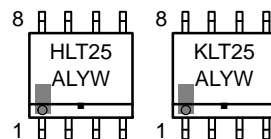
ON Semiconductor®

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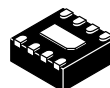
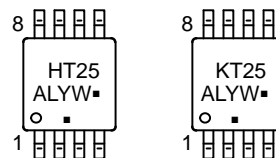
### MARKING DIAGRAMS\*



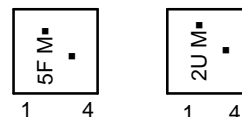
SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948R



DFN8  
MN SUFFIX  
CASE 506AA



H = MC10	A = Assembly Location
K = MC100	L = Wafer Lot
5F = MC10	Y = Year
2U = MC100	W = Work Week
M = Date Code	▪ = Pb-Free Package

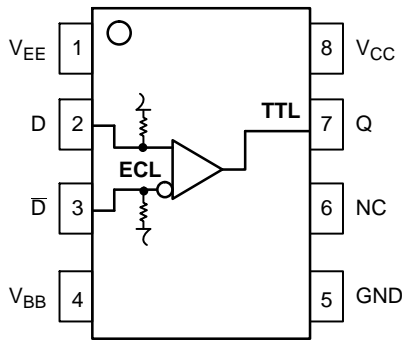
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC10ELT25, MC100ELT25



**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

Pin	Function
D, $\bar{D}$	ECL Differential Inputs
Q	TTL Output
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

**Table 2. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model
	> 1 kV > 400 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
	SOIC-8 TSSOP-8 DFN8
	Level 1 Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	38 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	GND = 0 V	$V_{EE} = -5.0$ V	7	V
$V_{EE}$	Negative Power Supply	GND = 0 V	$V_{CC} = +5.0$ V	-8	V
$V_{IN}$	Input Voltage	GND = 0 V		0 to $V_{EE}$	V
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}$ C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	$^{\circ}$ C/W $^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	$^{\circ}$ C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	$^{\circ}$ C/W $^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 $\pm 5\%$	$^{\circ}$ C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	$^{\circ}$ C/W $^{\circ}$ C/W
$T_{sol}$	Wave Solder	Pb-Free	<2 to 3 sec @ 260 $^{\circ}$ C	265	$^{\circ}$ C
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	$^{\circ}$ C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

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**Table 4. 10ELT SERIES NECL INPUT DC CHARACTERISTICS**  $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$ ;  $GND = 0\text{ V}$  (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 4)	-1230		-890	-1130		-810	-1060		-720	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) (Note 4)	-1950		-1500	-1950		-1480	-1950		-1445	mV
$V_{BB}$	Output Voltage Reference	-1.43		-1.30	-1.35		-1.25	-1.31		-1.19	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Notes 4 and 5)	-2.8		0.0	-2.8		0.0	-2.8		0.0	V
$I_{IH}$	Input HIGH Current			255			175			175	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.3			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

3. Input parameters vary 1:1 with GND.  $V_{EE}$  can vary +0.06 V to -0.5 V.

4. TTL output  $R_L = 500\ \Omega$  to GND

5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with GND.

**Table 5. 100ELT SERIES NECL INPUT DC CHARACTERISTICS**  $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$ ;  $GND = 0\text{ V}$  (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 7)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) (Note 7)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Notes 7 and 8)	-2.8		0.0	-2.8		0.0	-2.8		0.0	V
$I_{IH}$	Input HIGH Current			255			175			175	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Input parameters vary 1:1 with GND.  $V_{EE}$  can vary +0.8 V to -0.5 V.

7. TTL output  $R_L = 500\ \Omega$  to GND

8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with GND.

**Table 6. TTL OUTPUT DC CHARACTERISTICS**  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24\text{ mA}$			0.5	V
$I_{CCH}$	Power Supply Current			11	16	mA
$I_{CCL}$	Power Supply Current			13	18	mA
$I_{EE}$	Negative Power Supply Current			15	21	mA
$I_{OS}$	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

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**Table 7. AC CHARACTERISTICS**  $V_{CC}= 5.0\text{ V}$ ;  $V_{EE}= -5.0\text{ V}$ ;  $GND= 0\text{ V}$  (Note 9 and Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency					100					MHz
$t_{PLH}$	Propagation Delay @ 1.5 V	1.7		3.6	1.7		3.6	1.7		3.6	ns
$t_{PHL}$	Propagation Delay @ 1.5 V	2.6		4.1	2.6		4.1	2.6		4.1	ns
$t_{JITTER}$	Random Clock Jitter (RMS)					35					ps
$t_r$ $t_f$	Output Rise/Fall Times QTTL 10% – 90%					1.9 2.3					ns
$V_{PP}$	Input Swing (Note 11)	200		1000	200		1000	200		1000	mV

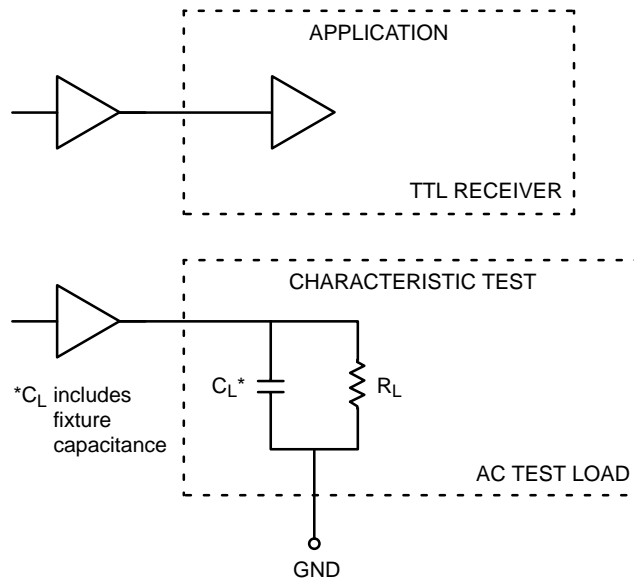
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

9.  $V_{CC}$  can vary  $\pm 0.25\text{ V}$ .

$V_{EE}$  can vary  $+0.06\text{ V}$  to  $-0.5\text{ V}$  for 10ELT;  $V_{EE}$  can vary  $+0.8\text{ V}$  to  $-0.5\text{ V}$  for 100ELT.

10.  $R_L = 500\ \Omega$  to GND and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 2.

11.  $V_{PP}(\text{min})$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 2. TTL Output Loading Used for Device Evaluation**

## MC10ELT25, MC100ELT25

### ORDERING INFORMATION

Device	Package	Shipping†
MC10ELT25DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC10ELT25DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT25DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10ELT25DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT25MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel
MC100ELT25DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100ELT25DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT25DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT25DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT25MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

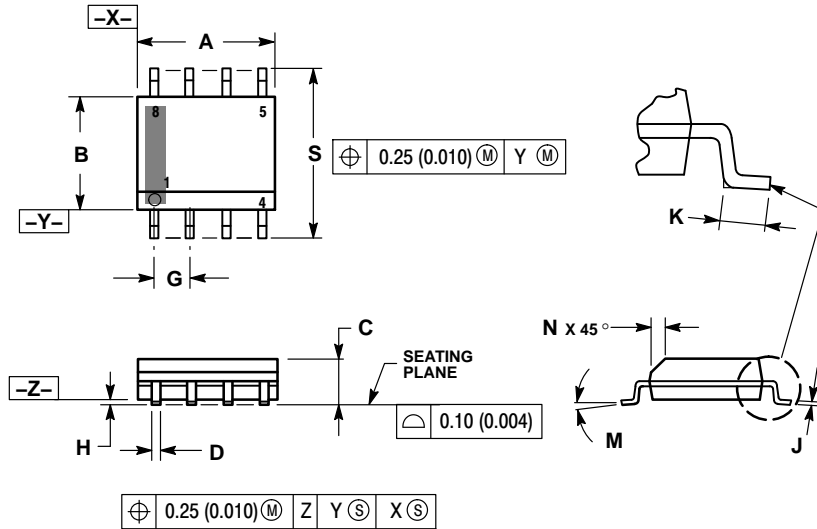
#### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10ELT25, MC100ELT25

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AK

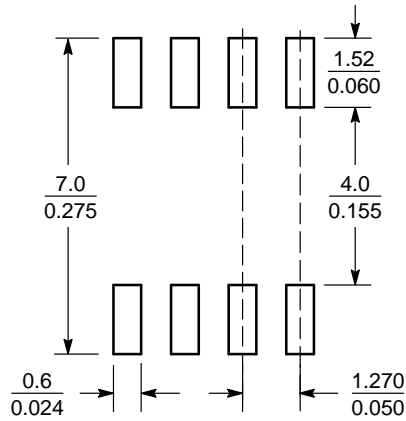


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



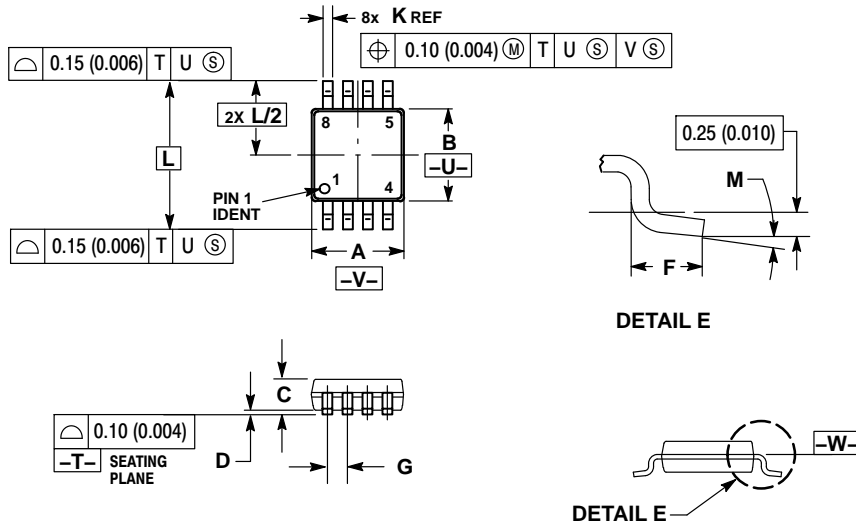
SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC10ELT25, MC100ELT25

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
CASE 948R-02  
ISSUE A



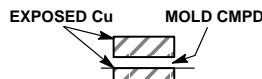
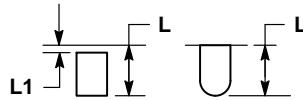
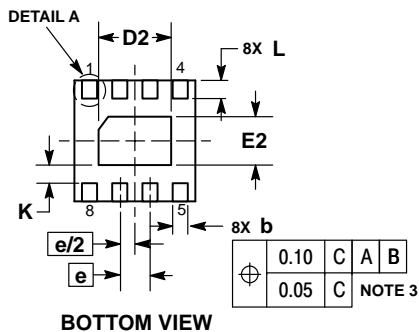
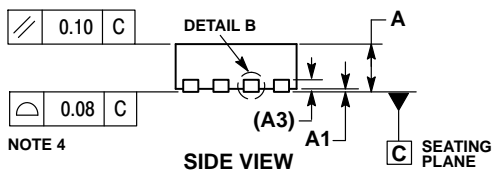
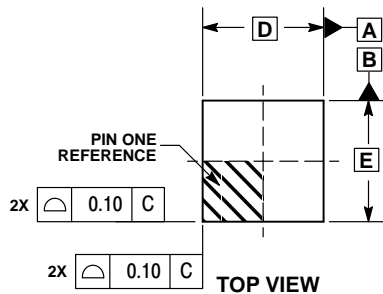
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

# MC10ELT25, MC100ELT25

## PACKAGE DIMENSIONS

DFN8 2x2, 0.5P  
CASE 506AA  
ISSUE E

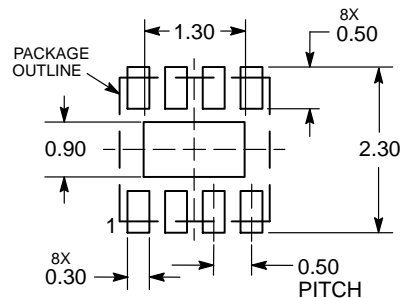


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management