THE DATASHEET OF

ONET1151LRGER

www.win-source.net 0086-755-83957316

11.3 Gbps Low-Power Laser Diode Driver

Check for Samples: ONET1151L

FEATURES

- **Digitally Selectable Modulation Current up to 85 mApp (10-Ω Load)**
- **Digitally Selectable Bias Current up to 100-mA Source or Sink**
- **2-Wire Digital Interface With Integrated Digital-to-Analog Converters (DACs) and Analog-to-Digital Converter (ADC) for Control and Diagnostic Management**
- **Automatic Power Control (APC) Loop**
- **Adjustable Output Resistance and De-Emphasis**
- **Programmable Input Equalizer**
- **Cross-Point Control**
- **Selectable Monitor PD Current Range and Polarity**
- **Includes Laser Safety Features**
- **Single +3.3-V Supply**
- **Temperature –40°C to 100°C**
- **Surface Mount 4-mm × 4-mm, 24-Pin RoHS-Compliant QFN Package**
- **Pin-Compatible to the ONET1101L Device**

APPLICATIONS

- **10-Gigabit Ethernet Optical Transmitters**
- **8× and 10× Fibre Channel Optical Transmitters**
- **SONET OC-192 and SDH STM-64 Optical Transmitters**
- **6-G and 10-G CPRI and OBSAI**
- **SFP+ and XFP Transceiver Modules**

DESCRIPTION

The ONET1151L device is a 3.3-V laser driver designed to directly modulate a laser at data rates from 1 to 11.3 Gbps.

The device provides a 2-wire serial interface, which allows digital control of the modulation and bias currents, eliminating the need for external components. Output waveform control, in the form of cross-point adjustment, de-emphasis, and output termination resistance are available to improve the optical eye mask margin. An optional input equalizer can be used for equalization of up to 150 mm (6 in.) of microstrip or stripline transmission line on FR4-printed circuit boards. The device contains internal ADC and DACs to eliminate the need for special purpose microcontrollers.

The ONET1151L device includes an integrated automatic power control (APC) loop, which compensates for variations in laser average power over voltage and temperature and circuitry to support laser safety and transceiver management systems.

The laser driver is characterized for operation from –40°C ambient to +100°C temperatures and is available in a small footprint 4-mm × 4-mm, 24-pin, RoHS-compliant QFN package that is pin-compatible to the ONET1101L device.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

24-Pin, RoHS-Compliant, QFN Package, 4 mm x 4 mm
With a Lead Pitch of 0,5 mm
(TOP VIEW)

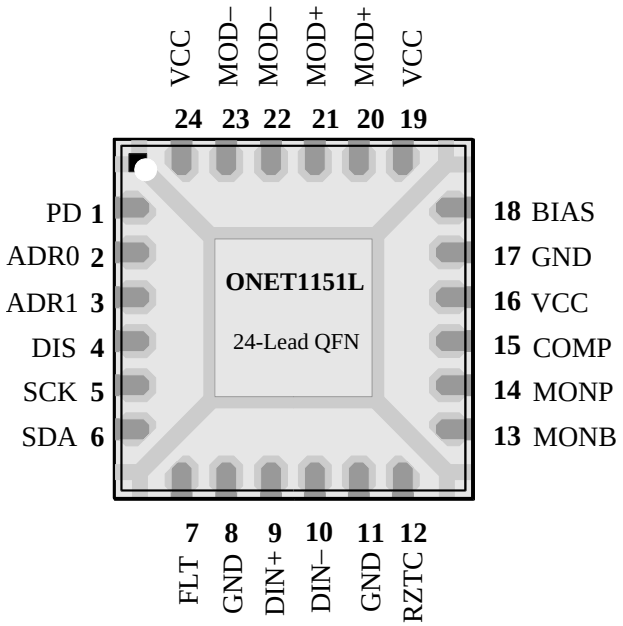

Table 1. PIN DESCRIPTION

PIN		Type	Description
NAME	NO.		
ADR0	2	Digital-in	I^2C address programming pin. Leave this pad open for a default address of 0001000. Pulling the pin to VCC changes the first address bit to 1 (address = 0001001).
ADR1	3	Digital-in	I^2C address programming pin. Leave this pad open for a default address of 0001000. Pulling the pin to VCC changes the second address bit to 1 (address = 0001010).
BIAS	18	Analog	Sinks or sources the bias current for the laser in both APC and open loop modes
COMP	15	Analog	Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01-µF capacitor to ground.
DIN+	9	Analog-in	Noninverted data input. On-chip differentially 100 Ω terminated to DIN–. Must be AC coupled.
DIN–	10	Analog-in	Inverted data input. On-chip differentially 100 Ω terminated to DIN+. Must be AC coupled.
DIS	4	Digital-in	Disables both bias and modulation currents when set to high state. Includes a 10-kΩ pullup resistor to VCC. Toggle to reset a fault condition.
FLT	7	Digital-out	Fault detection flag. High level indicates that a fault has occurred. Open-drain output. Requires an external 4.7-kΩ to 10-kΩ pullup resistor to VCC for proper operation.
GND	8, 11, 17, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
MOD+	20, 21	CML-out	Noninverted modulation current output. IMOD flows into this pin when input data is high.
MOD–	22, 23	CML-out	Inverted modulation current output. IMOD flows into this pin when input data is low.
MONB	13	Analog-out	Bias current monitor. Sources a 1% replica of the bias current. Connect an external resistor to ground (GND) to use the analog monitor (DMONB = 0). If the voltage at this pin exceeds 1.16 V, a fault is triggered. Typically choose a resistor to give MONB voltage of 0.8 V at the maximum desired bias current. If the digital monitor function is used (DMONB = 1), the resistor must be removed.

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Table 1. PIN DESCRIPTION (continued)

MONP	14	Analog-out	Photodiode current monitor. Sources a 12.5% replica of the photodiode current when PDRNG = 1X, a 25% replica when PDRNG = 01, and a 50% replica when PDRNG = 00. Connect an external resistor (5-kΩ typical) to ground (GND) to use the analog monitor (DMONP = 0). If the voltage at this pin exceeds 1.16 V, a fault is triggered when MONPFLT = 1. If the digital monitor function is used (DMONP = 1), the resistor must be removed.
PD	1	Analog	Photodiode input. Pin can source or sink current dependent on register setting.
RZTC	12	Analog	Connect external zero TC 28.7-kΩ resistor to ground (GND). Used to generate a defined zero TC reference current for internal DACs.
SCK	5	Digital-in	2-wire interface serial clock input. Includes a 10-kΩ or 40-kΩ pullup resistor to VCC.
SDA	6	Digital-in	2-wire interface serial data input. Includes a 10-kΩ or 40-kΩ pullup resistor to VCC.
VCC	16, 19, 24	Supply	3.3-V, –15% to +10% supply voltage

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BLOCK DIAGRAM

Figure 1 shows a simplified block diagram of the ONET1151L device. The laser driver consists of:

- Equalizer
- Limiter
- Output driver
- DC offset cancellation with cross-point control
- Power-on reset circuitry
- 2-wire serial interface including:
  - Control logic block
  - Modulation current generator
- Bias current generator
- Automatic power control loop
- Analog reference block

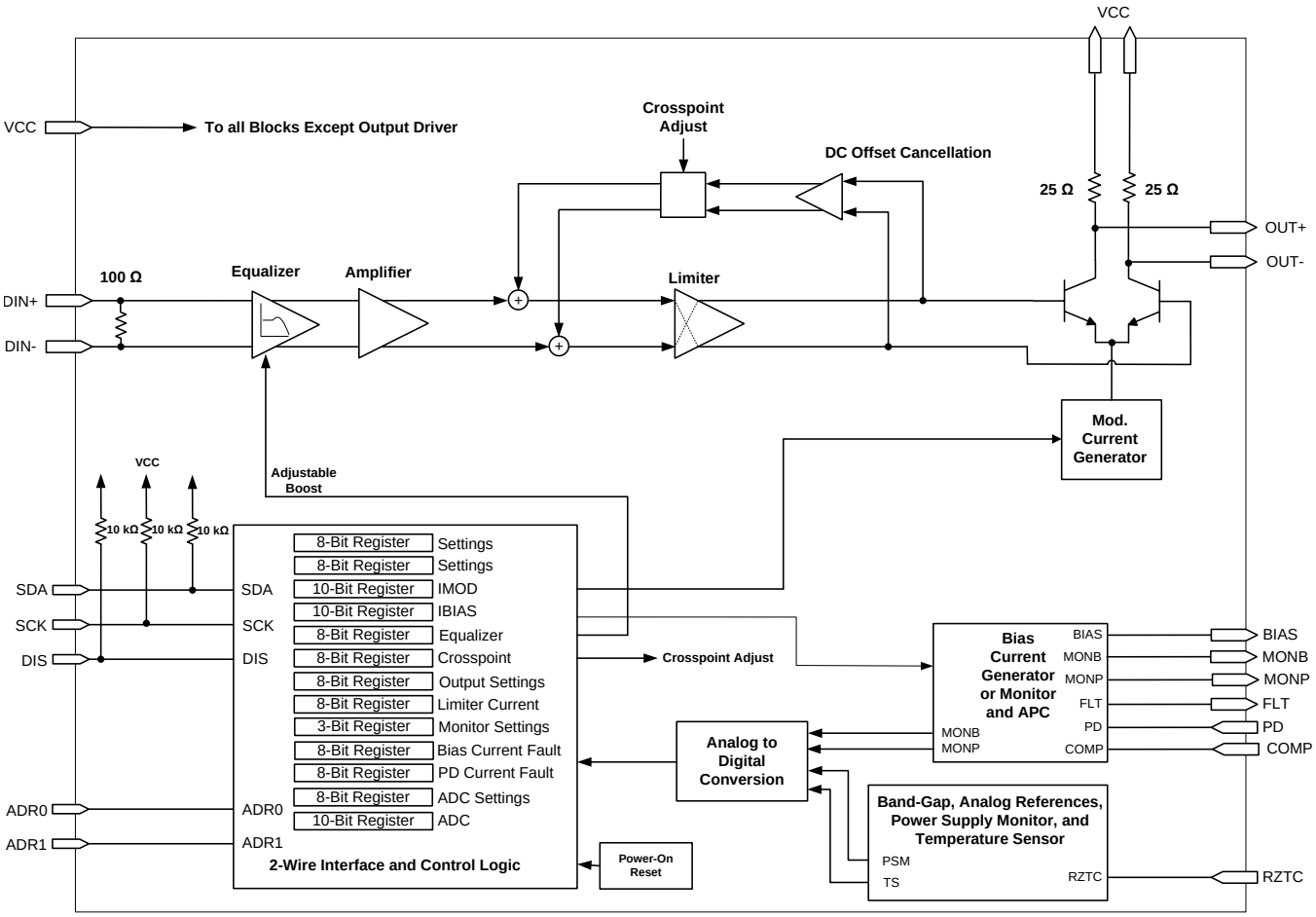

Figure 1. Simplified Block Diagram of the ONET1151L

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ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	Supply voltage[2]	–0.3	4.0	V
V_{ADR0}, V_{ADR1}, V_{DIS}, V_{RZTC}, V_{SCK}, V_{SDA}, V_{DIN+}, V_{DIN-}, V_{FLT}, V_{MONB}, V_{MONP}, V_{COMP}, V_{PD}, V_{BIAS}, V_{MOD+}, V_{MOD-}	Voltage at ADR0, ADR1, DIS, RZTC, SCK, SDA, DIN+, DIN–, FLT, MONB, MONP, COMP, PD, BIAS, MOD+, MOD–[2]	–0.3	4.0	
I_{DIN-}, I_{DIN+}	Max current at input pins		25	mA
I_{MOD+}, I_{MOD-}	Max current at output pins		120	
ESD	ESD rating at all pins		2	kV (HBM)
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range	–65	150	
T_C	Case temperature	–40	110	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.8	3.3	3.63	V
V_{IH}	Digital input high voltage	DIS, SCK, SDA, ADR0, ADR1	2			
V_{IL}	Digital input low voltage	DIS, SCK, SDA			0.8	
	Photodiode current range	Control bit PDRNG = 1X, step size = 3 µA		3 080		µA
		Control bit PDRNG = 01, step size = 1.5 µA		1 540		
		Control bit PDRNG = 00, step size = 0.75 µA		770		
R_{RZTC}	Zero TC resistor value[1]	1.16-V band-gap bias across resistor, E96, 1% accuracy	28.4	28.7	29	kΩ
v_{IN}	Differential input voltage swing		150		1200	mV_{p-p}
T_C	Temperature at the thermal pad		–40		100	°C

(1) Changing the value will alter the DAC ranges.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, with a 25-Ω single-ended output load, open-loop operation, I_{MOD} = 30 mA, I_{BIAS} = 30 mA, and R_{RZTC} = 28.7 kΩ, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.8	3.3	3.63	V
I_{VCC}	Supply current	I_{MOD} = 30 mA, I_{BIAS} = 30 mA, including I_{MOD} and I_{BIAS}, EQENA = 0		120	135	mA
		I_{MOD} = 30 mA, I_{BIAS} = 30 mA, including I_{MOD} and I_{BIAS}, EQENA = 1		123	140	
		Output off (DIS = HIGH), I_{MOD} = 30 mA, I_{BIAS} = 30 mA		44		
R_{IN}	Data input resistance	Differential between DIN+ and DIN–	80	100	120	Ω
R_{OUT}	Output resistance	Single-ended to VCC; ORADJ0 = ORADJ1 = 0	20	25	30	Ω
	Digital input current	SCK, SDA, pullup to VCC		360	470	µA
	Digital input current	DIS, pullup to VCC		360	470	µA
V_{OH}	Digital output high voltage	FLT, pullup to V_{CC}, I_{SOURCE} = 50 µA	2.3			V
V_{OL}	Digital output low voltage	FLT, pullup to V_{CC}, I_{SINK} = 350 µA			0.4	V
$I_{BIAS-MIN}$	Minimum bias current	See (1)			5	mA
$I_{BIAS-MAX}$	Maximum bias current	Sink or source. DAC set to maximum, open and closed loop	88	100		mA
$I_{BIAS-DIS}$	Bias current during disable				100	µA
	Average power stability	APC active		±0.5		dB
	Bias pin compliance voltage	BIASPOL = 0 (sink)	0.8			V
		BIASPOL = 1 (source)			V_{CC} – 0.8	
	Temperature sensor accuracy	With one-point external midscale calibration		±3		°C
V_{PD}	Photodiode reverse bias voltage	APC active, I_{PD} = max	1.3	2.3		V
	Photodiode fault current level	Percent of target I_{PD} (2)		150		%
	Photodiode current monitor ratio	I_{MONP} / I_{PD} with control bit PDRNG = 1X	10	12.5	15	%
		I_{MONP} / I_{PD} with control bit PDRNG = 01	20	25	30	
		I_{MONP} / I_{PD} with control bit PDRNG = 00	40	50	60	
	Monitor diode DMI accuracy	With external midscale calibration PD current > 200 µA, 400 µA, and 800 µA for PDRNG = 00, 01, and 1X, respectively	–10		+10	%
	Bias current monitor ratio	BIASPOL = 0, I_{MONB} / I_{BIAS} (nominal 1 / 100 = 1%)	0.9	1.0	1.1	%
		BIASPOL = 1, I_{MONB} / I_{BIAS} (nominal 1 / 70 = 1.43%)	1.25	1.43	1.61	
	Bias current DMI accuracy	Bias current ≥ 20 mA		±10		%
	Power supply monitor accuracy	With external midscale calibration	–2.5		+2.5	%
V_{CC-RST}	V_{CC} reset threshold voltage	V_{CC} voltage level which triggers power-on reset		2.5	2.8	V
$V_{CC-RSTHYS}$	V_{CC} reset threshold voltage hysteresis			100		mV
$V_{MONB-FLT}$	Fault voltage at MONB	Fault occurs if voltage at MONB exceeds value	1.1	1.16	1.24	V
$V_{MONP-FLT}$	Fault voltage at MONP	MONPFLT = 1, Fault occurs if voltage at MONP exceeds value	1.1	1.16	1.24	V

(1) The bias current can be set below the specified minimum according to the corresponding register setting; however, in closed-loop operation, settings below the specified value may trigger a fault.
(2) Assured by simulation over process, supply and temperature variation

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AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions with 25-Ω, single-ended output load, open-loop operation, I_{MOD} = 30 mA, I_{BIAS} = 30 mA, and R_{RZTC} = 28.7 kΩ, unless otherwise noted. Typical operating condition is at V_{CC} = 3.3 V and T_A = +25°C

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
SDD11	Differential input return gain	0.01 GHz < f ≤ 5 GHz		–15		dB
		5 GHz < f < 11.1 GHz		–8		
SCD11	Differential to common mode conversion gain	0.01 GHz < f < 11.1 GHz		–15		dB
SDD22	Differential output return gain	0.01 GHz < f ≤ 5 GHz		–20		dB
		5 GHz < f < 11.1 GHz		–12		
t_{R-OUT}	Output rise time	20% – 80%, t_{R-IN} < 40 ps, 25-Ω load, single-ended		23	35	ps
t_{F-OUT}	Output fall time	20% – 80%, t_{F-IN} < 40 ps, 25-Ω load, single-ended		23	35	ps
$I_{MOD-MIN}$	Minimum modulation current				5	mA
$I_{MOD-MAX}$	Maximum modulation current	AC-coupled outputs, 10-Ω differential load, CPENA = 1	75	85		mA
$I_{MOD-STEP}$	Modulation current step size	10-bit register		86		µA
DJ	Deterministic output jitter	EQENA = 0, PRBS7 + 72 ones + PRBS7 + 72 zeros at 11.3 Gbps, 150 mVpp, 600 mVpp, 1200 mVpp differential-input voltage		5	10	ps_{P-P}
		EQENA = 1, PRBS7 + 72 ones + PRBS7 + 72 zeros at 11.3 Gbps, maximum equalization with 6-in. transmission line at the input, 400 mVpp at input to transmission line		7		
RJ	Random output jitter			0.2	0.6	ps_{RMS}
τ_{APC}	APC time constant	CAPC 0.01 µF, IPD = 100 µA, PD-coupling ratio, CR = 40 (1)		120		µs
	Cross-point control range		30		70	%
T_{OFF}	Transmitter disable time	Rising edge of DIS to I_{BIAS} ≤ 0.1 × $I_{BIAS-NOMINAL}$ (1)		0.05	5	µs
T_{ON}	Disable negate time	Falling edge of DIS to I_{BIAS} ≥ 0.9 × $I_{BIAS-NOMINAL}$ (1)			1	ms
T_{INIT1}	Power-on to initialize	Power-on to registers ready to be loaded		1	10	ms
T_{INIT2}	Initialize to transmit	Register load STOP command to part ready to transmit valid data (1)			2	ms
T_{RESET}	DIS pulse width	Time DIS must held high to reset part (1)	100			ns
T_{FAULT}	Fault assert time	Time from fault condition to FLT high (1)			50	µs

(1) Assured by simulation over process, supply and temperature variation

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DETAILED DESCRIPTION

EQUALIZER

The data signal is applied to an input equalizer by means of the input signal pins DIN+ and DIN–, which provide on-chip differential 100-Ω line-termination. The equalizer is enabled by setting EQENA = 1 (bit 1 of register 0). Equalization of up to 150 mm (6 in.) of microstrip or stripline transmission line on FR4-printed circuit boards is achievable. The amount of equalization is digitally controlled by the 2-wire interface and control logic block and is dependent on the register settings EQADJ[0..7] (of register 6). To turn off and bypass the equalizer, set EQENA = 0; this reduces the supply current. For details about the equalizer settings, see Table 5.

LIMITER

By limiting the output signal of the equalizer to a fixed value, the limiter removes any overshoot after the input equalization and provides the input signal for the output driver. Make adjustments to the limiter bias current and emitter follower current to trade off the rise and fall times and supply current. Adjust the limiter bias current through LIMCSGN (bit 7 of register 9) and LIMC[0..2] (bits 4, 5, and 6 of register 9). Adjust the emitter follower current through EFCSGN (bit 3 of register 9) and EFC[0..2] (bits 0, 1, and 2 of register 9).

HIGH-SPEED OUTPUT DRIVER

The modulation current sinks from the common-emitter node of the limiting-output driver-differential pair by means of a modulation-current generator, which is digitally controlled by the 2-wire serial interface.

The collector nodes of the output stages connect to output pins MOD+ and MOD–. The collectors have internal 25-Ω back termination resistors to VCC. However, the resistance adjusts higher through ORADJ[0..1] (bits 3 and 4 of register 8). Setting ORADJ to 00, results in the lowest-output termination resistance and setting the bits to 11, results in the highest-output resistance. The outputs are optimized to drive a 25-Ω, single-ended load and obtain the maximum modulation current of 85 mA. AC coupling and inductive pullups to VCC are required and CPENA (bit 4 of register 1) should be set to 1.

To improve the eye-mask margin, output de-emphasis is applied by adjusting DE[0..2] (bits 0 to 2 of register 8).

The polarity of the output pins can be inverted by setting the output polarity switch bit, POL (bit 2 of register 0) to 1.

MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described previously. The circuit is digitally controlled by the 2-wire interface block.

A 10-bit-wide control bus, MODC[0..9] (registers 2 and 3), sets the desired modulation current.

The modulation current can be disabled by setting the DIS input pin to a high level or setting ENA = 0 (bit 7 of register 0). The modulation current is also disabled in a fault condition, if the internal fault detection enable register flag FLTEN is set to 1 (bit 3 of register 0). To reduce the disable time, only the output stage can be disabled by setting DISMODE = 1 (bit 1 of register 1).

DC OFFSET CANCELLATION AND CROSS-POINT CONTROL

The ONET1151L device has DC offset cancellation by default to compensate for internal offset voltages. To adjust the eye-crossing point, set CPENA = 1 (bit 4 of register 1) and disable the offset cancellation by setting OCDIS = 1 (bit 3 of register 1). Note that setting OCDIS = 1 with CPENA = 0 is an invalid state and results in the modulation current being disabled. The crossing point can be moved toward the one level by setting CPSGN = 1 (bit 7 of register 7) and toward the zero level by setting CPSGN = 0. The percentage of shift depends upon the register settings CPADJ[0..6] (register 7) and the cross-point adjustment range bits CPRNG[0..1] (register 1). Setting CPRNG1 = 0 and CPRNG0 = 0 results in minimum adjustment capability and setting CPRNG1 = 1 and CPRNG0 = 1 results in maximum adjustment capability.

In addition, the modulation current capability is increased by setting CPENA = 1 with or without the offset cancellation being disabled. Table 2 provides a truth table for the various options.

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Table 2. ADC Selection Bits and the Monitored Parameter

CPENA (Bit 4, Register 1)	OCDIS (Bit 3, Register 1)	Cross-Point Adjust	Offset Cancellation	High Modulation Current
0	0	Disabled	Enabled	Disabled
0	1	Invalid	Invalid	Invalid
1	0	Disabled	Enabled	Enabled
1	1	Enabled	Disabled	Enabled

BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by the 2-wire interface. In open-loop operation, selected by setting OLENA = 1 (bit 4 of register 0), the bias current is set directly by the 10-bit-wide control word BIASC[0..9] (registers 4 and 5). In automatic power control mode, selected by setting OLENA = 0, the bias current depends on the register settings BIASC[0..9] and the coupling ratio (CR) between the laser bias current and the photodiode current, CR = I_{BIAS} / I_{PD}. If the photodiode anode is connected to the PD pin (PD pin is sinking current), set PDPOL = 1 (bit 0 of register 0), and if the photodiode cathode is connected to the PD pin (PD pin is sourcing current), set PDPOL = 0.

Three photodiode current ranges are selected by means of the PDRNG[0..1] bits (register 0). Select the photodiode range to keep the laser bias control DAC, BIASC[0..9], close to the center of its range. This range keeps the laser bias current set-point resolution high. For details regarding the bias current setting in open-loop mode, as well as in closed-loop mode, see Table 5.

The ONET1151L device can source or sink the bias current. For the BIAS pin to act as a source, set BIASPOL = 1 (bit 2 of register 1) and for the BIAS pin to act as a sink, set BIASPOL = 0.

The bias current in sink mode is monitored using a current mirror with a gain equal to 1/100 and in source mode with a gain equal to 1/70. By connecting a resistor between MONB and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used. The bias current can also be monitored as a 10 bit unsigned digital word through the 2-wire interface by setting DMONB = 1 (bit 0 of register 10) and removing the resistor to ground.

ANALOG REFERENCE

The ONET1151L laser driver is supplied by a single 3.3-V ±10% supply voltage connected to the VCC pins. This voltage is referred to GND and can be monitored as a 10-bit unsigned digital word through the 2-wire interface.

On-chip band-gap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground (GND). This resistor is used to generate a precise, zero TC current, which is required as a reference current for the on-chip DACs.

To minimize the module component count, the ONET1151L device provides an on-chip temperature sensor. The temperature can be monitored as a 10-bit unsigned digital word through the 2-wire interface.

POWER-ON RESET

The ONE1151L device has power-on reset circuitry, which ensures that registers are reset to zero during start-up. After the power on to initialize time (t_{INIT1}), the internal registers are ready to be loaded. The device is ready to transmit data after the initialize-to-transmit time (t_{INIT2}), assuming that the chip enable bit ENA is set to 1 and the disable pin DIS is low. The DIS pin has an internal 10-kΩ pullup resistor, so the pin must be pulled low to enable the outputs.

The ONET1151L device can be disabled using either the ENA control register bit or the disable pin DIS. In both cases, the internal registers are not reset. After the disable pin DIS is set low and/or the enable bit ENA is reset to 1, the device returns to its previous output settings.

To reduce the disable time, only the output stage can be disabled by setting DISMODE = 1 (bit 1 of register 1).

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ANALOG-TO-DIGITAL CONVERTER

The ONE1151L device has an internal 10-bit ADC that converts the analog monitors for temperature, power-supply voltage, bias current, and photodiode current into a 10-bit unsigned digital word. The first 8 most significant bits (MSBs) are available in register 14 and the 2 least significant bits (LSBs) are available in register 15. Depending on the accuracy required, 8 or 10 bits can be read. However, to read the two registers, two separate read commands must be sent due to the architecture of the 2-wire interface.

The ADC is enabled by default, and to monitor a particular parameter, select the parameter with ADCSEL[0..1] (bits 0 and 1 of register 13). Table 3 shows the ADCSEL bits and the monitored parameter.

Table 3. ADC Selection Bits and the Monitored Parameter

ADCSEL1	ADCSEL0	Monitored Parameter
0	0	Temperature
0	1	Supply voltage
1	0	Photodiode current
1	1	Bias current

To digitally monitor the photodiode current, ensure that DMONP = 1 (bit 1 of register 10) and a resistor is not connected to the MONP pin. To digitally monitor the bias current, ensure that DMONB = 1 (bit 0 of register 10) and a resistor is not connected to the MONB pin. If the ADC is not used to monitor the various parameters, then it can be disabled by setting ADCDIS = 1 (bit 7 of register 13) and OSCDIS = 1 (bit 6 of register 13).

The recommended procedure for reading the ADC follows:

1. Disable the ADC (set bit 7 of register 13 to 1).
2. Set the desired ADC mode (set bits 0 and 1 of register 13 per Table 3).
3. Enable the ADC (set bit 7 of register 13 to 0).
4. Wait 500 µs.
5. Disable the ADC (set bit 7 of register 13 to 1).
6. Read the ADC conversion result from register 14 (MSB) and register 15 (LSB).

Convert the digital word read from the ADC to its analog equivalent through the following formulas.

Temperature without a midpoint calibration:

$$\text{Temperature (°C)} = \frac{\text{ADC}x - 264}{6} \tag{1}$$

Temperature with a midpoint calibration:

$$\text{Temperature (°C)} = \frac{(\text{T_cal(°C)} + 273) \times (\text{ADC}x + 1362)}{\text{ADC_cal} + 1362} - 273 \tag{2}$$

Power supply voltage:

$$\text{Power supply voltage (V)} = \frac{2.25 \times (\text{ADC}x + 1380)}{1409} \tag{3}$$

Photodiode current monitor:

$$\text{IPD}(\mu\text{A}) = 1.3 \times \text{ADC}x \quad \text{for PDRNG 00} \tag{4}$$

$$\text{IPD}(\mu\text{A}) = 2.6 \times \text{ADC}x \quad \text{for PDRNG 01} \tag{5}$$

$$\text{IPD}(\mu\text{A}) = 5.2 \times \text{ADC}x \quad \text{for PDRNG 1}x \tag{6}$$

Bias current monitor source mode:

$$I_{BIAS}\,(\text{mA}) = 0.12 \times \text{ADC}x \tag{7}$$

Bias current monitor sink mode:

$$I_{BIAS}\,(\text{mA}) = 0.19 \times \text{ADC}x$$

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where

- ADCx = the decimal value read from the ADC
- T_cal = the calibration temperature
- ADC_cal = the decimal value read from the ADC at the calibration temperature (8)

For the photodiode and bias current monitors, a nonzero current must be applied to the ADC in order to read back a valid result. For the cases when the bias current is set to zero, the DIS pin is set high or the ENA bit is set to 0, bias current is not applied to the ADC and the digital reading is not valid.

2-WIRE INTERFACE AND CONTROL LOGIC

The ONET1151L device uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. The SDA and SCK pins have internal 10-kΩ pullups to VCC. If a common interface is used to control multiple parts, the internal pullups can be switched to 40 kΩ by setting the TWITERM bit to 1 (bit 0 of register 1). The internal pullups automatically switch to 40 kΩ, if the slave address is changed from its default value using the ADR0 or ADR1 pins.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read the control signals. The ONET1151L device is a slave device, which means that it cannot initiate a transmission itself. The ONET1151L device always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (0001000) followed by an eighth bit, which is the data direction bit (R/W). 0 indicates a Write and 1 indicates a Read.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

The first 2 bits of the slave address can be changed to 1 by grounding the ADR0 and ADR1 pins.

Regarding timing, the ONET1151L device is I^2C compatible. Figure 2 shows the typical timing. Figure 3 shows a complete data transfer. Table 4 lists parameters for Figure 2.

Descriptions of various events on the 2-wire interface follow:

Bus idle: Both SDA and SCK lines remain High.

Start data transfer: A change in the state of the SDA line, from High to Low, while the SCK line is High, defines a Start condition (S). Each data transfer initiates with a Start condition.

Stop data transfer: A change in the state of the SDA line from Low to High while the SCK line is High, defines a Stop condition (P). Each data transfer is terminated with a Stop condition. However, if the master still wishes to communicate on the bus, it can generate a repeated Start condition and address another slave without first generating a Stop condition.

Data transfer: Only one data byte can be transferred between a Start and a Stop condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable Low during the High period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left High by the slave. The master can then generate a Stop condition to abort the transfer. If the slave-receiver does acknowledge the slave address, but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. The slave indicates by generating no acknowledgment on the first byte to follow. The slave leaves the data line High, and the master generates the Stop condition.

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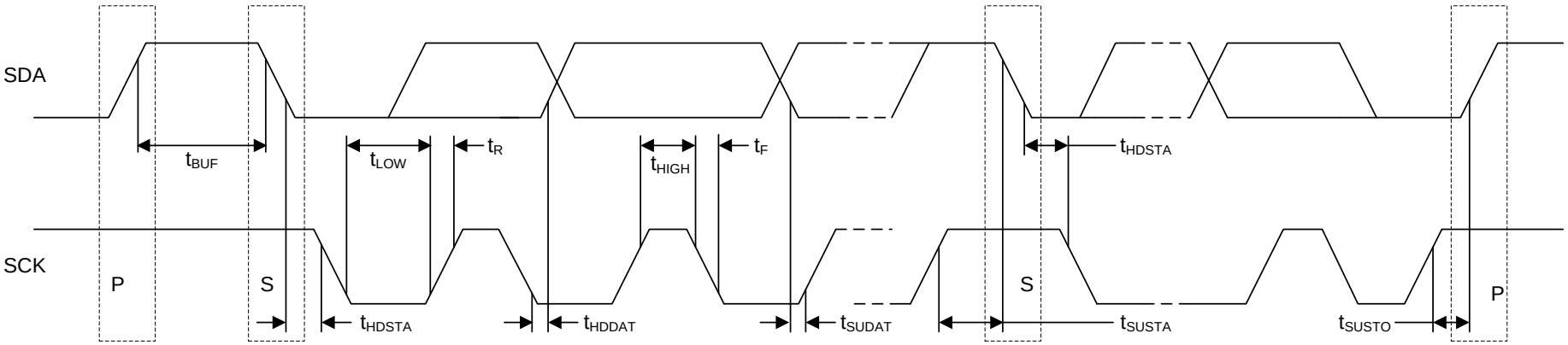

Figure 2. I²C Timing Diagram

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Table 4. Timing Diagram Definitions

PARAMETER		MIN	MAX	UNIT
f_{SCK}	SCK clock frequency		400	kHz
t_{BUF}	Bus free time between Start and Stop conditions	1.3		µs
t_{HDSTA}	Hold time after repeated Start condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCK clock	1.3		µs
t_{HIGH}	High period of the SCK clock	0.6		µs
t_{SUSTA}	Setup time for a repeated Start condition	0.6		µs
t_{HDDAT}	Data hold time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCK signals		300	ns
t_F	Fall time of both SDA and SCK signals		300	ns
t_{SUSTO}	Setup time for Stop condition	0.6		µs

Write Sequence

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	Data Byte	A	P

Read Sequence

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	S	Slave Address	Rd	A	Data Byte	N	P

Legend

S	Start Condition
Wr	Write Bit (bit value = 0)
Rd	Read Bit (bit value = 1)
A	Acknowledge
N	Not Acknowledged
P	Stop Condition

Figure 3. Programming Sequence

REGISTER MAPPING

Figure 4 through Figure 19 show the register mapping for register addresses 0 (0x00) through 15 (0x0F), respectively.

register address 0 (0x00)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ENA	PDRNG1	PDRNG0	OLENA	FLTEN	POL	EQENA	PDPOL

Figure 4. Register 0 (0x00) Mapping – Control Settings

register address 1 (0x01)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CPTC	CPRNG1	CPRNG0	CPENA	OCDIS	BIASPOL	DISMODE	TWITERM

Figure 5. Register 1 (0x01) Mapping – Control Settings

register address 2 (0x02)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	MODC1	MODC0

Figure 6. Register 2 (0x02) Mapping – Modulation Current

register address 3 (0x03)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MODC9	MODC8	MODC7	MODC6	MODC5	MODC4	MODC3	MODC2

Figure 7. Register 3 (0x03) Mapping – Modulation Current

register address 4 (0x04)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	BIASC1	BIASC0

Figure 8. Register 4 (0x04) Mapping – Bias Current

register address 5 (0x05)							
bit 7	bit 6	bit 5	bit 7	bit 6	bit 5	bit 4	bit 3
BIASC9	BIASC8	BIASC7	BIASC6	BIASC5	BIASC4	BIASC3	BIASC2

Figure 9. Register 5 (0x05) Mapping – Bias Current

register address 6 (0x06)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EQADJ7	EQADJ6	EQADJ5	EQADJ4	EQADJ3	EQADJ2	EQADJ1	EQADJ0

Figure 10. Register 6 (0x06) Mapping – Equalizer Adjust

register address 7 (0x07)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CPSGN	CPADJ6	CPADJ5	CPADJ4	CPADJ3	CPADJ2	CPADJ1	CPADJ0

Figure 11. Register 7 (0x07) Mapping – Cross-Point Adjust

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register address 8 (0x08)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LOWGAIN	–	–	ORADJ1	ORADJ0	DE2	DE1	DE0

Figure 12. Register 8 (0x08) Mapping – Output Adjustments

register address 9 (0x09)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LIMCSGN	LMC2	LIMC1	LIMC0	EFCSGN	EFC2	EFC1	EFC0

Figure 13. Register 9 (0x09) Mapping – Limiter Bias Current Adjust

register address 10 (0x0A)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	MONPFLT	DMONP	DMONB

Figure 14. Register 10 (0x0A) Mapping – Monitor Settings

register address 11 (0x0B)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BMF7	BMF6	BMF5	BMF4	BMF3	BMF2	BMF1	BMF0

Figure 15. Register 11 (0x0B) Mapping – Bias Monitor Fault Settings

register address 12 (0x0C)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PMF7	PMF6	PMF5	PMF4	PMF3	PMF2	PMF1	PMF0

Figure 16. Register 12 (0x0C) Mapping – Power Monitor Fault Settings

register address 13 (0x0D)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ADCDIS	OSCDIS	–	–	–	–	ADCSEL1	ADCSEL0

Figure 17. Register 13 (0x0D) Mapping – ADC Settings

register address 14 (0x0E)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2

Figure 18. Register 14 (0x0E) Mapping – ADC Output (Read Only)

register address 15 (0x0F)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	ADC1	ADC0

Figure 19. Register 15 (0x0F) Mapping – ADC Output (Read Only)

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Table 5 describes the circuit functionality based on the register settings.

Table 5. Register Functionality

Register	Bit	Symbol	Function
0	7	ENA	**Enable chip bit** 1 = Chip enabled, can be toggled low to reset a fault condition. 0 = Chip disabled
	6 5	PDRNG1 PDRNG0	**Photodiode current range bits** 1X: up to 3080-µA / 3-µA resolution 01: up to 1540-µA / 1.5-µA resolution 00: up to 770-µA / 0.75-µA resolution
	4	OLENA	**Open-loop enable bit** 1 = Open-loop bias current control 0 = Closed-loop bias current control
	3	FLTEN	**Fault detection enable bit** 1 = Fault detection on 0 = Fault detection off
	2	POL	**Output polarity switch bit** 1: pin 22 = OUT– and pin 21 = OUT+ 0: pin 22 = OUT+ and pin 21 = OUT–
	1	EQENA	**Equalizer enable bit** 1 = Equalizer is enabled 0 = Equalizer is disabled and bypassed
	0	PDPOL	**Photodiode polarity bit** 1 = Photodiode cathode connected to V_{CC} 0 = Photodiode anode connected to GND
1	7	CPTC	**Cross-point temperature coefficient adjustment bit** 1 = Cross-point temperature coefficient is enabled 0 = Cross-point temperature coefficient is disabled
	6 5	CPRNG1 CPRNG0	**Cross-point adjustment range bits** Minimum adjustment range for 00 Maximum adjustment range for 11
	4	CPENA	**Cross-point adjustment enable bit** 1 = Cross-point adjustment is enabled. Setting to 1 with OCDIS = 0 or 1 increases the modulation current. 0 = Cross-point adjustment is disabled
	3	OCDIS	**Offset cancellation disable bit** 1 = DC offset cancellation is disabled. Do not set to 1 with CPENA set to 0. 0 = DC offset cancellation is enabled
	2	BIASPOL	**Bias current polarity bit** 1 = Bias pin sources current 0 = Bias pin sinks current
	1	DISMODE	**Disable mode setting bit** 1 = Only the output stage is disabled (fast-disable mode) 0 = Major parts of the signal path are disabled
	0	TWITERM	**2-wire interface input termination select bit** 1 = 40 kΩ selected 0 = 10 kΩ selected
2	1	MODC1	**Modulation current setting:** sets the output voltage Modulation current : 85-mA or 86-µA steps
	0	MODC0	
3	7	MODC9	
	6	MODC8	
	5	MODC7	
	4	MODC6	
	3	MODC5	
	2	MODC4	
	1	MODC3	
	0	MODC2	

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Table 5. Register Functionality (continued)

Register	Bit	Symbol	Function
4	1	BIASC1	**Closed loop (APC):** Coupling ratio CR = I_{BIAS} / I_{PD}, BIASC = 0..1023, I_{BIAS} ≤ 100 mA: PDRNG = 00 (see above); I_{BIAS} = 0.75 µA × CR × BIASC PDRNG = 01 (see above); I_{BIAS} = 1.5 µA × CR × BIASC PDRNG = 1X (see above); I_{BIAS} = 3 µA × CR × BIASC **Open loop:** IBIAS = 102 µA × BIASC
	0	BIASC0	
5	7	BIASC9	
	6	BIASC8	
	5	BIASC7	
	4	BIASC6	
	3	BIASC5	
	2	BIASC4	
	1	BIASC3	
	0	BIASC2	
6	7	EQADJ7	**Equalizer adjustment setting** EQENA = 0 (see above) Equalizer is turned off and bypassed EQENA = 1 (see above) Maximum equalization for 00000000 Minimum equalization for 11111111
	6	EQADJ6	
	5	EQADJ5	
	4	EQADJ4	
	3	EQADJ3	
	2	EQADJ2	
	1	EQADJ1	
	0	EQADJ0	
7	7	CPSGN	**Eye cross-point adjustment setting** CPSGN = 1 (positive shift) Maximum shift for 1111111 Minimum shift for 0000000 CPSGN = 0 (negative shift) Maximum shift for 1111111 Minimum shift for 0000000
	6	CPADJ6	
	5	CPADJ5	
	4	CPADJ4	
	3	CPADJ3	
	2	CPADJ2	
	1	CPADJ1	
	0	CPADJ0	
8	7	LOWGAIN	**Path-gain control bit** 1 = Half gain used to reduce power if cross-point adjustment is not used 0 = Full gain
	6	–	
	5	–	
	4 3	ORADJ1 ORADJ0	**Output resistance adjustment setting** 00 = Lowest resistance 11 = Highest resistance
	2 1 0	DE2 DE1 DE0	**Output De-emphasis adjustment setting** 000 = No de-emphasis 111 = Maximum de-emphasis
9	7	LIMCSGN	**Limiter bias current sign bit** 1 = Decrease limiter bias current 0 = Increase limiter bias current
	6 5 4	LIMC2 LIMC1 LIMC0	**Limiter bias current selection bits** 000 = No change 111 = Maximum current change
	3	EFCSGN	**Emitter follower sign bit** 1 = Decrease emitter follower current 0 = Increase emitter follower current
	2 1 0	EFC2 EFC1 EFC0	**Emitter follower current selection bits** 000 = No change 111 = Maximum current change

Table 5. Register Functionality (continued)

Register	Bit	Symbol	Function
10	7	–	
	6	–	
	5	–	
	4	–	
	3	–	
	2	MONPFLT	**Analog photodiode current monitor fault trigger bit** 1 = Fault trigger on MONP pin is enabled 0 = Fault trigger on MONP pin is disabled
	1	DMONP	**Digital photodiode current monitor selection bit (MONP)** 1 = Digital photodiode monitor is active (no external resistor is needed) 0 = Analog photodiode monitor is active (external resistor is required)
	0	DMONB	**Digital bias current monitor selection bit (MONB)** 1 = Digital bias current monitor is active (no external resistor is needed) 0 = Analog bias current monitor is active (external resistor is required)
11	7	BMF7	**Bias current monitor fault threshold** With DMONB = 1 Register sets the value of the bias current that will trigger a fault. The external resistor on the MONB pin must be removed to use this feature.
	6	BMF6	
	5	BMF5	
	4	BMF4	
	3	BMF3	
	2	BMF2	
	1	BMF1	
	0	BMF0	
12	7	PMF7	**Power monitor fault threshold** With DMONP = 1 Register sets the value of the photodiode current that will trigger a fault. The external resistor on the MONP pin must be removed to use this feature.
	6	PMF6	
	5	PMF5	
	4	PMF4	
	3	PMF3	
	2	PMF2	
	1	PMF1	
	0	PMF0	
13	7	ADCDIS	**ADC disable bit** 1 = ADC disabled 0 = ADC enabled
	6	OSCDIS	**ADC oscillator bit** 1 = Oscillator disabled 0 = Oscillator enabled
	5	–	
	4	–	
	3	–	
	2	–	
	1 0	ADCSEL1 ADCSEL0	**ADC input selection bits** 00 selects the temperature sensor 01 selects the power supply monitor 10 selects MONP 11 selects MONB

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Table 5. Register Functionality (continued)

Register	Bit	Symbol	Function
14	7	ADC9 (MSB)	**Digital representation of the ADC input source (read only)**
	6	ADC8	
	5	ADC7	
	4	ADC6	
	3	ADC5	
	2	ADC4	
	1	ADC3	
	0	ADC2	
15	7	–	
	6	–	
	5	–	
	4	–	
	3	–	
	2	–	
	1	ADC1	**Digital representation of the ADC input source (read only)**
	0	ADC0 (LSB)	

LASER SAFETY FEATURES AND FAULT RECOVERY PROCEDURE

The ONET1151L device provides built-in laser safety features. The following fault conditions are detected:

- Voltage at MONB exceeds the voltage at RZTC (1.16 V), or alternately, if DMONB = 1 and the bias current exceeds the bias current monitor fault threshold set by BMF[0..7] (register 11). When using the digital monitor, the resistor to ground must be removed.
- Voltage at MONP exceeds the voltage at RZTC (1.16 V) and the analog photodiode current monitor fault trigger bit, MONPFLT (bit 2 of register 10), is set to 1. Alternately, a fault can be triggered if DMONP = 1 and the bias current exceeds the bias current monitor fault threshold set by PMF[0..7] (register 12). When using the digital monitor, the resistor to ground must be removed.
- Photodiode current exceeds 150% of its set value.
- Bias control DAC drops in value by more than 50% in one step.

If one or more fault conditions occur, and the fault enable bit FLTEN is set to 1, the ONET1151L device responds by:

1. Setting the bias current to 0
2. Setting the modulation current to 0
3. Asserting and latching the FLT pin

Fault recovery is achieved by performing the following procedure:

1. The disable pin DIS, or the internal enable control bit ENA, or both, are toggled for at least the fault latch reset time.
2. The FLT pin deasserts while the disable pin DIS is asserted or the enable bit ENA is deasserted.
3. If the fault condition is no longer present, the device returns to typical operation with its previous output settings, after the disable negate time.
4. If the fault condition is still present, FLT reasserts once DIS is set to a low level and the part does not return to typical operation.

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APPLICATIONS INFORMATION

Figure 20 shows a typical application circuit using the ONET1151L device with a differentially driven laser. The laser driver is controlled through the 2-wire interface SDA and SCK by a microcontroller.

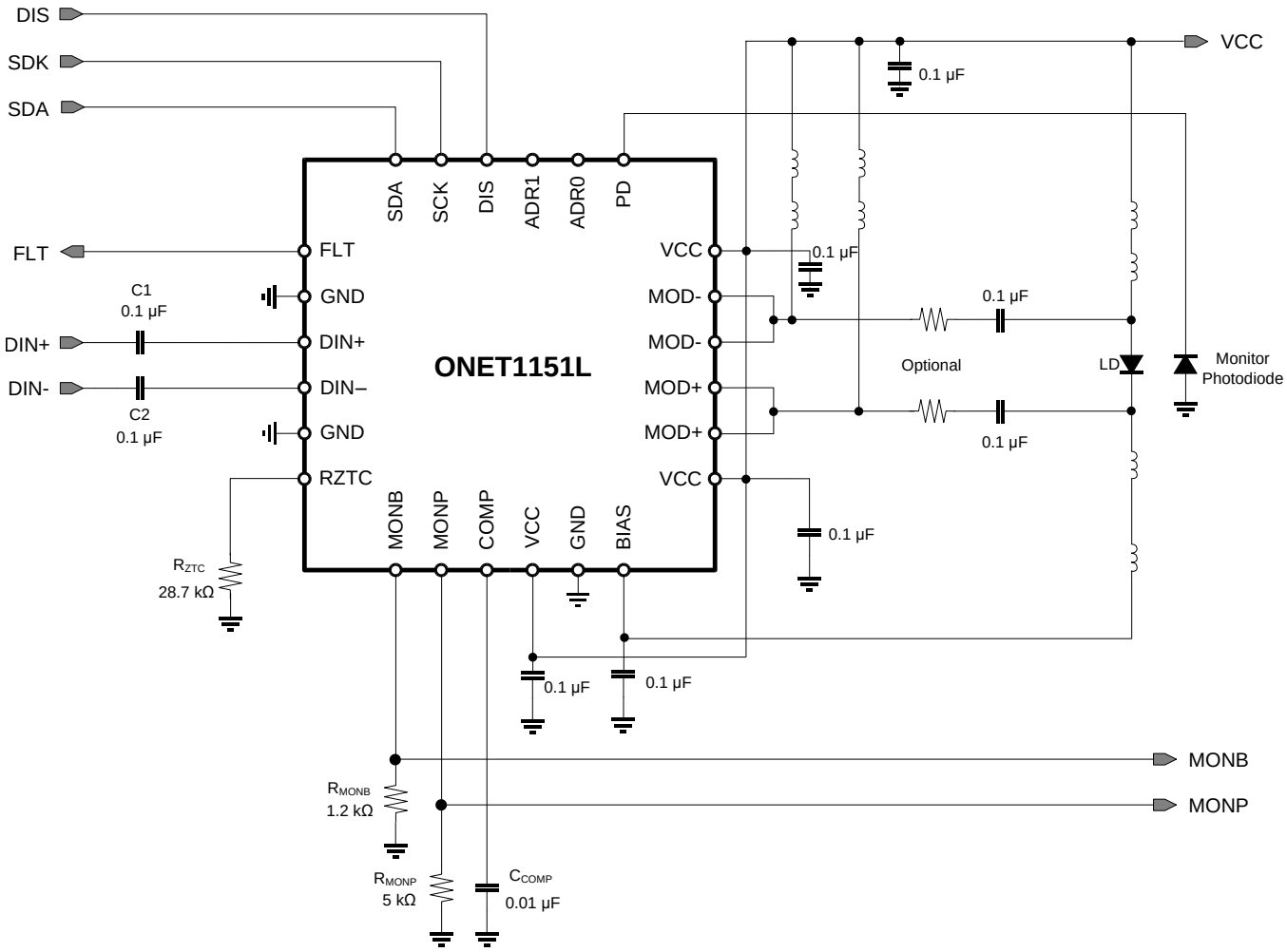

Figure 20. AC-Coupled Differential Drive

LAYOUT GUIDELINES

For optimum performance, use 50-Ω transmission lines (100-Ω differential) for connecting the signal source to the DIN+ and DIN– pins and 25-Ω transmission lines (50-Ω differential) for connecting the modulation current outputs, MOD+ and MOD-, to the laser. The length of the transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter. TI recommends assembling the series matching resistor as close as possible to the TOSA, if required.

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TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at V_{CC} = +3.3 V, T_A = +25°C, I_{BIASC} = 30 mA, I_{MODC} = 30 mA, V_{IN} = 600 mVpp (unless otherwise noted).

DETERMINISTIC JITTER vs MODULATION CURRENT

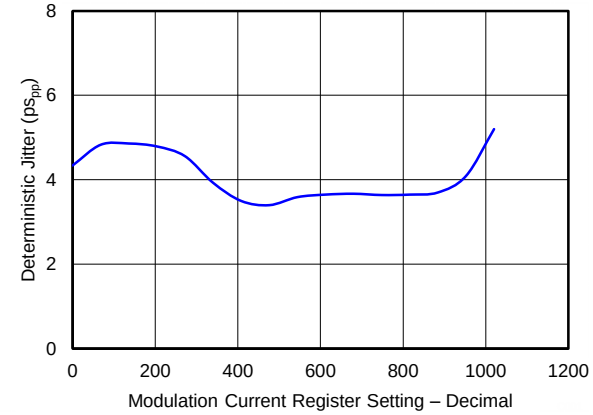

Figure 21.

DETERMINISTIC JITTER vs TEMPERATURE

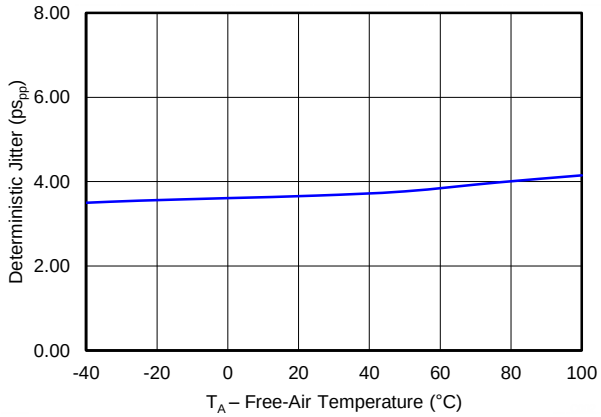

Figure 22.

RANDOM JITTER vs MODULATION CURRENT

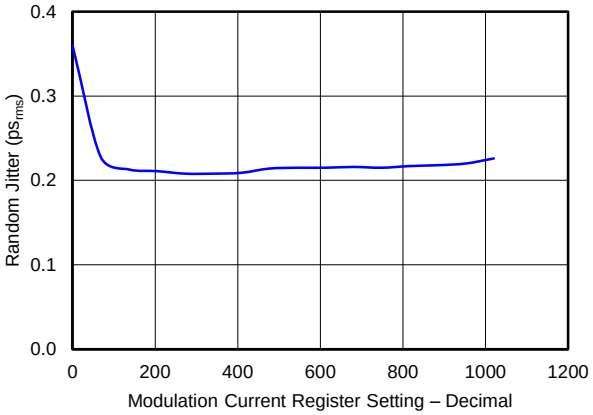

Figure 23.

RANDOM JITTER vs TEMPERATURE

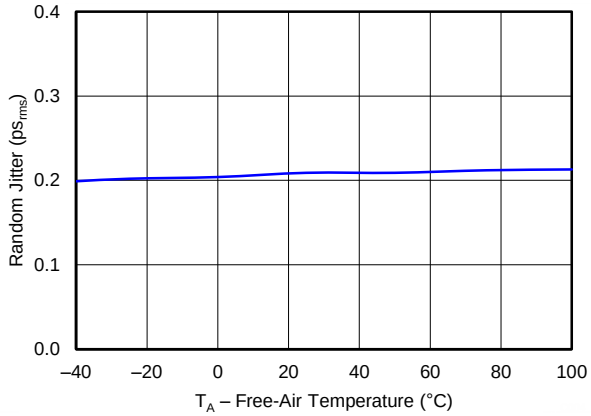

Figure 24.

RISE-TIME AND FALL-TIME vs MODULATION CURRENT

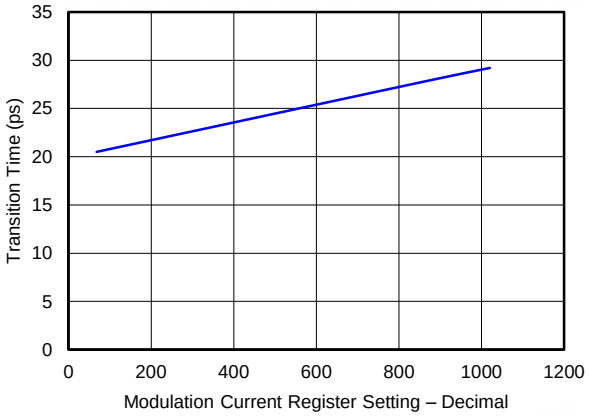

Figure 25.

RISE-TIME AND FALL-TIME vs TEMPERATURE

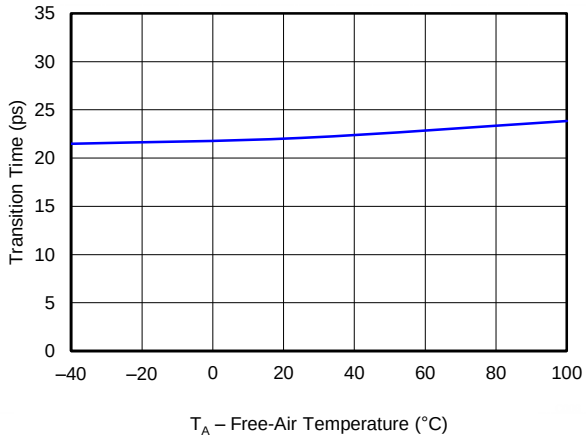

Figure 26.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = +3.3 V, T_A = +25°C, I_{BIASC} = 30 mA, I_{MODC} = 30 mA, V_{IN} = 600 mVpp (unless otherwise noted).

BIAS CURRENT IN OPEN LOOP MODE vs BIASC REGISTER SETTING

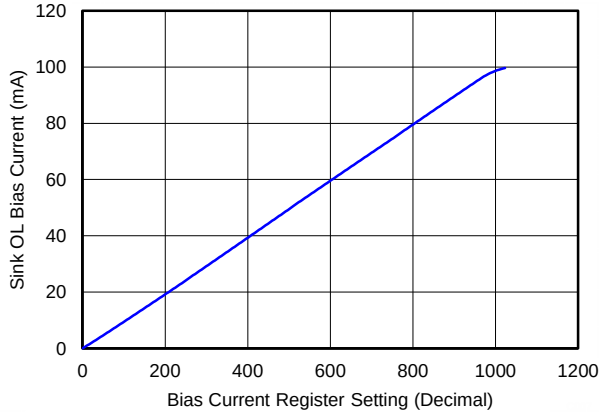

Figure 27.

BIAS-MONITOR CURRENT I_{MONB} vs BIAS CURRENT

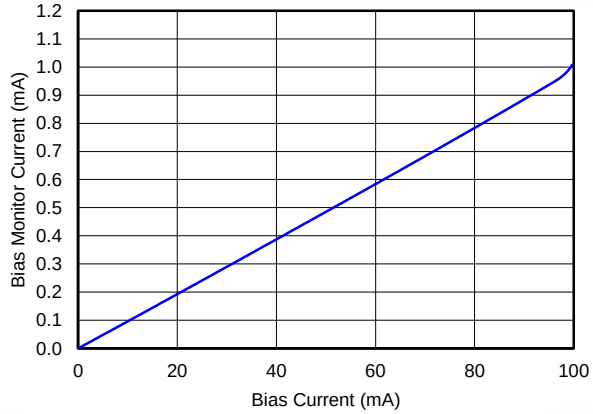

Figure 28.

PHOTODIODE-MONITOR CURRENT I_{MONP} vs PD CURRENT, PDRNG = 01

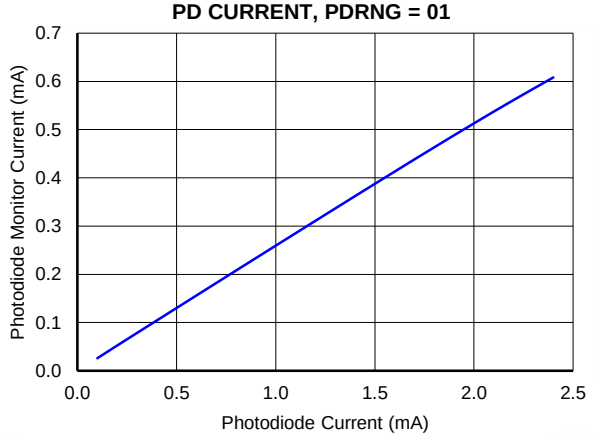

Figure 29.

MODULATION CURRENT vs MODC REGISTER SETTING

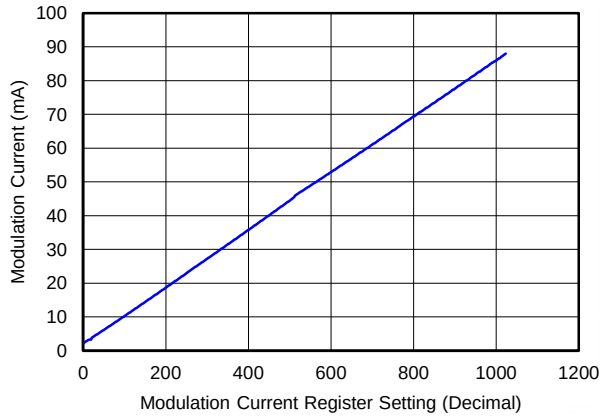

Figure 30.

SUPPLY CURRENT vs TEMPERATURE

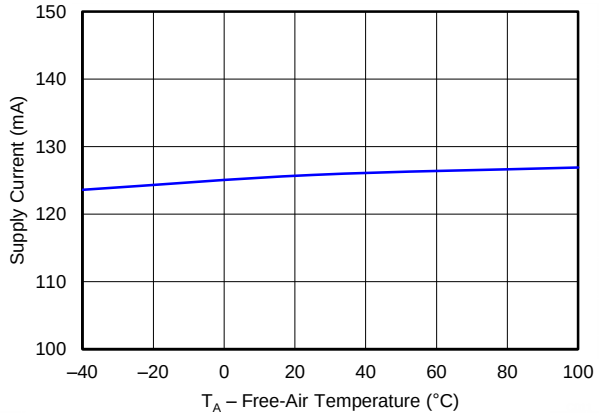

Figure 31.

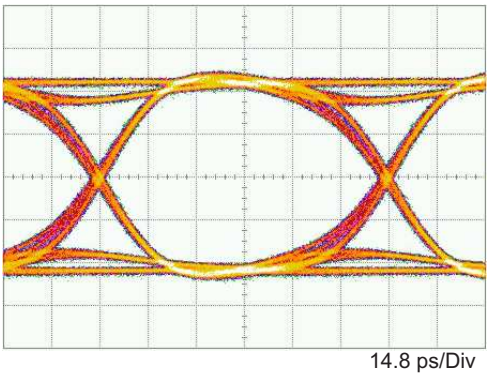

Figure 32. Eye-Diagram at 11.3 Gbps I_{MOD} = 20 mA, EQENA = 0

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TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = +3.3 V, T_A = +25°C, I_{BIASC} = 30 mA, I_{MODC} = 30 mA, V_{IN} = 600 mVpp (unless otherwise noted).

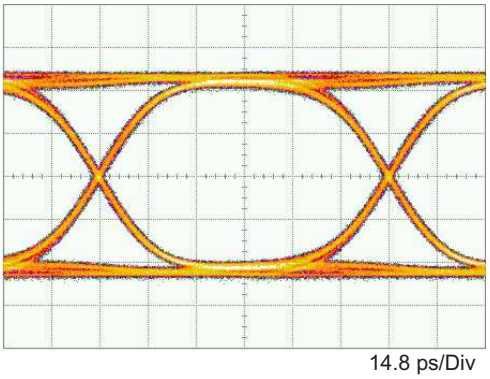

Figure 33. Eye-Diagram at 11.3 Gbps I_{MOD} = 40 mA, EQENA = 0

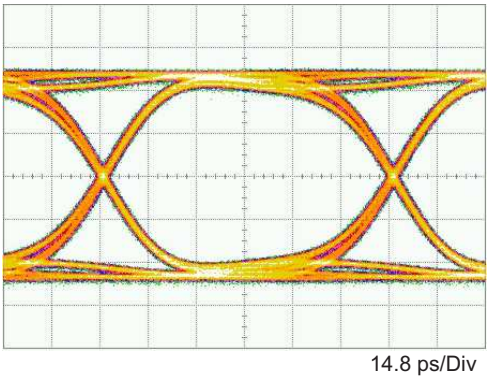

Figure 34. Eye-Diagram at 11.3 Gbps PRBS-31 Pattern, I_{MOD}= 60 mA, EQENA = 0

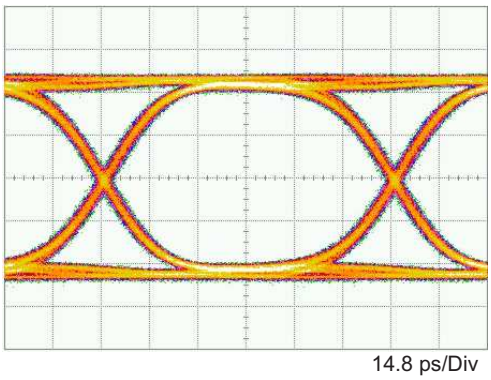

Figure 35. Eye-Diagram at 11.3 Gbps I_{MOD} = 40 mA, EQENA = 1, 12 in. of FR4 at Inputs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET1151LRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1151L	Samples
ONET1151LRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1151L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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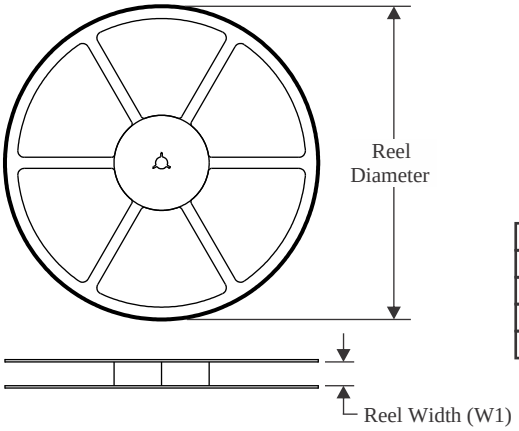
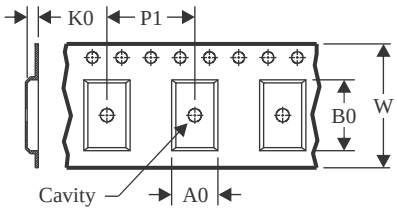
TAPE AND REEL INFORMATION

REEL DIMENSIONS

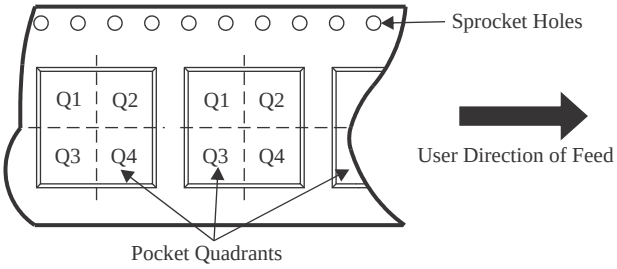


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

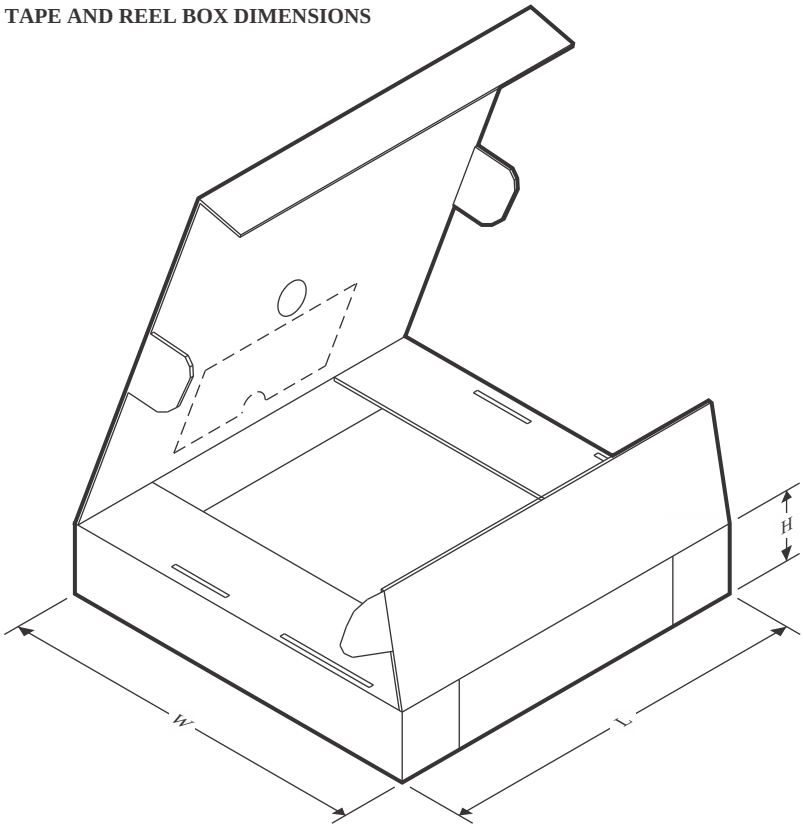
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET1151LRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ONET1151LRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

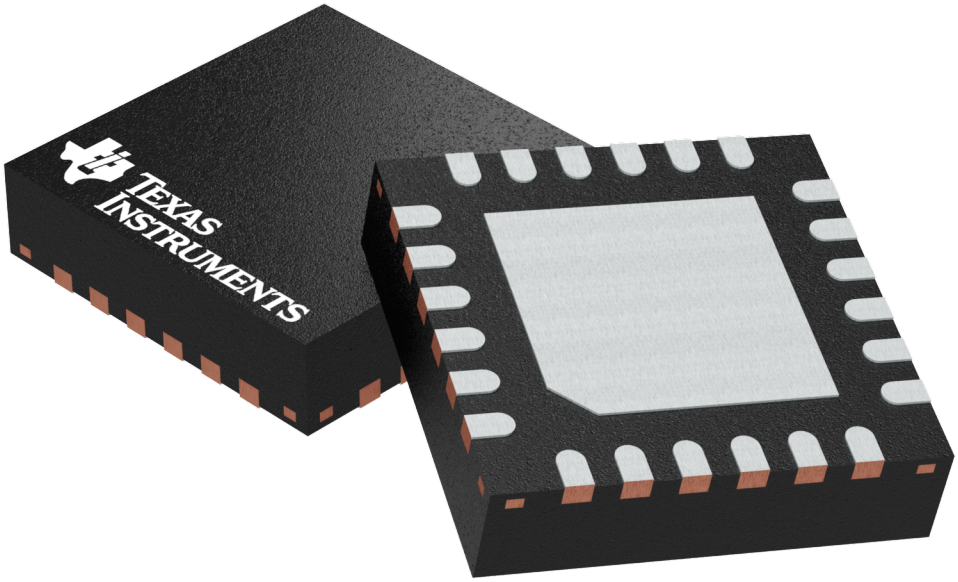


*All dimensions are nominal

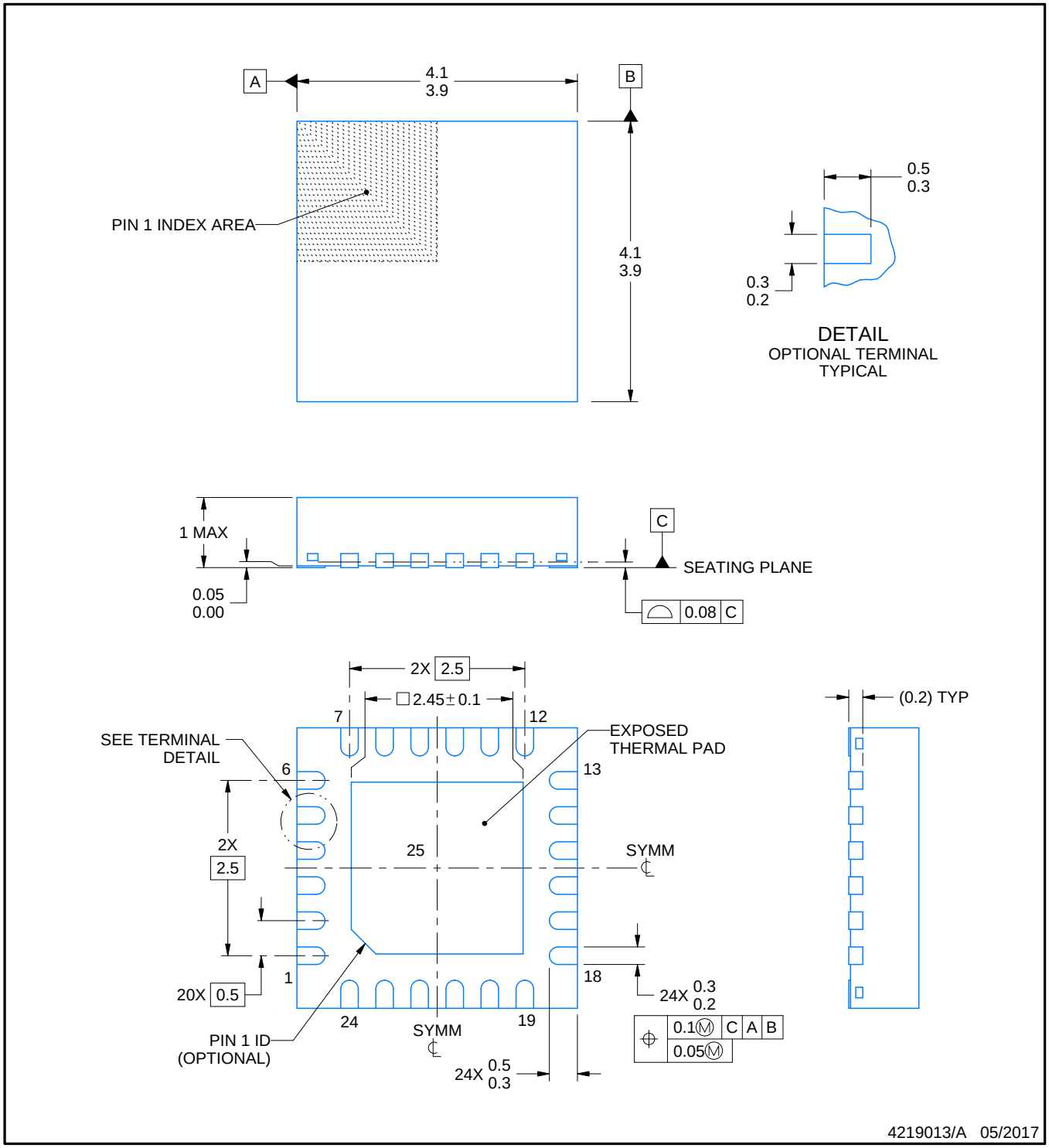
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET1151LRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
ONET1151LRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

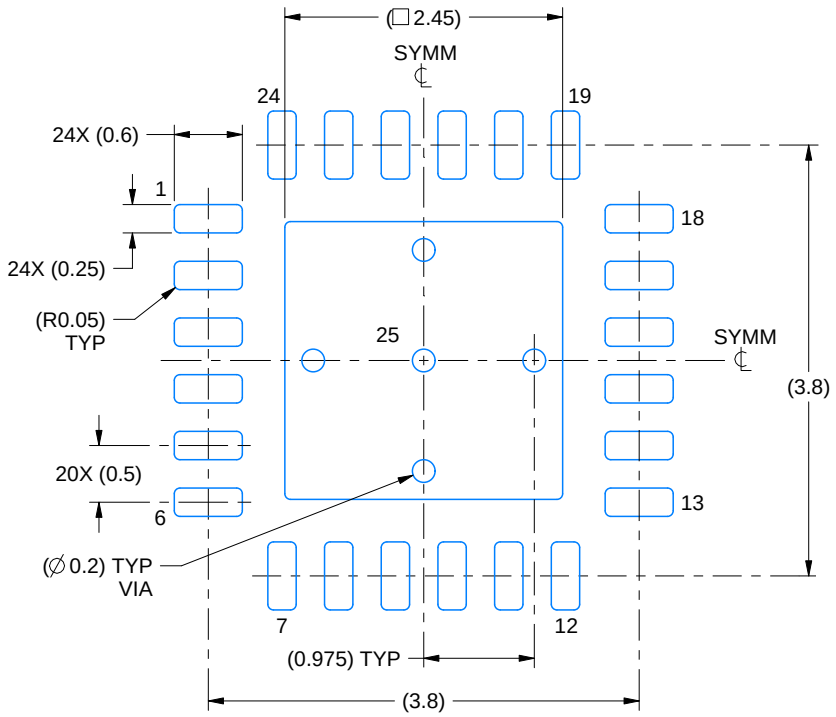


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

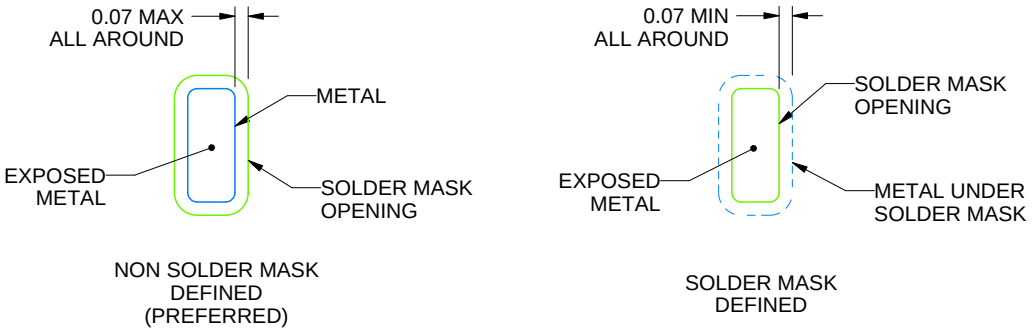


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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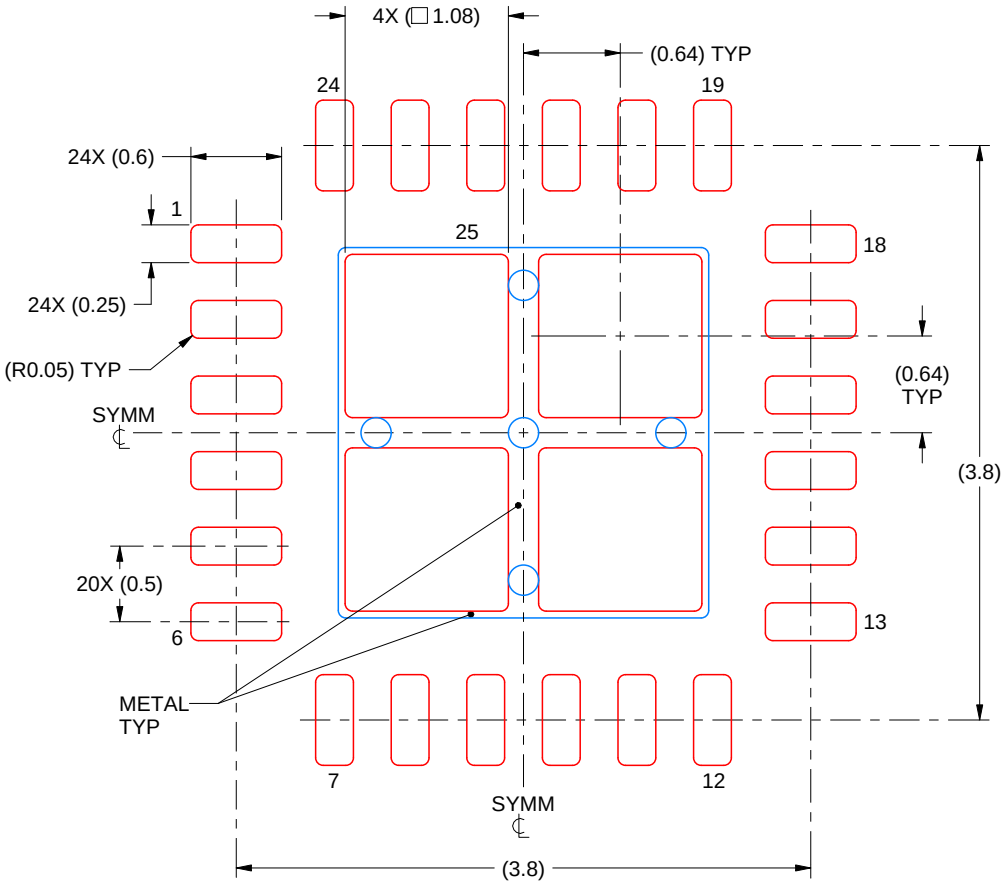
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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