THE DATASHEET OF

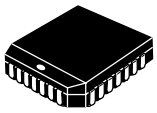
MC100H641FNR2

MC10H641, MC10H641

Single Supply PECL to TTL 1:9 Clock Distribution Chip

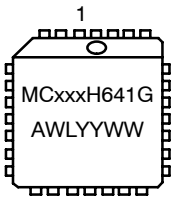
ON Semiconductor®

http://onsemi.com



PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Description

The MC10H/100H641 is a single supply, low skew translating 1:9 clock driver. Devices in the ON Semiconductor H641 translator series utilize the PLCC−28 for optimal power pinning, signal flow through and electrical performance.

The device features a 24 mA TTL output stage, with AC performance specified into a 50 pF load capacitance. A latch is provided on−chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldown) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW. Both the LEN and $\overline{EN}$ pins are positive ECL inputs.

The V_{BB} output is provided in case the user wants to drive the device with a single−ended input. For single−ended use, the V_{BB} should be connected to the $\overline{D}$ input and bypassed with a 0.01 μF capacitor.

The 10H version of the H641 is compatible with positive MECL 10H™ logic levels. The 100H version is compatible with positive 100K levels.

Features

- PECL – TTL Version of Popular ECLinPS E111
- Low Skew
- Guaranteed Skew Spec
- Latched Input
- Differential ECL Internal Design
- V_{BB} Output for Single−Ended Use
- Single +5.0 V Supply
- Logic Enable
- Extra Power and Ground Supplies
- Separate ECL and TTL Supply Pins
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

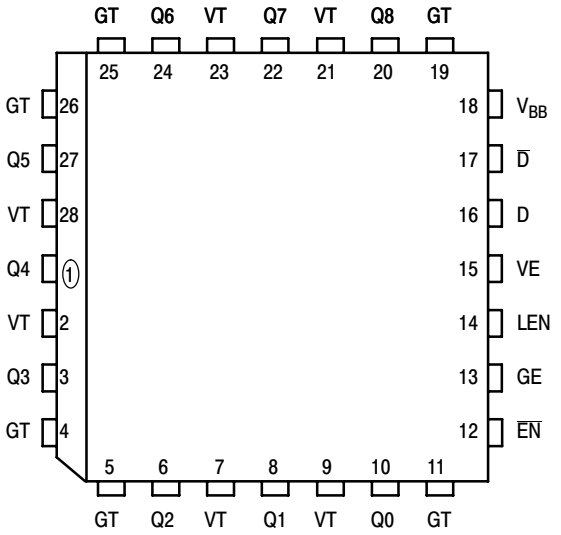


Figure 1. Pinout: PLCC−28 (Top View)

Table 1. PIN DESCRIPTION

Pins	Function
GT, VT	TTL GND, TTL V_{CC}
GE, VE	ECL GND, ECL V_{CC}
D, $\overline{D}$	Signal Input (Positive ECL)
V_{BB}	V_{BB} Reference Output (Positive ECL)
Q0 − Q8	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (Positive ECL)
LEN	Latch Enable Input (Positive ECL)

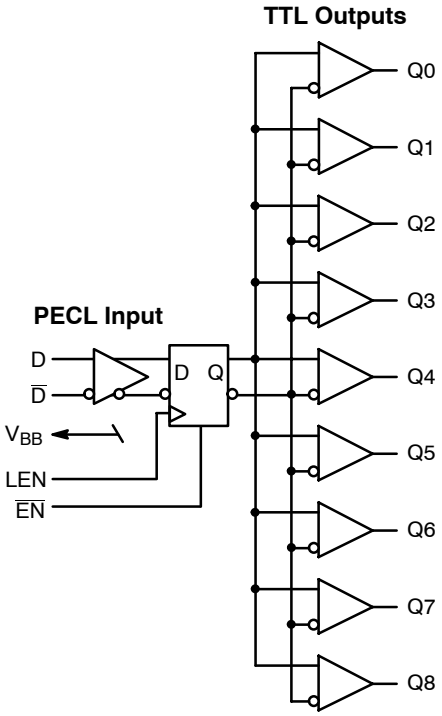


Figure 2. Logic Diagram

Table 2. 10H PECL DC CHARACTERISTICS

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH}	Input HIGH Current			255		175		175	μA
I_{IL}	Input LOW Current		0.5		0.5		0.5		μA
V_{IH}	Input HIGH Voltage	V_E = 5.0 V (Note 1)	3.83	4.16	3.87	4.19	3.94	4.28	V
V_{IL}	Input LOW Voltage	V_E = 5.0 V (Note 1)	3.05	3.52	3.05	3.52	3.05	3.55	V
V_{BB}	Output Reference Voltage	V_E = 5.0 V (Note 1)	3.62	3.73	3.65	3.75	3.69	3.81	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. PECL V_{IH}, V_{IL}, and V_{BB} are referenced to VE and will vary 1:1 with the power supply. The levels shown are for VE = 5.0 V.

Table 3. 100H PECL DC CHARACTERISTICS

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH}	Input HIGH Current			255		175		175	μA
I_{INL}	Input LOW Current		0.5		0.5		0.5		μA
V_{IH}	Input HIGH Voltage	V_E = 5.0 V (Note 2)	3.835	4.120	3.835	4.120	3.835	4.120	V
V_{IL}	Input LOW Voltage	V_E = 5.0 V (Note 2)	3.190	3.525	3.190	3.525	3.190	3.525	V
V_{BB}	Output Reference Voltage	V_E = 5.0 V (Note 2)	3.62	3.74	3.62	3.74	3.62	3.74	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. PECL V_{IH}, V_{IL}, and V_{BB} are referenced to VE and will vary 1:1 with the power supply. The levels shown are for VE = 5.0 V.

Table 4. DC CHARACTERISTICS (V_T = V_E = 5.0 V ±5%)

Symbol	Characteristic	T_A = 0°C			T_A = + 25°C			T_A = + 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current PECL		24	30		24	30		24	30	mA
I_{CCH}	TTL		24	30		24	30		24	30	mA
I_{CCL}			27	35		27	35		27	35	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. TTL DC CHARACTERISTICS (V_T = V_E = 5.0 V ±5%)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = −15 mA	2.5		2.5		2.5		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA		0.5		0.5		0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	−100	−225	−100	−225	−100	−225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS ($V_T = V_E = 5.0$ V ±5%)

Symbol	Characteristic	Condition	T_J = 0°C			T_J = + 25°C			T_J = + 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay D to Q	CL = 50 pF (Note 3)	5.00 5.36	5.50 5.86	6.00 6.36	4.86 5.27	5.36 5.77	5.86 6.27	5.08 5.43	5.58 5.93	6.08 6.43	ns
t_{skew}	Device Skew Part−to−Part Single V_{CC} Output−to−Output	 CL = 50 pF (Note 4) CL = 50 pF (Note 5) CL = 50 pF (Note 6)			 1000 750 350			 1000 750 350			 1000 750 350	ps
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	CL = 50 pF	4.9		6.9	4.9		6.9	5.0		7.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Q	CL = 50 pF	5.0		7.0	4.9		6.9	5.0		7.0	ns
t_r t_f	Output Rise/Fall 0.8 V to 2.0 V	CL = 50 pF			1.7 1.6			1.7 1.6			1.7 1.6	ns
f_{MAX}	Max Input Frequency	CL = 50 pF (Note 7)	65			65			65			MHz
t_S	Setup Time		0.75	0.50		0.75	0.50		0.75	0.50		ns
t_H	Hold Time		0.75	0.50		0.75	0.50		0.75	0.50		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Propagation delay measurement guaranteed for junction temperatures. Measurements performed at 50 MHz input frequency.
4. Skew window guaranteed for a single temperature across a $V_{CC} = V_T = V_E$ of 4.75 V to 5.25 V (See Application Note in this data sheet).
5. Skew window guaranteed for a single temperature and single $V_{CC} = V_T = V_E$
6. Output−to−output skew is specified for identical transitions through the device.
7. Frequency at which output levels will meet a 0.8 V to 2.0 V minimum swing.

Determining Skew for a Specific Application

The H641 has been designed to meet the needs of very low skew clock distribution applications. In order to optimize the device for this application special considerations are necessary in the determining of the part−to−part skew specification limits. Older standard logic devices are specified with relatively slack limits so that the device can be guaranteed over a wide range of potential environmental conditions. This range of conditions represented all of the potential applications in which the device could be used. The result was a specification limit that in the vast majority of cases was extremely conservative and thus did not allow for an optimum system design. For non−critical skew designs this practice is acceptable, however as the clock speeds of systems increase overly conservative specification limits can kill a design.

The following will discuss how users can use the information provided in this data sheet to tailor a part−to−part skew specification limit to their application. The skew determination process may appear somewhat tedious and time consuming, however if the utmost in performance is required this procedure is necessary. For applications which do not require this level of skew performance a generic part−to−part skew limit of 2.5 ns can be used. This limit is good for the entire ambient temperature range, the guaranteed V_{CC} (V_T, V_E) range and the guaranteed operating frequency range.

Temperature Dependence

A unique characteristic of the H641 data sheet is that the AC parameters are specified for a junction temperature rather than the usual ambient temperature. Because very few designs will actually utilize the entire commercial temperature range of a device a tighter propagation delay window can be established given the smaller temperature range. Because the junction temperature and not the ambient temperature is what affects the performance of the device the parameter limits are specified for junction temperature. In addition the relationship between the ambient and junction temperature will vary depending on the frequency, load and board environment of the application. Since these factors are all under the control of the user it is impossible to provide specification limits for every possible application. Therefore a baseline specification was established for specific junction temperatures and the information that follows will allow these to be tailored to specific applications.

Since the junction temperature of a device is difficult to measure directly, the first requirement is to be able to “translate” from ambient to junction temperatures. The standard method of doing this is to use the power dissipation of the device and the thermal resistance of the package. For a TTL output device the power dissipation will be a function of the load capacitance and the frequency of the output. The total power dissipation of a device can be described by the following equation:

P_D (watts) = I_{CC} (no load) * V_{CC} +
V_S * V_{CC} * f * C_L * # Outputs
where:
V_S= Output Voltage Swing = 3.0 V
f = Output Frequency
C_L = Load Capacitance
$I_{CC} = I_{EE} + I_{CCH}$

Figure 1 plots the I_{CC} versus Frequency of the H641 with no load capacitance on the output. Using this graph and the information specific to the application a user can determine the power dissipation of the H641.

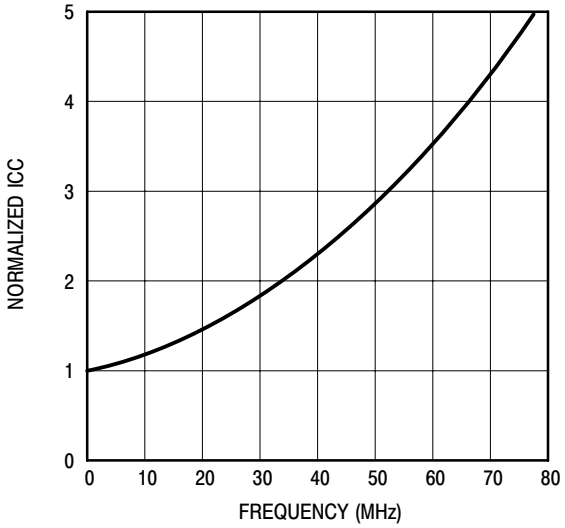


Figure 1. I_{CC} versus f (No Load)

Figure 2 illustrates the thermal resistance (in °C/W) for the PLCC−28 under various air flow conditions. By reading the thermal resistance from the graph and multiplying by the power dissipation calculated above the junction temperature increase above ambient of the device can be calculated.

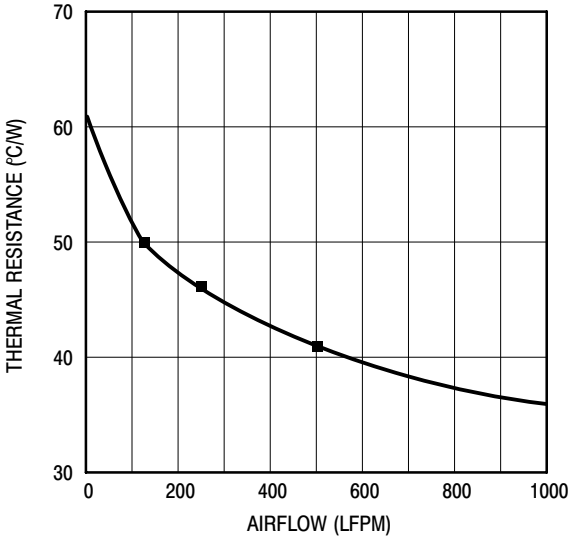


Figure 2. $\varnothing_{JA}$ versus Air Flow

Finally taking this value for junction temperature and applying it to Figure 3 allows the user to determine the

propagation delay for the device in question. A more common use would be to establish an ambient temperature range for the H641's in the system and utilize the above methodology to determine the potential increased skew of the distribution network. Note that for this information if the T_{PD} versus Temperature curve were linear the calculations would not be required. If the curve were linear over all temperatures a simple temperature coefficient could be provided.

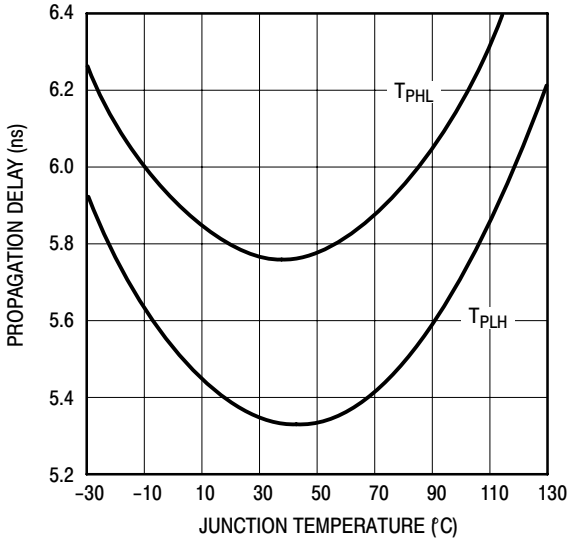


Figure 3. T_{PD} versus Junction Temperature

V_{CC} Dependence

TTL and CMOS devices show a significant propagation delay dependence with V_{CC}. Therefore the V_{CC} variation in a system will have a direct impact on the total skew of the clock distribution network. When calculating the skew between two devices on a single board it is very likely an assumption of identical V_{CC}'s can be made. In this case the number provided in the data sheet for part−to−part skew would be overly conservative. By using Figure 4 the skew given in the data sheet can be reduced to represent a smaller or zero variation in V_{CC}. The delay variation due to the specified V_{CC} variation is ≈±270 ps. Therefore, the 1 ns window on the data sheet can be reduced by 270 ps if the devices in question will always experience the same V_{CC}. The distribution of the propagation delay ranges given in the data sheet is actually a composite of three distributions whose means are separated by the fixed difference in propagation delay at the typical, minimum and maximum V_{CC}.

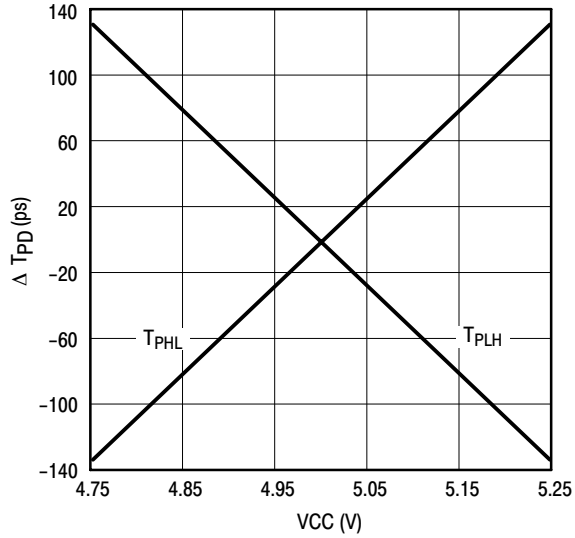


Figure 4. ΔT_{PD} versus V_{CC}

Capacitive Load Dependence

As with V_{CC} the propagation delay of a TTL output is intimately tied to variation in the load capacitance. The skew specifications given in the data sheet, of course, assume equal loading on all of the outputs. However situations could arise where this is an impossibility and it may be necessary to estimate the skew added by asymmetric loading. In addition the propagation delay numbers are provided only for 50 pF loads, thus necessitating a method of determining the propagation delay for alternative loads.

Figure 5 shows the relationship between the two propagation delays with respect to the capacitive load on the output. Utilizing this graph and the 50 pF limits the specification of the H641 can be mapped into a spec for either a different value load or asymmetric loads.

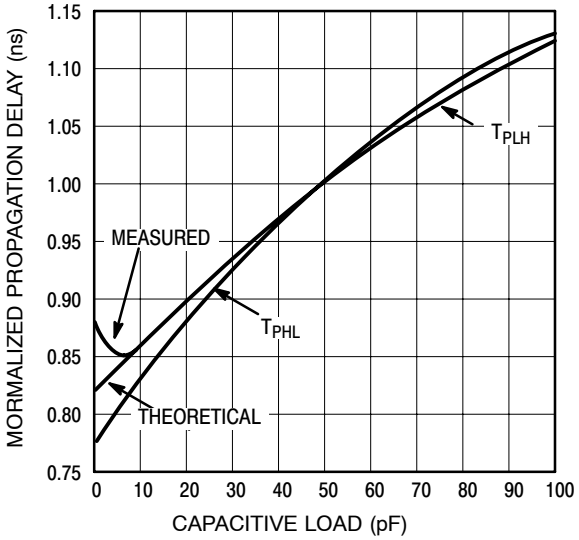


Figure 5. T_{PD} versus Load

Rise/Fall Skew Determination

The rise−to−fall skew is defined as simply the difference between the T_{PLH} and the T_{PHL} propagation delays. This skew for the H641 is dependent on the V_{CC} applied to the device. Notice from Figure 4 the opposite relationship of T_{PD} versus V_{CC} between T_{PLH} and T_{PHL}. Because of this the rise−to−fall skew will vary depending on V_{CC}. Since in all likelihood it will be impossible to establish the exact value for V_{CC}, the expected variation range for V_{CC} should be used. If this variation will be the ± 5% shown in the data sheet the rise−to−fall skew could be established by simply subtracting the fastest T_{PLH} from the slowest T_{PHL}; this exercise yields 1.41 ns. If a tighter V_{CC} range can be realized Figure 4 can be used to establish the rise−to−fall skew.

Specification Limit Determination Example

The situation pictured in Figure 6 will be analyzed as an example. The central clock is distributed to two different cards; on one card a single H641 is used to distribute the clock while on the second card two H641's are required to supply the needed clocks. The data sheet as well as the graphical information of this section will be used to calculate the skew between H641a and H641b as well as the skew between all three of the devices. Only the T_{PLH} will be analyzed, the T_{PHL} numbers can be found using the same technique. The following assumptions will be used:

- All outputs will be loaded with 50 pF
- All outputs will toggle at 30 MHz
- The V_{CC} variation between the two boards is ±3 %
- The temperature variation between the three devices is ±15°C around an ambient of 45°C.
- 500 lfpm air flow

The first task is to calculate the junction temperature for the devices under these conditions. Using the power equation yields:

P_D = I_{CC} (no load) * V_{CC} + V_{CC} * V_S * f * C_L * # outputs
=4.3 * 48m A * 5.0 V + 5.0 V * 3.0 V * 30 MHz * 50 pF * 9
=432 mW + 203 mW = 635 mW

Using the thermal resistance graph of Figure 2 yields a thermal resistance of 41°C/W which yields a junction temperature of 71°C with a range of 56°C to 86°C. Using the T_{PD} versus Temperature curve of Figure 3 yields a propagation delay of 5.42 ns and a variation of 0.19 ns.

Since the design will not experience the full ±5% V_{CC} variation of the data sheet the 1.0 ns window provided will be unnecessarily conservative. Using the curve of Figure 4 shows a delay variation due to a ±3% V_{CC} variation of ±0.075 ns. Therefore the 1.0 ns window can be reduced to 1.0 ns − (0.27 ns − 0.15 ns) = 0.88 ns. Since H641a and H641b are on the same board we will assume that they will always be at the same V_{CC}; therefore the propagation delay window will only be 1 ns − 0.27 ns = 0.73 ns.

Putting all of this information together leads to a skew between all devices of

0.19 ns + 0.88 ns

(temperature + supply, and inherent device),

while the skew between devices A and B will be only

0.19 ns + 0.73 ns

(temperature + inherent device only).

In both cases, the propagation delays will be centered around 5.42 ns, resulting in the following t_{PLH} windows:

T_{PLH} = 4.92 ns − 5.99 ns; 1.07 ns window (all devices)

T_{PLH}= 5.00 ns − 5.92 ns; 0.92 ns window (devices a & b)

Of course the output−to−output skew will be as shown in the data sheet since all outputs are equally loaded.

This process may seem cumbersome, however the delay windows, and thus skew, obtained are significantly better than the conservative worst case limits provided at the beginning of this note. For very high performance designs, this extra information and effort can mean the difference between going ahead with prototypes or spending valuable engineering time searching for alternative approaches.

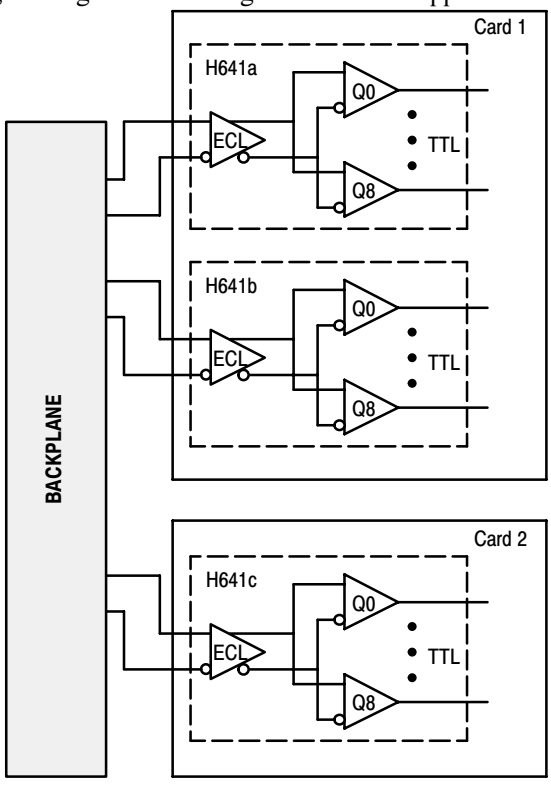


Figure 6. Example Application

ORDERING INFORMATION

Device	Package	Shipping†
MC10H641FN	PLCC−28	37 Units / Rail
MC10H641FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H641FNR2	PLCC−28	500 / Tape & Reel
MC10H641FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H641FN	PLCC−28	37 Units / Rail
MC100H641FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100H641FNR2	PLCC−28	500 / Tape & Reel
MC100H641FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

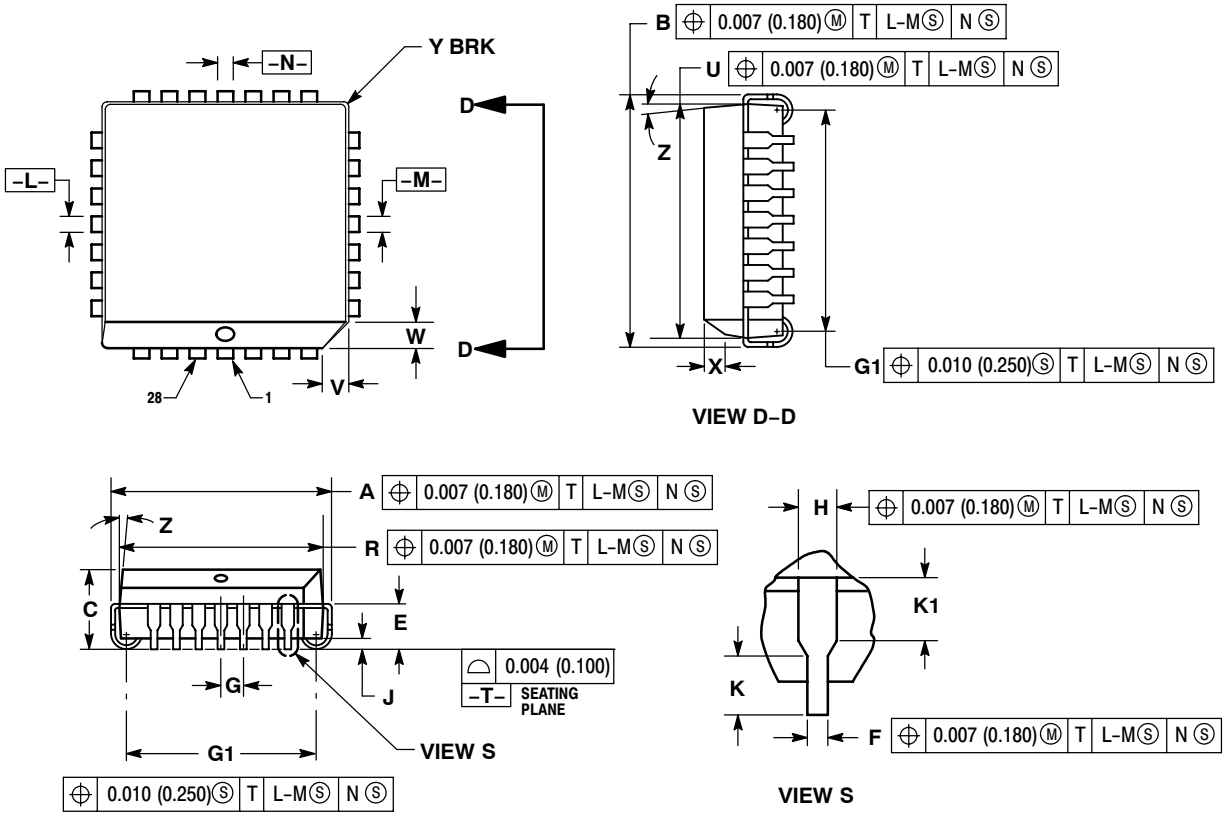
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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MECL 10H is a trademark of Motorola, Inc.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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MC10H640/D

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