THE DATASHEET OF

AOZ8105CI

AOZ8105CI

Ultra-Low Capacitance TVS Diode

General Description

The AOZ8105CI is a transient voltage suppressor array designed to protect high speed data lines such as HDMI and Gigabit Ethernet from damaging ESD events.

This device incorporates eight surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

The AOZ8105CI provides a typical line to line capacitance of 0.35pF and low insertion loss up to 3GHz providing greater signal integrity making it ideally suited for HDMI 1.3 applications, such as Digital TVs, DVD players, set-top boxes and mobile computing devices.

The AOZ8105CI comes in RoHS compliant, tiny SOT-23-6 package and is rated -40°C to +85°C junction temperature range.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - ±30kV (air discharge) and ±24kV (contact discharge)
  - IEC 61000-4-5 (Lightning) 3A (8/20μs)
  - Human Body Model (HBM) ±24kV
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects four I/O lines
- Low capacitance between I/O lines: 0.35pF
- Low clamping voltage
- Low operating voltage: 5.0V

Applications

- HDMI ports
- Monitors and flat panel displays
- Set-top box
- USB 2.0 power and data line protection
- Video graphics cards
- Digital Video Interface (DVI)
- 10/100/1000 Ethernet
- Notebook computers

Green Product

Typical Application

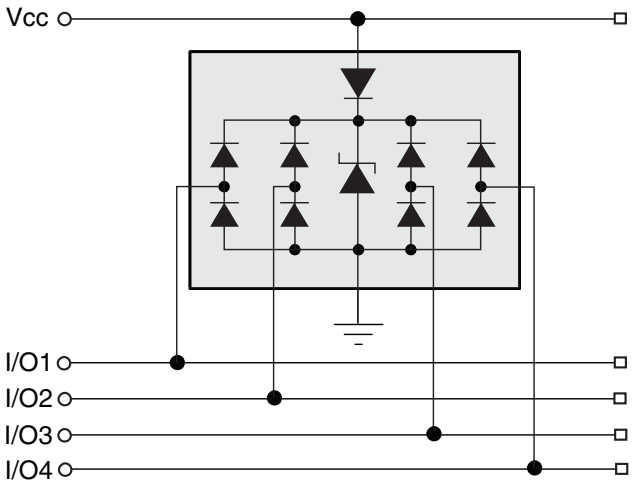


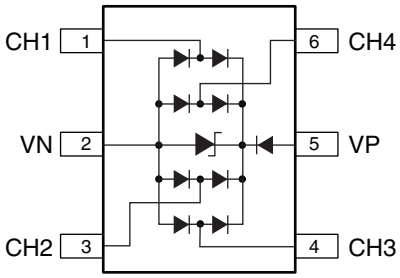
Figure 1. HDMI Ports

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8105CI	-40°C to +85°C	SOT-23-6	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



SOT23-6
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating per IEC61000-4-2, contact(1)	±24kV
ESD Rating per IEC61000-4-2, air(1)	±30kV
ESD Rating per Human Body Model(2)	±24kV

Notes:

1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40°C to +125°C

Electrical Characteristics

T_A = 25°C unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

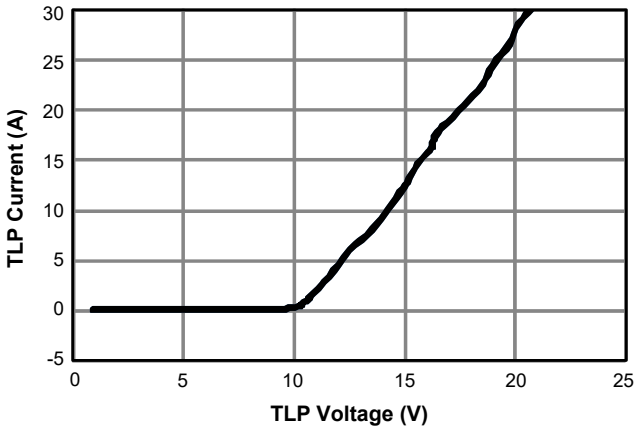
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between VP and VN[3]			5.5	V
V_{BR}	Reverse Breakdown Voltage	I_T = 1mA, between VP and VN[4]	6.6			V
I_R	Reverse Leakage Current	V_{RWM} = 5V, between VP and VN			1	µA
V_F	Diode Forward Voltage	I_F = 15mA	0.70	0.85	1	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 1A, tp = 100ns, any I/O pin to Ground[5]		 12 -1.4		 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 5A, tp = 100ns, any I/O pin to Ground[5]		 16.5 -2.8		 V V
C_j	Channel Input Capacitance	V_R = 0V, f = 1MHz, between I/O pins[6]		0.35		pF
		V_R = 0V, f = 1MHz, any I/O pin to Ground[6]		0.80	0.9	pF
		V_P = 5.0V, V_R = 2.5V, f = 1MHz, any I/O pins to Ground		0.43	0.5	pF
ΔC_j	Channel Input Capacitance Matching	V_R = 0V, f = 1MHz, between I/O pins			0.03	pF

Notes:

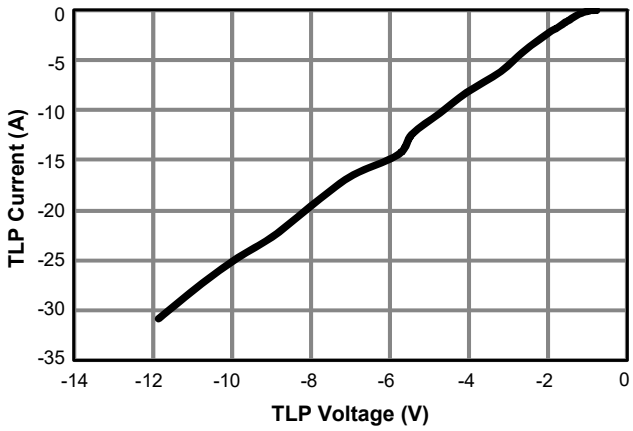
3. The working peak reverse voltage, V_{RWM}, should be equal to or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at the pulse test current I_T.
5. Measurements performed using a 100ns Transmission Line Pulse (TLP) system.
6. Measure performed with no external capacitor on V_P.

Typical Operating Characteristics

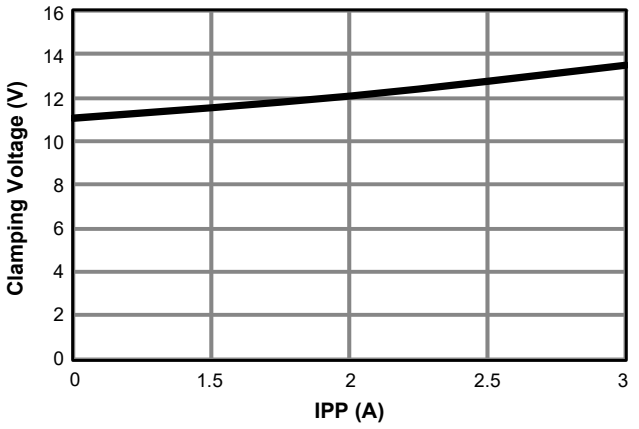
Positive Transmission Line Pulse (tp = 100ns, tr = 0.2ns)



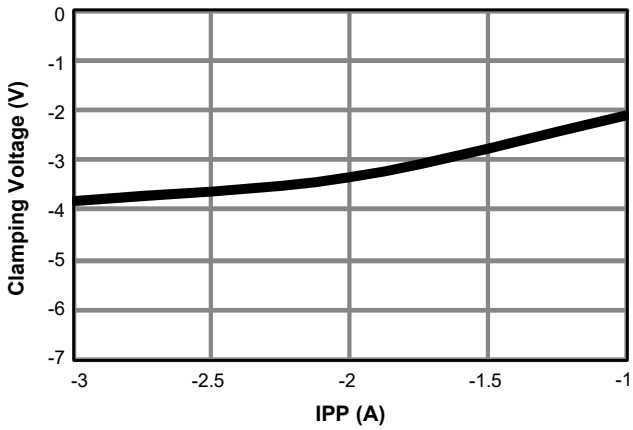
Negative Transmission Line Pulse (tp = 100ns, tr = 0.2ns)



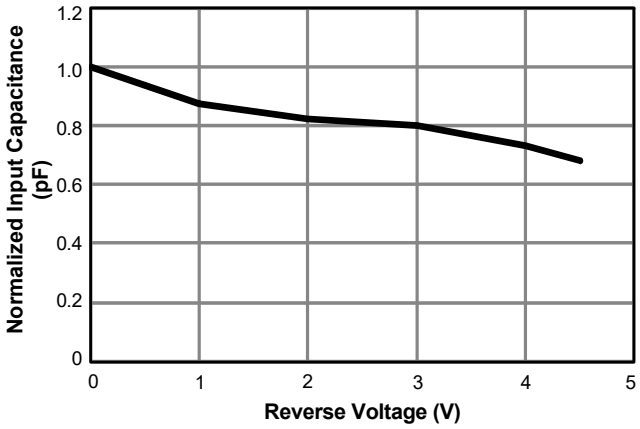
IEC61000-4-5 Positive Surge 8/20µs



IEC61000-4-5 Negative Surge 8/20µs



Typical Variation of CIN vs. VR (f = 1MHz, T = 25°C)



Application Information

The AOZ8105CI TVS is designed to protect four high speed data lines from ESD and transient over-voltage by clamping them to a fixed voltage. When the voltages on the protected lines exceed the limit, the internal steering diode are forward bias will conduct the harmful transient away from the sensitive circuitry. As system frequency increases, printed circuit board layout becomes more complex. A successful high speed board must integrate the device and traces while avoiding signal transmission problems associated with HDMI data speed.

VGA Ports

With VGA ports back-drive current is a concern for system instability, start ups and power loss. The back-drive current occurs when two systems are connected through a cable and one system is OFF and another system is ON. In this case the system that is ON is the monitor. The monitor can inject current into the system that is turned OFF via the cable. To inhibit the back-drive current from happening, an integrated diode is designed into the AOZ8105CI to prevent current from going into the system that is turned OFF. Figure 2 shows the schematics where the back-drive current is flowing in a system that is turned OFF.

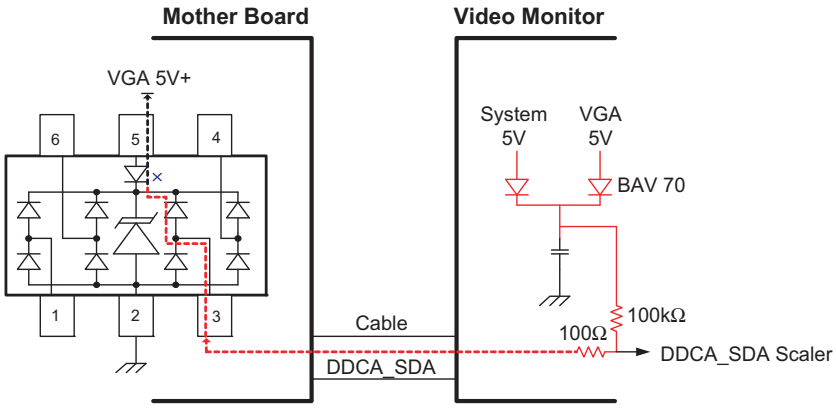


Figure 2. Back-Drive Current Path

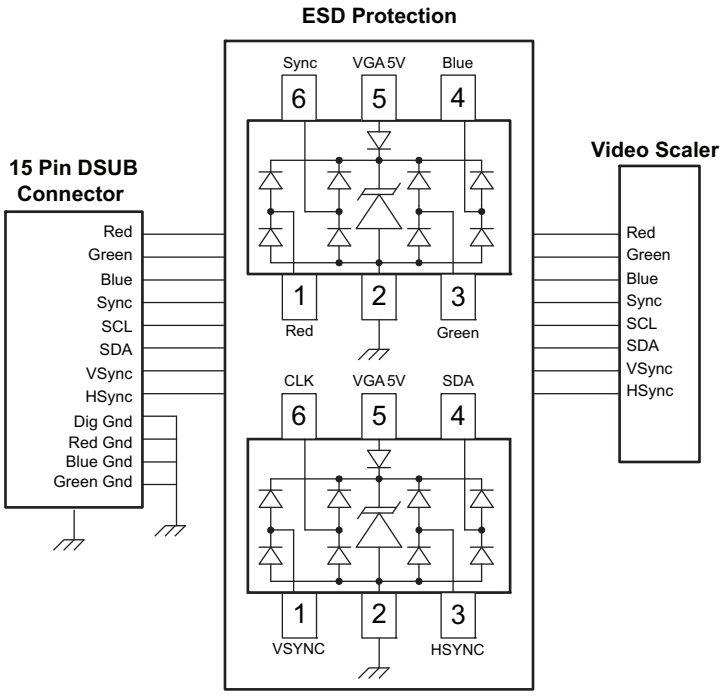


Figure 3. ESD Design for VGA Ports in which Two AOZ8105CI are Used

PCB Layout Example for VGA Port

Figure 4 shows an example for a VGA port with two AOZ8105CI being used. Place the AOZ8105CI device as close to the connector as possible. Use ground plane wherever to ensure maximum performance of the device.

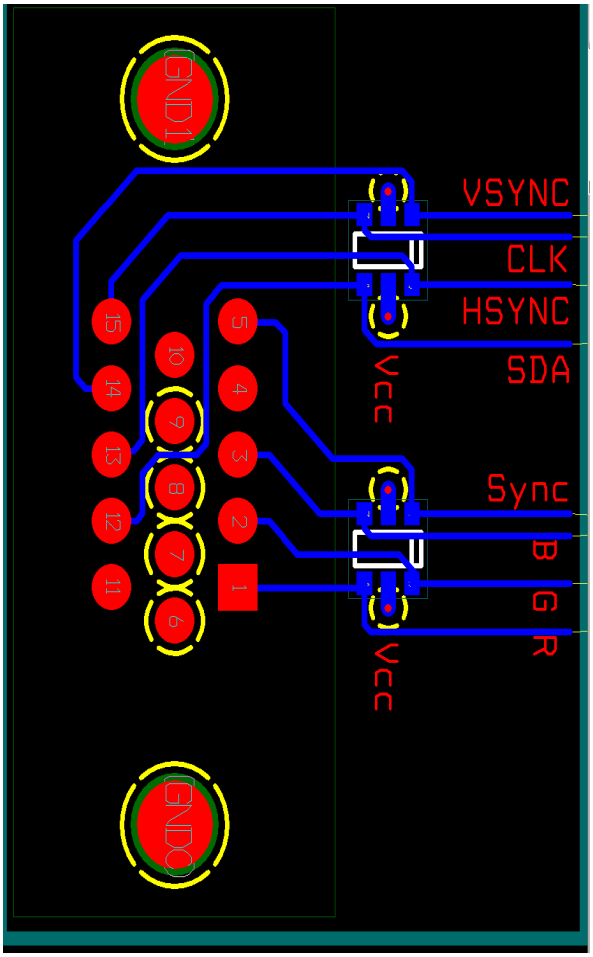


Figure 4. PCB Layout Example for VGA Port

High Speed HDMI PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8105CI devices should be located as close as possible to the noise source. The placement of the AOZ8105CI devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8105CI devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8105CI device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The AOZ8105CI ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The AOZ8105CI is designed for the ease of PCB layout by allowing the traces to run underneath the device. The pinout of the AOZ8105CI is design to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI) design without having to divert the signal lines that may add more parasitic inductance.

It is crucial that the layout is successful for a HDMI design PCB board. Some of the problems associated with high speed design are matching impedance of the traces and to minimize the crosstalk between parallel traces. This application note is to provide you as much information to successfully design a high speed PCB using Alpha & Omega devices.

The HDMI video signals are transmitted on a very high speed pair of traces and any amount of capacitance, inductance or even bends in a trace can cause the impedance of a differential pair to drop as much as 40Ω. This is not desirable because HDMI ports must maintain a 100Ω ±15% on each of the four pairs of its differential lines per HDMI Compliance Test Specifications. The HDMI CTS specifies that the impedance on the differential pair of a receiver must be measured using a Time Domain Reflectometry method with a pulse rise time of

≤200pS. The TDR measurements of the PCB traces allows to locate and model discontinuities cause by the geometrical features of a bend and by the frequency-dependant losses of the trace itself. These fast edge rates can contribute to noise and crosstalk, depending on the traces and PCB dielectric construction material.

Material selection is another aspect that determines good characteristic impedance in the lines. Different material will give you different results. The dielectric material will have the dielectric constant (ε_r).

Where Q_1, Q_2 = charges, r = distance between charges (m), F = force(N), ε = permittivity of dielectric (F/m).

$$F = \frac{Q_1 Q_2}{4\pi\varepsilon r^2} \quad (1)$$

Each PCB substrate has a different relative dielectric constant. The dielectric constant is the permittivity of a relative that of empty space. Where ε_r = dielectric constant, ε = permittivity, and ε_o = permittivity of empty space.

$$\varepsilon_r = \frac{\varepsilon}{\varepsilon_o} \quad (2)$$

The dielectric constant affects the impedance of a transmission line and can propagate faster in materials that have a lower ε_r. The frequency in your design will depend on the material being used. With equation 1 you can determine the type of material to use. If higher frequency is required other board material maybe considered. GETEK is another material that can be used in high speed boards. They have a typical ε_r between 3.6 to 4.0. The most common type of dielectric material used for PCB is FR-4. Typical dielectric constant for FR-4 is between 4.0 to 4.5. Most PCB manufacture will be able to give you the exact value of the FR-4 dielectric constant. Once you determined the dielectric constant of the board material you can start to calculate the impedance of each trace. Below are the formulas for a microstrip layout. This impedance is dependant on the width of the microstrip (W) the thickness (t) of the trace and the height (h) of the FR4 material, and (D) trace edge to edge spacing.

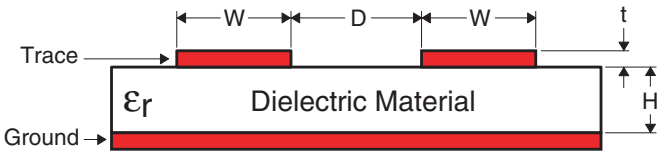


Figure 5. Dimensions of Microstrip Layout

Typical value of W = 12.6 mil, h = 10mils, D = 10mils, t = 1.4mils and ε_r = 4.0 with the equation below for a microstrip impedance yields:

$$Zo = \frac{87}{\sqrt{\varepsilon_r + 1.41}} = ln\left(\frac{5.98 \times h}{0.8W + t}\right) \quad (3)$$

$$Zo = 61.73\Omega$$

By solving for Zo you can calculate the differential impedance with the equation below.

$$Zdiff = 2 \times Zo\left(1 - 0.48e^{-0.96\frac{D}{h}}\right) \quad (4)$$

$$Zdiff = 100.77$$

Adjust the trace width, height, distance between the traces and FR4 thickness to obtain the desired 100Ω differential impedance. The general rule of thumb is to route the traces as short as possible, use differential routing strategies whenever feasible and match the length and bends to each of the differential traces.

The graphs below show the differential impedance with varying trace width without the package part on it. Each of the graphs and board layout represent changing trace width from 100Ω to 160Ω in increment of 20Ω.

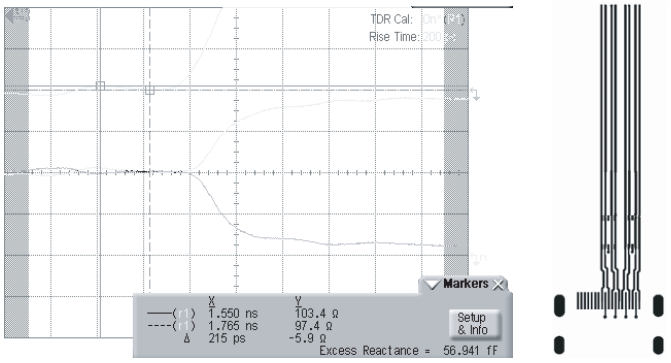


Figure 6. 100Ω Differential Impedance Max 103Ω, Min 97Ω

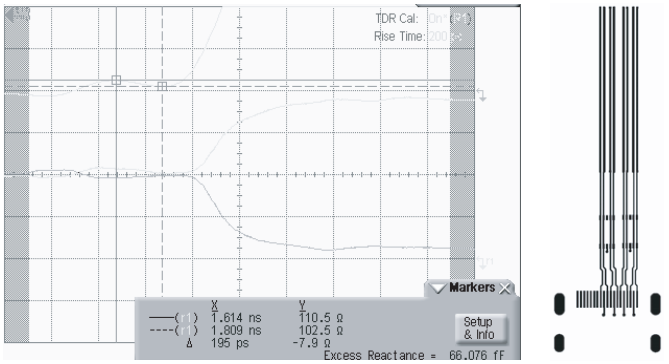


Figure 7. 120Ω Differential Impedance Max 110Ω, Min 102Ω

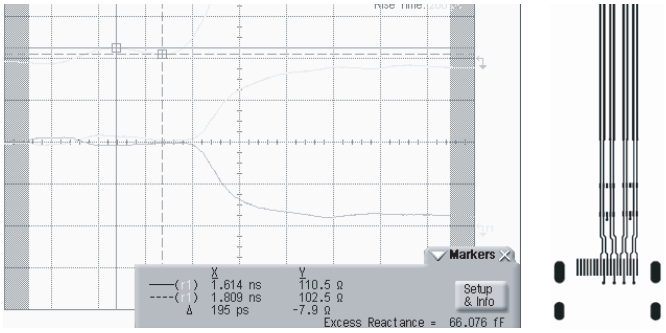


Figure 8. 140Ω Differential Impedance Max 102Ω, Min 92Ω

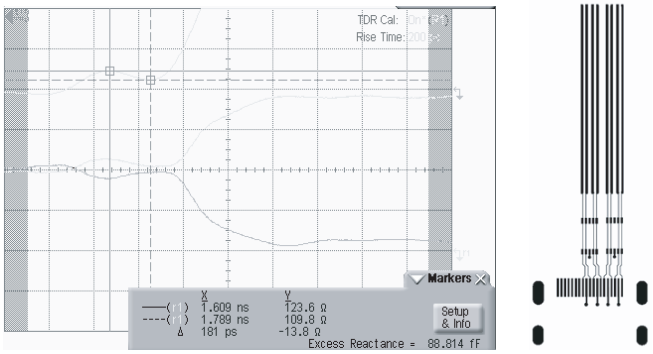


Figure 9. 160Ω Differential Impedance Max 123Ω, Min 109Ω

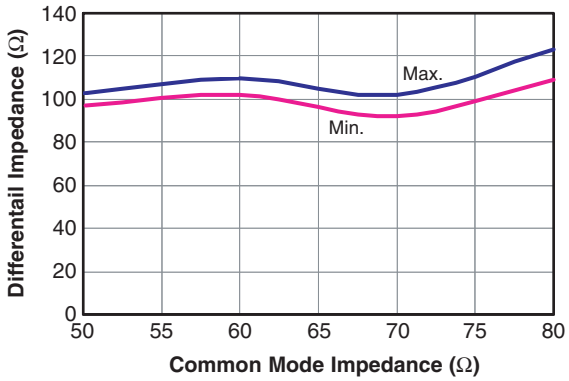


Figure 10. Differential Impedance

By adding a TVS onto the traces it can have a large effect on the impedance of the line. This addition of a capacitance added to a 100Ω differential transmission line without any compensation may decrease the impedance as much as 20Ω or more. Below is a formula to calculate the length for the compensation of $C_{(TVS)}$.

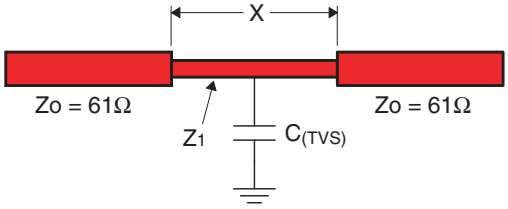


Figure 11. Impedance Compensation

$$K = \frac{Z_1}{Z_2} \quad (5)$$

$$X = \left(\frac{Z_0 C_{TVS}}{\tau}\right)\left(\frac{K}{K^2 - 1}\right) \quad (6)$$

Z_0 is the normal 61Ω differential impedance on the trace.

Z_1 is the need impedance to compensate for the added $C_{(TVS)}$

K is defined as the unloaded impedance of the adjusted trace.

X is the length of the trace needed for the compensation.

τ is the propagation delay time required for a signal to travel from one point to another. This value should be less than 200pS.

From the above method the designer should layout the boards with a 50Ω common mode trace. The result should give you approximately 100Ω differential impedance. Z_1 is the impedance that you choose in order to compensate the TVS capacitance. Based on Z_1 value, we can get the length of the segment from the above equations. With the value of Z_1 = 98Ω, Zo = 61Ω, $C_{(TVS)}$ = 0.7 and τ = 180. The X(mils) equates to 250 mils.

Page 9 has a series of graph that represent changing width and length of the trace from 100Ω to 160Ω in increment of 20Ω with a package solder onto the board. As you can observe from the graphs, a small incremental capacitance that is added to the differential lines can significantly decrease the differential impedance. Thus violated the HDMI specification of 100Ω±15%.

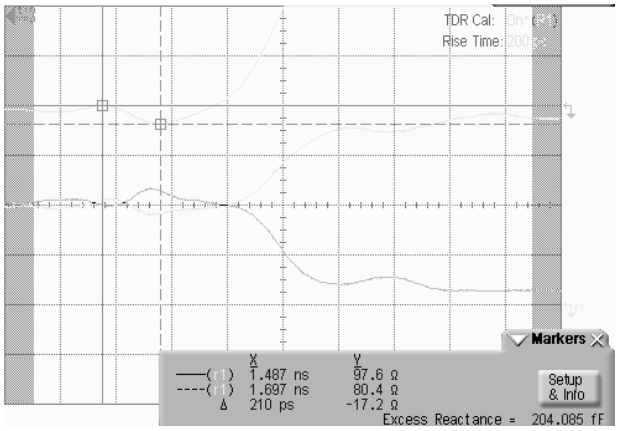


Figure 12. 100Ω Differential Impedance with Package on it Max. 97Ω, Min. 80Ω

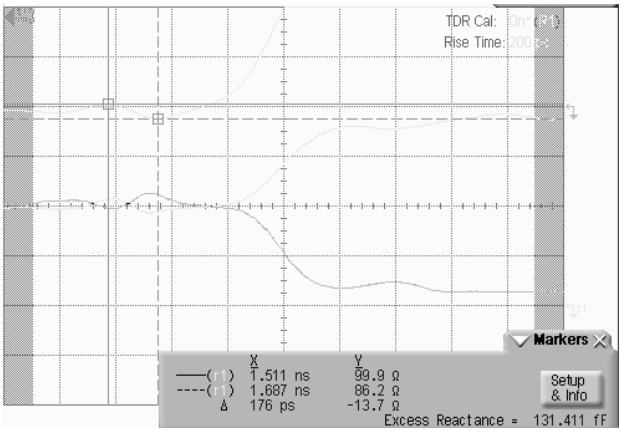


Figure 13. 120Ω Differential Impedance with Package on it Max. 99Ω, Min. 86Ω

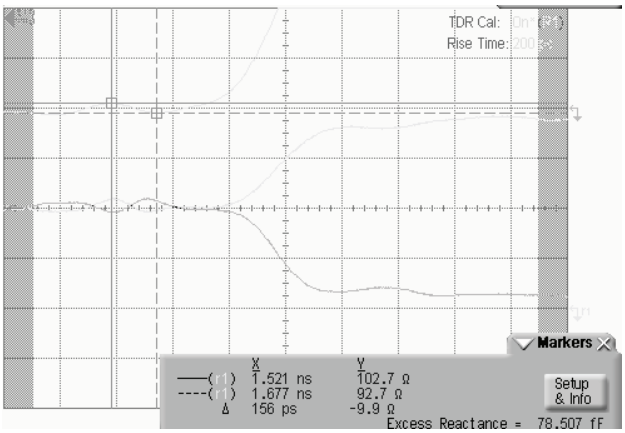


Figure 14. 140Ω Differential Impedance with Package on it Max. 102Ω, Min. 92Ω

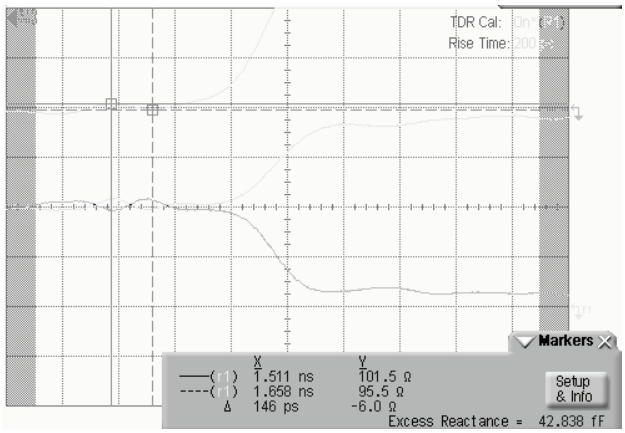


Figure 15. 160Ω Differential Impedance with Package on it Max. 101Ω, Min. 95Ω

From Figure 15 we are able to get the best result from using all of the equation above. With the value of Z_1 = 98Ω, Z_0 = 61Ω, $C_{(TVS)}$ = 0.7, τ = 180. The X(mils) equates to 250 mils to give the best compensated differential impedance on the traces for the added capacitance from the AOZ8105CI.

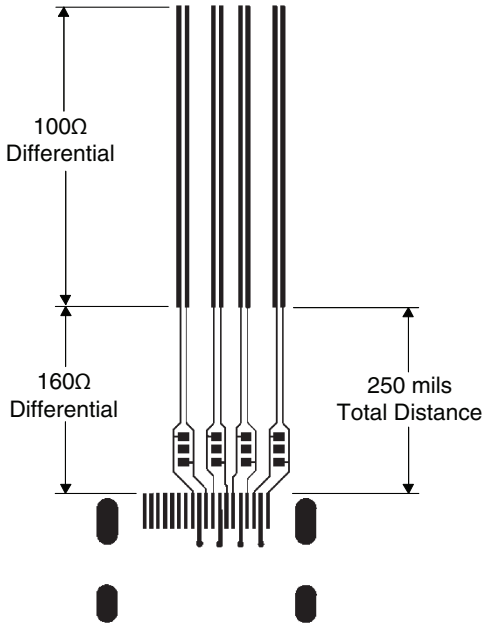


Figure 16. Recommended Layout for SOT-23 Package

Table 1. AOZ8105CI SOT-23-6 Evaluation Board Specifications

Number of layers	4
Copper Trace Thickness	1.4 mils
Dielectric Constant ε_r	4
Overall Board Thickness	62 mils
Dielectric thickness between top and ground layer	10 mils

Conclusion

This application section discusses ESD protection while maintaining the differential impedance of a HMDI sink device. Since the TVS add capacitance we must design the board to meet the HDMI requirements. This application note is a guideline to calculate and layout the PCB. Different board manufacture and process will fluctuate and will cause the final board to vary slightly. You must carefully plan out a successful high speed HDMI PCB. Factor such as PCB stack up, ground bounce, crosstalk and signal reflection can interfere with a signal. The layout, trace routing, board materials and impedance calculation discussed in this application note can help you design a more effective PCB.

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