THE DATASHEET OF

CDCM61004RHBT

CDCM61004 Four Output, Integrated VCO, Low-Jitter Clock Generator

1 Features

- One Crystal/LVCMOS Reference Input Including 24.8832 MHz, 25 MHz, and 26.5625 MHz
- Input Frequency Range: 21.875 MHz to 28.47 MHz
- On-Chip VCO Operates in Frequency Range of 1.75 GHz to 2.05 GHz
- 4x Output Available:
  - Pin-Selectable Between LVPECL, LVDS, or 2-LVCMOS; Operates at 3.3 V
- LVCMOS Bypass Output Available
- Output Frequency Selectable by /1, /2, /3, /4, /6, /8 from a Single Output Divider
- Supports Common LVPECL/LVDS Output Frequencies:
  - 62.5 MHz, 74.25 MHz, 75 MHz, 77.76 MHz, 100 MHz, 106.25 MHz, 125 MHz, 150 MHz, 155.52 MHz, 156.25 MHz, 159.375 MHz, 187.5 MHz, 200 MHz, 212.5 MHz, 250 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz, 625 MHz
- Supports Common LVCMOS Output Frequencies:
  - 62.5 MHz, 74.25 MHz, 75 MHz, 77.76 MHz, 100 MHz, 106.25 MHz, 125 MHz, 150 MHz, 155.52 MHz, 156.25 MHz, 159.375 MHz, 187.5 MHz, 200 MHz, 212.5 MHz, 250 MHz
- Output Frequency Range: 43.75 MHz to 683.264 MHz (See Table 4)
- Internal PLL Loop Bandwidth: 400 kHz
- High-Performance PLL Core:
  - Phase Noise typically at –146 dBc/Hz at 5-MHz Offset for 625-MHz LVPECL Output
  - Random Jitter typically at 0.509 ps, RMS (10 kHz to 20 MHz) for 625-MHz LVPECL Output
- Output Duty Cycle Corrected to 50% (± 5%)
- Low Output Skew of 30 ps on LVPECL Outputs
- Divider Programming Using Control Pins:
  - Two Pins for Prescaler/Feedback Divider
  - Three Pins for Output Divider
  - Two Pins for Output Select
- Chip Enable Control Pin Available
- 3.3-V Core and I/O Power Supply
- Industrial Temperature Range: –40°C to 85°C
- 5-mm × 5-mm, 32-pin, VQFN (RHB) Package
- ESD Protection Exceeds 2 kV (HBM)

2 Applications

- Low-Jitter Clock Driver for High-End Datacom Applications Including SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- Cost-Effective High-Frequency Crystal Oscillator Replacement

3 Description

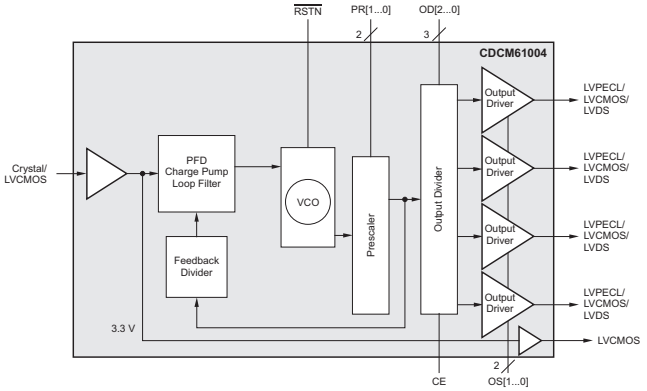
The CDCM61004 is a highly versatile, low-jitter frequency synthesizer capable of generating four low-jitter clock outputs, selectable between low-voltage positive emitter coupled logic (LVPECL), low-voltage differential signaling (LVDS), or low-voltage complementary metal oxide semiconductor (LVCMOS) outputs, from a low-frequency crystal of LVCMOS input for a variety of wireline and data communication applications. The CDCM61004 features an onboard PLL that can be easily configured solely through control pins. The overall output random jitter performance is less than 1 ps, RMS (from 10 kHz to 20 MHz), making this device a perfect choice for use in demanding applications such as SONET, Ethernet, Fibre Channel, and SAN. The CDCM61004 is available in a small, 32-pin, 5-mm × 5-mm VQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCM61004	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

CDCM61004 Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2011) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed input capacitance, only typical. ... 6
- Added Allowable Temperature Drift for Continuous PLL Lock parameter ... 7
- Changed on-chip load capacitance, only typical. ... 11
- Changed parisitic to parasitic. ... 17
- Added paragraph about temperature drift while locked. ... 18

Changes from Revision F (February 2011) to Revision G — **Page**

- Changed the On-Chip VCO section ... 18
- Changed Figure 15 ... 18
- Moved the LVCMOS INPUT INTERFACE section prior to the Output Divider section ... 18

Changes from Revision E (July 2010) to Revision F — **Page**

- Changed Note 1 of the Pin Functions table From: Pullup and Pull-down see...To: Pullup refers to ... 6
- Deleted $R_{PULLDOWN}$ from the Table 1 table ... 6
- Changed the text of Configuring the PLL, deleted the last sentence ... 16
- Changed the On-Chip VCO section ... 18
- Changed the Output Buffer section ... 19
- Changed values in row 24.75 of Table 3 ... 19
- Changed the power dissipation equation From: 610.5 mW – 4 × 50 mW = 41.7 mW To: 617.1 mW – 4 × 50 mW =

417.1 mW 28

- Deleted figure "Recommended PCB Layout for CDCM61001" from the Thermal Management section. Added text "See the mechanical data at the end of the data sheet.." 29

Changes from Revision D (February 2010) to Revision E **Page**

- Added LVCMOS reference to first Features bullet 1
- Added reference to LVCMOS input in *Description* 1
- Added reference to LVCMOS inputs in XIN parameter of Pin Functions table 6
- Changed name of *Control Pin LVCMOS Input Characteristics* section in Electrical Characteristics table 9
- Changed description of *Crystal Input Interface* section 16
- Changed description of *LVCMOS Input Interface* section 18

Changes from Revision C (July 2009) to Revision D **Page**

- Deleted references to *Single-Ended* and *LVCMOS input* throughout the document 1
- Deleted f_{IN}, $\Delta V/\Delta T$, and DutyREF parameters from Electrical Characteristics table 9
- Added *LVCMOS Input Interface* section 18

5 Description (Continued)

The CDCM61004 is a high-performance, low-phase noise, fully-integrated voltage-controlled oscillator (VCO) clock synthesizer with four universal output buffers that can be configured to be LVPECL, LVDS, or LVCMOS compatible. Each universal output can also be converted to two LVCMOS outputs. Additionally, an LVCMOS bypass output clock is available in an output configuration which can help with crystal loading to achieve an exact desired input frequency. It has one fully-integrated, low-noise, LC-based VCO that operates in the 1.75 GHz to 2.05 GHz range.

The phase-locked loop (PLL) synchronizes the VCO with respect to the input, which can either be a low-frequency crystal. The output share an output divider sourced from the VCO core. All device settings are managed through a control pin structure, which has two pins that control the prescaler and feedback divider, three pins that control the output divider, two pins that control the output type, and one pin that controls the output enable. Any time the PLL settings (including the input frequency, prescaler divider, or feedback divider) are altered, a reset must be issued through the Reset control pin (active low for device reset). The reset initiates a PLL recalibration process to ensure PLL lock. When the device is in reset, the outputs and dividers are turned off.

The output frequency (f_{OUT}) is proportional to the frequency of the input clock (f_{IN}). The feedback divider, output divider, and VCO frequency set f_{OUT} with respect to f_{IN}. For a configuration setting for common wireline and datacom applications, see Table 3. For other applications, use Equation 1 to calculate the exact crystal oscillator frequency required for the desired output.

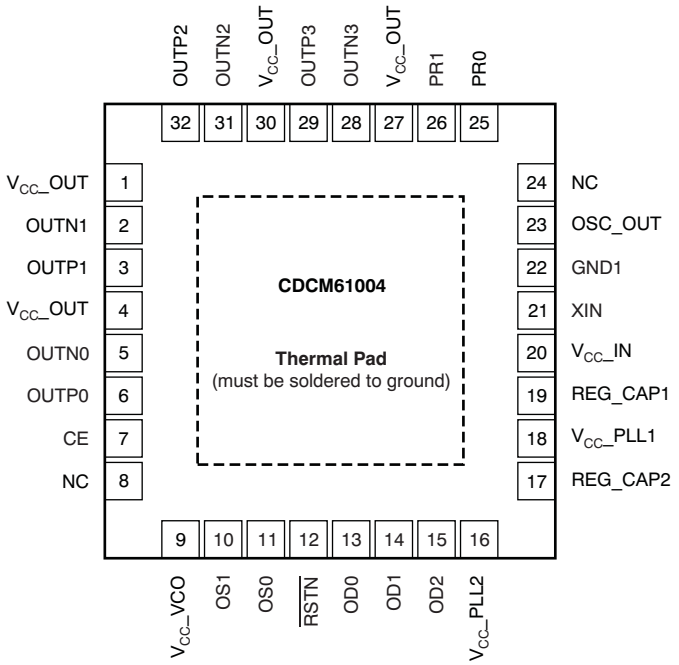
$$f_{IN} = \left(\frac{\text{Output Divider}}{\text{Feedback Divider}}\right) f_{OUT} \quad (1)$$

The output divider can be chosen from 1, 2, 3, 4, 6, or 8 through the use of control pins. Feedback divider and prescaler divider combinations can be chosen from 25 and 3, 24 and 3, 20 and 4, or 15 and 5, respectively, also through the use of control pins. *CDCM61004 Block Diagram* shows a high-level diagram of the CDCM61004.

The device operates in a 3.3-V supply environment and is characterized for operation from –40°C to 85°C.

6 Pin Configuration and Functions

RHB Package
32-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DIRECTION (1)	DESCRIPTION
NAME	NO.			
CE	7	Input	Pullup	Chip enable control pin (see Table 8)
GND1	22	Ground	—	Additional ground for device. (GND1 shorted on-chip to GND)
GND	Pad	Ground	—	Ground is on thermal pad. See *Thermal Management*
NC	8, 24	—	—	No connection
OD2, OD1, OD0	15, 14, 13	Input	Pullup	Output divider control pins (see Table 6)
OS1, OS0	10, 11	Input	Pullup	Output type select control pin (see Table 7)
OSC_OUT	23	Output	—	Bypass LVCMOS output
OUTP0, OUTN0	6, 5	Output	—	Differential output pair or two single-ended outputs
OUTP1, OUTN1	3, 2	Output	—	Differential output pair or two single-ended outputs
OUTP2, OUTN2	32, 31	Output	—	Differential output pair or two single-ended outputs
OUTP3, OUTN3	29, 28	Output	—	Differential output pair or two single-ended outputs
PR1, PR0	26, 25	Input	Pullup	Prescaler and Feedback divider control pins (see Table 5)
REG_CAP1	19	Output	—	Capacitor for internal regulator (connect to a 10-µF Y5V capacitor to GND)
REG_CAP2	17	Output	—	Capacitor for internal regulator (connect to a 10-µF Y5V capacitor to GND)
$\overline{\text{RSTN}}$	12	Input	Pullup	Device reset (active low) (see Table 9)
VCC_OUT	1, 4, 27, 30	Power	—	3.3-V supply for the output buffers
VCC_PLL1	18	Power	—	3.3-V supply for the PLL circuitry
VCC_PLL2	16	Power	—	3.3-V supply for the PLL circuitry
VCC_VCO	9	Power	—	3.3-V supply for the internal VCO
VCC_IN	20	Power	—	3.3-V supply for the input buffers
XIN	21	Input	—	Parallel resonant crystal or LVCMOS inputs

(1) *Pullup* refers to internal input resistors; see Table 1, *Pin Characteristics* for typical values.

Table 1. Pin Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance		10		pF
R_{PULLUP}	Input pullup resistor		150		kΩ

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

PARAMETER			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC_OUT}, V_{CC_PLL1}, V_{CC_PLL2}, V_{CC_VCO}, V_{CC_IN}	–0.5	4.6	V
VIN	Input voltage(3)		–0.5	V_{CC_IN} + 0.5	V
VOUT	Output voltage range(3)		–0.5	V_{CC_OUT} + 0.5	V
IN	Input current		–20	20	mA
IOUT	Output current		–50	50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All supply voltages must be supplied simultaneously.
(3) Input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{CC_OUT}	Output supply voltage	3	3.3	3.6	V
V_{CC_PLL1}	PLL supply voltage	3	3.3	3.6	V
V_{CC_PLL2}	PLL supply voltage	3	3.3	3.6	V
V_{CC_VCO}	On-chip VCO supply voltage	3	3.3	3.6	V
V_{CC_IN}	Input supply voltage	3	3.3	3.6	V
T_A	Ambient temperature	–40		85	°C
$\lvert T_{CL} \rvert$	Allowable temperature drift for continuous PLL lock(1)			100	°C

(1) The maximum allowable temperature drift for continuous lock is how far the temperature can drift in either direction from the value it was at the time when the On-Chip VCO was calibrated with the condition that the PLL stays in lock throughout the temperature drift. The internal VCO calibration takes place at device start-up and when the device is reset using the $\overline{RSTN}$ pin. A more detailed description can be found in *On-Chip VCO* and *Start-Up Time Estimation*.This implies the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable temperature drift for continuous lock, then it is necessary to re-calibrate the VCO to ensure the PLL stays in lock. Regardless of what temperature the part was initially calibrated at, the temperature can never drift outside the ambient temperature range of –40 °C to 85 °C.

7.4 Thermal Information

THERMAL METRIC[1]		CDCM61004 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	0.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.12	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At V_{CC} = 3 V to 3.6 V and T_A = –40°C to 85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL PIN LVCMOS INPUT CHARACTERISTICS						
V_{IH}	Input high voltage		0.6 V_{CC}			V
V_{IL}	Input low voltage				0.4 V_{CC}	V
I_{IH}	Input high current	V_{CC} = 3.6 V, V_{IL} = 0 V			200	µA
I_{IL}	Input low current	V_{CC} = 3 V, V_{IH} = 3.6 V			–200	µA
LVCMOS OUTPUT CHARACTERISTICS(1) (See Figure 7 and Figure 8)						
f_{OSC_OUT}	Bypass output frequency		21.875		28.47	MHz
f_{OUT}	Output frequency		43.75		250	MHz
V_{OH}	Output high voltage	V_{CC} = min to max, I_{OH} = –100 µA	V_{CC} –0.5			V
V_{OL}	Output low voltage	V_{CC} = min to max, I_{OL} = 100 µA			0.3	V
t_{RJIT}	RMS phase jitter	250 MHz (10 kHz to 20 MHz)			0.85	ps, RMS
$t_{SLEW-RATE}$	Output rise/fall slew rate	20% to 80%	2.4			V/ns
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				60	ps
I_{CC}, LVCMOS	Device current, LVCMOS	f_{IN} = 25 MHz, f_{OUT} = 250 MHz, C_L = 5 pF		175	205	mA
LVPECL OUTPUT CHARACTERISTICS(2) (See Figure 9 and Figure 10)						
f_{OUT}	Output frequency		43.75		683.264	MHz
V_{OH}	Output high voltage		V_{CC} –1.18		V_{CC} –0.73	V
V_{OL}	Output low voltage		V_{CC} –2		V_{CC} –1.55	V
$\|V_{OD}\|$	Differential output voltage		0.6		1.23	V
t_{RJIT}	RMS phase jitter	625 MHz (10 kHz to 20 MHz)			0.77	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%			175	ps
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				30	ps
I_{CC}, LVPECL	Device current, LVPECL	f_{IN} = 25 MHz, f_{OUT} = 625 MHz		180	215	mA
LVDS OUTPUT CHARACTERISTICS(3) (See Figure 11 and Figure 12)						
f_{OUT}	Output frequency		43.75		683.264	MHz
$\|V_{OD}\|$	Differential output voltage		0.247		0.454	V
ΔV_{OD}	V_{DD} magnitude change				50	mV
V_{OS}	Common-mode voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} magnitude change				50	mV
t_{RJIT}	RMS phase jitter	625 MHz (10 kHz to 20 MHz)			0.73	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%			255	ps
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				40	ps
I_{CC}, LVDS	Device current, LVDS	f_{IN} = 25 MHz, f_{OUT} = 625 MHz		150	195	mA

(1) Figure 7 and Figure 8 show DC and AC test setups, respectively. Jitter measurements made using 25-MHz quartz crystal inches.
(2) Figure 9 and Figure 10 show DC and AC test setups, respectively. Jitter measurements made using 25-MHz quartz crystal inches.
(3) Figure 11 and Figure 12 show DC and AC test setups, respectively. Jitter measurements made using 25-MHz quartz crystal inches.

7.6 Typical Output Phase Noise Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
250-MHz LVCMOS OUTPUT(1) (See Figure 8)						
phn_{100}	Phase noise at 100-Hz offset			–95		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset			–110		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset			–117		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset			–120		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset			–135		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset			–148		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset			–148		dBc/Hz
t_{RJIT}	RMS phase jitter from 10 kHz to 20 MHz			544		fs, RMS
t_{PJIT}	Total period jitter			27.4		ps, PP
$t_{STARTUP}$	Start-up time, power supply ramp time of 1 ms, final frequency accuracy of ±10 ppm			2.25		ms
625-MHz LVPECL OUTPUT(2) (See Figure 10)						
phn_{100}	Phase noise at 100-Hz offset			–81		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset			–101		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset			–109		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset			–112		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset			–129		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset			–146		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset			–146		dBc/Hz
t_{RJIT}	RMS phase jitter from 10 kHz to 20 MHz			509		fs, RMS
t_{PJIT}	Total period jitter			26.9		ps, PP
$t_{STARTUP}$	Start-up time, power supply ramp time of 1 ms, final frequency accuracy of ±10 ppm			2.25		ms
625-MHz LVDS OUTPUT(3) (See Figure 12)						
phn_{100}	Phase noise at 100-Hz offset			–88		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset			–102		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset			–109		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset			–112		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset			–129		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset			–146		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset			–146		dBc/Hz
t_{RJIT}	RMS phase jitter from 10 kHz to 20 MHz			510		fs, RMS
t_{PJIT}	Total period jitter			27		ps, PP
$t_{STARTUP}$	Start-up time, power supply ramp time of 1 ms, final frequency accuracy of ±10 ppm			2.25		ms

(1) Figure 8 shows test setup and uses 25-MHz quartz crystal in, V_{CC} = 3.3 V, and T_A = 25°C.
(2) Figure 10 shows test setup and uses 25-MHz quartz crystal in, V_{CC} = 3.3 V, and T_A = 25°C.
(3) Figure 12 shows test setup and uses 25-MHz quartz crystal in, V_{CC} = 3.3 V, and T_A = 25°C.

7.7 Typical Output Jitter Characteristics(1)

OUTPUT FREQUENCY (MHz)	INPUT (MHz)	LVCMOS OUTPUT		LVPECL OUTPUT		LVDS OUTPUT	
		t_{RJIT} (fs, RMS)	t_{PJIT} (ps_{PP})	t_{RJIT} (fs, RMS)	t_{PJIT} (ps_{PP})	t_{RJIT} (fs, RMS)	t_{PJIT} (ps_{PP})
62.5	25	592	32.9	611	20.7	667	28.4
75	25	518	27.5	533	19.4	572	25.7
77.76	24.8832	506	29.2	526	20.9	567	26.9
100	25	507	24.5	510	20.7	533	26.5
106.25	26.5625	535	23.5	524	20.2	553	26.5
125	25	557	39.6	556	21.4	570	27.1
150	25	518	38.4	493	18.9	515	26.2
155.52	24.8832	498	36.9	486	19.8	502	26.7
156.25	25	510	37.7	503	20.7	518	26.5
159.375	26.5625	535	37.4	510	19.9	534	26.3
187.5	25	506	32.8	506	20.3	509	25.5
200	25	491	23.3	492	30	499	34.9
212.5	26.5625	520	47.8	509	30.8	530	37.3
250	25	544	27.4	541	21.4	550	27.5
311.04	24.8832			481	20.5	496	24.7
312.5	25			501	20.8	508	25.8
622.08	24.8832			492	27.2	500	27.2
625	25			515	26.9	509	27

(1) Figure 8, Figure 10, and Figure 12 show LVCMOS, LVPECL, and LVDS test setups (respectively) using appropriate quartz crystal in, V_{CC} = 3.3 V, and T_A = 25°C.

7.8 Crystal Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Mode of oscillation		Fundamental		MHz
Frequency	21.875		28.47	MHz
Equivalent series resistance (ESR)			50	Ω
On-chip load capacitance		8	10	pF
Drive level	0.1		1	mW
Maximum shunt capacitance			7	pF

7.9 Dissipation Ratings(1)(2)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			4 × 4 VIAS ON PAD	
θ_{JA}	Thermal resistance, junction-to-ambient	0 LFM	35	°C/W
θ_{JP}(3)	Thermal resistance, junction-to-pad		4	°C/W

(1) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).
(2) Connected to GND with nine thermal vias (0.3-mm diameter).
(3) θ_{JP} (junction-to-pad) is used for the VQFN package, because the primary heat flow is from the junction to the GND pad of the VQFN package.

7.10 Typical Characteristics

Over operating free-air temperature range (unless otherwise noted).

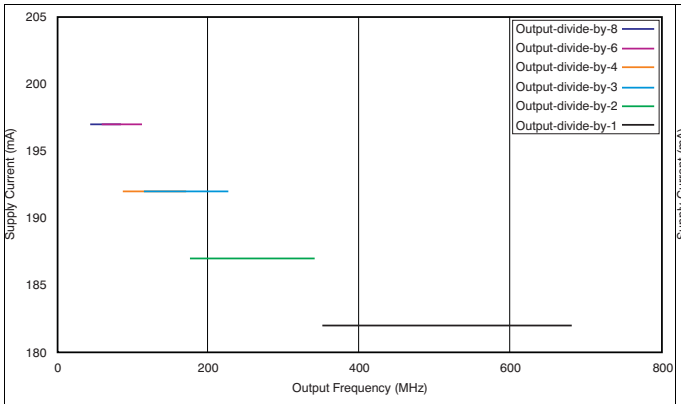


Figure 1. Typical Current Consumption for LVPECL Output vs Output Frequency

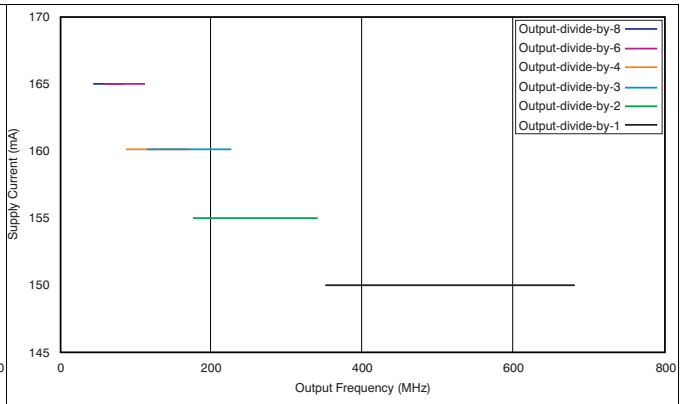


Figure 2. Typical Current Consumption for LVDS Output vs Output Frequency

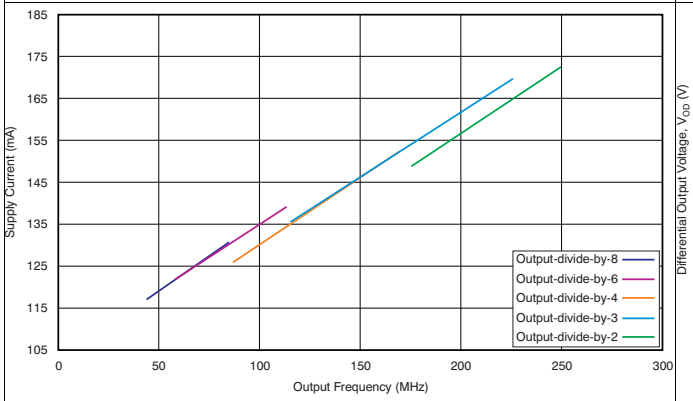


Figure 3. Typical Current Consumption for LVCMOS Output With 5-pF Load vs Output Frequency

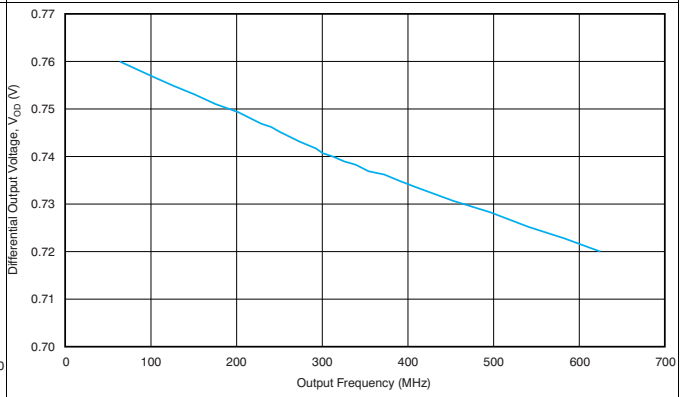


Figure 4. Typical LVPECL Differential Output Voltage vs Output Frequency

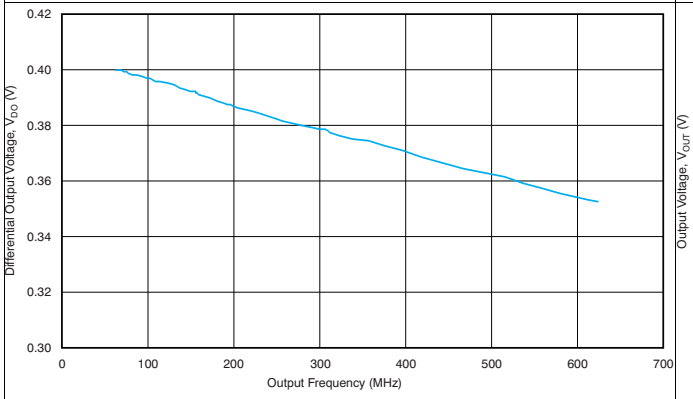


Figure 5. Typical LVDS Differential Output Voltage vs Output Frequency

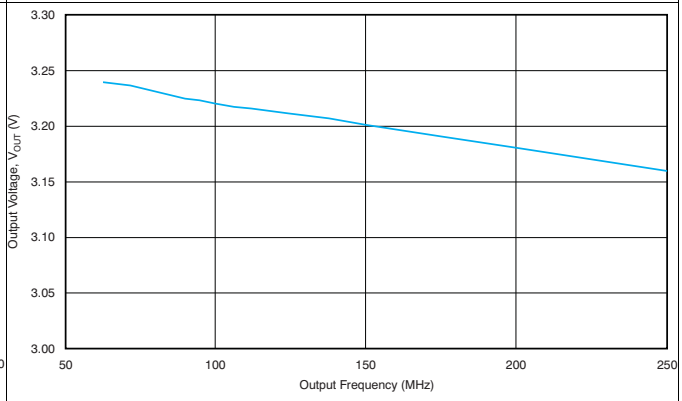


Figure 6. Typical LVCMOS Output Voltage With 5-pF Load vs Output Frequency

8 Parameter Measurement Information

This section describes the function of each block for the CDCM61004. Figure 7 through Figure 13 illustrate how the device should be set up for a variety of output configurations.

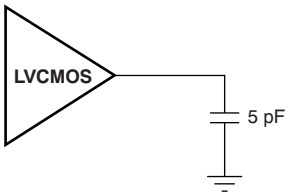


Figure 7. LVCMOS Output Loading During Device Test

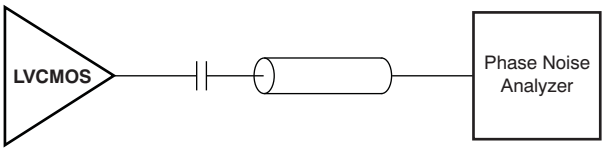


Figure 8. LVCMOS AC Configuration During Device Test

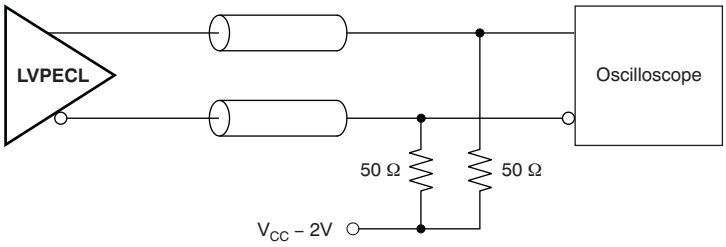


Figure 9. LVPECL DC Configuration During Device Test

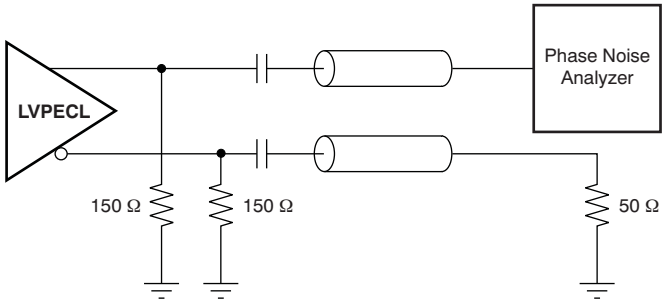


Figure 10. LVPECL AC Configuration During Device Test

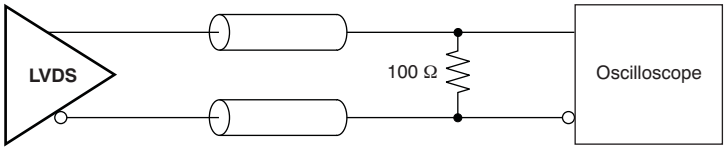


Figure 11. LVDS DC Configuration During Device Test

Parameter Measurement Information (continued)

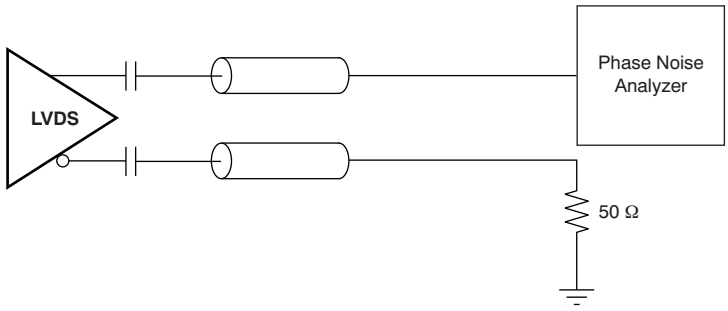


Figure 12. LVDS AC Configuration During Device Test

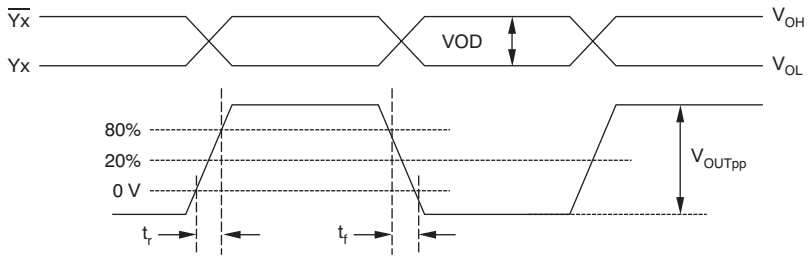


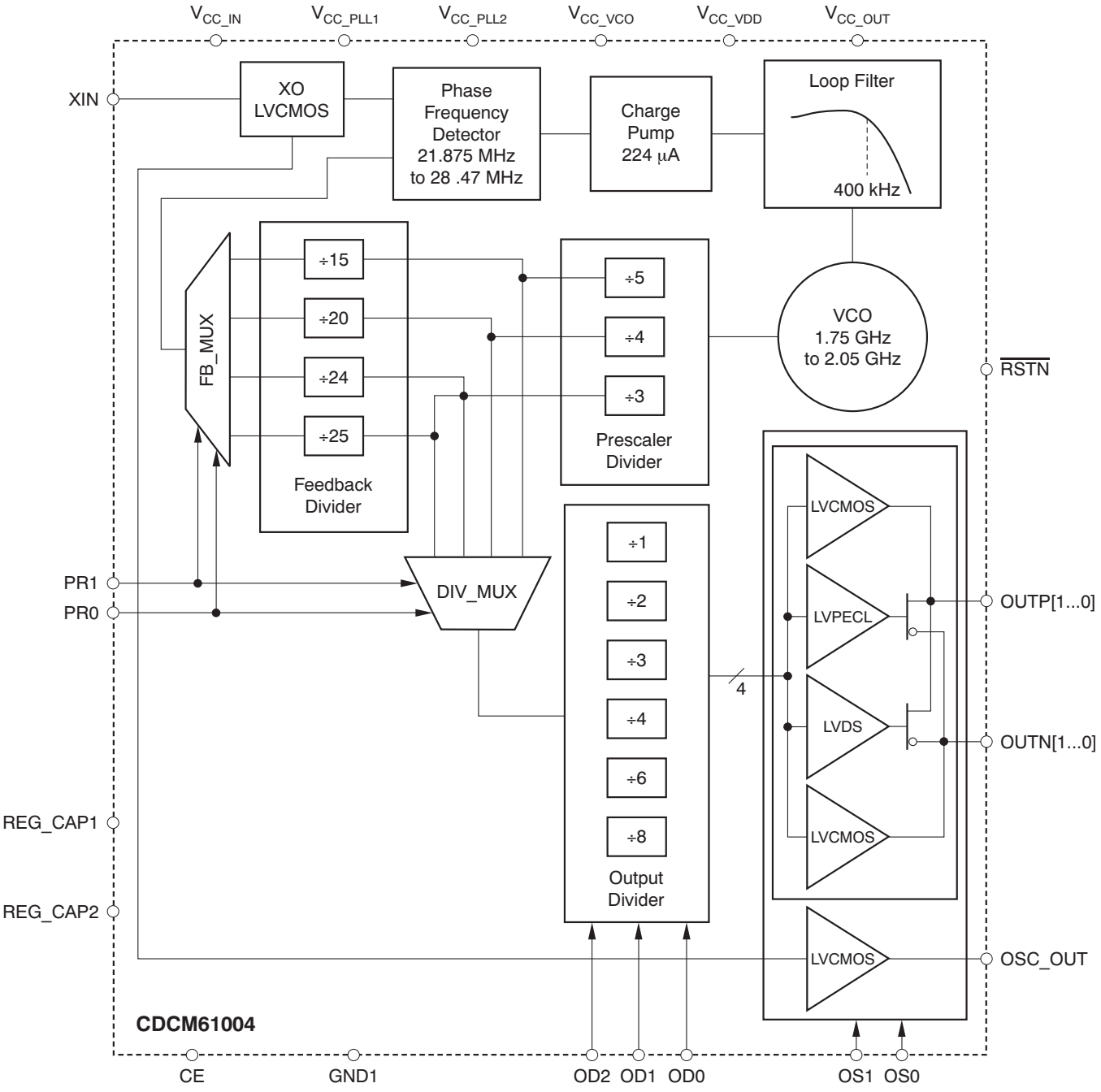
Figure 13. Output Voltage and Rise and Fall Times

9 Detailed Description

9.1 Overview

The CDCM61004 is a high-performance PLL that generates 4 copies of commonly used reference clocks with less than 1 ps, RMS jitter from a low-cost crystal.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Phase-Locked Loop (PLL)

The CDCM61004 includes an on-chip PLL with an on-chip VCO. The PLL blocks consist of a crystal input interface, which can also accept an LVCMOS signal, a phase frequency detector (PFD), a charge pump, an on-chip loop filter, and prescaler and feedback dividers. Completing the CDCM61004 device are the output divider and universal output buffer.

The PLL is powered by on-chip, low-dropout (LDO) linear voltage regulators. The regulated supply network is partitioned such that the sensitive analog supplies are powered from separate LDOs rather than the digital supplies which use a separate LDO regulator. These LDOs provide isolation for the PLL from any noise in the external power-supply rail. The REG_CAP1 and REG_CAP2 pins should each be connected to ground by 10-µF capacitors to ensure stability.

9.3.2 Configuring the PLL

The CDCM61004 permits PLL configurations to accommodate the various input and output frequencies listed in Table 3 and Table 4. These configurations are accomplished by setting the prescaler divider, feedback divider and output divider. The various dividers are managed by setting the device control pins as shown in Table 5 and Table 6.

9.3.3 Crystal Input Interface

Fundamental mode is the recommended oscillation mode of operation for the input crystal and parallel resonance is the recommended type of circuit for the crystal.

A crystal load capacitance refers to all capacitances in the oscillator feedback loop. It is equal to the amount of capacitance seen between the terminals of the crystal in the circuit. For parallel resonant mode circuits, the correct load capacitance is necessary to ensure the oscillation of the crystal within the expected parameters.

The CDCM61004 implements an input crystal oscillator circuitry, known as the *Colpitts oscillator*, and requires one pad of the crystal to interface with the XIN pin; the other pad of the crystal is tied to ground. In this crystal interface, it is important to account for all sources of capacitance when calculating the correct value for the discrete capacitor component, C_L, for a design.

The CDCM61004 has been characterized with 10-pF parallel resonant crystals. The input crystal oscillator stage in the CDCM61004 is designed to oscillate at the correct frequency for all parallel resonant crystals with low-pull capability and rated with a load capacitance that is equal to the sum of the onchip load capacitance at the XIN pin (10-pF), crystal stray capacitance, and board parasitic capacitance between the crystal and XIN pin.

The normalized frequency error of the crystal, as a result of load capacitance mismatch, can be calculated as Equation 2:

$$\frac{\Delta f}{f} = \frac{C_S}{2(C_{L,R} + C_O)} - \frac{C_S}{2(C_{L,A} + C_O)} \quad (2)$$

where

- C_S is the motional capacitance of the crystal,
- C_0 is the shunt capacitance of the crystal,
- $C_{L,R}$ is the rated load capacitance for the crystal,
- $C_{L,A}$ is the actual load capacitance in the implemented PCB for the crystal,
- Δf is the frequency error of the crystal,
- and f is the rated frequency of the crystal.
- The first three parameters can be obtained from the crystal vendor.

To minimize the frequency error of the crystal to meet application requirements, the difference between the rated load capacitance and the actual load capacitance should be minimized and a crystal with low-pull capability (low C_S) should be used.

Feature Description (continued)

For example, if an application requires less than ±50-ppm frequency error and a crystal with less than ±50-ppm frequency tolerance is picked, the characteristics are as follows: C_0 = 7 pF, C_S = 10 fF, and $C_{L,R}$ = 12 pF. In order to meet the required frequency error, calculate $C_{L,A}$ using Equation 2 to be 17 pF. Subtracting $C_{L,R}$ from $C_{L,A}$, results in 5 pF; take care during printed-circuit-board (PCB) layout with the crystal and the CDCM61004 to ensure that the sum of the crystal stray capacitance and board parasitic capacitance is less than the calculated 5 pF.

Good layout practices are fundamental to the correct operation and reliability of the oscillator. It is critical to locate the crystal components very close to the XIN pin to minimize routing distances. Long traces in the oscillator circuit are a very common source of problems. Do not route other signals across the oscillator circuit. Also, make sure power and high-frequency traces are routed as far away as possible to avoid crosstalk and noise coupling. Avoid the use of vias; if the routing becomes very complex, it is much better to use 0-Ω resistors as bridges to go over other signals. Vias in the oscillator circuit should only be used for connections to the ground plane. Do not share ground connections; instead, make a separate connection to ground for each component that requires grounding. If possible, place multiple vias in parallel for each connection to the ground plane. Especially in the Colpitts oscillator configuration, the oscillator is very sensitive to capacitance in parallel with the crystal. Therefore, the layout must be designed to minimize stray capacitance across the crystal to less than 5 pF total under all circumstances to ensure proper crystal oscillation. Be sure to consider both PCB and crystal stray capacitance.

Table 2 lists several recommended crystals and the respective manufacturer of each.

Table 2. Recommended Crystal Manufacturers

MANUFACTURER	PART NUMBER
Vectron	VXC1-1133
Fox	218-3
Saronix	FP2650002

9.3.4 Phase Frequency Detector (PFD)

The PFD takes inputs from the input interface and the feedback divider and produces an output that depends on the phase and frequency differences between the two inputs. The allowable range of frequencies at the PFD inputs is 21.875 MHz to 28.47 MHz.

9.3.5 Charge Pump (CP)

The charge pump is controlled by the PFD, which dictates either to pump up or down to charge or discharge the integrating section of the on-chip loop filter. The integrated and filtered charge pump current is then converted to a voltage that drives the control voltage node of the internal VCO through the on-chip loop filter. The charge pump current is preset to 224 µA and cannot be changed.

9.3.6 On-Chip PLL Loop Filter

Figure 14 shows the on-chip active loop filter topology implemented in the device. This design corresponds to a PLL bandwidth of 400 kHz for a PFD in the range of 21.875 MHz to 28.47 MHz, and a charge pump current of 224 µA.

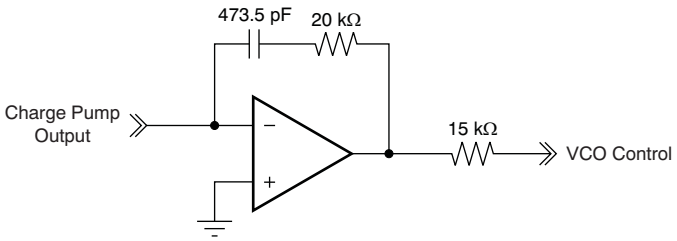


Figure 14. On-Chip PLL Loop Filter Topology

9.3.7 Prescaler Divider and Feedback Divider

The VCO output is routed to the prescaler divider and then to the feedback divider. The prescaler divider and feedback divider are set in tandem with each other, according to the control pin settings given in Table 5. The allowable combinations of the two dividers ensure that the VCO frequency and the PFD frequency are within the specified limits.

9.3.8 On-Chip VCO

The CDCM61004 includes an on-chip, LC oscillator-based VCO with low phase noise covering a frequency range of 1.75 GHz to 2.05 GHz. The VCO must be calibrated to ensure proper operation over the valid device operating conditions. This calibration requires that the PLL be set up properly to lock the PLL loop and that the reference clock input be present. During the first device initialization after power-up, which occurs after the Power-On-Reset is released (2.64 V or lower, over valid device operating conditions) or a device reset with the $\overline{\text{RSTN}}$ pin, a VCO calibration sequence is initiated after 16,384 × Reference Input Clock Cycles. The VCO calibration then takes about 20 µs over the allowable range of the reference clock input.

The VCO calibration can also be reinitiated with a pulse on the $\overline{\text{RSTN}}$ pin at any time after POR is released on power-up; the $\overline{\text{RSTN}}$ pulse must be at least 100 ns wide.

For proper device operation, the reference input must be stable at the start of VCO calibration. Since inputs from crystals or crystal oscillators can typically take up to 1-2ms to be stable, TI recommends to establish circuitry on the $\overline{\text{RSTN}}$ pin that ensures device initialization including VCO calibration after a delay of greater than 5 ms compared to the power-up ramp, as shown in Figure 15. A possible implementation of the delay circuitry on the $\overline{\text{RSTN}}$ pin would be a 47-nF capacitor to GND, and this in tandem with the 150-kΩ on-chip pullup resistor ensures the appropriate delay. The CE pin has an internal 150-kΩ pullup resistor and can be left unconnected or pulled to high for proper device operation.

The device can operate at temperatures within the ambient temperature range T_A. Within the ambient temperature limits and after the point in time when the VCO calibrated, the absolute temperature drift must be smaller than the maximum allowable temperature drift for continuous lock $|T_{CL}|$ for the PLL to stay in lock to an appropriate input reference. When a larger absolute temperature drift has to be covered, the VCO needs to be re-calibrated as described above.

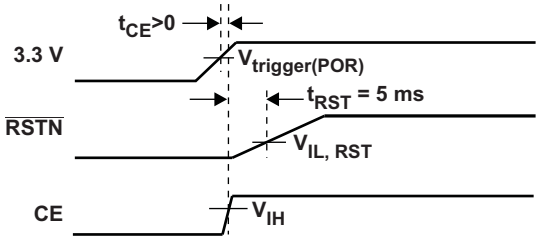


Figure 15. Suggested Timing Recommendations

9.3.9 LVCMOS Input Interface

Alternately, the CDCM61004 can be operated with an external AC-coupled 2.5-V LVCMOS or DC-coupled 3.3-V LVCMOS reference input applied to the XIN pin. For proper operation, the LVCMOS reference should be available and fairly stable by the time the power supply voltages or the RSTN pin voltage on the CDCM61004 reaches 2.27 V. For more details about the LVCMOS input interface to the CDCM61004, see the application report, *Using LVCMOS Input to the CDM6100x* (SCAA111), available on ti.com.

9.3.10 Output Divider

The output from the prescaler divider is also routed to the output divider. The output divider can be set with control pins according to Table 6.

9.3.11 Output Buffer

Each output buffer can be set to LVPECL or LVDS or 2x LVCMOS, according to Table 7. OSC_OUT is an LVCMOS output that can be used to monitor proper loading of the input crystal to achieve the necessary crystal frequency with the least error. The OSC_OUT turns on as soon as power is available and remains on during deviec calibration. The output buffers are disabled during VCO calibration and are enabled only after calibration is complete.

The output buffers on the CDCM61004 can also be disabled, along with other sections of the device, using the CE pin according to Table 8.

9.4 Device Functional Modes

Table 3. Common Configuration

INPUT (MHz)	PRESCALER DIVIDER	FEEDBACK DIVIDER	VCO FREQUENCY (MHz)	OUTPUT DIVIDER	OUTPUT FREQUENCY (MHz)	APPLICATION
25	4	20	2000	8	62.5	GigE
24.75	3	24	1782	8	74.25	HDTV
25	3	24	1800	8	75	SATA
24.8832	3	25	1866.24	8	77.76	SONET
25	3	24	1800	6	100	PCI express
26.5625	3	24	1912.5	6	106.25	Fibre channel
25	4	20	2000	4	125	GigE
25	3	24	1800	4	150	SATA
24.8832	3	25	1866.24	4	155.52	SONET
25	3	25	1875	4	156.25	10 GigE
26.5625	3	24	1912.5	4	159.375	10-G Fibre channel
25	5	15	1875	2	187.5	12 GigE
25	3	24	1800	3	200	PCI Express
26.5625	3	24	1912.5	3	212.5	4-G Fibre channel
25	4	20	2000	2	250	GigE
24.8832	3	25	1866.24	2	311.04	SONET
25	3	25	1875	2	312.5	XGMII
24.8832	3	25	1866.24	1	622.08	SONET
25	3	25	1875	1	625	10 GigE

Table 4. Generic Configuration

INPUT FREQUENCY RANGE (MHz)	PRESCALER DIVIDER	FEEDBACK DIVIDER	VCO FREQUENCY RANGE (MHz)	OUTPUT DIVIDER	OUTPUT FREQUENCY RANGE (MHz)
21.875 to 25.62	4	20	1750 to 2050	8	54.6875 to 64.05
21.875 to 25.62	4	20	1750 to 2050	6	72.92 to 85.4
21.875 to 25.62	4	20	1750 to 2050	4	109.375 to 128.1
21.875 to 25.62	4	20	1750 to 2050	3	145.84 to 170.8
21.875 to 25.62	4	20	1750 to 2050	2	218.75 to 256.2
21.875 to 25.62	4	20	1750 to 2050	1	437.5 to 512.4
23.33 to 27.33	3	25	1750 to 2050	8	72.906 to 85.408
23.33 to 27.33	3	25	1750 to 2050	6	97.21 to 113.875
23.33 to 27.33	3	25	1750 to 2050	4	145.812 to 170.816
23.33 to 27.33	3	25	1750 to 2050	3	194.42 to 227.75
23.33 to 27.33	3	25	1750 to 2050	2	291.624 to 341.632
23.33 to 27.33	3	25	1750 to 2050	1	583.248 to 683.264
23.33 to 27.33	5	15	1750 to 2050	8	43.75 to 51.25
23.33 to 27.33	5	15	1750 to 2050	6	58.33 to 68.33
23.33 to 27.33	5	15	1750 to 2050	4	87.5 to 102.5
23.33 to 27.33	5	15	1750 to 2050	3	116.66 to 136.66
23.33 to 27.33	5	15	1750 to 2050	2	175 to 205
23.33 to 27.33	5	15	1750 to 2050	1	350 to 410
24.305 to 28.47	3	24	1750 to 2050	8	72.915 to 85.41
24.305 to 28.47	3	24	1750 to 2050	6	97.22 to 113.88
24.305 to 28.47	3	24	1750 to 2050	4	145.83 to 170.82
24.305 to 28.47	3	24	1750 to 2050	3	194.44 to 227.76
24.305 to 28.47	3	24	1750 to 2050	2	291.66 to 341.64
24.305 to 28.47	3	24	1750 to 2050	1	583.32 to 683.28

Table 5. Programmable Prescaler and Feedback Divider Settings

CONTROL INPUTS		PRESCALER DIVIDER	FEEDBACK DIVIDER	PFD FREQUENCY	
PR1	PR0			MIN	MAX
0	0	3	24	24.305	28.47
0	1	5	15	23.33	27.33
1	0	3	25	23.33	27.33
1	1	4	20	21.875	25.62

Table 6. Programmable Output Divider

CONTROL INPUTS			OUTPUT DIVIDER
OD2	OD1	OD0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	Reserved
1	0	1	6
1	1	0	Reserved
1	1	1	8

Table 7. Programmable Output Type

CONTROL INPUTS		OUTPUT TYPE
OS1	OS0	
0	0	LVCMOS, OSC_OUT Off
0	1	LVDS, OSC_OUT Off
1	0	LVPECL, OSC_OUT Off
1	1	LVPECL, OSC_OUT On

Table 8. Output Enable

CONTROL INPUT	OPERATING CONDITION	OUTPUT
CE		
0	Power down	High-Z
1	Normal	Active

Table 9. Reset

CONTROL INPUT	OPERATING CONDITION	OUTPUT
$\overline{\text{RSTN}}$		
0	Device reset	High-Z
0 → 1	PLL recalibration	High-Z
1	Normal	Active

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Start-Up Time Estimation

The CDCM61004 start-up time can be estimated based on the parameters defined in Table 10 and graphically shown in Figure 16.

Table 10. Start-Up Time Dependencies

PARAMETER	DEFINITION	DESCRIPTION	FORMULA/METHOD OF DETERMINATION
t_{REF}	Reference clock period	The reciprocal of the applied reference frequency in seconds.	$t_{REF} = \frac{1}{f_{REF}}$
t_{pul}	Power-up time (low limit)	Power-supply rise time to low limit of Power On Reset (POR) trip point	Time required for power supply to ramp to 2.27 V
t_{puh}	Power-up time (high limit)	Power supply rise time to high limit of POR trip point	Time required for power supply to ramp to 2.64 V
t_{rsu}	Reference start-up time	After POR releases, the Colpits oscillator is enabled. This start-up time is required for the oscillator to generate the requisite signal levels for the delay block to be clocked by the reference input.	500 µs best-case and 800 µs worst-case
t_{delay}	Delay time	Internal delay time generated from the reference clock. This delay provides time for the reference oscillator to stabilize.	$t_{delay} = 16384 \times t_{ref}$
t_{VCO_CAL}	VCO calibration time	VCO Calibration Time generated from the reference clock. This process selects the operating point for the VCO based on the PLL settings.	$t_{VCO\_CAL} = 550 \times t_{ref}$
t_{PLL_LOCK}	PLL lock time	Time required for PLL to lock within ±10 ppm of f_{REF}	Based on the 400-kHz loop bandwidth, the PLL settles in 5τ or 12.5 µs.

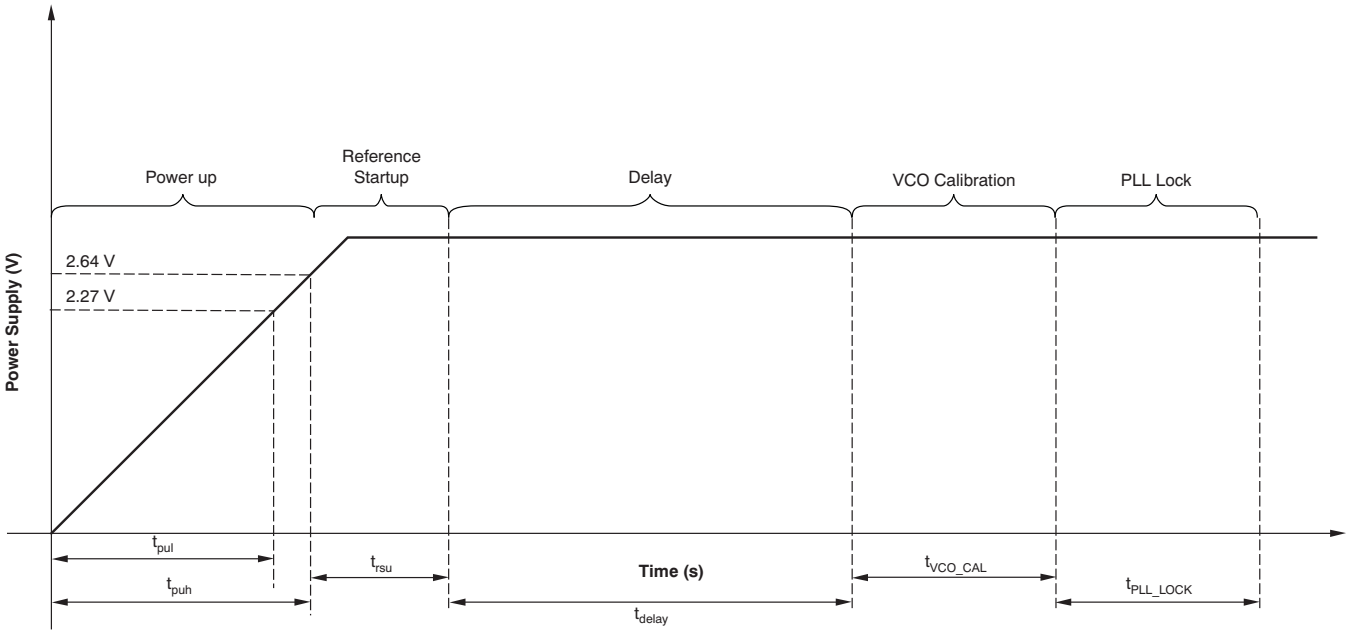


Figure 16. Start-up Time Dependencies

The CDCM61004 start-up time limits, t_{MAX} and t_{MIN}, can be calculated as follows in Equation 3 and Equation 4:

$$t_{MAX} = t_{puh} + t_{rsu} + t_{delay} + t_{VCO\_CAL} + t_{PLL\_LOCK} \quad (3)$$

$$t_{MIN} = t_{pul} + t_{rsu} + t_{delay} + t_{VCO\_CAL} + t_{PLL\_LOCK} \quad (4)$$

10.1.2 Output Termination

The CDCM61004 is a 3.3-V clock driver with the following output options: LVPECL, LVDS, or LVCMOS.

10.1.3 LVPECL Termination

The CDCM61004 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL is 50 Ω to (V_{CC}–2) V, but this DC voltage is not readily available on most PCBs. Thus, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (DC) and ac-coupled (AC) cases, as shown in Figure 17 and Figure 18. TI recommends placing all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and receiver are different, ac-coupling is required.

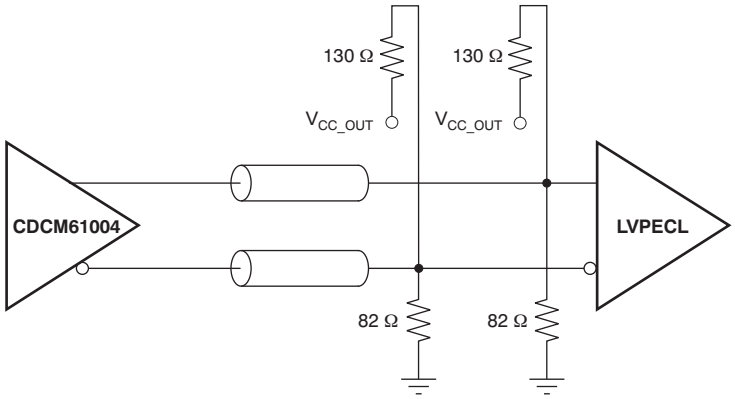


Figure 17. LVPECL Output DC Termination

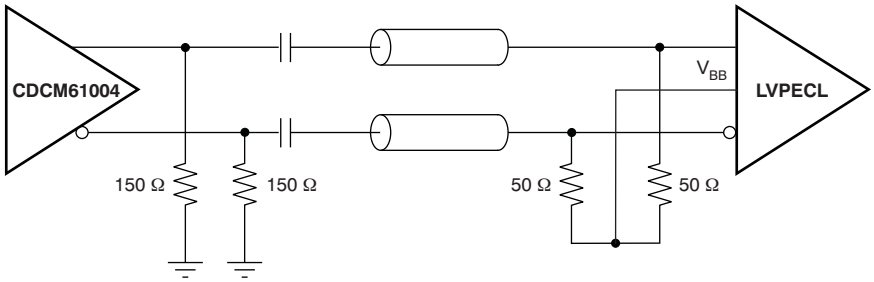


Figure 18. LVPECL Output AC Termination

10.1.4 LVDS Termination

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either direct-coupled termination or ac-coupled termination can be used for LVDS outputs, as shown in Figure 19 and Figure 20. TI recommends placing all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and the receiver are different, ac-coupling is required.

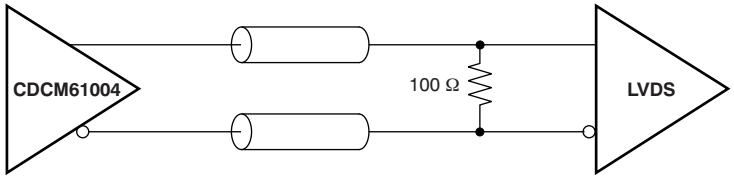


Figure 19. LVDS Output DC Termination

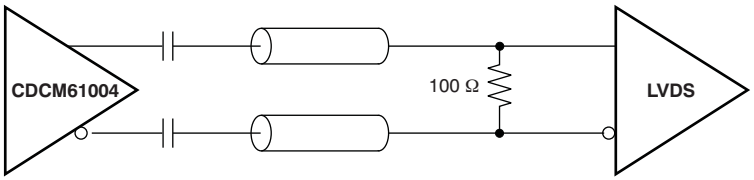


Figure 20. LVDS Output AC Termination

10.1.5 LVCMOS Termination

Series termination is a common technique used to maintain the signal integrity for LVCMOS drivers, if connected to a receiver with a high-impedance input with a pullup or a pulldown resistor. For series termination, a series resistor (R_S) is placed close to the driver, as shown in Figure 21. The sum of the driver impedance and R_S should be close to the transmission line impedance, which is usually 50 Ω. Because the LVCMOS driver in the CDCM61004 has an impedance of 30 Ω, R_S is recommended to be 22 Ω to maintain proper signal integrity.

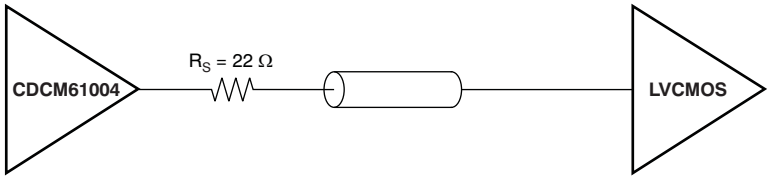


Figure 21. LVCMOS Output Termination

10.1.6 Interfacing Between LVPECL and HCSL

Because the LVPECL common-mode voltage is different from the HCSL common-mode voltage, ac-coupled termination is used. The 150-Ω resistor ensures proper biasing of the CDCM61004 LVPECL output stage, while the 471-Ω and 56-Ω resistor network biases the HCSL receiver input stage, as shown in Figure 22.

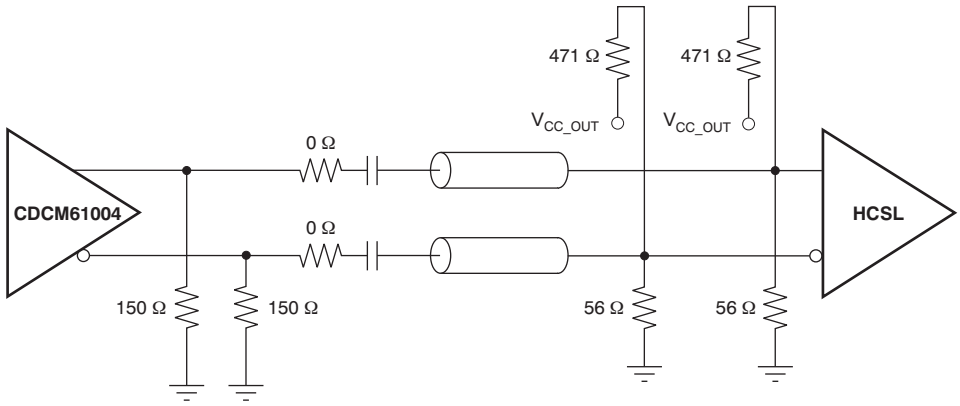


Figure 22. LVPECL to HCSL Interface

10.2 Typical Application

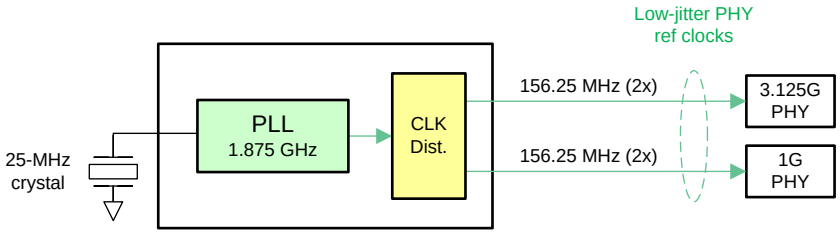


Figure 23. Ethernet Switch

10.2.1 Design Requirements

Consider a typical wired communications application, like a top-of-rack switch, which needs to clock 1-Gbps or 3.125-Gbps Ethernet PHYs. For such asynchronous systems, the reference input can be a crystal. In such systems, the clocks are expected to be available upon power up without the need for any device-level programming. An example of clock input and output requirements is shown below:

- Clock Input:
  - 25-MHz crystal
- Clock Outputs:
  - 2× 156.25 MHz clock for uplink 3.125 Gbps, LVPECL
  - 2× 156.25 MHz clock for downlink 3.125 Gbps, LVPECL

The section below describes the detailed design procedure to generate the required output frequencies for the above scenario using CDCM61004.

10.2.2 Detailed Design Procedure

Design of all aspects of the CDCM61004 is quite involved and software support is available to assist in part selection and phase noise simulation. This design procedure will give a quick outline of the process.

1. Device Selection
   - The first step is to calculate the VCO frequency given the required output frequency. The device must be able to produce the VCO frequency that can be divided down to the required output frequency.
   - The WEBENCH Clock Architect Tool from TI will aid in the selection of the right device that meets the customer's output frequencies and format requirements.

Typical Application (continued)

2. Device Configuration
   – The WEBENCH Clock Architect Tool attempts to maximize the phase detector frequency, use smallest dividers, and maximizes PLL bandwidth.

10.2.2.1 Device Selection

Use the WEBENCH Clock Architect Tool. Enter the required frequencies and formats into the tool. To use this device, find a solution using the CDCM61004.

10.2.2.1.1 Calculation Using LCM

In this example, the valid VCO frequency for CDCM61004 is 1.875 GHz.

10.2.2.2 Device Configuration

For this example, when using the WEBENCH Clock Architect Tool, the reference would have been manually entered as 25 MHz according to input frequency requirements. Enter the desired output frequencies and click on Generate Solutions. Select CDCM61004 from the solution list.

From the simulation page of the WEBENCH Clock Architect Tool, it can be seen that to maximize phase detector frequencies, the N divider is set to 25 and prescaler divider is set to 3. This results in a VCO frequency of 1.875 GHz. The output divider is set to 4. At this point the design meets all input and output frequency requirements and it is possible to design a loop filter for system and simulate performance on the clock outputs. Figure 24 shows the typical phase noise plot of the 156.25 MHz LVPECL output.

10.2.3 Application Curve

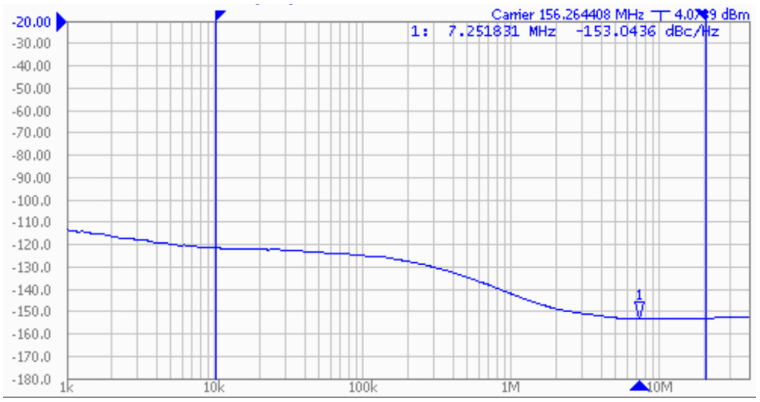


Figure 24. Typical Phase Noise Plot of 156.25 MHz LVPECL Output

11 Power Supply Recommendations

11.1 Power Considerations

As a result of the different possible configurations of the CDCM61004, Table 11 is intended to provide enough information on the estimated current consumption of the device. Unless otherwise noted, V_{CC} = 3.3 V and T_A = 25°C.

Table 11. Estimated Block Power Consumption

BLOCK	CONDITION	CURRENT CONSUMPTION (mA)	IN-DEVICE POWER DISSIPATION (mW)	EXTERNAL RESISTOR POWER DISSIPATION (mW)
Entire device, core current	Output off, no termination resistors	65	214.5	
Output buffer	LVPECL output, active mode	28	42.4	50
	LVCMOS output pair, static	4.5	14.85	
	LVCMOS output pair, transient, 'C_L' load, 'f' MHz output frequency	$V \times f_{OUT} \times (C_L + 20 \times 10^{-12}) \times 10^3$	$V^2 \times f_{OUT} \times (C_L + 20 \times 10^{-12}) \times 10^3$	
	LVDS output, active mode	20	66	
Divide circuitry	Divide enabled, divide = 1	5	16.5	
	Divide enabled, divide = 2	10	33	
	Divide enabled, divide = 3, 4	15	49.5	
	Divide enabled, divide = 6, 8	20	66	

From Table 11, the current consumption can be calculated for any configuration. For example, the current for the entire device with four LVPECL outputs in active mode can be calculated by adding up the following blocks: core current, 4x LVPECL output buffer current, and the divide circuitry current. The overall in-device power consumption can also be calculated by summing the in-device power dissipated in each of these blocks.

As an example scenario, let us consider the use case of a crystal input frequency of 25 MHz and device output frequency of 312.5 MHz in LVPECL mode. For this case, the typical overall power dissipation can be calculated as seen in Equation 5:

$$3.3\ V \times (65 + 4 \times 28 + 10)\ mA = 617.1\ mW \quad (5)$$

Because each LVPECL output has two external resistors and the power dissipated by these resistors is 50 mW, the typical overall in-device power dissipation is as seen in Equation 6:

$$617.1\ mW - 4 \times 50\ mW = 417.1\ mW \quad (6)$$

When the LVPECL output is active, the average voltage is approximately 1.9 V on each output as calculated from the LVPECL V_{OH} and V_{OL} specifications. Therefore, the power dissipated in each emitter resistor is approximately $(1.9\ V)^2/150\Omega$ = 25 mW.

When the LVCMOS output is active and drives a load capacitance, C_L, the overall LVCMOS output current consumption is the sum of a static pre-driver current and a dynamic switching current (which is a function of the output frequency and the load capacitance).

Let us consider another use case of a crystal input frequency of 26.5625 MHz and device output frequency of 212.5 MHz in LVCMOS mode and driving a 5-pF load capacitance with a typical signal swing of 3.18 V. For this case, the typical overall power dissipation can be calculated as seen in Equation 7:

$$3.3\ V \times (65 + 15 + 4 \times 21.4)\ mA = 546.48\ mW \quad (7)$$

11.2 Thermal Management

Power consumption of the CDCM61004 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125°C.

The device package has an exposed pad that provides the primary heat removal path as well as an electrical grounding to the printed circuit board (PCB). To maximize the removal of heat from the package, a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Check the mechanical data at the end of the data sheet for land and via pattern examples.

11.3 Power-Supply Filtering

PLL-based frequency synthesizers are very sensitive to noise on the power supply, which can dramatically increase the jitter of the PLL. This characteristic is especially true for analog-based PLLs. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL would have attenuated jitter as a result of power-supply noise at frequencies beyond the PLL bandwidth because of attenuation by the loop response.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use these bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-μF) bypass capacitors as there are supply pins in the package.

The CDCM61004 power-supply requirements can be grouped into two sets: the analog supply line and the output/input supply line. The analog supply line consists of the following power-supply pins on the CDCM61004: VCC_PLL1, VCC_PLL2, and VCC_VCO. These pins can be shorted together. The output/input supply line consists of the VCC_OUT and the VCC_IN power-supply pins on the CDCM61004. These pins can be shorted together. Inserting a ferrite bead between the analog supply line and the output/input supply line isolates the high-frequency switching noises generated by the device input and outputs, preventing them from leaking into the sensitive analog supply line. Choosing an appropriate ferrite bead with very low DC resistance is important because it is imperative to provide adequate isolation between the sensitive analog supply line and the other board supply lines, and to maintain a voltage at the analog power-supply pins of the CDCM61004 that is greater than the minimum voltage required for proper operation.

Figure 25 shows a general recommendation for decoupling the power supply.

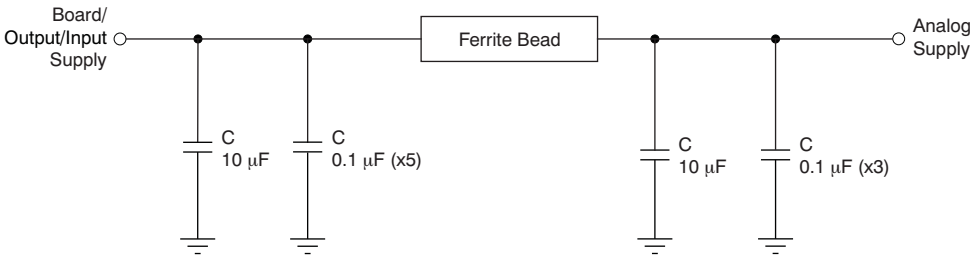


Figure 25. Recommended Power-Supply Decoupling

12 Layout

12.1 Layout Guidelines

The CDCM61004 is a high-performance device; therefore careful attention must be paid to device configuration and printed circuit board layout with respect to power consumption. Observing good thermal layout practices enables the thermal pad on the backside of the VQFN-32 package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

12.2 Layout Example

Figure 26 shows a general recommendation of PCB layout with the CDCM61004 that ensures good system-level thermal reliability.

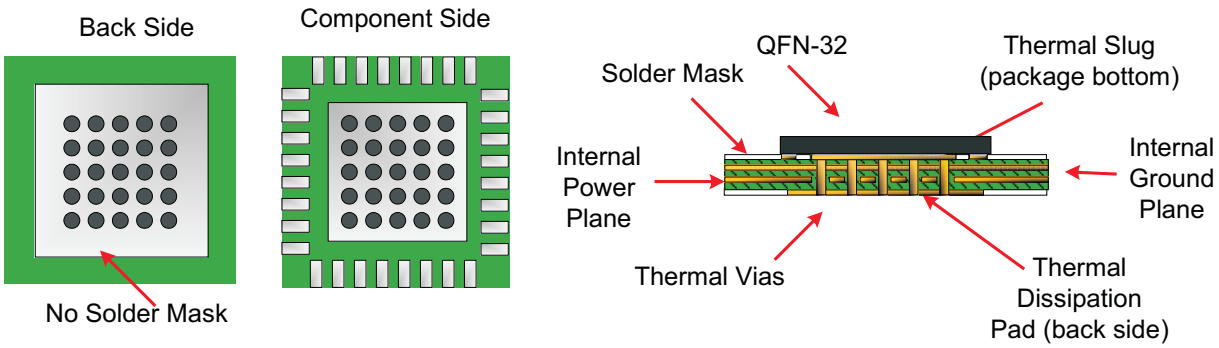


Figure 26. Recommended PCB Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

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All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCM61004RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61004	Samples
CDCM61004RHBR/2801	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61004	Samples
CDCM61004RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61004	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

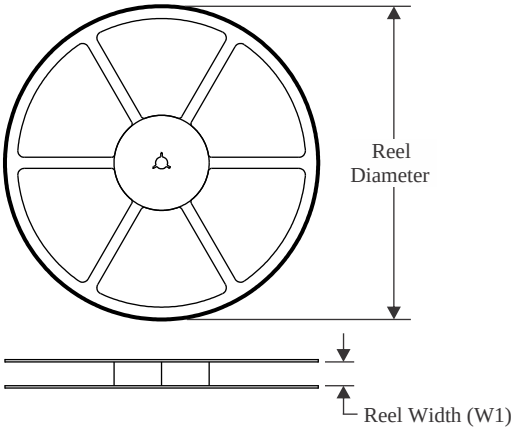
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

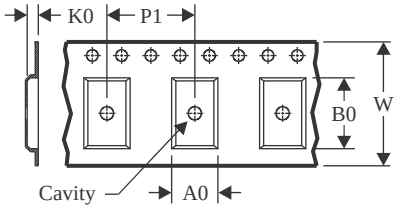
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

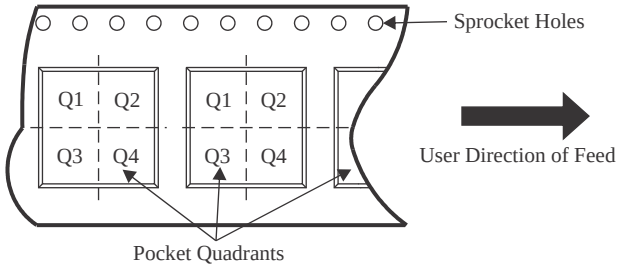


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

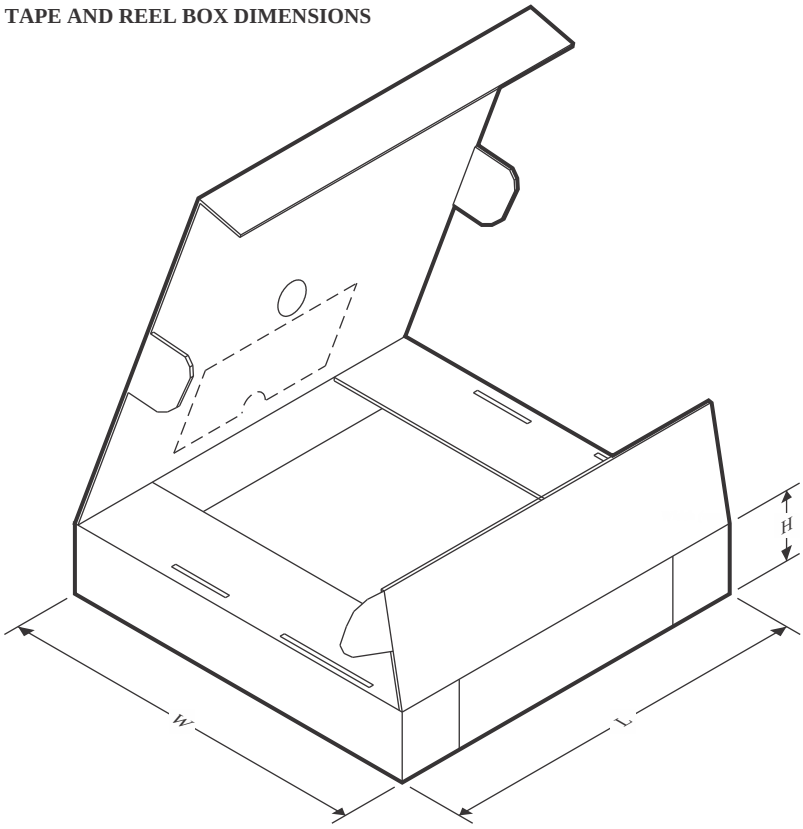
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM61004RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCM61004RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM61004RHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
CDCM61004RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

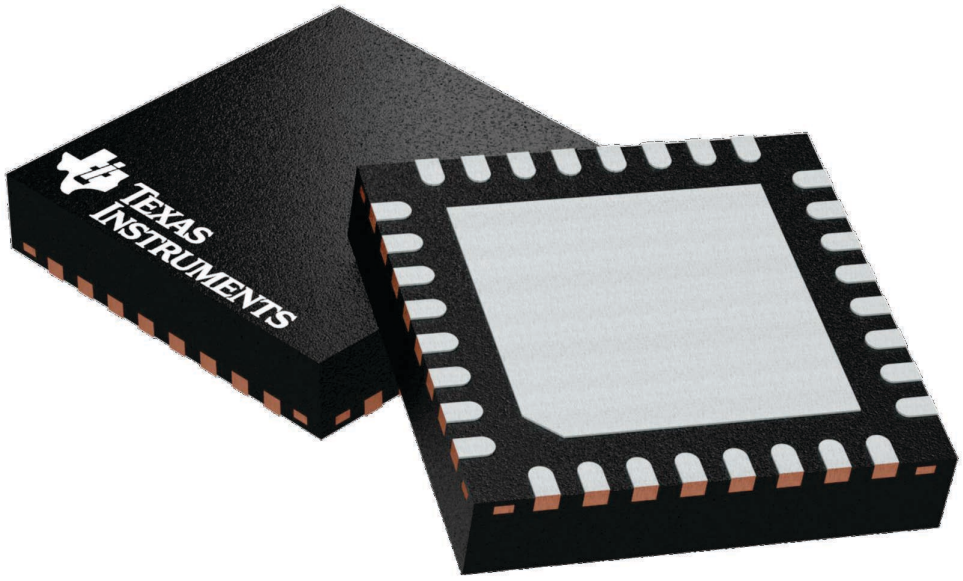
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

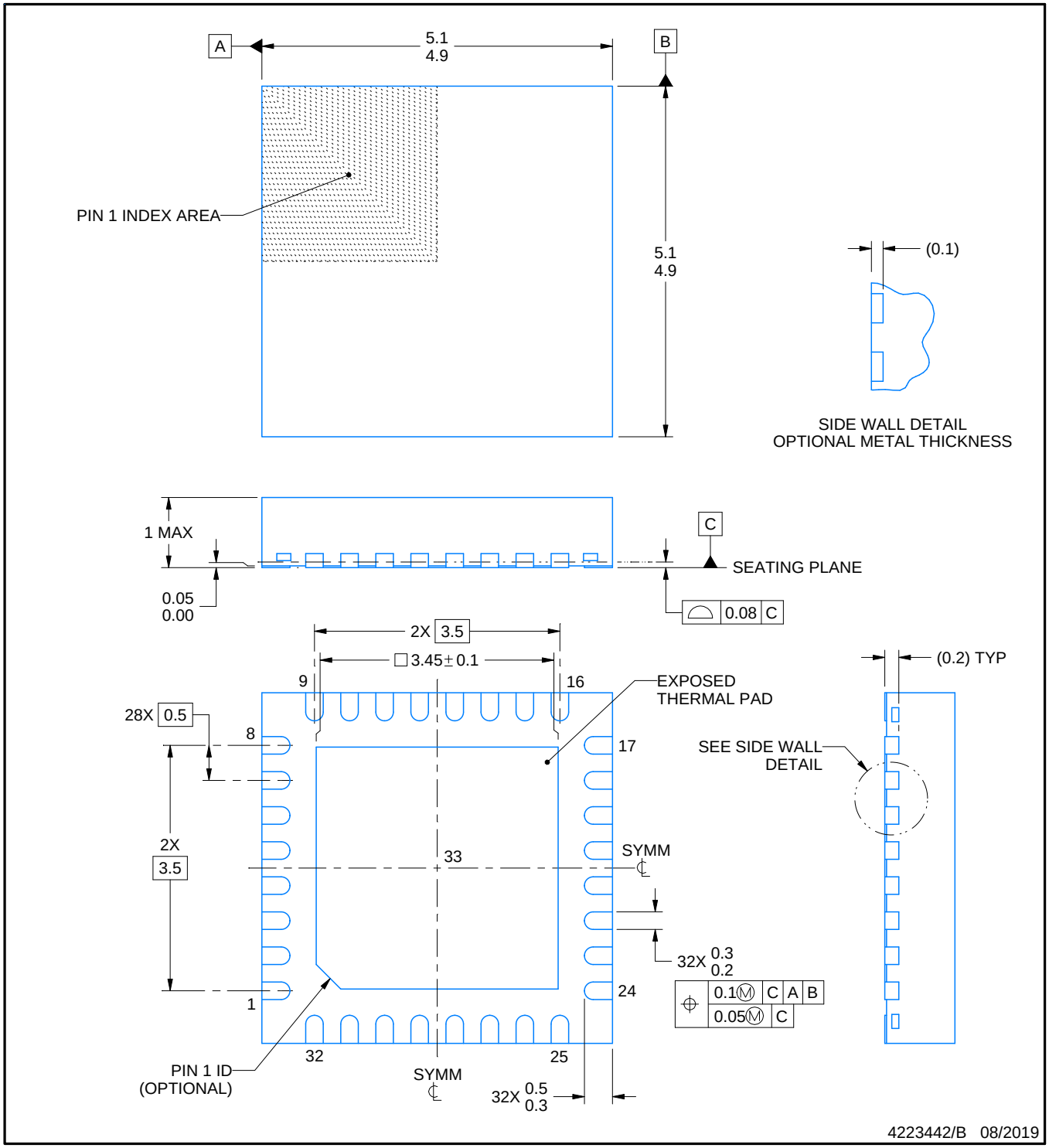
4224745/A

RHB0032E

PACKAGE OUTLINE

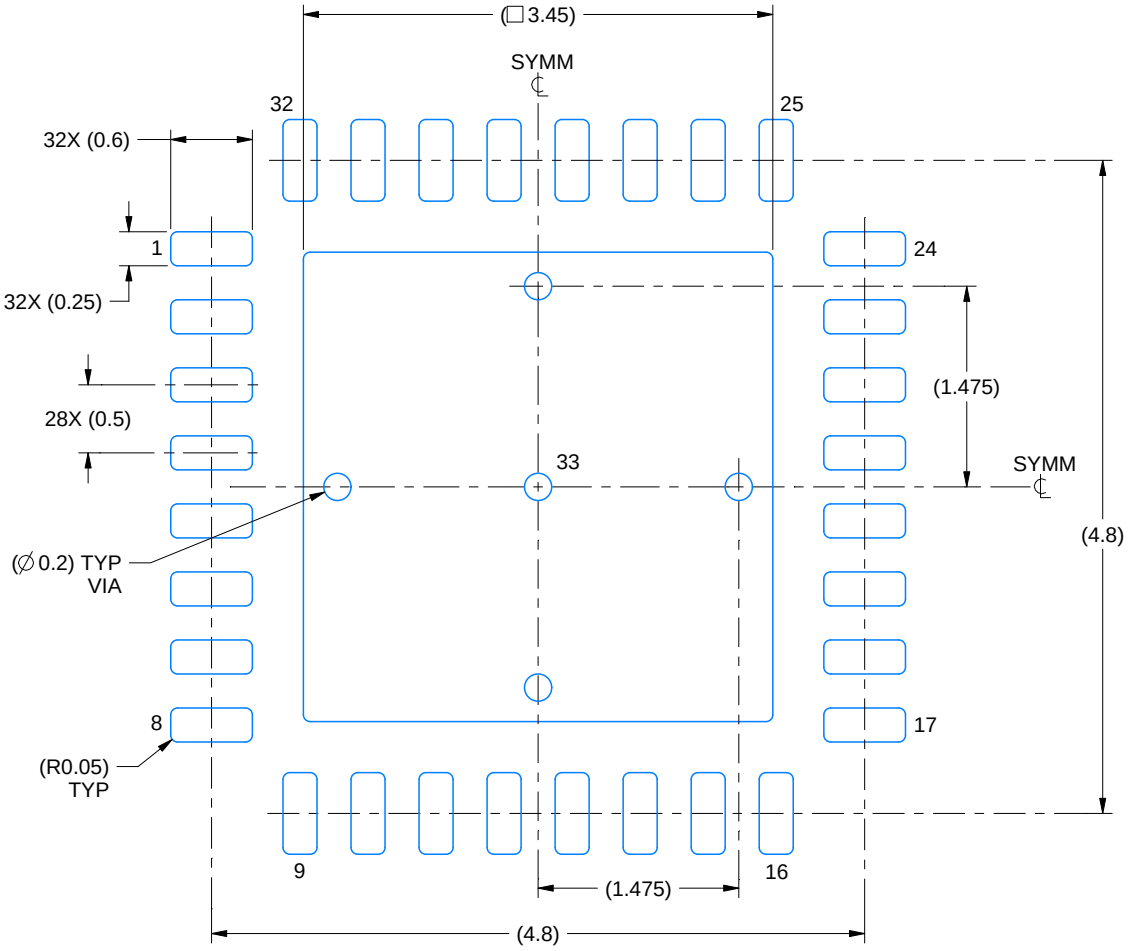
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

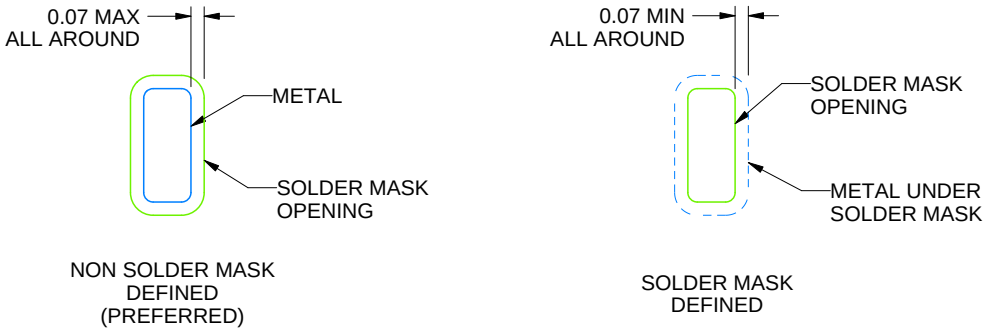


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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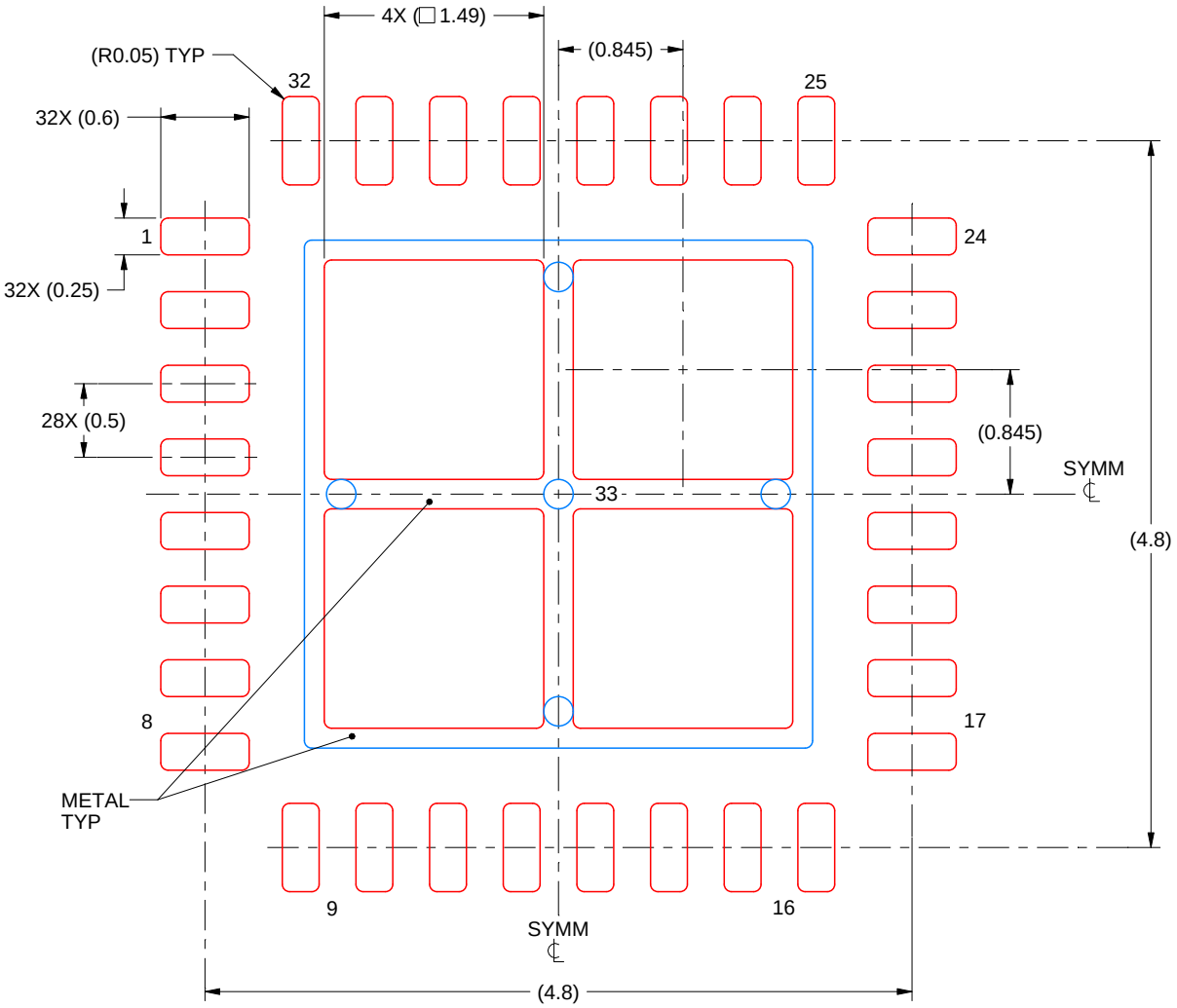
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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- Alternative Solution
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