



**THE DATASHEET OF  
SN74LV245AZQNR**



# SN74LV245A Octal Bus Transceivers With 3-State Outputs

## 1 Features

- 2-V to 5.5-V  $V_{CC}$  operation
- Maximum  $t_{pd}$  of 6.5 ns at 5 V
- Typical  $V_{OLP}$  (output ground bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot) > 2.3 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support mixed-mode voltage operation on all ports
- $I_{off}$  supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Servers
- LED displays
- Network switches
- Telecom infrastructure
- Motor drivers
- I/O expanders

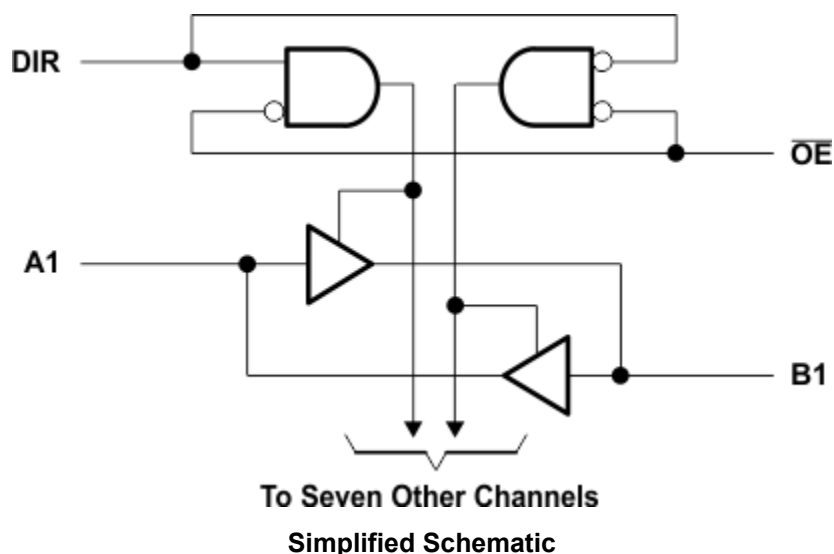
## 3 Description

These octal bus transceivers are designed for 2-V to 5.5-V  $V_{CC}$  operation.

### Package Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV245A	DB (SSOP, 20)	7.20 mm × 5.30 mm
	DGV (TVSOP, 20)	5.00 mm × 4.40 mm
	PW (TSSOP, 20)	6.50 mm × 4.40 mm
	RGY (VQFN, 20)	4.50 mm × 3.50 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
	RKS (VQFN, 20)	4.50 mm × 2.50 mm
	DGS (VSSOP, 20)	5.10 mm × 3.00 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
	N (PDIP, 20)	24.33 mm × 6.35 mm
	NS (SO, 20)	12.60 mm × 5.30 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



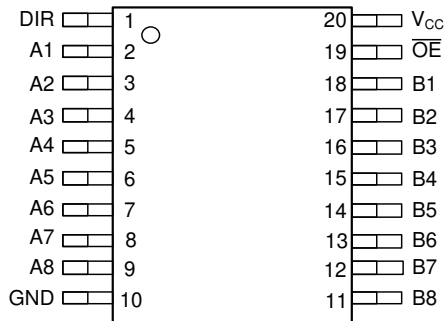
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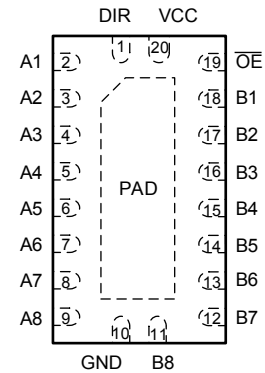
## 4

<b>Changes from Revision Q (April 2023) to Revision R (July 2023)</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Updated R<math>\theta</math>JA values: DB = 94.6 to 113.1, DW = 77.5 to 96.2, NS = 76.6 to 101.1; Updated DB, DW, and PW packages for R<math>\theta</math>JC(top), R<math>\theta</math>JB, <math>\Psi</math>JT, <math>\Psi</math>JB, and R<math>\theta</math>JC(bot), all values in °C/W .....</li> </ul>	5
<b>Changes from Revision P (December 2022) to Revision Q (April 2023)</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added DGS package information.....</li> <li>Updated <i>Package Information</i> table.....</li> </ul>	1
<b>Changes from Revision O (September 2014) to Revision P (December 2022)</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Updated the numbering format for tables, figures, and cross-references throughout the document.....</li> <li>Added RKS package information.....</li> </ul>	1

## 5 Pin Configuration and Functions



**Figure 5-1. SN74LV245A: DB, DGV, DW, N, NS, PW or DGS, 20-Pin SSOP, TVSOP, SOIC, PDIP, SO, TSSOP, or VSSOP (Top View)**



**Figure 5-2. SN74LV245A: RGY or RKS Package, 20-Pin VQFN (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
DIR	1	I	Direction Pin
A1	2	I/O	A1 I/O
A2	3	I/O	A2 I/O
A3	4	I/O	A3 I/O
A4	5	I/O	A4 I/O
A5	6	I/O	A5 I/O
A6	7	I/O	A6 I/O
A7	8	I/O	A7 I/O
A8	9	I/O	A8 I/O
GND	10	—	Ground Pin
B8	11	I/O	B8 I/O
B7	12	I/O	B7 I/O
B6	13	I/O	B6 I/O
B5	14	I/O	B5 I/O
B4	15	I/O	B4 I/O
B3	16	I/O	B3 I/O
B2	17	I/O	B2 I/O
B1	18	I/O	B1 I/O
OE	19	I	Output Enable
V <sub>CC</sub>	20	—	Power Pin

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	-0.5	7	V	
V <sub>I</sub>	Input voltage range	Except I/O ports <sup>(2)</sup>	-0.5	7	V
		I/O ports <sup>(2) (3)</sup>	-0.5	7	
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V	
V <sub>O</sub>	Output voltage range applied in the high or low state <sup>(2) (3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA	
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±35	mA	
	Continuous current through V <sub>CC</sub> or GND		±70	mA	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 5.5-V maximum.

### 6.2 ESD Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN74LV245A		UNIT	
		MIN	MAX		
V <sub>CC</sub>	Supply voltage	2	5.5	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V	
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V	
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3		
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		-2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		-8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		-16	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV245A								UNIT
		DB	DGV	DW	NS	PW	RGY	RKS	DGS	
		20 PINS								
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	113.1	114.8	96.2	101.1	101.5	34.1	67.7	118.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	72.9	30.1	63.6	67	35.6	38.4	72.4	57.7	
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.9	56.3	64.7	66.1	52.5	12.0	40.4	73.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	39.3	0.9	40.5	37.6	2.2	0.8	10.3	5.7	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	67.5	55.6	64.3	65.8	52.0	12.0	40.4	72.7	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	7.1	24.1	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	–40°C to 85°C SN74LV245A			–40°C to 125°C SN74LV245A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	2 V to 5.5 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –2 mA	2.3 V	2			2			
	I <sub>OH</sub> = –8 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = –16 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V				0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V				0.4			
	I <sub>OL</sub> = 8 mA	3 V				0.44			
	I <sub>OL</sub> = 16 mA	4.5 V				0.55			
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±1			±1	μA
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±5			±5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		20			20	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0		5			5	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3				pF
			5 V		3				
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5.5				pF
			5 V		5.5				

## 6.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	C <sub>L</sub> = 15 pF		8.3	13	1	15	1	17	ns
t <sub>en</sub>	$\overline{OE}$	A or B			11.8	19.9	1	22	1	24	
t <sub>dis</sub>	$\overline{OE}$	A or B			11.8	18.1	1	20	1	22	
t <sub>pd</sub>	A or B	B or A	C <sub>L</sub> = 50 pF		11.2	15.9	1	18	1	21	ns
t <sub>en</sub>	$\overline{OE}$	A or B			14.1	22.7	1	26	1	28	
t <sub>dis</sub>	$\overline{OE}$	A or B			17.6	23.1	1	25	1	27	
t <sub>sk(o)</sub>							2	2			

## 6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	B or A	$C_L = 15\text{ pF}$		5.9	8.4	1	10	1	11	ns
$t_{en}$	$\overline{OE}$	A or B			8.2	13.2	1	15.5	1	16.5	
$t_{dis}$	$\overline{OE}$	A or B			9.6	16.5	1	19.5	1	20.5	
$t_{pd}$	A or B	B or A	$C_L = 50\text{ pF}$		7.9	11.9	1	13.5	1	14.5	ns
$t_{en}$	$\overline{OE}$	A or B			9.9	16.7	1	19	1	20	
$t_{dis}$	$\overline{OE}$	A or B			13.9	19.8	1	22	1	23	
$t_{sk(o)}$								1.5		1.5	

## 6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	B or A	$C_L = 15\text{ pF}$		4.3	5.5	1	6.5	1	7	ns
$t_{en}$	$\overline{OE}$	A or B			5.7	8.5	1	10	1	10.5	
$t_{dis}$	$\overline{OE}$	A or B			7.8	12.8	1	14.2	1	14.7	
$t_{pd}$	A or B	B or A	$C_L = 50\text{ pF}$		5.6	7.5	1	8.5	1	9	ns
$t_{en}$	$\overline{OE}$	A or B			7	10.6	1	12	1	12.5	
$t_{dis}$	$\overline{OE}$	A or B			10.9	14.7	1	16	1	16.5	
$t_{sk(o)}$								1		1	

## 6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		SN74LV245A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

## 6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	20	pF
			5 V	25	

### 6.11 Typical Characteristics

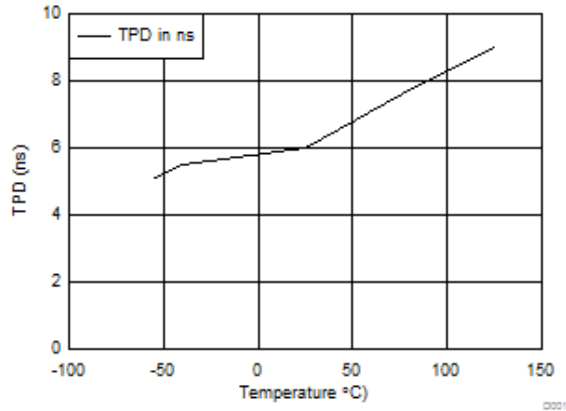


Figure 6-1. TPD vs Temperature at 3.3 V

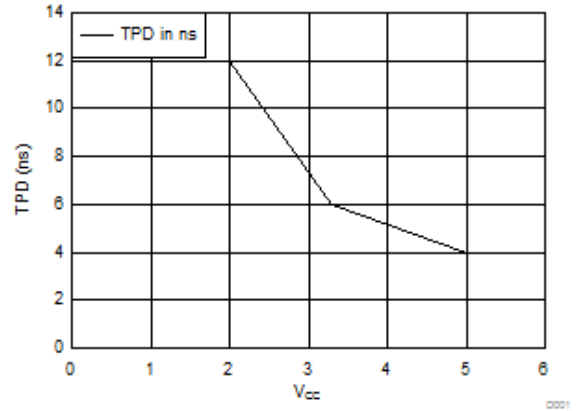
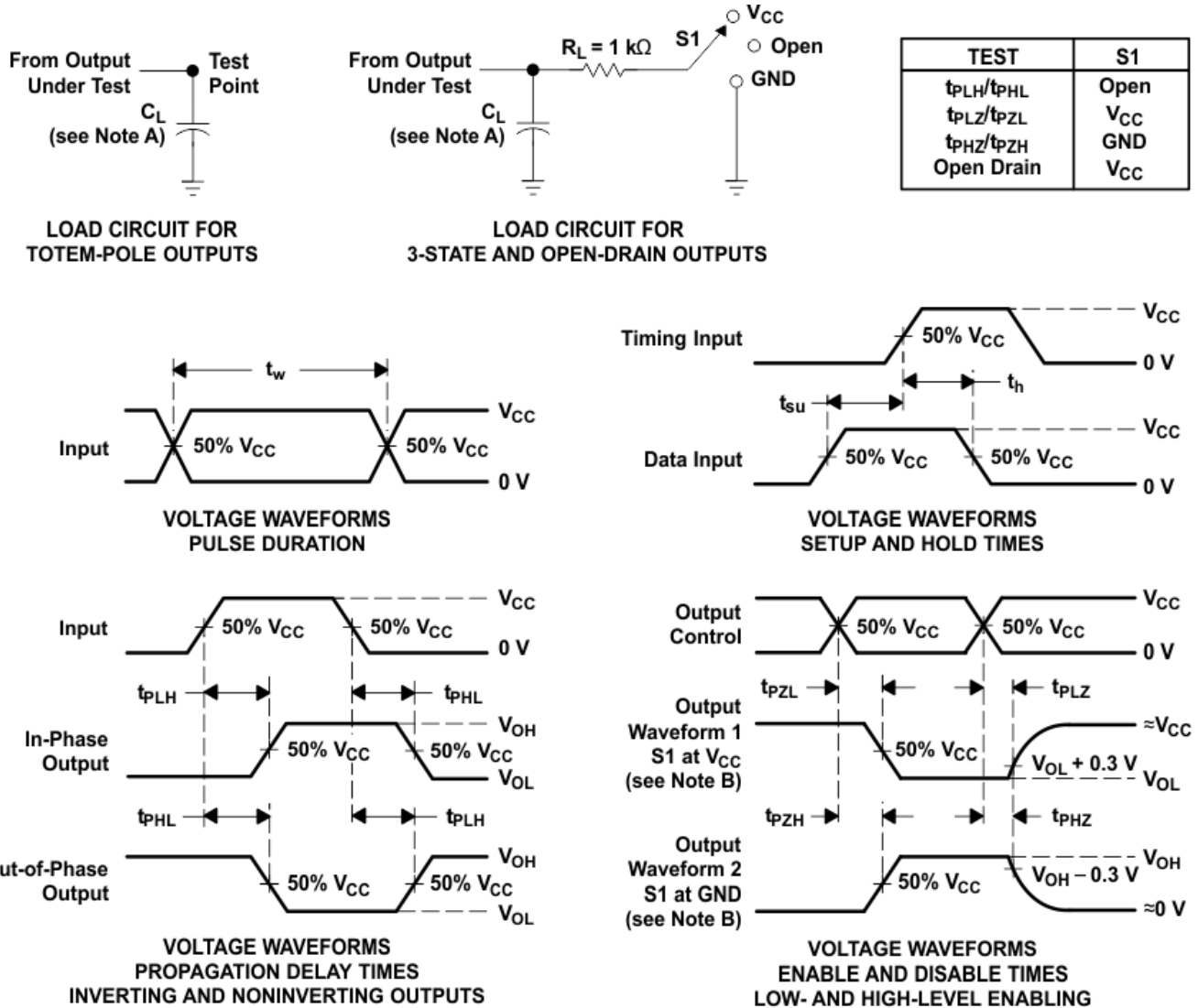


Figure 6-2. TPD vs V<sub>CC</sub>

## 7 Parameter Measurement Information



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram

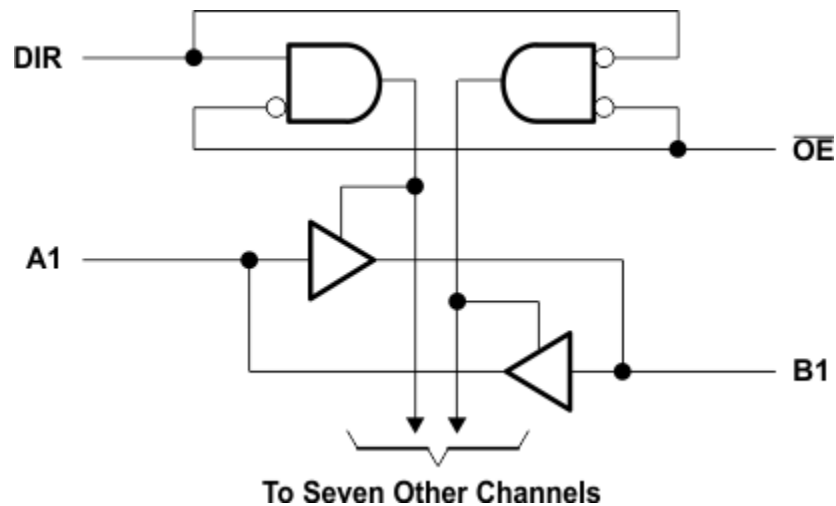


Figure 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

- Allows down voltage translation from 5 V to 3.3 V
  - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

### 8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## 9 Application and Implementation

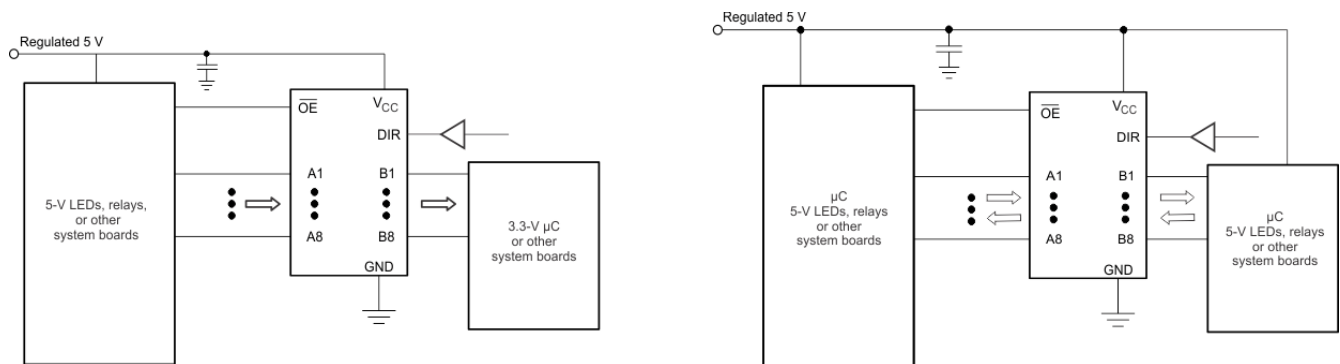
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LV245A is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making the device ideal for down translation.

### 9.2 Typical Application



**Figure 9-1. Typical Application Schematic**

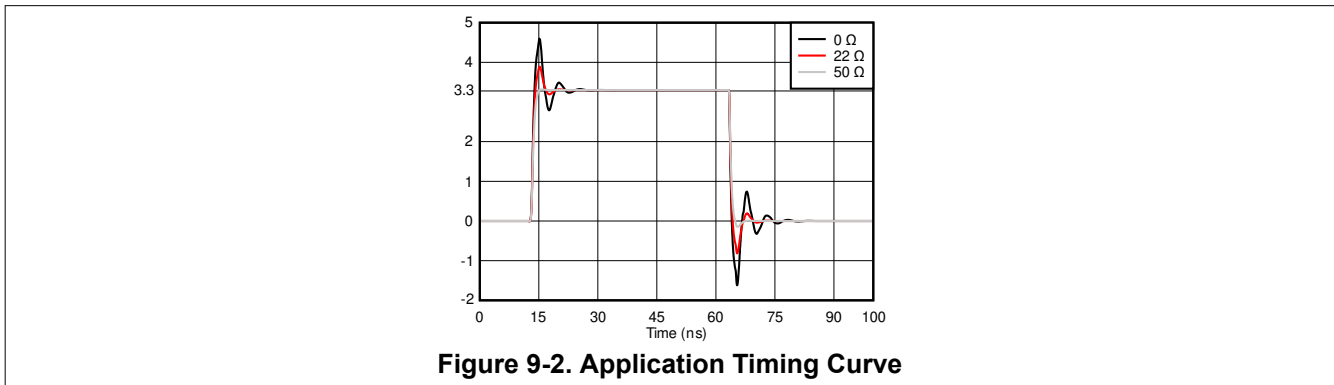
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention, because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive will also create faster edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - Rise time and fall time specifications, see  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#) table.
  - Specified high and low levels, see  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant, allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend output conditions:
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curves



### 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended and if there are multiple  $V_{CC}$  terminals then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

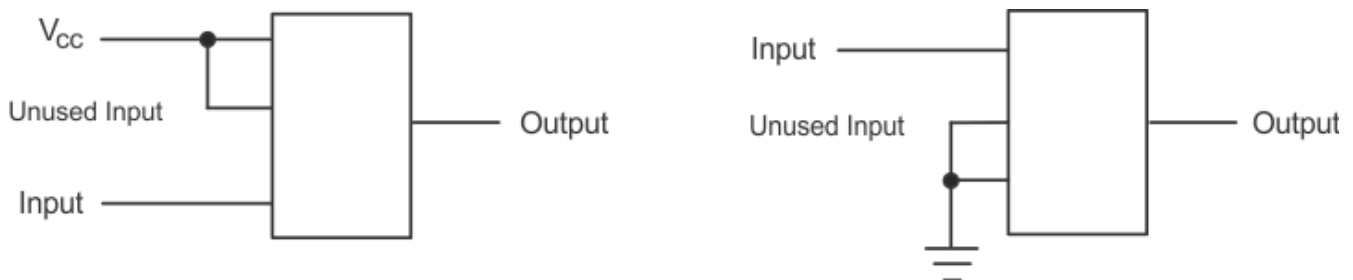
### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 9-3](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they cannot float when disabled.

#### 9.4.2 Layout Example



## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV245ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245ADGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L245A	<a href="#">Samples</a>
SN74LV245ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV245A	<a href="#">Samples</a>
SN74LV245APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245APWRG3	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV245A	<a href="#">Samples</a>
SN74LV245ARKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	<a href="#">Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV245ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV245ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LV245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV245ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV245ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV245APWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV245APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV245APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LV245ARKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV245ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV245ADGSR	VSSOP	DGS	20	5000	356.0	356.0	35.0
SN74LV245ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV245ADWR	SOIC	DW	20	2000	356.0	356.0	41.0
SN74LV245ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV245ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV245ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV245APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV245APWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LV245APWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV245APWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV245ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0
SN74LV245ARKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

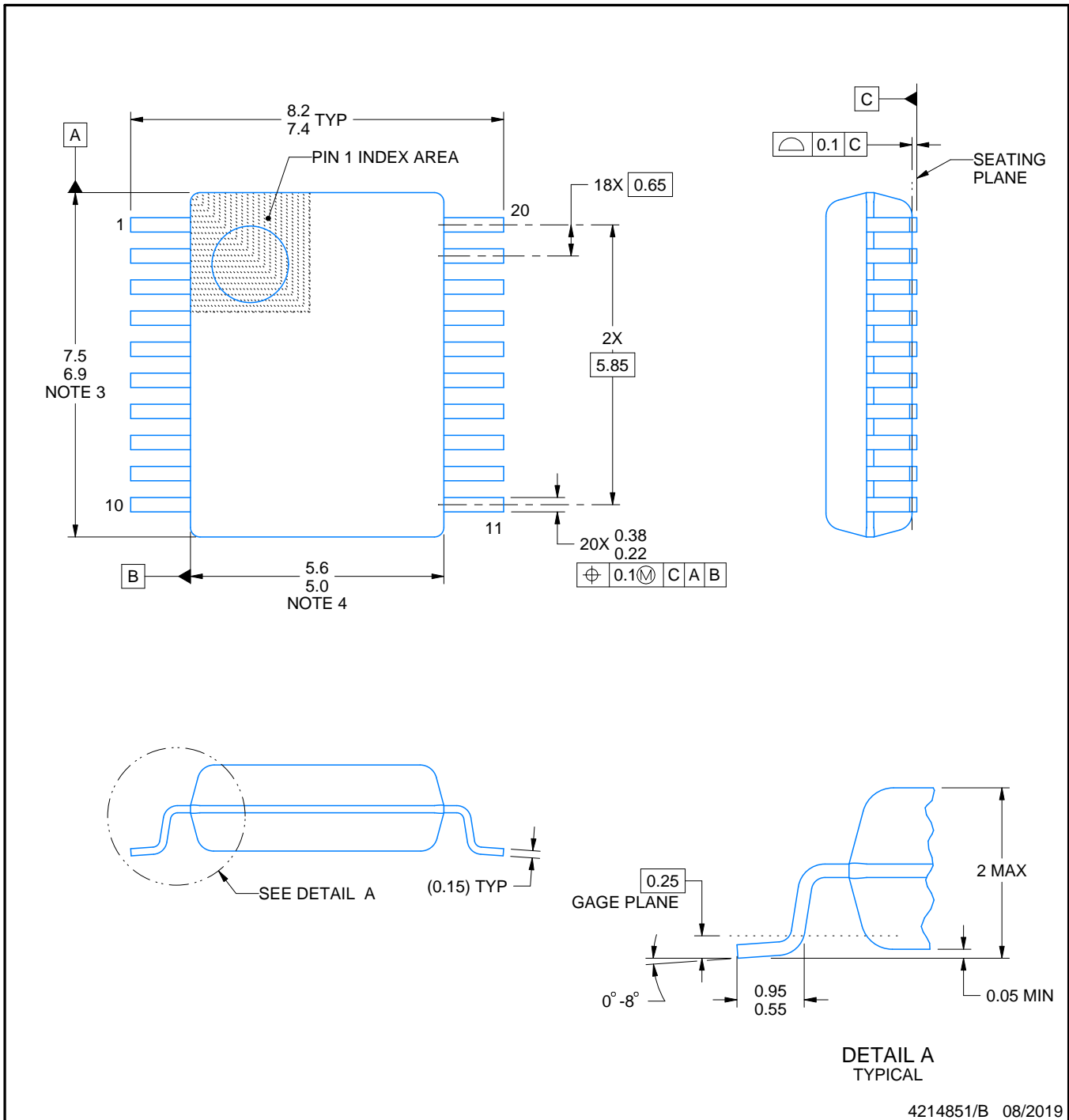
# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

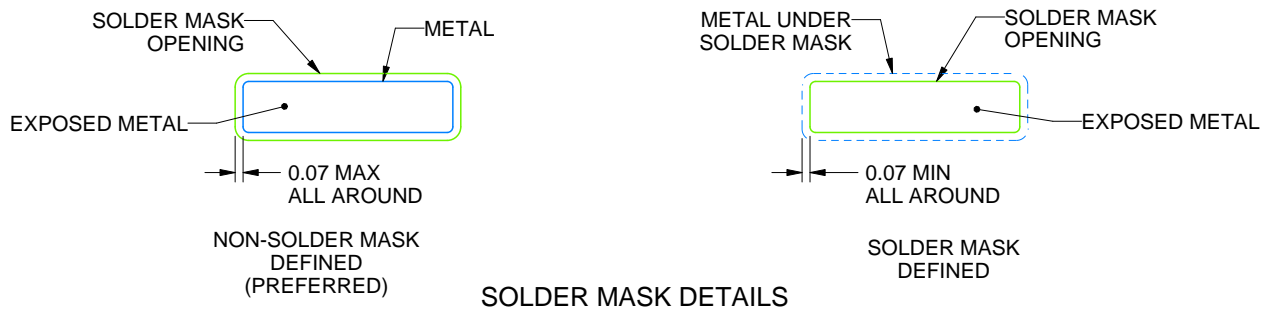
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

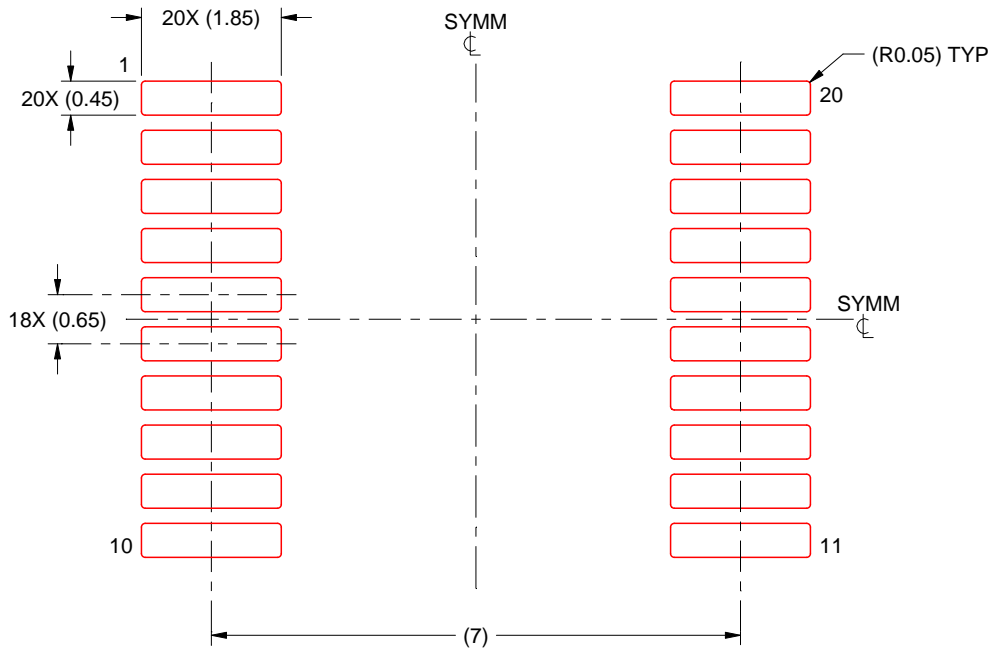
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

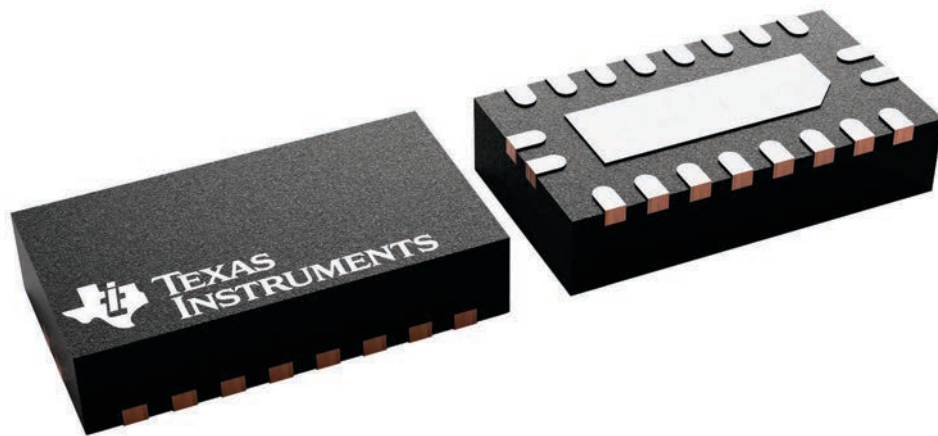
**RKS 20**

**VQFN - 1 mm max height**

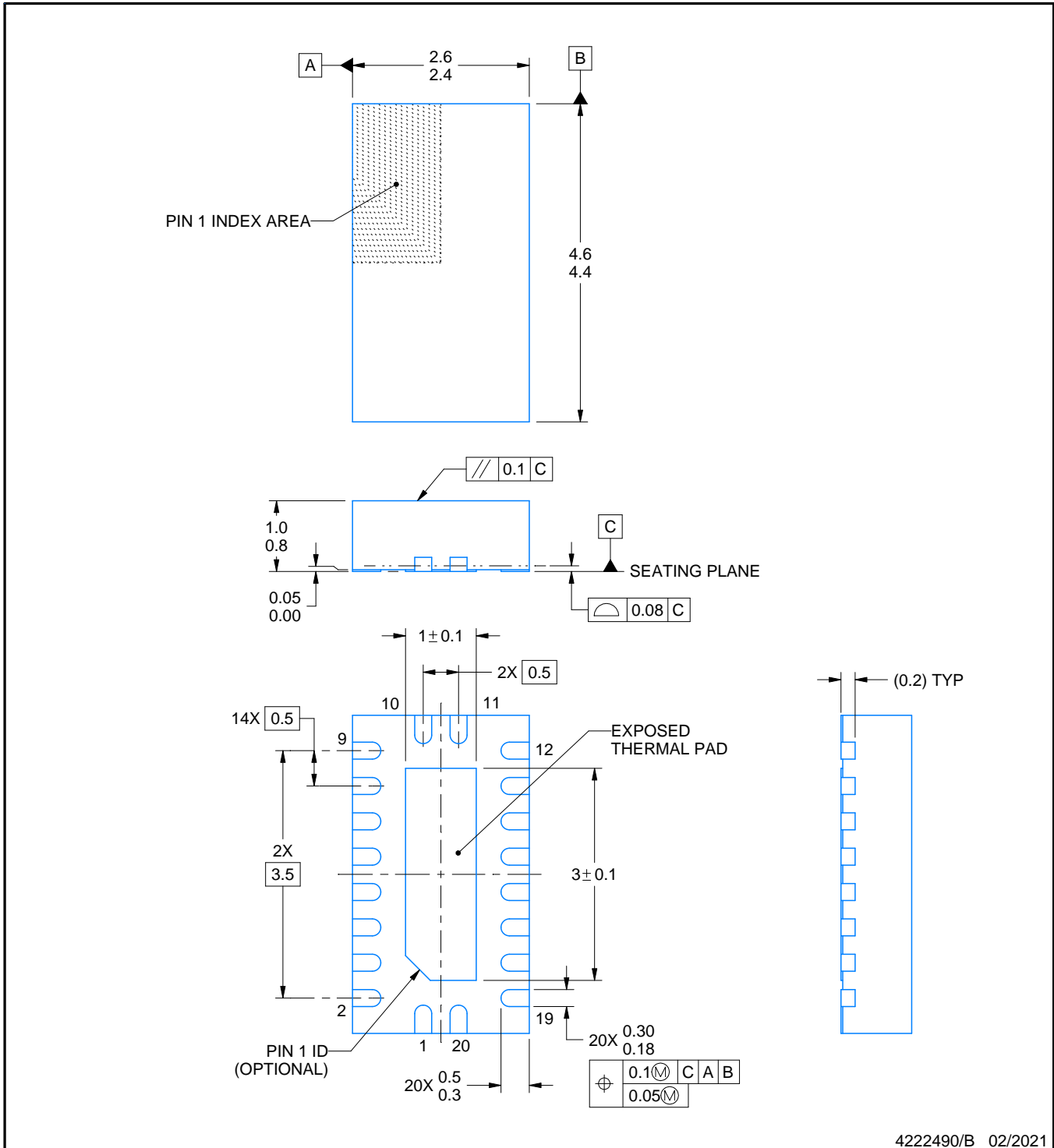
2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226872/A



NOTES:

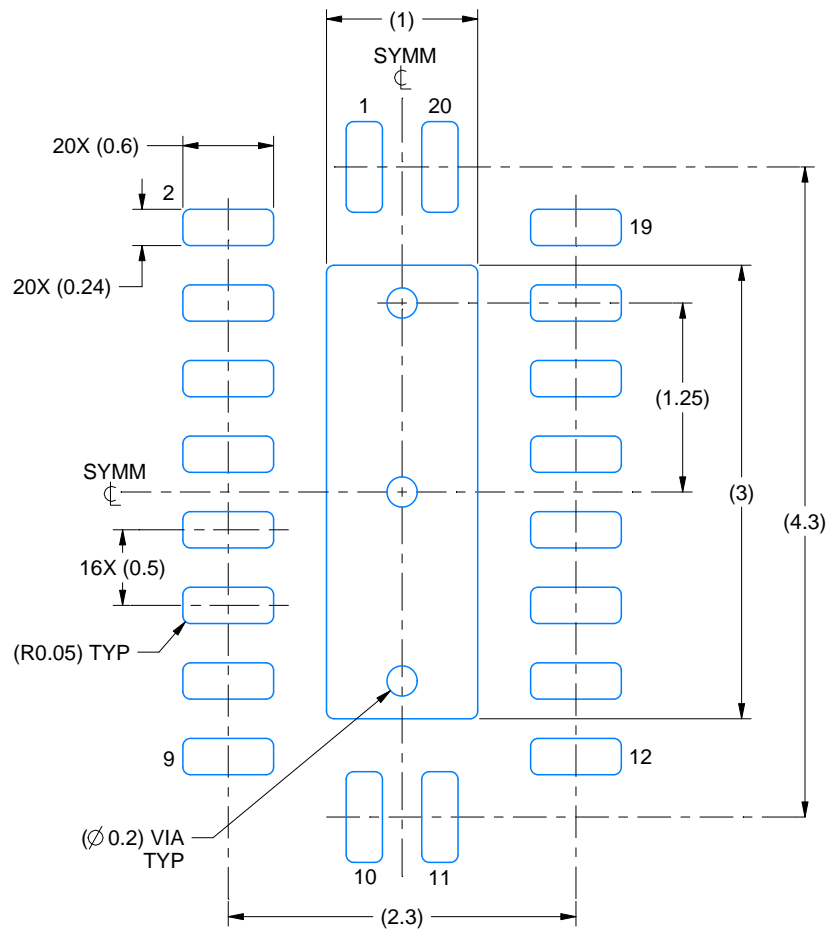
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

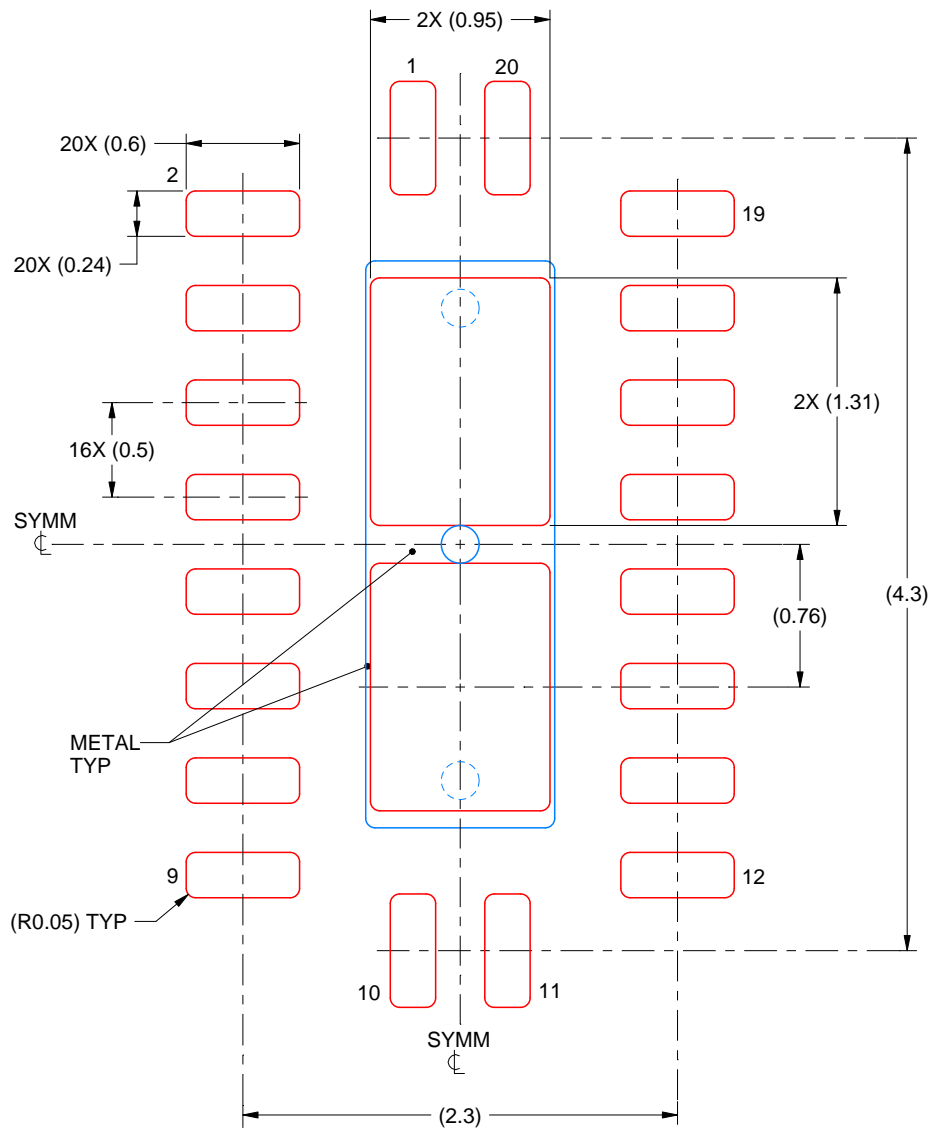
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 83% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:25X

4222490/B 02/2021

NOTES: (continued)

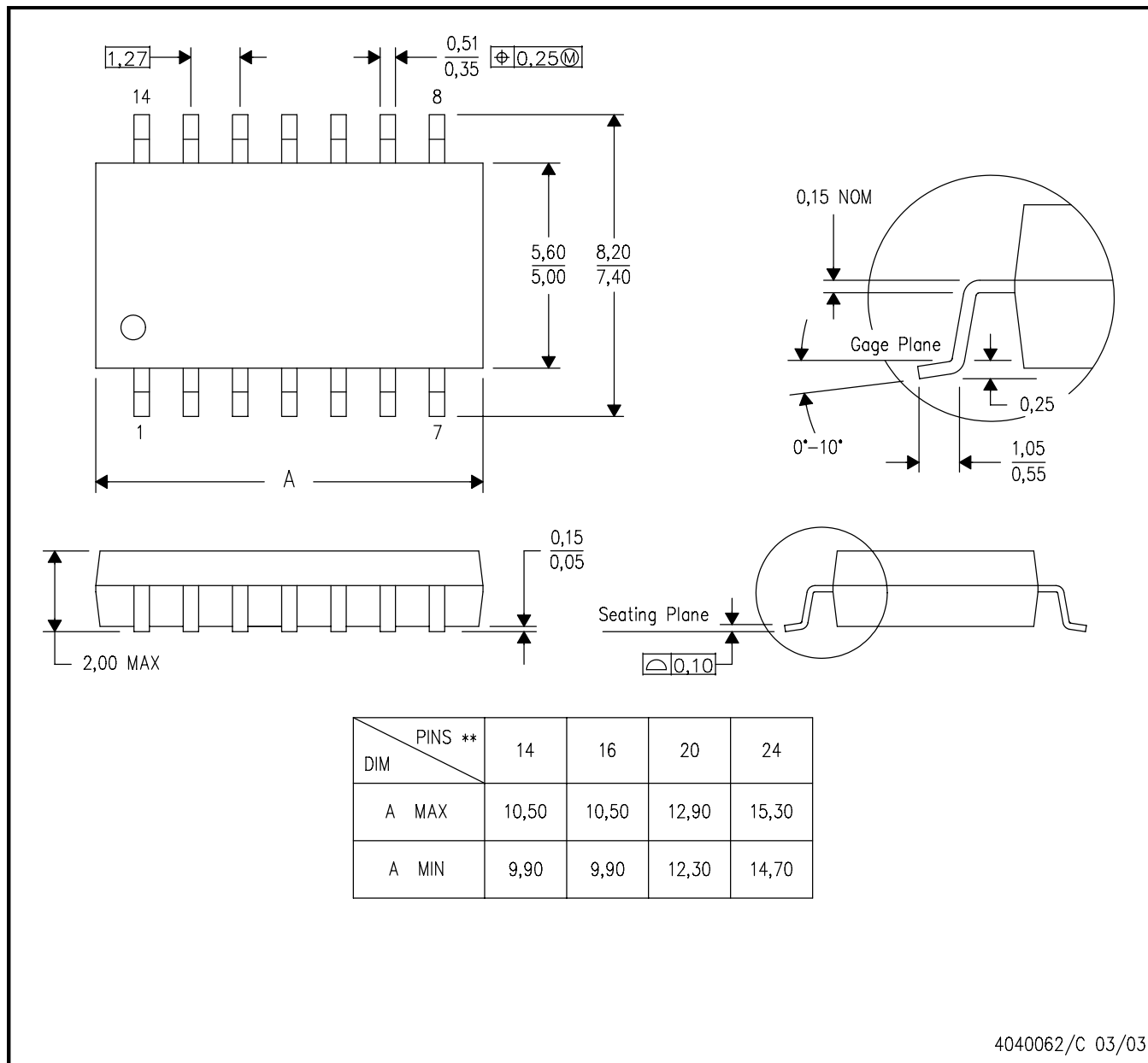
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

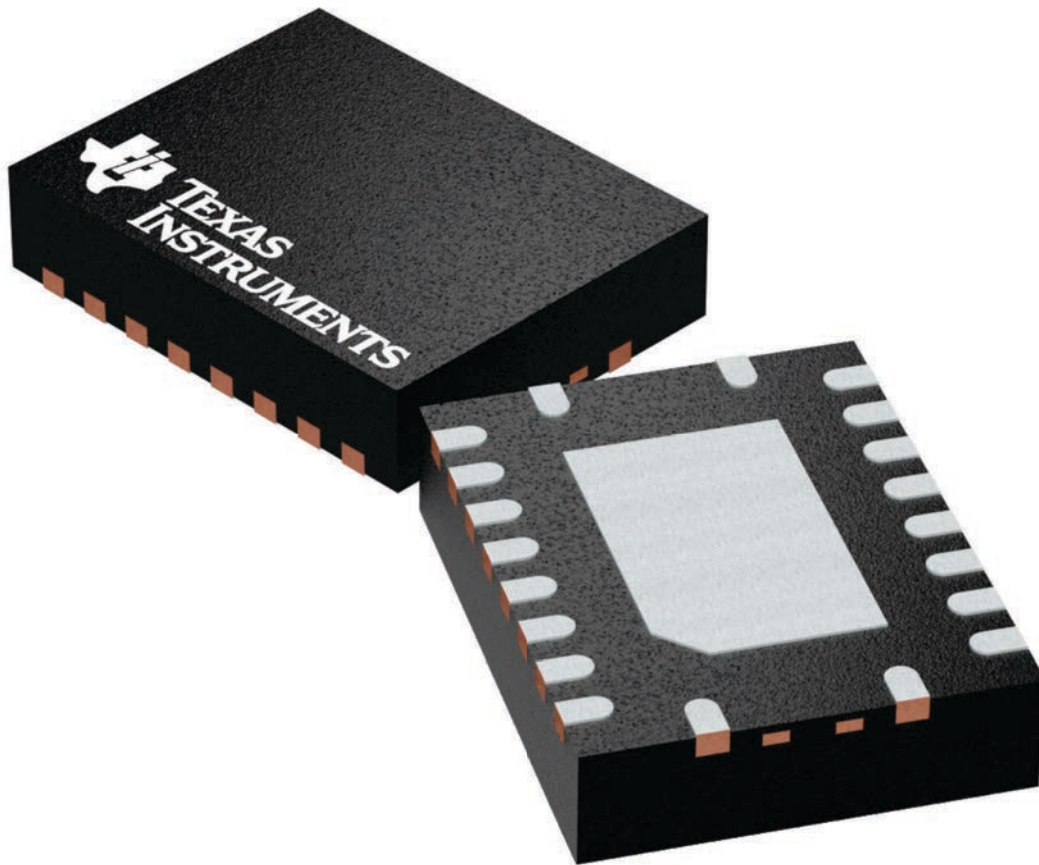
**RGY 20**

**VQFN - 1 mm max height**

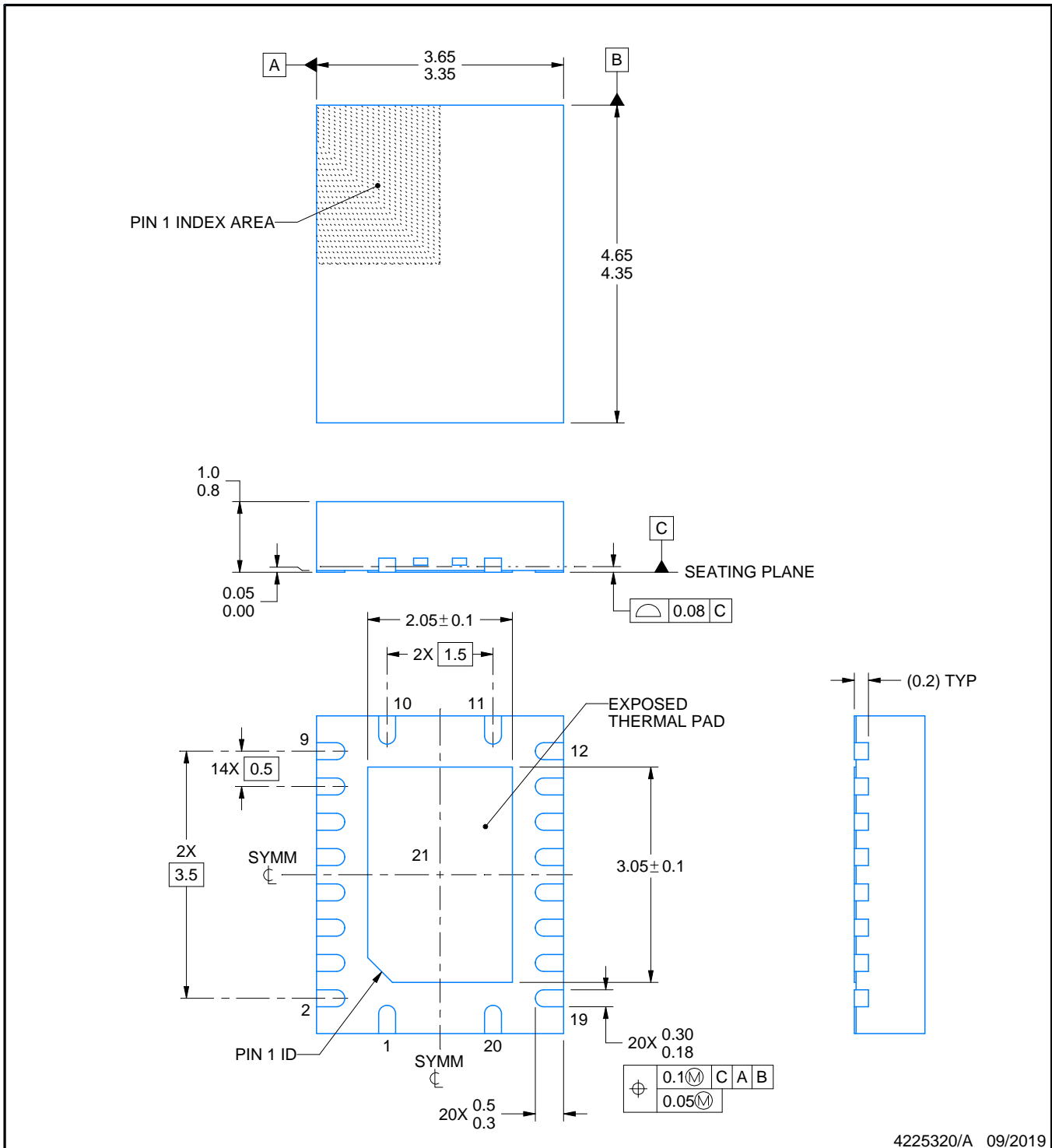
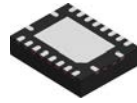
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

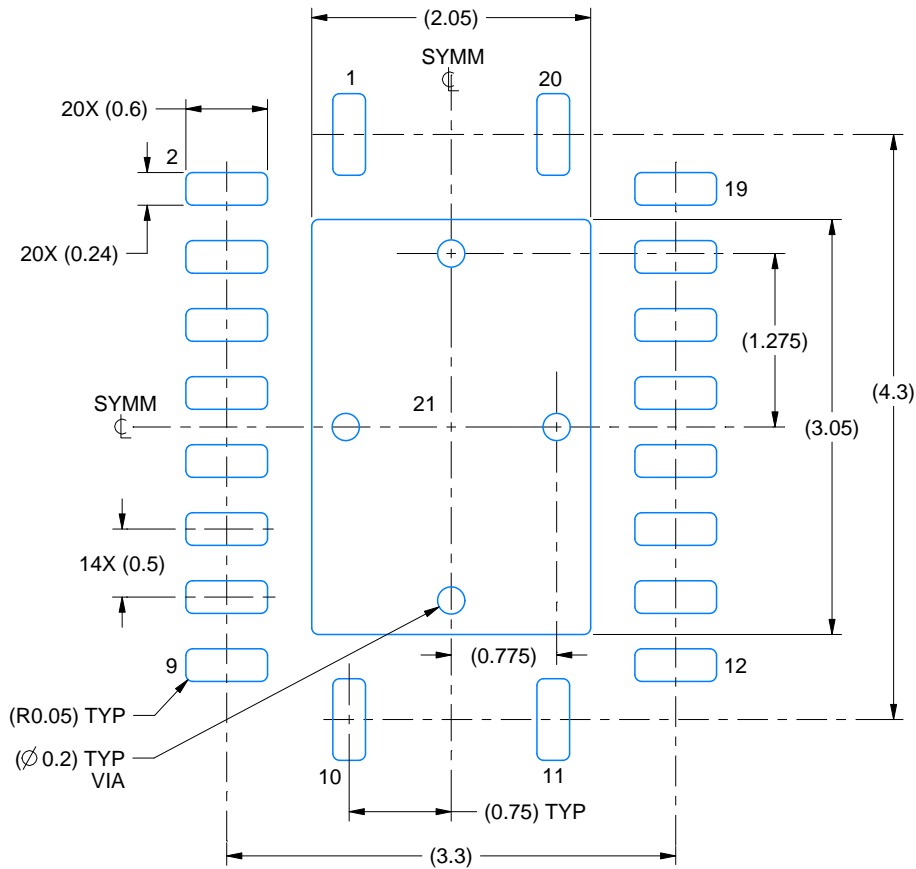
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

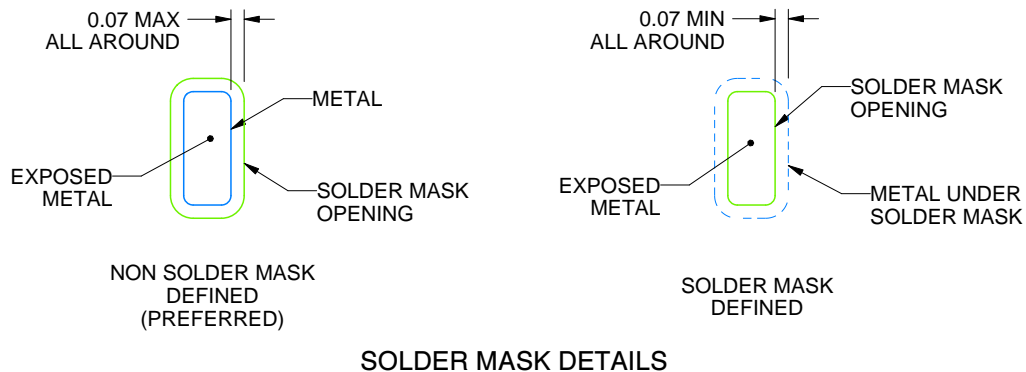
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

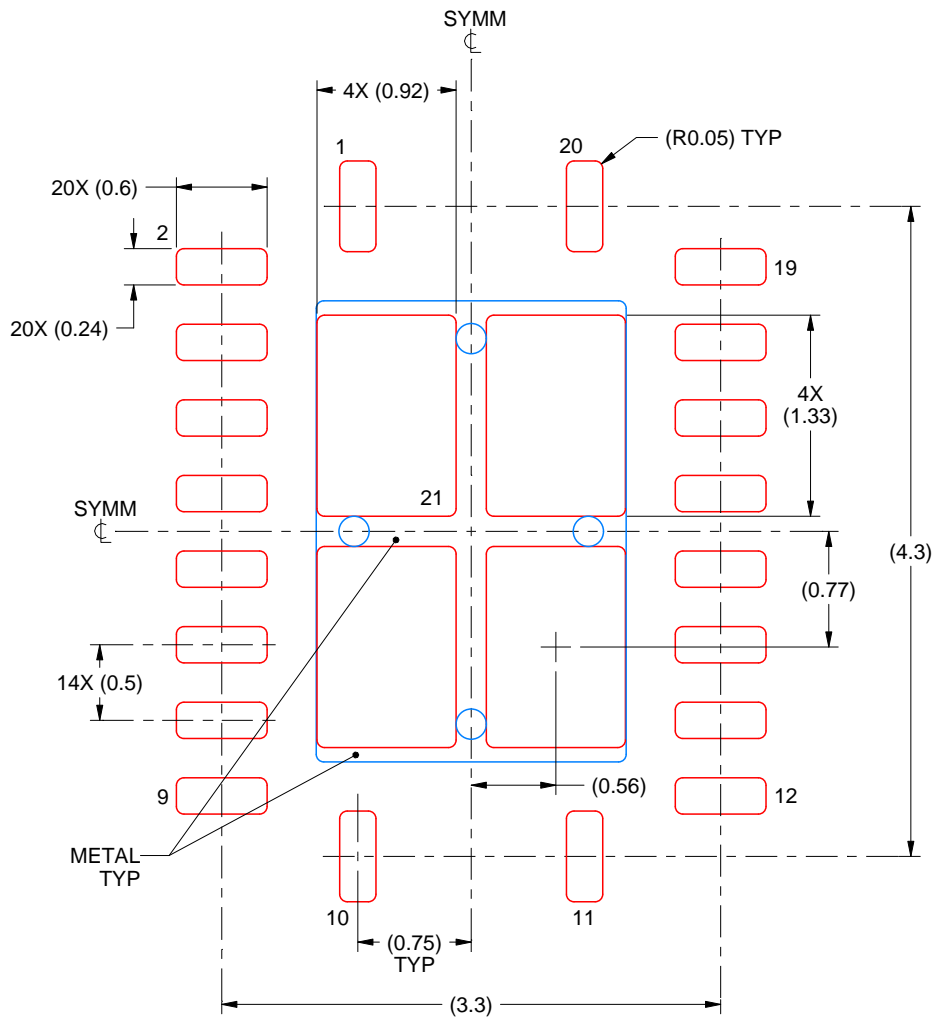
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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