



**THE DATASHEET OF  
AON6450L**



### General Description

The AON6450L is fabricated with SDMOS™ trench technology that combines excellent  $R_{DS(ON)}$  with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free

### Product Summary

#### Parameter

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	52A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 14.5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 7V$ )	< 17.5m $\Omega$

**100% UIS Tested!**  
**100%  $R_g$  Tested!**

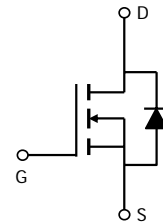
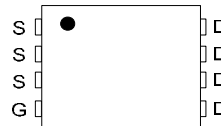


**Fits SOIC8 footprint !**



DFN5X6

#### Top View



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	52
		$T_C=100^\circ\text{C}$	33
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	110	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	9
		$T_A=70^\circ\text{C}$	7
Avalanche Current <sup>C</sup>	$I_{AR}$	41	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	84	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	83
		$T_C=100^\circ\text{C}$	33
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2.3
		$T_A=70^\circ\text{C}$	1.4
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	14	17	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A D</sup>		Steady-State	40	55
Maximum Junction-to-Case	$R_{\theta JC}$	1	1.5	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			10 50	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±25V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	2.8	3.4	4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	110			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		12.1 22.8	14.5 27.5	mΩ
		V <sub>GS</sub> =7V, I <sub>D</sub> =20A		14	17.5	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		52		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				52	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz	2000	2570	3100	pF
C <sub>oss</sub>	Output Capacitance		170	250	330	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		50	80	120	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.4	0.8	1.2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =20A	34	43	52	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge		9	11.5	14	nC
Q <sub>gs</sub>	Gate Source Charge		11	14	17	nC
Q <sub>gd</sub>	Gate Drain Charge		8	13.5	19	nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		15		ns
t <sub>r</sub>	Turn-On Rise Time			5		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			28.5		ns
t <sub>f</sub>	Turn-Off Fall Time			5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	17	24	31	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	75	108	140	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

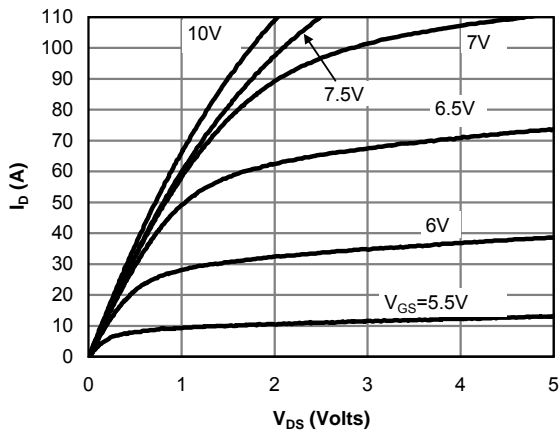
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

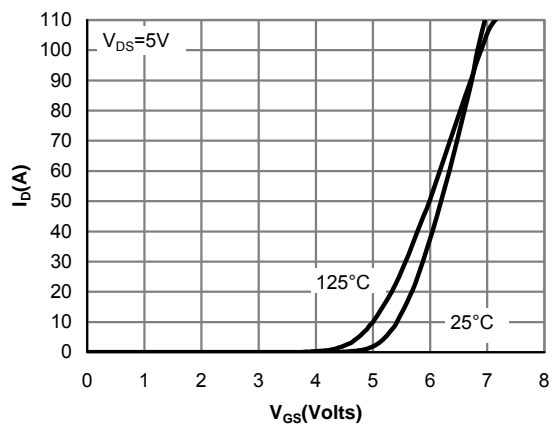
Rev 0: January 2009

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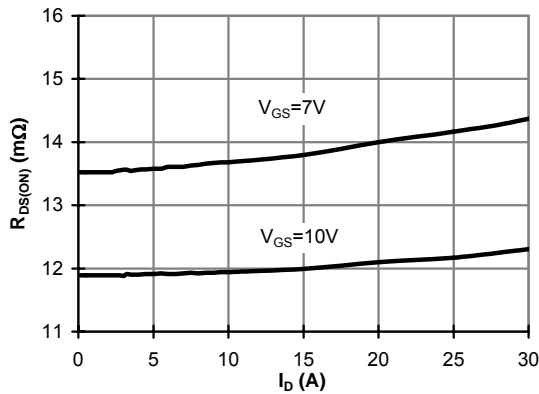
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



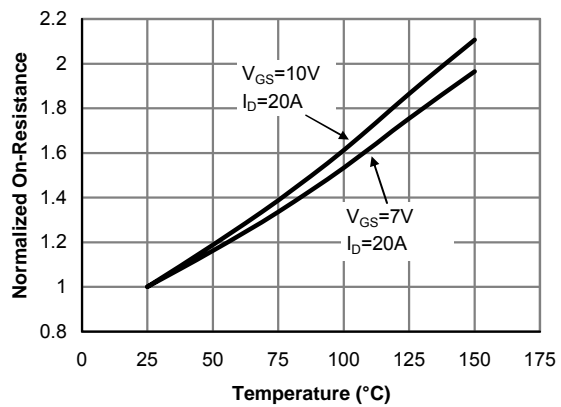
**Fig 1: On-Region Characteristics (Note E)**



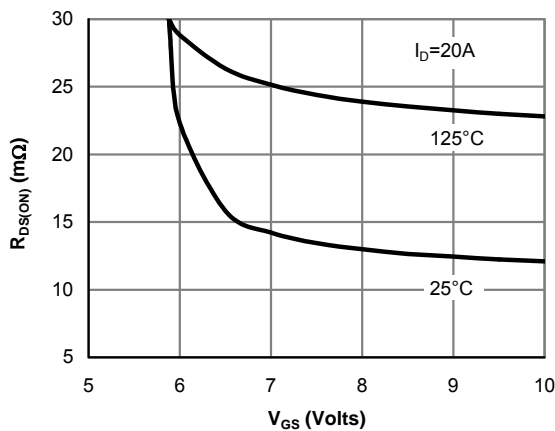
**Figure 2: Transfer Characteristics (Note E)**



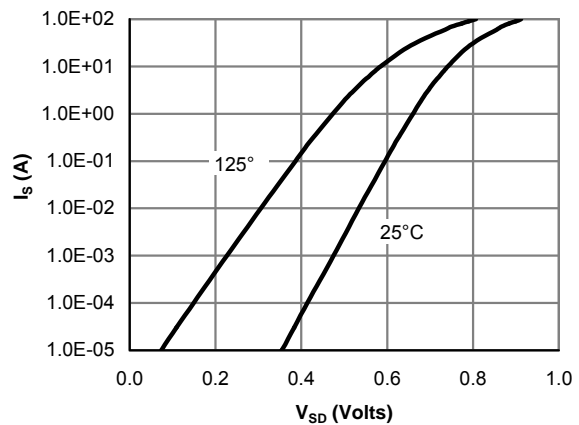
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

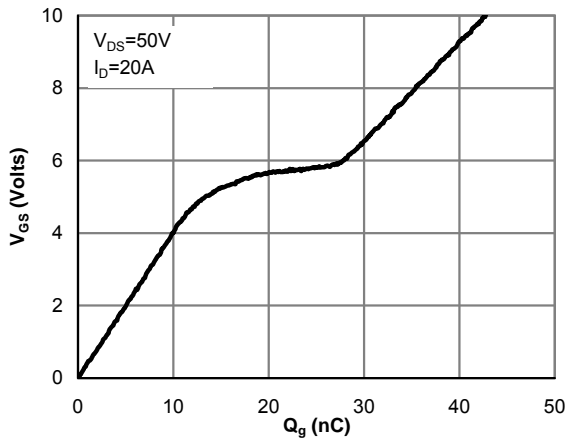


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

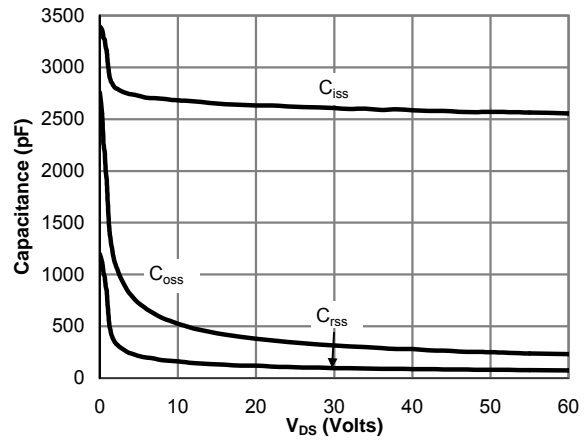


**Figure 6: Body-Diode Characteristics (Note E)**

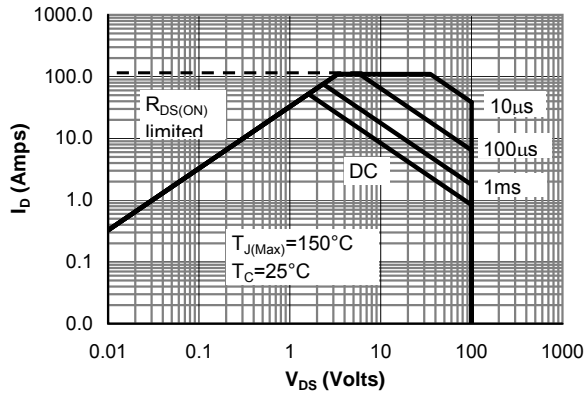
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



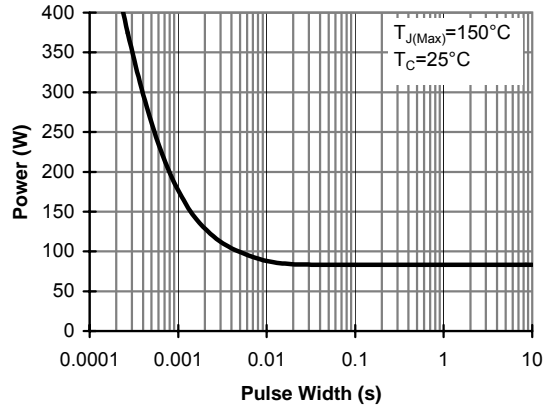
**Figure 7: Gate-Charge Characteristics**



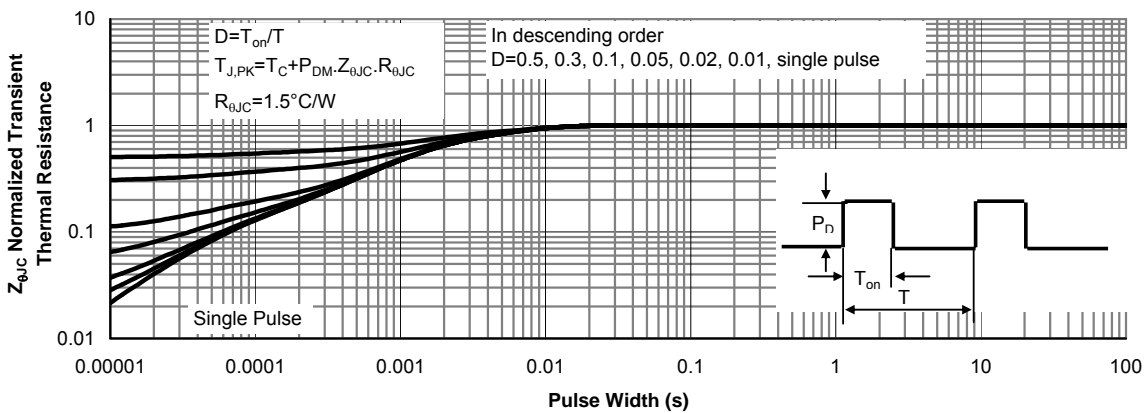
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

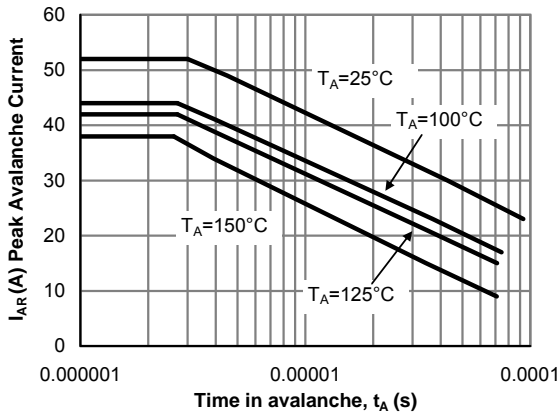


**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

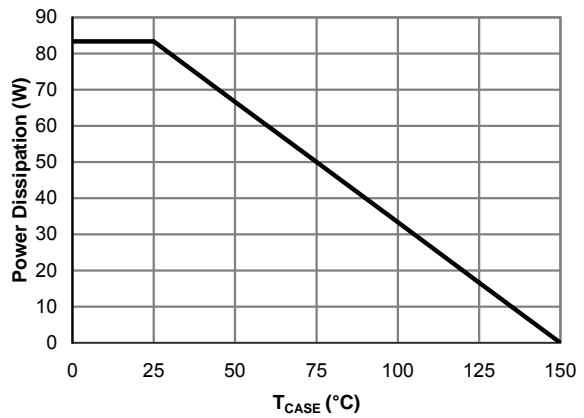


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

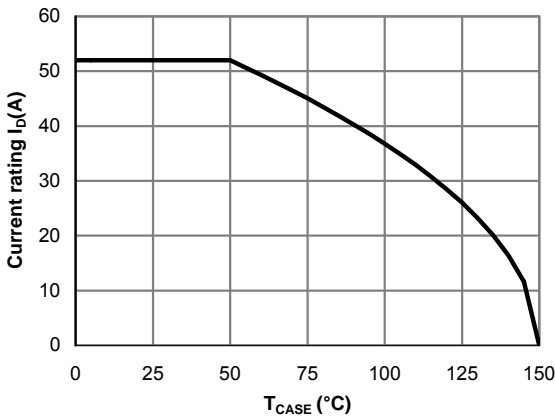
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



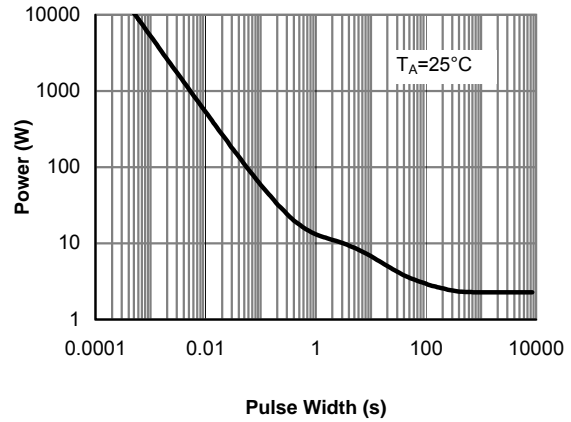
**Figure 12: Single Pulse Avalanche capability (Note C)**



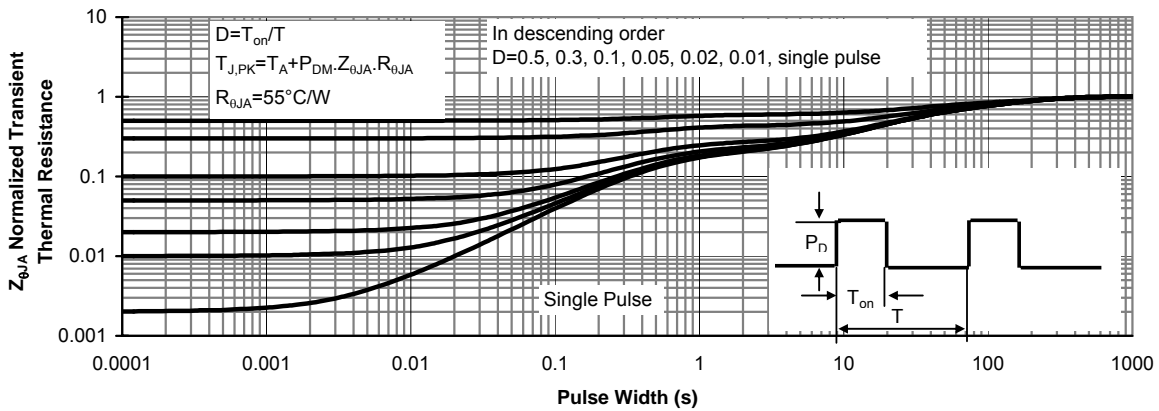
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

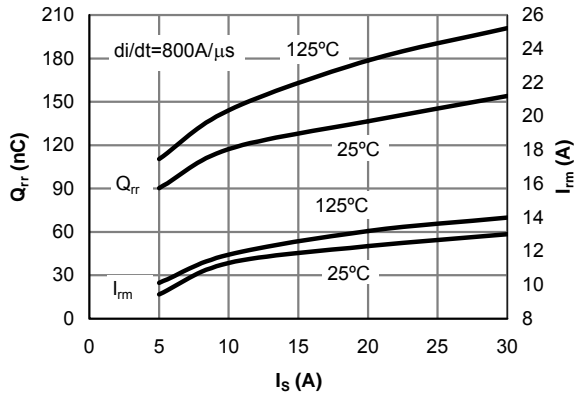


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)**

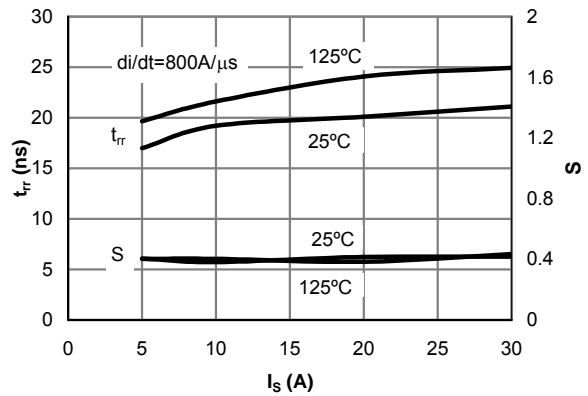


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)**

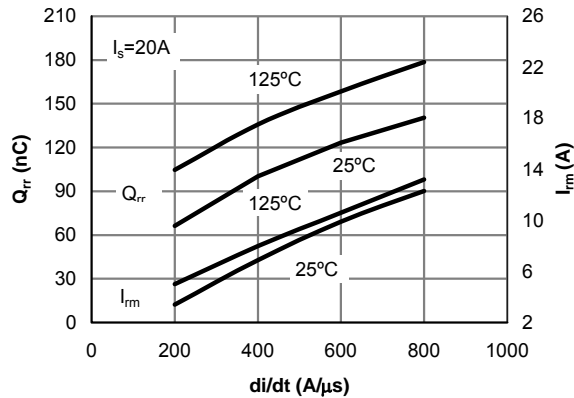
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



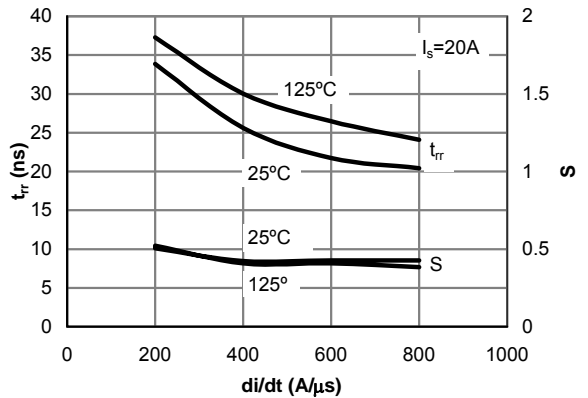
**Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current**



**Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current**

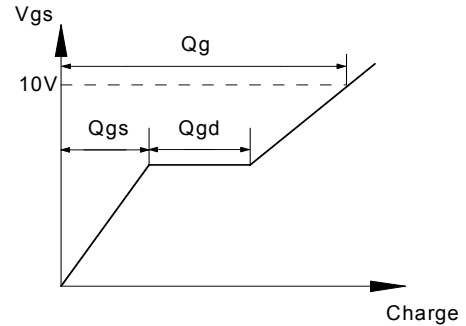
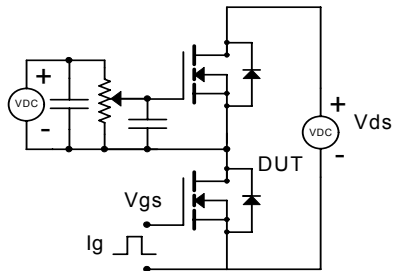


**Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt**

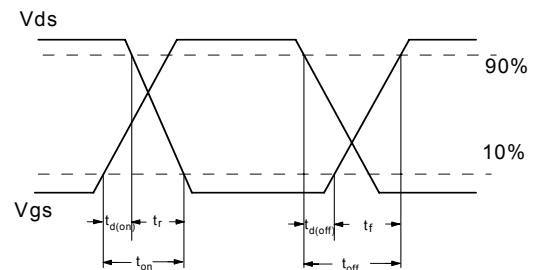
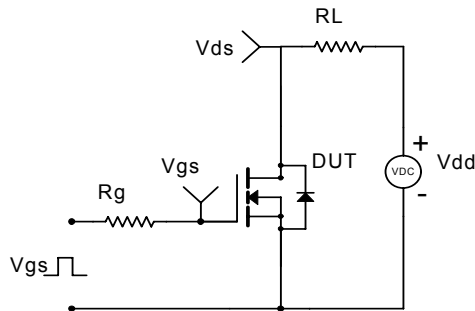


**Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt**

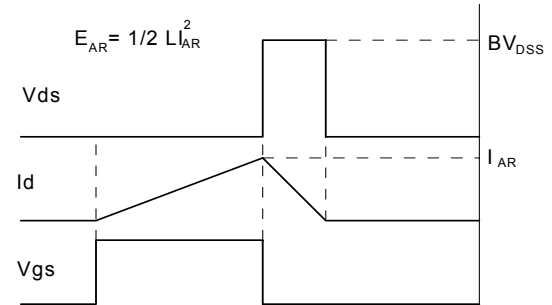
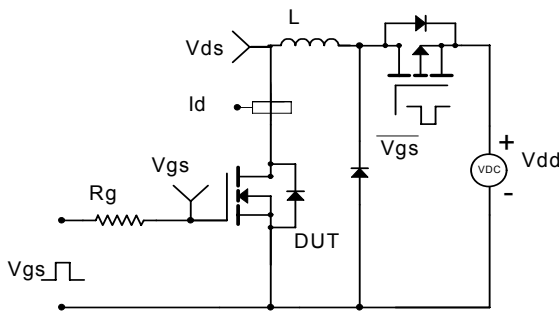
**Gate Charge Test Circuit & Waveform**



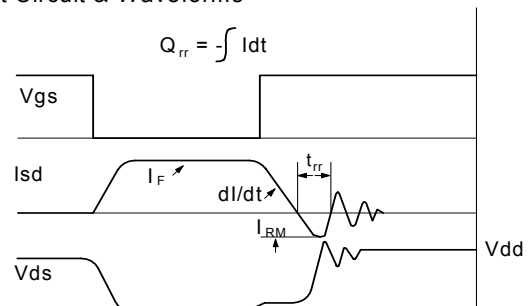
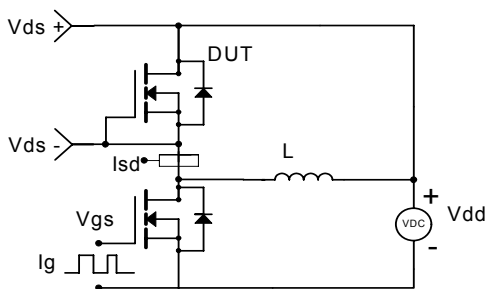
**Resistive Switching Test Circuit & Waveforms**



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