



**THE DATASHEET OF
SN65HVDA100QDRQ1**



SN65HVDA100-Q1 LIN Physical Interface

1 Features

- AEC-Q100 (Grade 1) qualified for automotive applications
- Compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, and ISO/DIS 17987-4 electrical physical layer (EPL) specification
- Extended operation with supply from 5 V to 27 V DC
- LIN Transmits speed up to 20-kbps (LIN specified maximum), high-speed receive capable
- Sleep mode: ultra-low current consumption allows wake-up events from:
 - LIN bus
 - wake-up through EN
- Wake-up request on RXD pin
- Wake-up source recognition on TXD pin
- Interfaces to MCU with 5-V or 3.3-V I/O pins
- High electromagnetic compatibility (EMC)
- Control of external voltage regulator (INH Pin)
- Supports ISO9141 (K-line)
- ESD protection to ± 12 kV (human body model) on LIN pin
- LIN pin handles voltage from -27 V to 45 V (short to battery or ground)
- Survives transient damage in automotive environment (ISO 7637)
- Undervoltage protection on V_{SUP}
- TXD dominant state time-out protection
- Prevention of false wakeups with false wake-up lockout
- Thermal shutdown
- Unpowered node or ground disconnection failsafe at system level, node does not disturb bus (no load on bus)

2 Applications

- Automotive
- [Industrial sensing](#)
- White goods distributed control

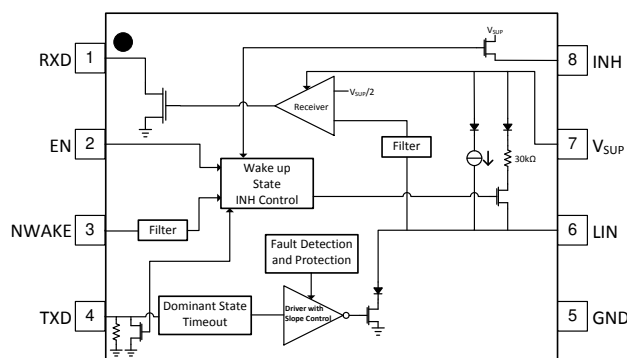
3 Description

The SN65HVDA100-Q1 device is a Local Interconnect Network (LIN) physical interface, which integrates the serial transceiver with wakeup and protection features. The LIN bus is a single-wire bidirectional bus typically used for low-speed in-vehicle networks using data rates from 2.4 kbps to 20 kbps. The LIN protocol output data stream on TXD is converted by the SN65HVDA100-Q1 into the LIN bus signal through a current-limited wave-shaping driver as outlined by the LIN Physical Layer Specification and ISO 17987. The receiver converts the data stream from the LIN bus and outputs the data stream through RXD. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pullup resistor (30 k Ω) and series diode, so no external pullup components are required for responder applications. Commander applications require an external pullup resistor (1 k Ω) plus a series diode per the LIN specification.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|----------------|------------------------|--------------------------|
| SN65HVDA100-Q1 | SOIC (8) | 4.90 mm \times 3.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



SN65HVDA100-Q1 Block Diagram



Table of Contents

| | | | |
|---|----|--|----|
| 1 Features | 1 | 9.3 Feature Description..... | 14 |
| 2 Applications | 1 | 9.4 Device Functional Modes..... | 18 |
| 3 Description | 1 | 10 Application and Implementation | 21 |
| 4 Description (continued) | 2 | 10.1 Application Information..... | 21 |
| 5 Revision History | 3 | 10.2 Typical Application..... | 21 |
| 6 Pin Configuration and Functions | 4 | 11 Power Supply Recommendations | 22 |
| 7 Specifications | 5 | 12 Layout | 23 |
| 7.1 Absolute Maximum Ratings ^{(1) (2)} | 5 | 12.1 Layout Guidelines..... | 23 |
| 7.2 ESD Ratings..... | 5 | 12.2 Layout Example..... | 24 |
| 7.3 Recommended Operating Conditions..... | 5 | 13 Device and Documentation Support | 25 |
| 7.4 Thermal Information..... | 6 | 13.1 Documentation Support..... | 25 |
| 7.5 Electrical Characteristics..... | 6 | 13.2 Receiving Notification of Documentation Updates..... | 25 |
| 7.6 Switching Characteristics..... | 8 | 13.3 Support Resources..... | 25 |
| 7.7 Dissipation Ratings..... | 9 | 13.4 Trademarks..... | 25 |
| 7.8 Typical Characteristics..... | 12 | 13.5 Electrostatic Discharge Caution..... | 25 |
| 8 Parameter Measurement Information | 13 | 13.6 Glossary..... | 25 |
| 9 Detailed Description | 14 | 14 Mechanical, Packaging, and Orderable Information | 25 |
| 9.1 Overview..... | 14 | | |
| 9.2 Functional Block Diagram..... | 14 | | |

4 Description (continued)

In sleep mode, low quiescent current is needed even though the wake-up circuits remain active and allow for remote wake up through the LIN bus or local wake up through the NWake or EN pins.

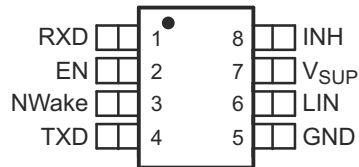
The SN65HVDA100-Q1 has been designed for operation in the harsh automotive environment. The device also prevents back-feed current through LIN to the supply input in case of a ground shift or supply voltage disconnection. The device also features undervoltage, overtemperature, and loss-of-ground protection. In the event of a fault condition, the transmitter is immediately switched off and remains off until the fault condition is removed.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (July 2015) to Revision D (April 2022) | Page |
|--|-------------|
| • Changed the <i>Features</i> list | 1 |
| • Changed all instances of legacy terminology to commander and responder where mentioned..... | 1 |
| • Replaced LIN 2.1 with ISO 17987-4 in the Absolute Maximum Ratings table..... | 5 |
| • Added HBM and CDM classification levels to the ESD Ratings table | 5 |
| • Replaced LIN 2.1 with ISO 17987-4 in the Recommended Operating Conditions table..... | 5 |
| • Replaced LIN 2.1 with ISO 17987-4 in the Electrical Characteristics table..... | 6 |
| • Deleted test Conditions for V_{SUP} in the Electrical Characteristics table..... | 6 |
| • Replaced LIN 2.1 with ISO 17987-4 in the Switching Characteristics table..... | 8 |
| • Changed the Application hint to a Note in the TXD Dominant State Timeout section..... | 16 |
| • Changed the Application hint to a Note in the Standby Mode section..... | 19 |
| • Changed the Application hint to a Note in the Mode Transitions section..... | 20 |
| <hr/> | |
| Changes from Revision B (January 2014) to Revision C (July 2015) | Page |
| • Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| <hr/> | |
| Changes from Revision A (January 2013) to Revision B (January 2014) | Page |
| • Added new Mode Transitions section, including a new figure..... | 20 |
| • Revised the application schematic diagram..... | 21 |
| <hr/> | |
| Changes from Revision * (November 2011) to Revision A (January 2013) | Page |
| • Deleted -03V to 45V from the 1.5 row in the abs max table, units column..... | 5 |
| • Changed added Delta and corrected Hysteresis in Electrical Characteristics table, row 4.4 and changed the TYP column from 4.5 to 0.2..... | 6 |
| • Deleted rows 9.1 and 9.2 from the Electrical Characteristics table..... | 6 |
| • Added Minimum to the statement in parens in front of dominant, row 11.9 of the Switching Characteristics table..... | 8 |

6 Pin Configuration and Functions



**Figure 6-1. D Package, 8-Pin SOIC
(Top View)**

Table 6-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|------------------|-----|--------|---|
| NAME | NO. | | |
| EN | 2 | I | Enable input |
| GND | 5 | GND | Ground |
| INH | 8 | O | Inhibit controls external voltage regulator with inhibit input |
| LIN | 6 | I/O | LIN bus single-wire transmitter and receiver |
| NWake | 3 | I | High-voltage input for device wake up |
| RXD | 1 | O | RXD output (open-drain) interface reporting state of LIN bus voltage |
| TXD | 4 | I | TXD input interface to control state of LIN output |
| V _{SUP} | 7 | Supply | Device supply voltage (connected to battery in series with external reverse blocking diode) |

7 Specifications

7.1 Absolute Maximum Ratings^{(1) (2)}

| | | MIN | MAX | UNIT | |
|--------------------|--|--------------|------------------------|------|---|
| V _{SUP} | Supply line supply voltage (ISO 17987-4 Param 11) | -0.3 | 45 | V | |
| V _{LIN} | LIN input voltage | -27 | 45 | V | |
| V _{NWAKE} | NWake input voltage (through serial resistor ≥ 2 kΩ) | -0.3 | 45 | V | |
| I _O | Output current | -50 | 2 | mA | |
| V _{INH} | INH voltage | -0.3 | V _{sup} + 0.3 | V | |
| V _{Logic} | Logic pin voltage | RXD, TXD, EN | -0.3 | 5.5 | V |
| T _A | Operational free-air (ambient) temperature | -40 | 125 | °C | |
| T _J | Junction temperature | -40 | 150 | °C | |
| T _{LEAD} | Lead temperature (soldering, 10 seconds) | | 260 | °C | |
| T _{stg} | Storage temperature | -65 | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

7.2 ESD Ratings

| | | | VALUE | UNIT | |
|--------------------|-------------------------|---|---|--------|---|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins HBM ESD classification level 3A | ±4000 | V |
| | | | LIN bus pin ⁽²⁾ HBM ESD classification level 3B | ±12000 | |
| | | | NWake pin ⁽³⁾ HBM ESD classification level 3B | ±11000 | |
| | | Charged device model (CDM), per AEC Q100-011 ⁽¹⁾ | CDM ESD classification level C6 | ±1500 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) Test method based upon AEC-Q100-002, LIN bus pin stressed with respect to GND.
- (3) Test method based upon AEC-Q100-002, NWake pin stressed with respect to GND.

7.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|--------------------|---|-----|------|------|
| V _{SUP} | Supply line supply voltage (ISO 17987-4 Param 10) | 5 | 27 | V |
| V _{LIN} | LIN input voltage | 0 | 18 | V |
| V _{NWAKE} | NWake input voltage | 0 | 27 | V |
| V _{INH} | INH voltage | 0 | 27 | V |
| V _{Logic} | Logic voltage | 0 | 5.25 | V |
| T _A | Operational free-air temperature (see Section 7.4) | -40 | 125 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN65HVDA100-Q1 | |
|-------------------------------|--|----------------|------|
| | | D (SOIC) | |
| | | 8 PINS | |
| | | | UNIT |
| R _{θJA} | Junction-to-ambient thermal resistance | 112.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 66.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 52.9 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 19.3 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 52.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

V_{SUP} = 5V to 27 V, T_J = –40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|------------------------------------|--|---|------|--------------------|------|------|----|
| V_{SUP} SUPPLY | | | | | | | |
| V _{SUP} | Operational supply voltage (ISO 17987-4 Param 10) ⁽²⁾ | | 5 | 14 | 27 | V | |
| V _{SUP} | Nominal supply voltage (ISO 17987-4 Param 10) | Normal and standby modes | 7 | 14 | 18 | V | |
| | | Sleep mode | 7 | 12 | 18 | | |
| UV _{SUP} | Undervoltage V _{SUP} threshold | | 4.35 | | 4.65 | V | |
| UV _{HYS} | Delta hysteresis voltage for V _{SUP} undervoltage threshold | | | 0.2 | | V | |
| I _{SUP} | Supply current | Normal mode, EN = high, Bus dominant (total bus load where R _{LIN} ≥ 500 Ω and C _{LIN} ≤ 10 nF (see Figure 8-1) ⁽³⁾ , INH = V _{SUP} , NWake = V _{SUP} | | 1.2 | 7.5 | mA | |
| | | Standby mode, EN = low, Bus dominant (total bus load where R _{LIN} ≥ 500 Ω and C _{LIN} ≤ 10 nF (see Figure 8-1) ⁽³⁾ , INH = V _{SUP} , NWake = V _{SUP} | | 1 | 2.1 | mA | |
| | | Normal mode, EN = high, Bus recessive, LIN = V _{SUP} , INH = V _{SUP} , NWake = V _{SUP} | | | 450 | 775 | μA |
| | | Standby mode, EN = low, Bus recessive, LIN = V _{SUP} , INH = V _{SUP} , NWake = V _{SUP} | | | 450 | 775 | μA |
| | | Sleep mode, 7 V < V _{SUP} ≤ 14 V, LIN = V _{SUP} , NWake = V _{SUP} , EN = 0 V, TXD and RXD floating | | | 10 | 20 | μA |
| | | Sleep mode, 14 V < V _{SUP} < 27 V, LIN = V _{SUP} , NWake = V _{SUP} , EN = 0 V, TXD and RXD floating | | | | | 30 |
| RXD OUTPUT PIN (OPEN DRAIN) | | | | | | | |
| V _O | Output voltage ⁽⁴⁾ | | –0.3 | | 5.5 | V | |
| I _{OL} | Low-level output current, open drain | LIN = 0 V, RXD = 0.4 V | 3.5 | | | mA | |
| I _{IKG} | Leakage current, high-level | LIN = V _{SUP} , RXD = 5 V | –5 | 0 | 5 | μA | |
| TXD INPUT/OUTPUT PIN | | | | | | | |
| V _{IL} | Low-level input voltage | | –0.3 | | 0.8 | V | |
| V _{IH} | High-level input voltage | | 2 | | 5.5 | V | |
| V _{IT} | Input threshold hysteresis voltage | | 30 | | 500 | mV | |

7.5 Electrical Characteristics (continued)

 $V_{SUP} = 5V \text{ to } 27V$, $T_J = -40^\circ C \text{ to } 150^\circ C$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|---|---|------------------------|----------------------|------------------------|-------------|
| | Pulldown resistor | | 125 | 350 | 800 | k Ω |
| I_{IL} | Low-level input leakage current | TXD = Low | -5 | 0 | 5 | μA |
| I_{TXD_Wake} | Local wake up source re recognition TXD open drain drive | Standby mode after a local wake up event, $V_{LIN} = V_{SUP}$, $N_{Wake} = 0V$, TXD = 1V | 1.3 | 4.6 | 8 | mA |
| LIN PIN (REFERENCED TO V_{SUP}) | | | | | | |
| V_{OH} | High-level output voltage | LIN recessive, TXD = high, $I_O = 0mA$, $V_{SUP} = 14V$ | $V_{SUP} - 1$ | | | V |
| V_{OL} | Low-level output voltage | LIN dominant, TXD = low, $I_O = 40mA$, $V_{SUP} = 14V$ | $0.2 \times V_{SUP}$ | | | V |
| I_L | Limiting current (ISO 17987-4 Param 12) | TXD = 0V, $V_{LIN} = 7V \text{ to } 27V$ | 40 | 90 | 200 | mA |
| I_{LKG} | Receiver leakage current, dominant (ISO 17987-4 Param 13) | LIN = 0V, $7V \leq V_{SUP} \leq 18V$, Driver off | -1 | | | mA |
| | Receiver leakage current, recessive (ISO 17987-4 Param 14) | LIN $\geq V_{SUP}$, $7 \leq V_{SUP} \leq 18V$, Driver off LIN = V_{SUP} , driver off | 20 5 | | | μA |
| I_{LKG} | Leakage current, loss of ground (ISO 17987-4 Param 15) | GND = V_{SUP} , $V_{SUP} = 12V$, $0V < V_{LIN} < 18V$ | -1 | | | mA |
| I_{LKG} | Leakage current, loss of supply (ISO 17987-4 Param 16) | $7V < LIN \leq 12V$, $V_{SUP} = GND$ | 5 | | | μA |
| | | $12V < LIN \leq 18V$, $V_{SUP} = GND$ | 10 | | | |
| V_{IL} | Low-level input voltage (ISO 17987-4 Param 17) | LIN dominant (including LIN dominant for wake up) | $0.4 \times V_{SUP}$ | | | V |
| V_{IH} | High-level input voltage (ISO 17987-4 Param 18) | LIN recessive | $0.6 \times V_{SUP}$ | | | V |
| V_{BUS_CNT} | Receiver center threshold (ISO 17987-4 Param 19) | $V_{BUS_CNT} = (V_{IL} + V_{IH}) / 2$ | $0.475 \times V_{SUP}$ | $0.5 \times V_{SUP}$ | $0.525 \times V_{SUP}$ | V |
| V_{HYS} | Hysteresis voltage (ISO 17987-4 Param 20) | $V_{HYS} = (V_{IL} - V_{IH})$ | $0.05 \times V_{SUP}$ | | $0.175 \times V_{SUP}$ | V |
| V_{SERIAL_DIODE} | Serial diode in LIN termination pull up path (ISO 17987-4 Param 21) | By design and characterization | 0.4 | 0.7 | 1.0 | V |
| $R_{RESPONDER}$ | Pullup resistor to V_{SUP} (ISO 17987-4 Param 26) | Normal and standby modes | 20 | 30 | 60 | k Ω |
| R_{SLEEP} | Pullup current source to V_{SUP} | Sleep mode, $V_{SUP} = 14V$, LIN = GND | -2 | | | -20 μA |
| EN INPUT PIN | | | | | | |
| V_{IL} | Low-level input voltage | | -0.3 | | | 0.8 V |
| V_{IH} | High-level input voltage | | 2 | | | 5.5 V |
| V_{hys} | Hysteresis voltage | By design and characterization | 30 | | | 500 mV |
| | Pulldown resistor | | 125 | 350 | 800 | k Ω |
| I_{IL} | Low-level input current | EN = Low | -5 | | | 0 5 μA |

7.5 Electrical Characteristics (continued)

$V_{SUP} = 5V$ to $27V$, $T_J = -40^{\circ}C$ to $150^{\circ}C$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---------------------------|--|--|---------------|--------------------|-----------------|----------|
| INH OUTPUT PIN | | | | | | |
| $R_{DS(on)}$ | ON-state resistance | Between V_{SUP} and INH, INH = 2-mA drive, Normal or standby mode | | 25 | 50 | Ω |
| I_{IKG} | Leakage current | Low-power mode, $0 < INH < V_{SUP}$ | -5 | 0 | 5 | μA |
| NWAKE INPUT PIN | | | | | | |
| V_{IL} | Low-level input voltage | | -0.3 | | $V_{SUP} - 3.3$ | V |
| V_{IH} | High-level input voltage | | $V_{SUP} - 1$ | | $V_{SUP} + 0.3$ | V |
| | Pullup current | NWAKE = 0 V | -45 | -10 | -2 | μA |
| I_{IKG} | Leakage current | $V_{SUP} = NWAKE$ | -5 | 0 | 5 | μA |
| AC CHARACTERISTICS | | | | | | |
| D1 | Duty cycle 1 ⁽⁵⁾ (ISO 17987-4 Param 27) | $TH_{REC(max)} = 0.744 \times V_{SUP}$, $TH_{DOM(maximum)} = 0.581 \times V_{SUP}$, $V_{SUP} = 7V$ to $18V$, $t_{BIT} = 50 \mu s$ (20 kbps), $D1 = t_{Bus_rec(min)} / (2 \times t_{BIT})$ (see Figure 7-1) | 0.396 | | | |
| D2 | Duty cycle 2 ⁽⁵⁾ (ISO 17987-4 Param 28) | $TH_{REC(min)} = 0.422 \times V_{SUP}$, $TH_{DOM(min)} = 0.284 \times V_{SUP}$, $V_{SUP} = 7.6V$ to $18V$, $t_{BIT} = 50 \mu s$ (20 kbps), $D2 = t_{Bus_rec(max)} / (2 \times t_{BIT})$ (see Figure 7-1) | | | 0.581 | |
| D3 | Duty cycle 3 ⁽⁵⁾ (ISO 17987-4 Param 29) | $TH_{REC(max)} = 0.778 \times V_{SUP}$, $TH_{DOM(max)} = 0.616 \times V_{SUP}$, $V_{SUP} = 7V$ to $18V$, $t_{BIT} = 96 \mu s$ (10.4 kbps), $D3 = t_{Bus_rec(min)} / (2 \times t_{BIT})$ (see Figure 7-1) | 0.417 | | | |
| D4 | Duty cycle 4 ⁽⁵⁾ (ISO 17987-4 Param 30) | $TH_{REC(min)} = 0.389 \times V_{SUP}$, $TH_{DOM(min)} = 0.251 \times V_{SUP}$, $V_{SUP} = 7.6V$ to $18V$, $t_{BIT} = 96 \mu s$ (10.4 kbps), $D4 = t_{Bus_rec(max)} / (2 \times t_{BIT})$ (see Figure 7-1) | | | 0.59 | |

- (1) Typical values are given for $V_{SUP} = 14V$ at $25^{\circ}C$, except for low power mode where typical values are given for $V_{SUP} = 12V$ at $25^{\circ}C$.
- (2) All voltages are defined with respect to ground; positive currents flow into the SN65HVDA100-Q1 device.
- (3) In the dominant state, the supply current increases as the supply voltage increases due to the integrated LIN responder termination resistance. At higher voltages the majority of supply current is through the termination resistance. The minimum resistance of the LIN responder termination is 20 k Ω , so the maximum supply current attributed to the termination is: $I_{SUP(dom)max\ termination} \neq (V_{SUP} - (V_{LIN_Dominant} + 0.7V)) / 20\ k\Omega$.
- (4) RXD pin output is open drain. Output voltage is through external pullup resistance to logic supply of the system and impedance of the RXD pin.
- (5) Duty cycles: LIN driver bus load conditions (C_{LINBUS} , R_{LINBUS}): Load1 = 1 nF, 1 k Ω ; Load2 = 10 nF, 500 Ω . Duty cycles 3 and 4 are defined for 10.4-kbps operation. The SN65HVDA100-Q1 also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--|---|-----|-----|-----|---------|
| AC CHARACTERISTICS | | | | | | |
| t_{rx_pdr} | Receiver rising propagation delay time (ISO 17987-4 Param 31) | $R_{RXD} = 2.4\ k\Omega$, $C_{RXD} = 20\ pF$ (see Figure 7-2 and Figure 8-1) | | | 6 | μs |
| t_{rx_pdf} | Receiver falling propagation delay time (ISO 17987-4 Param 31) | $R_{RXD} = 2.4\ k\Omega$, $C_{RXD} = 20\ pF$ (see Figure 7-2 and Figure 8-1) | | | 6 | μs |

7.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|-----|-----|-----|---------|
| t_{rx_sym} | Rising edge with respect to falling edge ($t_{rx_sym} = t_{rx_pdf} - t_{rx_pdr}$) $R_{RXD} = 2.4$ k Ω , $C_{RXD} = 20$ pF (see Figure 7-2 and Figure 8-1) | -2 | | 2 | μ s |
| t_{NWake} | NWake filter time for local wakeup | 25 | 50 | 150 | μ s |
| t_{LINBUS} | LIN wake-up time (Minimum dominant time on LIN bus for wakeup) | 25 | 100 | 150 | μ s |
| t_{CLEAR} | Time to clear false wake-up prevention logic if LIN Bus had bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault) | 8 | 17 | 50 | μ s |
| t_{DST} | Dominant state time-out ⁽¹⁾ | 20 | 34 | 80 | ms |
| t_{MODE_CHANGE} | Mode change delay time | | | 5 | μ s |

(1) TXD Dominant state timeout limits the minimum data rate to 650 bps. The minimum datarates may be calculated by the following formulas. $DataRate_{Commander(min)} = t_{SYNC_DOM(max)} / t_{DST(min)}$ and $DataRate_{Responder(min)} = 9 + n_{margin} / t_{DST(min)}$ where n_{margin} is a safety margin. For responder node cases where $n_{margin} \leq 4$, the commander node case will be the limiting calculation.

7.7 Dissipation Ratings

| | TYP | MAX | UNIT |
|---|-----|-----|--------------|
| Thermal shutdown temperature | | 180 | $^{\circ}$ C |
| Thermal shutdown hysteresis | | 15 | $^{\circ}$ C |
| P_D Power Dissipation in normal mode (dominant) | 17 | 230 | mW |

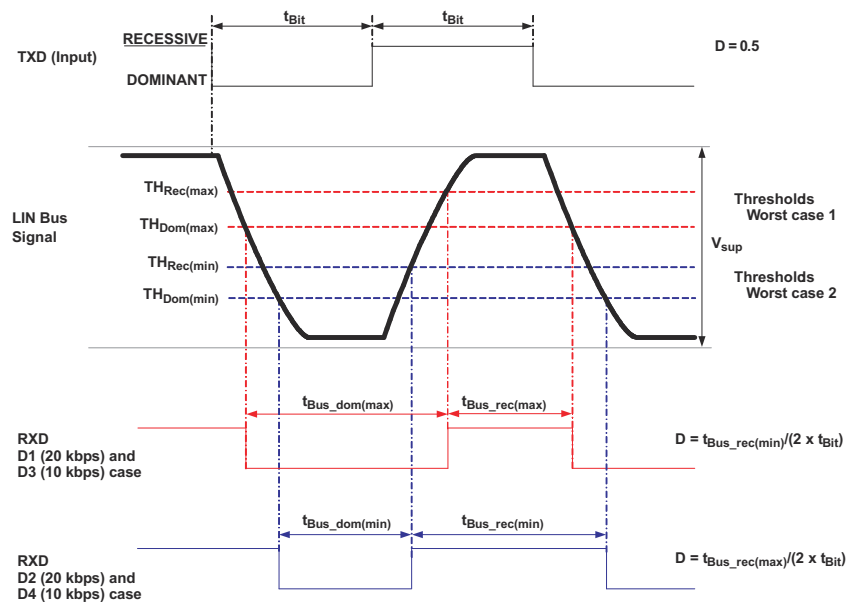


Figure 7-1. Definition of Bus Timing Parameters

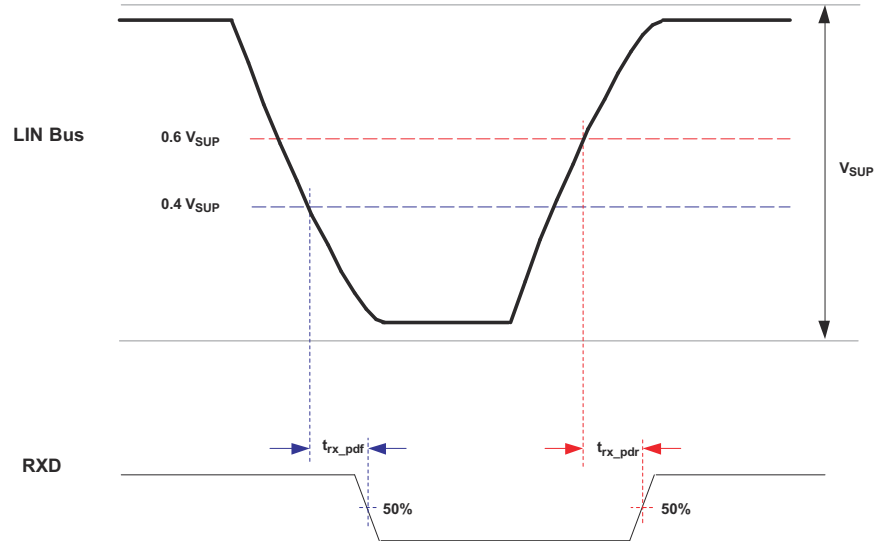


Figure 7-2. Propagation Delay

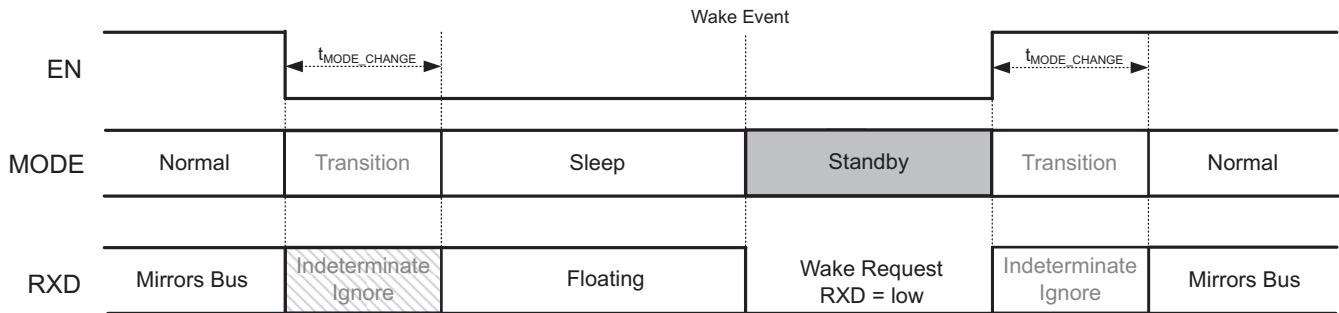


Figure 7-3. Mode Transitions

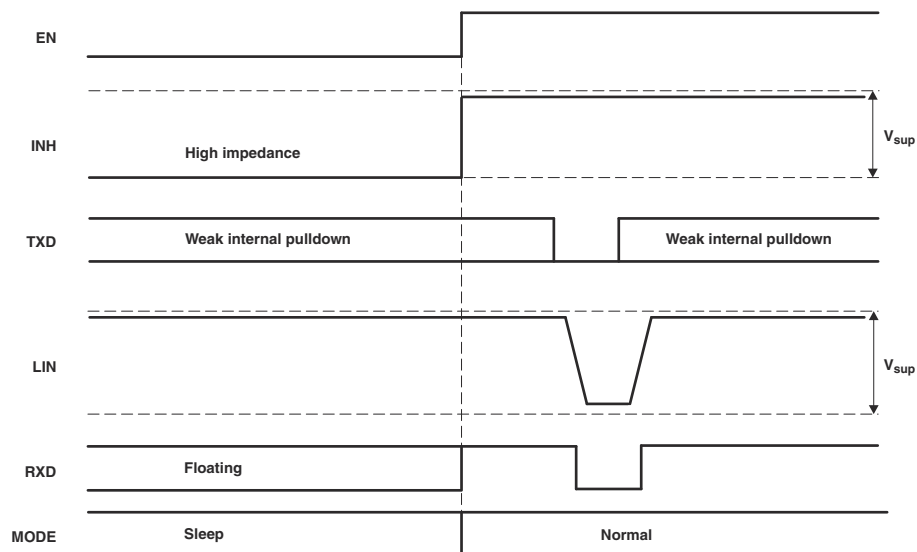


Figure 7-4. Wakeup Through EN

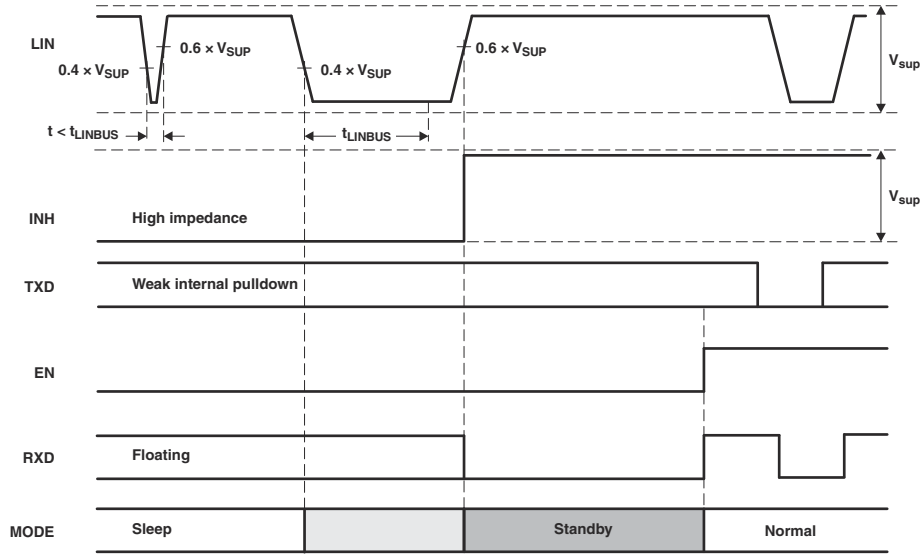


Figure 7-5. Wakeup Through LIN

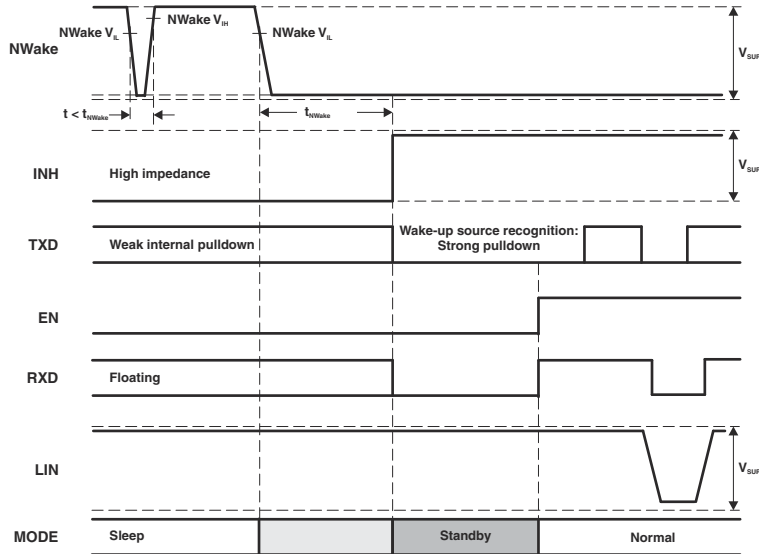


Figure 7-6. Wakeup Through NWake

7.8 Typical Characteristics

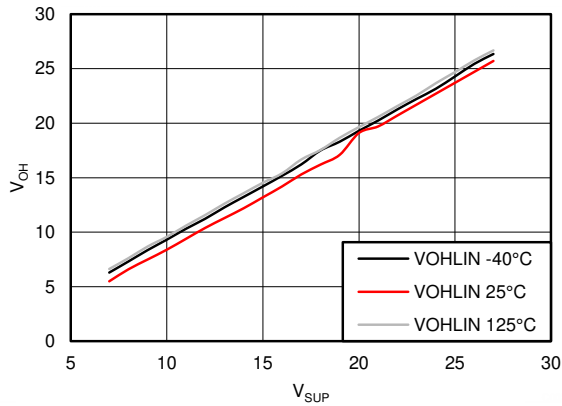


Figure 7-7. V_{OH} vs V_{SUPPLY} and Temperature

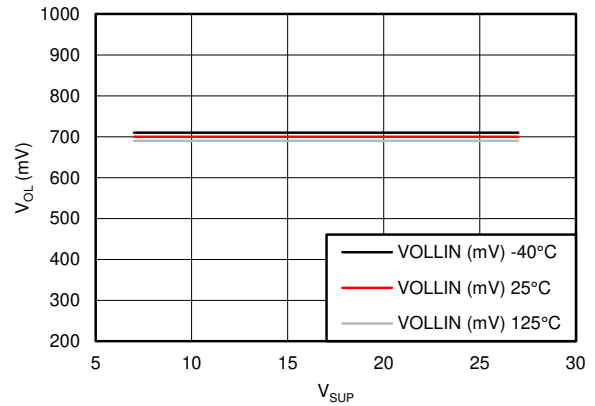


Figure 7-8. V_{OL} vs V_{SUPPLY} and Temperature

8 Parameter Measurement Information

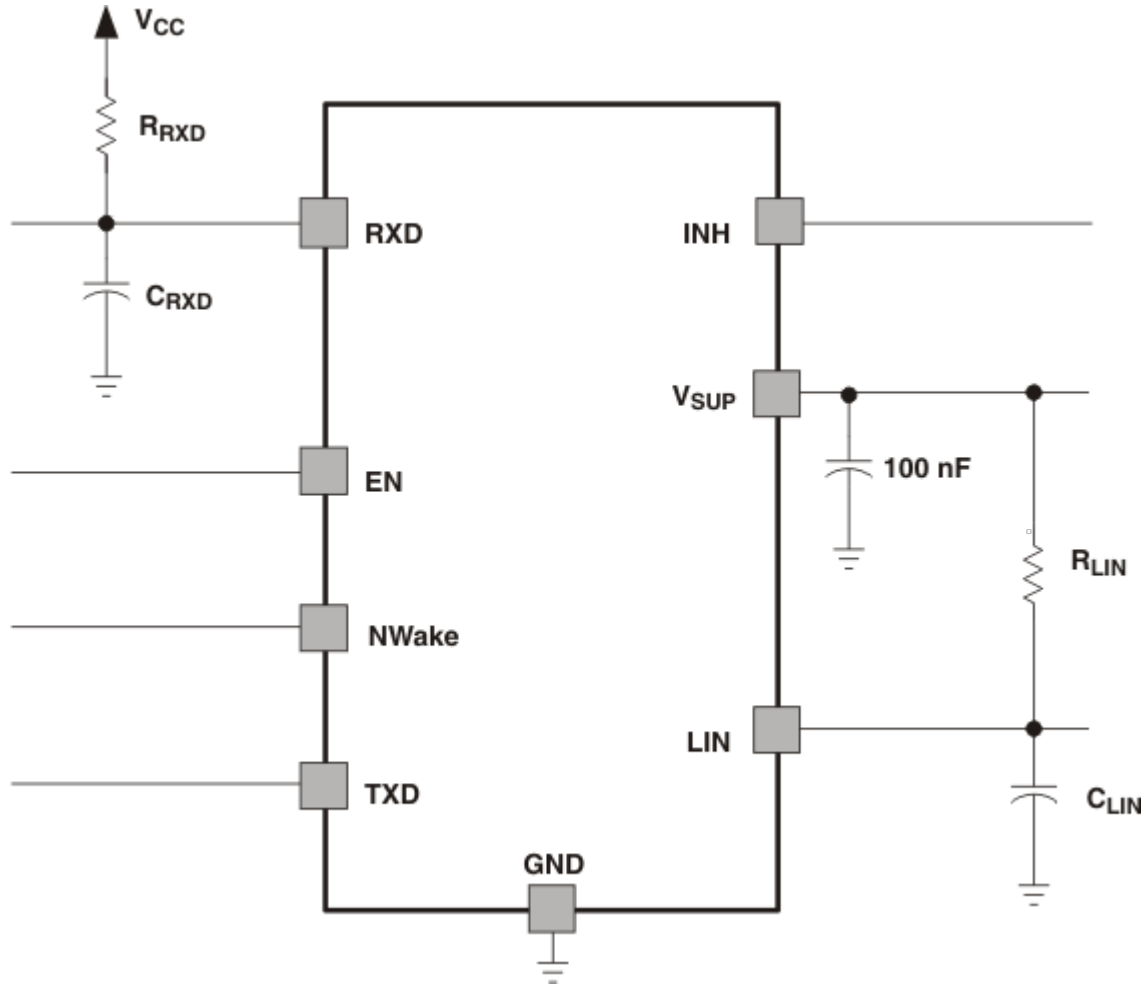


Figure 8-1. Test Circuit for AC Characteristics

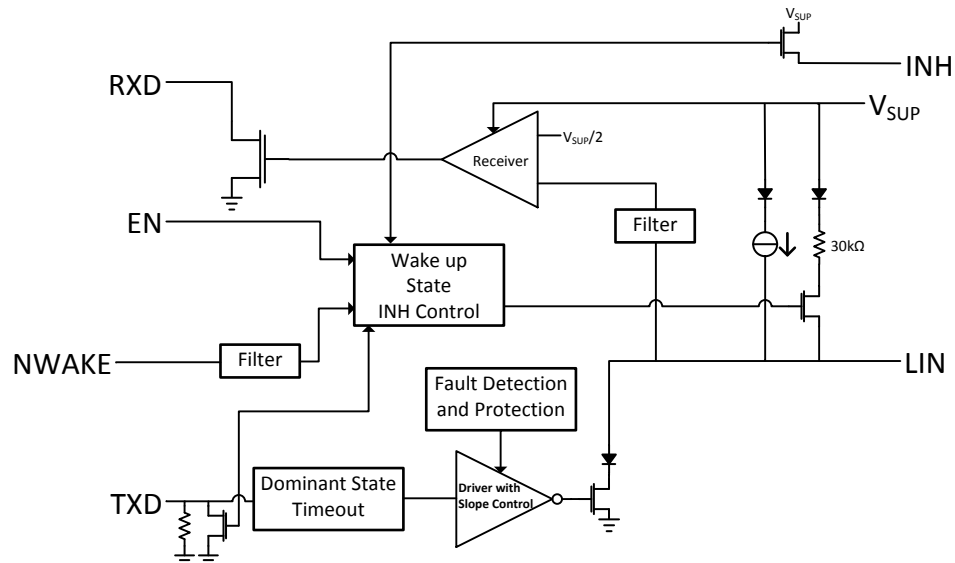
8.1

9 Detailed Description

9.1 Overview

The SN65HVDA100-Q1 LIN transceiver is a LIN (Local Interconnect Network) physical layer transceiver which integrates a serial transceiver with wake up and protection features. The LIN bus is a single wire, bi-directional bus that typically is used in low speed in vehicle networks with data rates that range from 2.4 kbps to 20 kbps.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

This I/O pin is the single-wire LIN bus transmitter and receiver. The LIN pin can survive excessive DC and transient voltages. There are no reverse currents from the LIN to supply (V_{SUP}), even in the event of a ground shift or loss of supply (V_{SUP}).

9.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low-side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pullup resistor with a serial diode structure to V_{SUP} , so no external pullup components are required for LIN responder mode applications. An external pullup resistor and a series diode to V_{SUP} must be added when the device is used for commander node applications.

9.3.1.2 LIN Receiver Characteristics

The receiver's characteristic thresholds are ratiometric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (>100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the SN65HVDA100-Q1 to be used for high-speed downloads at end-of-line production or other applications. The actual data rates achievable depend on system time constants (bus capacitance and pullup resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pullup resistor with a serial diode structure from LIN to V_{SUP} , so no external pullup components are required for LIN responder mode applications. An external pullup resistor (1 k Ω) and a series diode to V_{SUP} must be added when the device is used for commander node applications per the LIN specification.

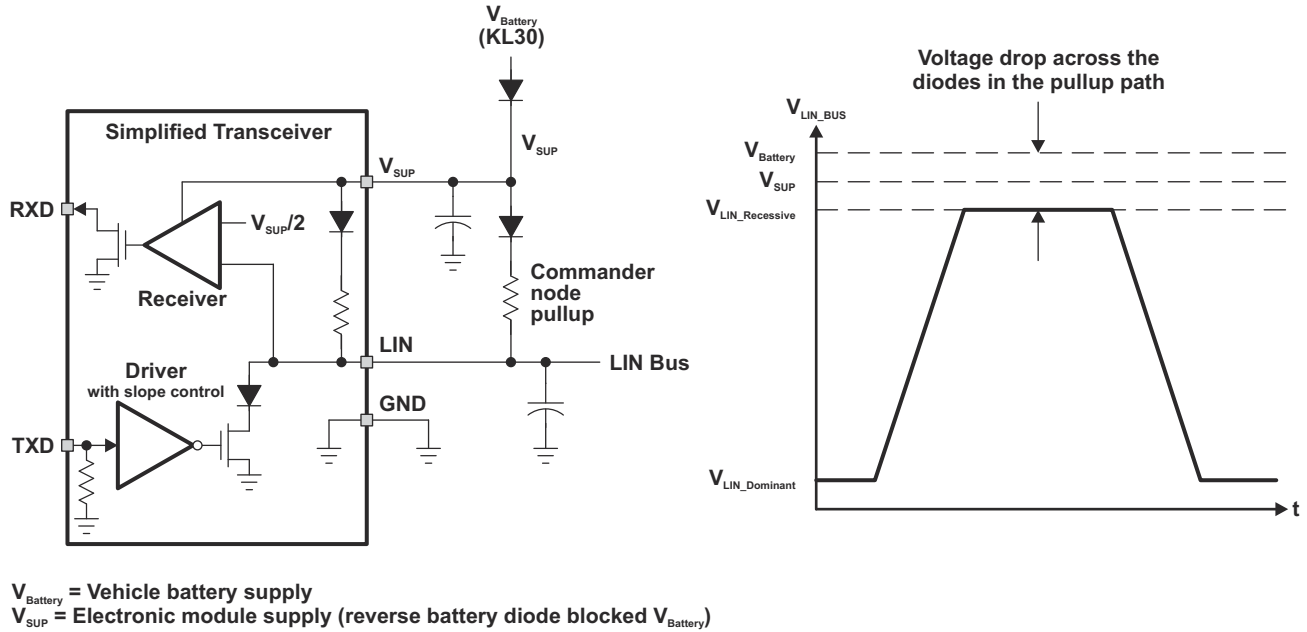


Figure 9-1. Definition of Voltage Levels

9.3.2 TXD (Transmit Input / Output)

TXD is the interface to the MCU's LIN protocol controller or SCI/UART that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near battery). The TXD input structure is compatible with microcontrollers with 3.3-V and 5-V I/O. TXD has an internal pulldown resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state time-out timer. The TXD pin is pulled down strongly in standby mode after a wake-up event on the NWake pin.

9.3.3 RXD (Receive Output)

RXD is the interface to the MCU's LIN protocol controller or SCI/UART, which reports the state of the LIN bus voltage. LIN recessive (near battery) is represented by a high level on RXD and LIN dominant (near ground) is represented by a low level on RXD. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3-V and 5-V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pullup, an external pullup resistor to the microcontroller I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake-up request from LIN or NWake.

9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse battery blocking diode. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high, the device is in normal mode, allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode

and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to make sure the device remains in low-power mode even if EN floats.

9.3.7 NWake (High Voltage Wake Up Input)

NWake is a high-voltage input used to wake up from sleep mode. NWake is usually connected to an external switch in the application. A low on NWake that is asserted longer than the filter time (t_{NWAKE}) results in a local wakeup. NWake provides an internal pullup source to V_{SUP} .

9.3.8 INH (Inhibit Output)

INH is used to control an external voltage regulator that has an inhibit or enable input. When the device is in normal operating mode, the inhibit switch is enabled and the external voltage regulator is activated. When device is in sleep mode, the inhibit switch is disabled, which turns off the system voltage regulator. A wake-up event transitions the device to standby by mode and re-enables INH which, in turn, restarts the system by turning on the voltage regulators. INH can also drive an external transistor connected to an MCU interrupt input.

9.3.9 TXD Dominant State Timeout

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on TXD. If the low signal remains on TXD for longer than t_{DST} , the transmitter is disabled, thus allowing the LIN bus to return to the recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to make sure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus, INH remains on, and the LIN bus pullup termination remains on.

Note

The maximum dominant TXD time allowed by the TXD Dominant state time-out limits the minimum possible data rate of the device. The LIN protocol has different constraints for commander and responder applications thus there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

Commander node: The maximum continuous dominant is the maximum dominant of the SYNC BREAK FIELD, $t_{SYNC_DOM(max)}$. The SYNC BREAK FIELD notifies the 'start of frame' to all LIN responders. It consists of 13 to 26 dominant bits (low phase) followed by a delimiter. Thus the minimum TXD dominant time out, $t_{DST(min)}$ and the maximum SYNC BREAK FIELD for the commander determine the minimum data rate for a commander node, which may be calculated using [Equation 1](#).

$$DataRate_{Commander(min)} = t_{SYNC_DOM(max)} / t_{DST(min)} \quad (1)$$

Responder node: sends the response part of the LIN message frame which has a maximum consecutive dominant length of 9 bits (start bit + 8 data bits). As a result the minimum baud rate of a responder can be calculated using [Equation 2](#).

$$DataRate_{Responder(min)} = (9 + n_{margin}) / t_{DST(min)} \text{ where } n_{margin} \text{ is a safety margin.} \quad (2)$$

9.3.10 Thermal Shutdown

The LIN transmitter is protected through a current limit, however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the LIN transmitter circuit. Once the overtemperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus, INH remains on, and the LIN bus pullup termination remains on.

9.3.11 Bus Stuck Dominant System Fault: False Wake-Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevent the device from waking up falsely during this system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus "clears" the bus stuck dominant condition. This logic prevents the potential for a cyclical false wakeup of the system if the bus is stuck dominant, preventing excessive current use. [Figure 9-2](#) and [Figure 9-3](#) show the behavior of this protection feature.

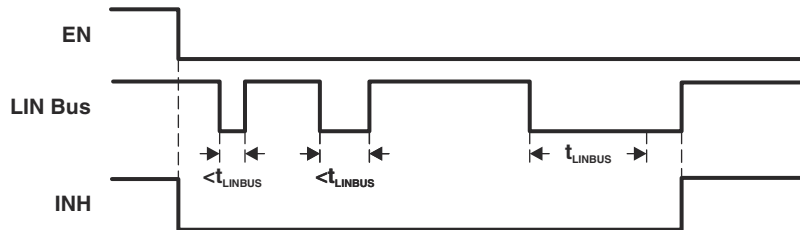


Figure 9-2. No Bus Fault: Entering Sleep Mode With Bus Recessive Condition and Wakeup

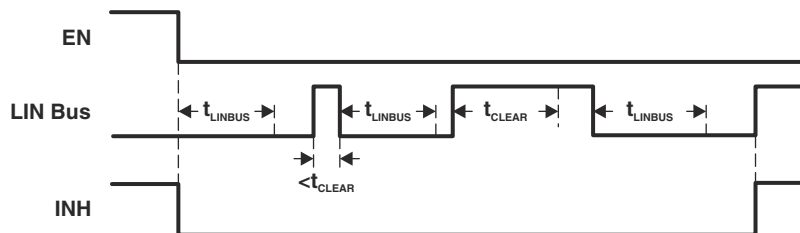


Figure 9-3. Bus Fault: Entering Sleep Mode With Bus Stuck Dominant Fault, Clearing, and Wakeup

9.3.12 Undervoltage on V_{SUP}

The device contains a power-on reset circuit to avoid false bus messages during undervoltage conditions when V_{SUP} is less than UV_{VSUP} .

9.3.13 Unpowered Device Does Not Affect the LIN Bus

The device has extremely low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.4 Device Functional Modes

9.4.1 Operating States

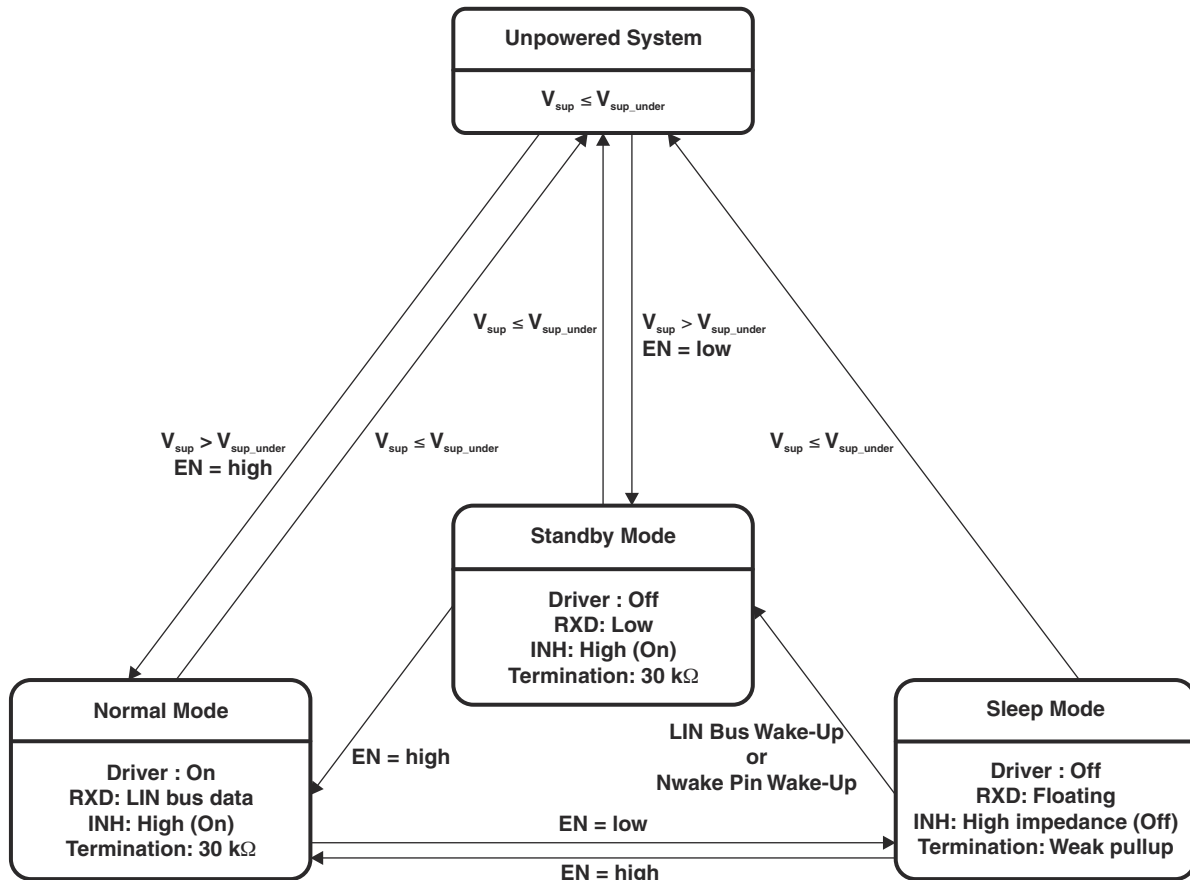


Figure 9-4. Operating States Diagram

Table 9-1. Operating Modes

| MODE | EN | RXD | LIN BUS TERMINATION | INH | TRANSMITTER | COMMENTS |
|---------|------|--------------|-------------------------|----------------|-------------|--|
| Sleep | Low | Floating | Weak current pullup | High impedance | Off | |
| Standby | Low | Low | 30 k Ω (typical) | High | Off | Wake-up event detected, waiting on MCU to set EN |
| Normal | High | LIN bus data | 30 k Ω (typical) | High | On | LIN transmission up to 20 kbps |

9.4.2 Normal Mode

This is the normal operational mode, in which the receiver and driver are active, and LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller, where recessive on the LIN bus is a digital high, and dominate on the LIN bus is digital low. The driver transmits input data on TXD to the LIN bus. Normal mode is entered as EN transitions high while the SN65HVDA100-Q1 is in sleep or standby mode.

9.4.3 Sleep Mode

Sleep mode is the power saving mode for the SN65HVDA100-Q1. Even with the extremely low current consumption in this mode, the SN65HVDA100-Q1 can still wake up from LIN bus through a wake-up signal, a low on NWake, or if EN is set high. The LIN bus and NWake are filtered to prevent false wake-up events. The wake-up events must be active for their respective time periods (t_{LINBUS} , t_{NWake}).

The sleep mode is entered by setting EN low.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pullup is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- INH is high impedance.
- EN input, NWake input, and the LIN wake-up receiver are active.

9.4.4 Wake-Up Events

There are three ways to wake up from sleep mode:

- Remote wakeup through recessive (high) to dominant (low) state transition on LIN bus. The dominant state must be held for t_{LINBUS} filter time and then the bus must return to the recessive state (to eliminate false wakeups from disturbances on the LIN bus or if the bus is shorted to ground).
- Local wakeup through a low on NWake, which is asserted low longer than the filter time t_{NWake} (to eliminate false wakeups from disturbances on NWake).
- Local wakeup through EN being set high.

9.4.4.1 Wake-Up Request (RXD)

When the device encounters a wake-up event from the LIN bus or NWake pin, RXD goes low, and the device transitions to standby mode (until EN is reasserted high and the device enters normal mode). Once the device enters normal mode, the RXD pin is releasing the wake-up request signal, and the RXD pin then reflects the receiver output from the bus.

9.4.4.2 Wake-Up Source Recognition (TXD)

When the device encounters a wake-up event from the LIN bus or NWake pin, TXD indicates the source while the device enters and remains in standby mode (until EN is reasserted high and the device enters normal mode). In addition to the internal pullup resistor on TXD, typically an external pullup resistor (approximately 5 k Ω) is used in the system's I/O supply voltage. A high on TXD in standby mode indicates a remote wakeup through the LIN bus, and a low (strong pulldown) on the TXD pin indicates a local wakeup through the NWAKE pin.

9.4.5 Standby Mode

This mode is entered whenever a wake-up event occurs through LIN bus or NWake while the device is in sleep mode. The LIN bus responder termination circuit and INH are turned on when standby mode is entered. The application system powers up once INH is turned on, assuming the system is using a voltage regulator connected through INH. Standby mode is signaled through a low level on RXD.

When EN is set high while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

During power up if EN is low the device goes into Standby mode and if EN is high the device goes into Normal mode. EN has an internal pull-down resistor, so if the pin is floating in the system, the internal pull-down makes sure it is pulled low.

Note

If the INH output of the SN65HVDA100-Q1 is not used to control the system power management (voltage regulators) and monitor wake-up sources, but sleep mode is used to reduce system current, the RXD pin is monitored to make sure SN65HVDA100-Q1 remains in sleep mode. If the SN65HVDA100-Q1 detects an undervoltage on V_{SUP} , the RXD pin transitions low and signals to the software that the SN65HVDA100-Q1 is in standby mode and should be returned to sleep mode to return to the lowest power state.

9.4.6 Mode Transitions

When the device is transitioning between modes the device needs the time, t_{MODE_CHANGE} , to allow the change to fully propagate from the EN pin through the device into the new state.

Note

When using the SN65HVDA100-Q1 in systems which are not controlled through the INH output, but rather are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE} . This is shown in [Figure 7-3](#).

10 Application and Implementation

Note

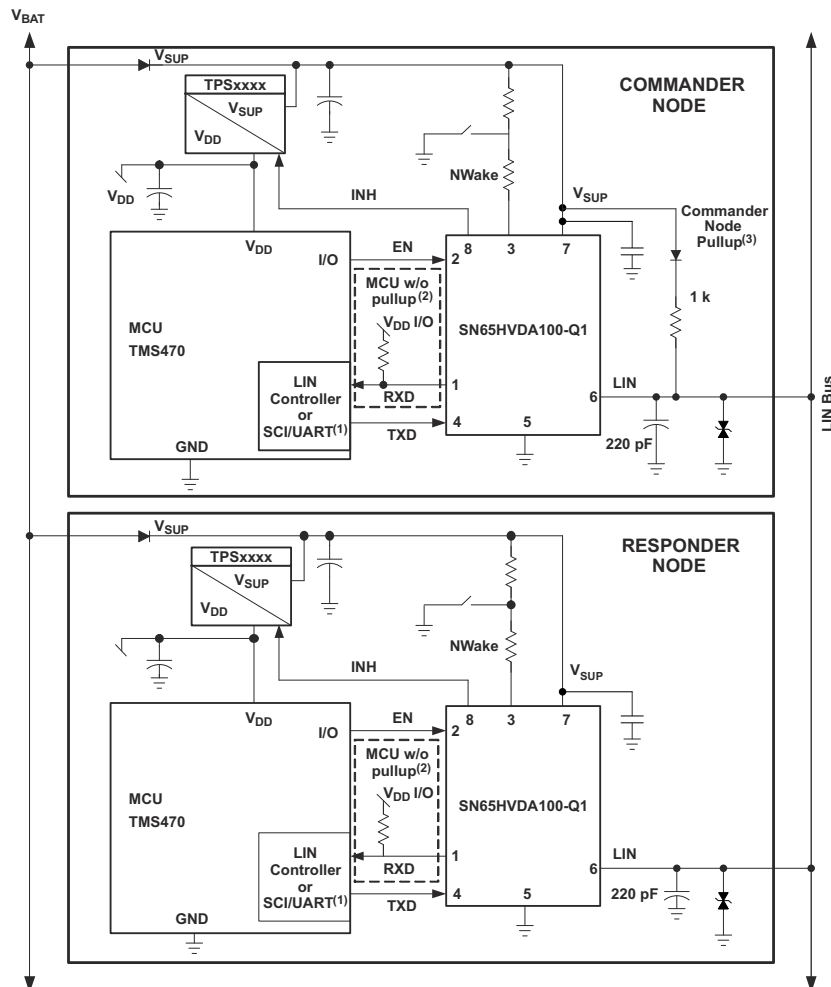
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The responder-Q1 can be used as both a responder device and a commander device in a LIN network. The device comes with the ability to support both remote wake-up requests and local wake-up requests.

10.2 Typical Application

The device comes with an integrated 30-k Ω pullup resistor and series diode for responder applications, and for commander applications an external 1-k Ω pullup with series blocking diode can be used. Figure 10-1 shows the device being used in both types of applications.



- A. RXD on MCU or LIN responder has internal pullup, no external pullup resistor is needed.
- B. RXD on MCU or LIN responder without internal pullup, requires external pullup resistor.
- C. Commander node applications require an external 1-k Ω pullup resistor and serial diode.

Figure 10-1. SN65HVDA100-Q1 Application Diagram

10.2.1 Design Requirements

For this design, use these requirements:

1. RXD on MCU or LIN responder has internal pullup, no external pullup resistor is needed.
2. RXD on MCU or LIN responder without internal pullup, requires external pullup resistor.
3. Commander Node applications require an external 1-k Ω pullup resistor and serial diode.

10.2.2 Detailed Design Procedure

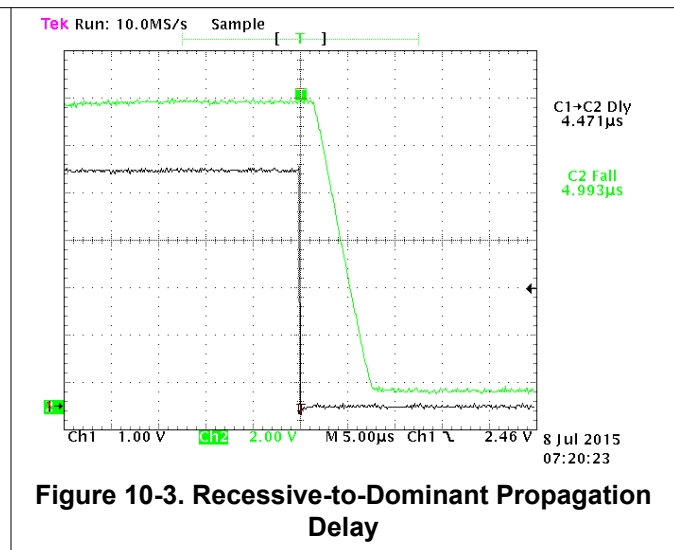
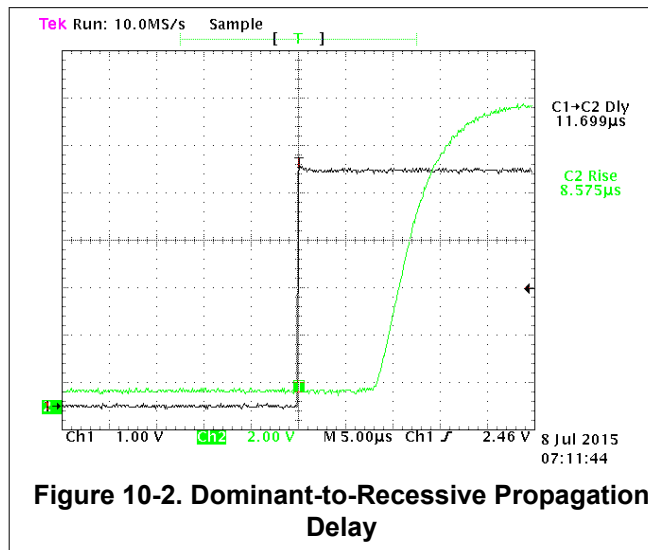
The RXD output structure is an open-drain output stage. This allows the SN65HVDA100-Q1 to be used with 3.3-V and 5-V I/O microcontrollers. If the RXD pin of the microcontroller does not have an integrated pullup, an external pullup resistor to the microcontroller I/O supply voltage is required.

The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor as close to the supply pin of the device as possible.

The NWAKE pin is a high voltage wake-up input to the device. If this pin is not being used it should be tied to V_{SUP} .

10.2.3 Application Curves

Figure 10-2 and Figure 10-3 show the propagation delay from the TXD pin to the LIN pin for both the recessive-to-dominant and dominant-to-recessive states under lightly loaded conditions.



11 Power Supply Recommendations

The SN65HVDSA100-Q1 was designed to operate directly off a car battery or any other DC supply ranging from 7 V to 27 V. A 100-nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.

12 Layout

12.1 Layout Guidelines

Pin 1 is the RXD output of the SN65HVDA100-Q1. The pin is an open-drain output and requires an external pullup resistor in the range of 1 k Ω to 10 k Ω to function properly. If the microprocessor paired with the transceiver does not have an integrated pullup, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.

Pin 2 is the EN input pin for the device that is used to place the device in low power sleep mode. If this feature is not used on the device, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series 1-k Ω to 10-k Ω series resistor. Additionally, a series resistor may be placed on the pin to limit the current on the digital lines in the case of a overvoltage fault.

Pin 3 is a high-voltage local wake up input pin. The device is typically externally controlled by a normally open switch tied between NWAKE and ground. When the momentary switch is pressed the NWAKE pin is pulled to ground signaling a local wake-up event. A series resistor between V_{BATT} and the switch, and NWAKE and the switch should be placed to limit current. If the NWAKE local wake-up feature is not used, the pin can be tied to V_{SUP} through a 1-k Ω to 10-k Ω pullup resistor.

Pin 4 is the transmit input signal to the device. A series resistor can be placed to limit the input current to the device in the case of a overvoltage on this pin. Also, a capacitor to ground can be placed close to the input pin of the device to filter noise.

Pin 5 is the ground connection of the device. This pin should be tied to a ground plane through a short trace with the use of two vias to limit total return inductance.

Pin 6 is the LIN bus connection of the device. For responder applications a 220-pF bus capacitor is implemented. For commander applications an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin.

Pin 7 is the supply pin for the device. A 100-nF decoupling capacitor should be placed as close to the device as possible.

Pin 8 is a high-voltage output pin that may be used to control the local power supplies. If this feature is not used the pin may be left floating.

Note

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

12.2 Layout Example

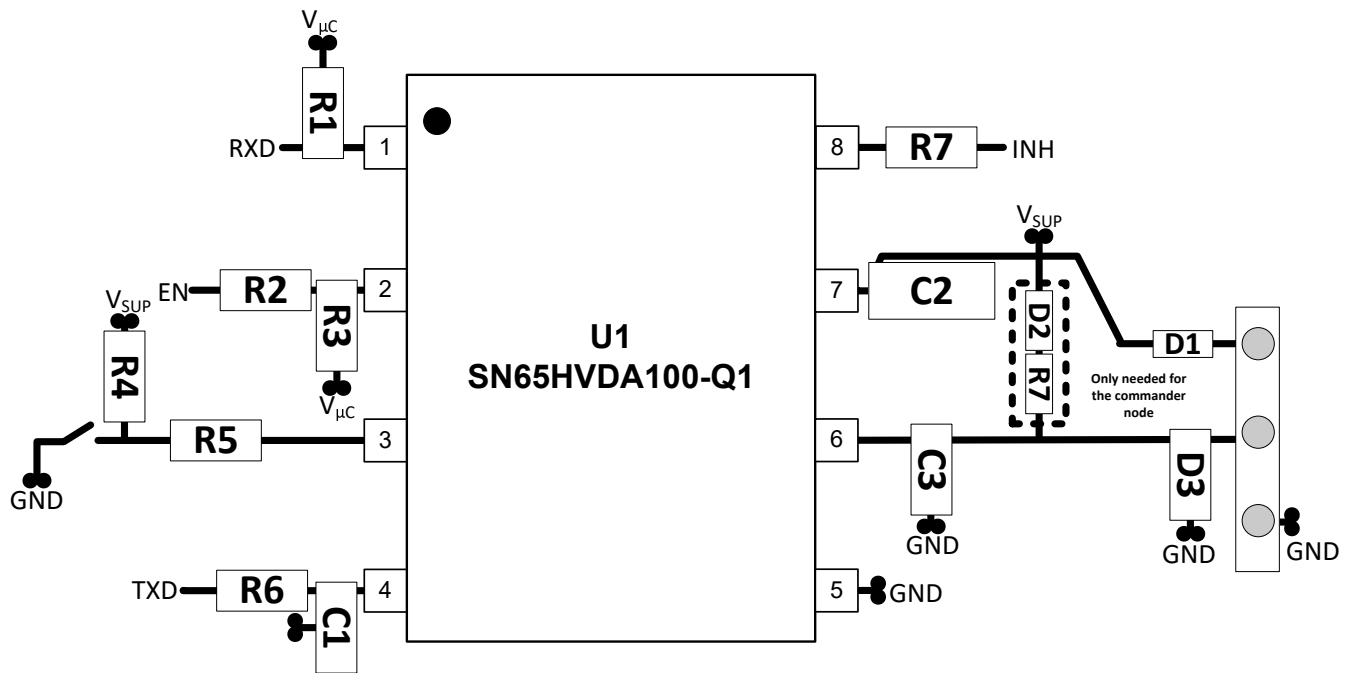


Figure 12-1. Layout Schematic

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN65HVDA100QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A100Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

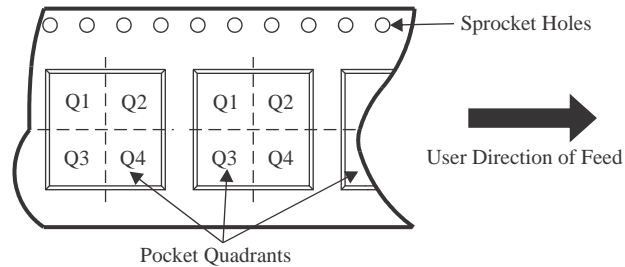
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVDA100QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVDA100QDRQ1 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN65HVDA100QDRQ1 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management