



**THE DATASHEET OF  
NTST40120CTG**



# NTST40120CT, NTSJ40120CTG, NTSB40120CT-1G, NTSB40120CTG, NTSB40120CTT4G



ON Semiconductor®

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## Very Low Forward Voltage Trench-based Schottky Rectifier

Exceptionally Low  $V_F = 0.43\text{ V}$  at  $I_F = 5\text{ A}$

### Features

- Fine Lithography Trench-based Schottky Technology for Very Low Forward Voltage and Low Leakage
- Fast Switching with Exceptional Temperature Stability
- Low Power Loss and Lower Operating Temperature
- Higher Efficiency for Achieving Regulatory Compliance
- Low Thermal Resistance
- High Surge Capability
- Pb-Free and Halide-Free Packages are Available

### Typical Applications

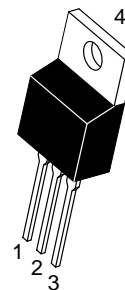
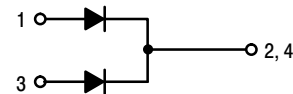
- Switching Power Supplies including Notebook/Netbook Adapters, ATX and Flat Panel Display
- High Frequency and DC-DC Converters
- Freewheeling and OR-ing Diodes
- Reverse Battery Protection
- Instrumentation

### Mechanical Characteristics

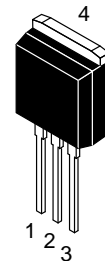
- Case: Epoxy, Molded
- Epoxy Meets Flammability Rating UL 94-0 @ 0.125 in
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Maximum for 10 sec

VERY LOW FORWARD  
VOLTAGE, LOW LEAKAGE  
SCHOTTKY BARRIER  
RECTIFIERS 40 AMPERES,  
120 VOLTS

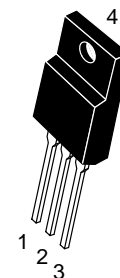
### PIN CONNECTIONS



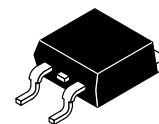
TO-220  
CASE 221A  
STYLE 6



I<sup>2</sup>PAK  
CASE 418B  
STYLE 3



TO-220FP  
CASE 221AH



D<sup>2</sup>PAK  
CASE 418B

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTST40120CT, NTSJ40120CTG, NTSB40120CT-1G, NTSB40120CTG, NTSB40120CTT4G

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	$V_{RRM}$ $V_{RWM}$ $V_R$	120	V
Average Rectified Forward Current (Rated $V_R$ , $T_C = 120^\circ\text{C}$ )	$I_{F(AV)}$ Per Device Per Diode	40 20	A
Peak Repetitive Forward Current (Rated $V_R$ , Square Wave, 20 kHz, $T_C = 125^\circ\text{C}$ )	$I_{FRM}$ Per Device Per Diode	80 40	A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	$I_{FSM}$	250	A
Operating Junction Temperature	$T_J$	-40 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-40 to +150	$^\circ\text{C}$
Voltage Rate of Change (Rated $V_R$ )	dv/dt	10,000	V/ $\mu\text{s}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Rating	Symbol	NTST40120CTG, NTSB40120CT-1G	NTSB40120CTG	NTSJ40120CTG	Unit
Maximum Thermal Resistance per Diode Junction-to-Case Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.3 70	0.79 46.3	4.0 105	$^\circ\text{C/W}$ $^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS (Per Leg unless otherwise noted)

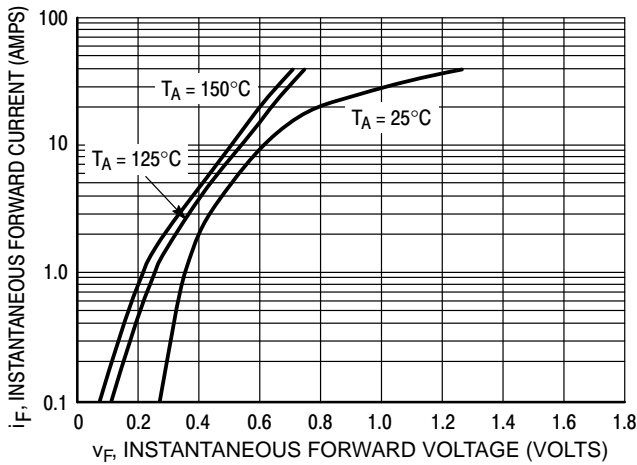
Rating	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage (Note 1) ( $I_F = 5\text{ A}$ , $T_J = 25^\circ\text{C}$ ) ( $I_F = 10\text{ A}$ , $T_J = 25^\circ\text{C}$ ) ( $I_F = 20\text{ A}$ , $T_J = 25^\circ\text{C}$ )  ( $I_F = 5\text{ A}$ , $T_J = 125^\circ\text{C}$ ) ( $I_F = 10\text{ A}$ , $T_J = 125^\circ\text{C}$ ) ( $I_F = 20\text{ A}$ , $T_J = 125^\circ\text{C}$ )	$V_F$	0.50 0.60 0.78  0.43 0.53 0.63	- - 0.91  - - 0.71	V
Maximum Instantaneous Reverse Current (Note 1) ( $V_R = 90\text{ V}$ , $T_J = 25^\circ\text{C}$ ) ( $V_R = 90\text{ V}$ , $T_J = 125^\circ\text{C}$ )  (Rated dc Voltage, $T_J = 25^\circ\text{C}$ ) (Rated dc Voltage, $T_J = 125^\circ\text{C}$ )	$I_R$	16 16  - 30	- -  500 100	$\mu\text{A}$ mA  $\mu\text{A}$ mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

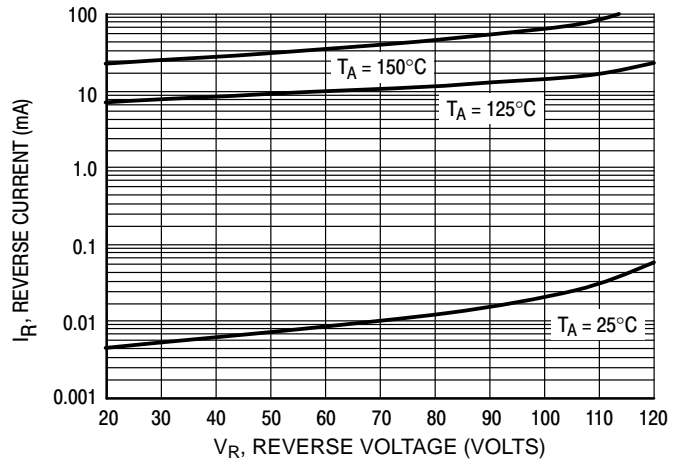
1. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

**NTST40120CT, NTSJ40120CTG, NTSB40120CT-1G, NTSB40120CTG,  
NTSB40120CTT4G**

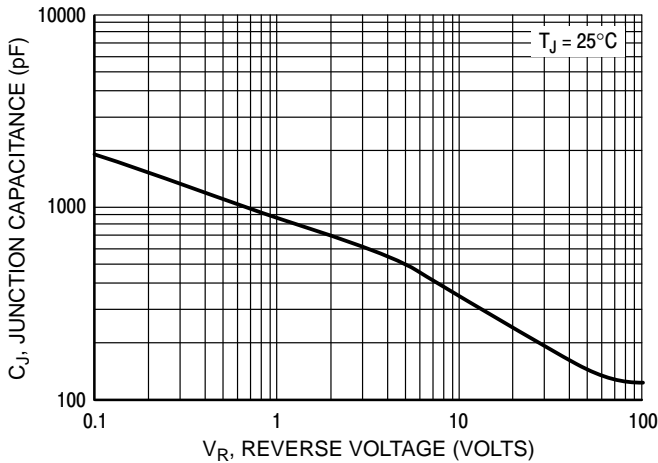
**TYPICAL CHARACTERISTICS**



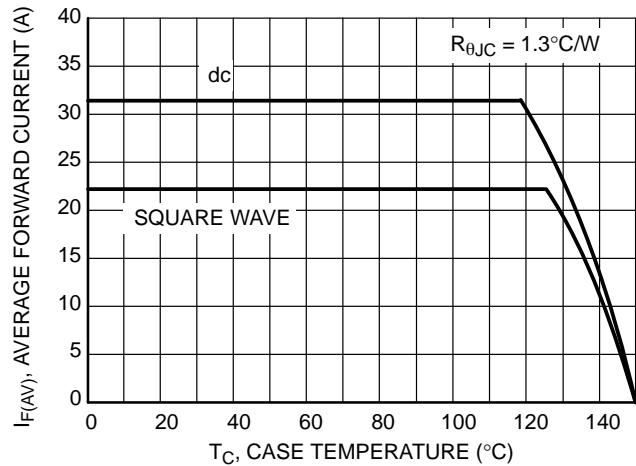
**Figure 1. Typical Forward Voltage**



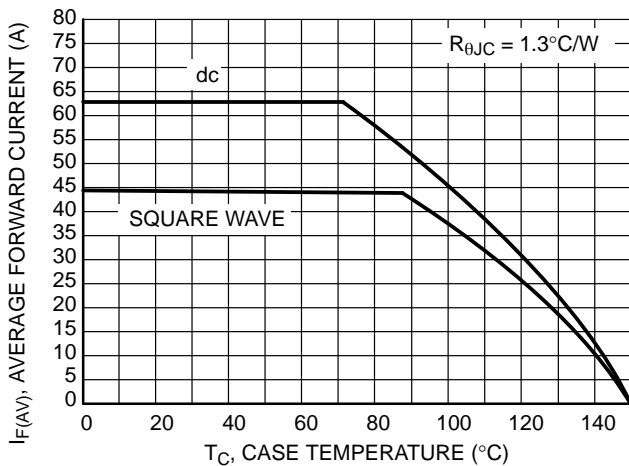
**Figure 2. Typical Reverse Current**



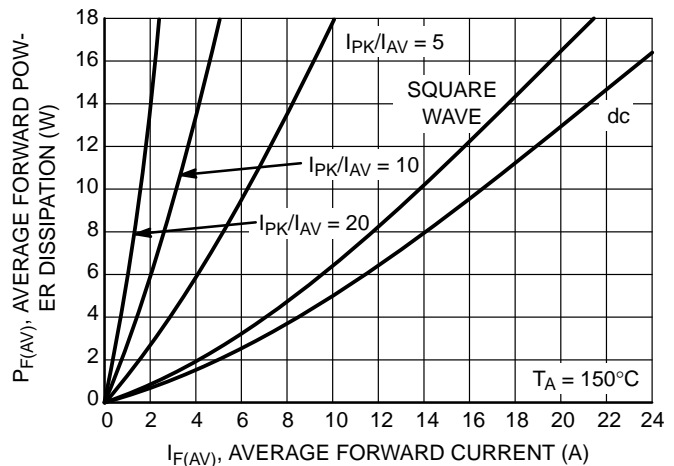
**Figure 3. Typical Junction Capacitance**



**Figure 4. Current Derating per Leg**



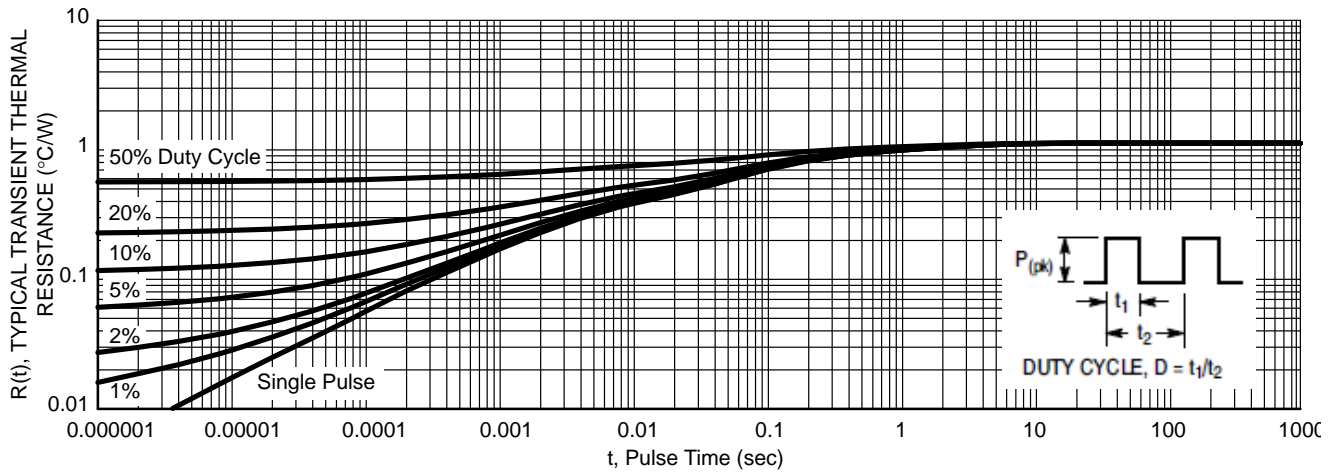
**Figure 5. Current Derating, Case**



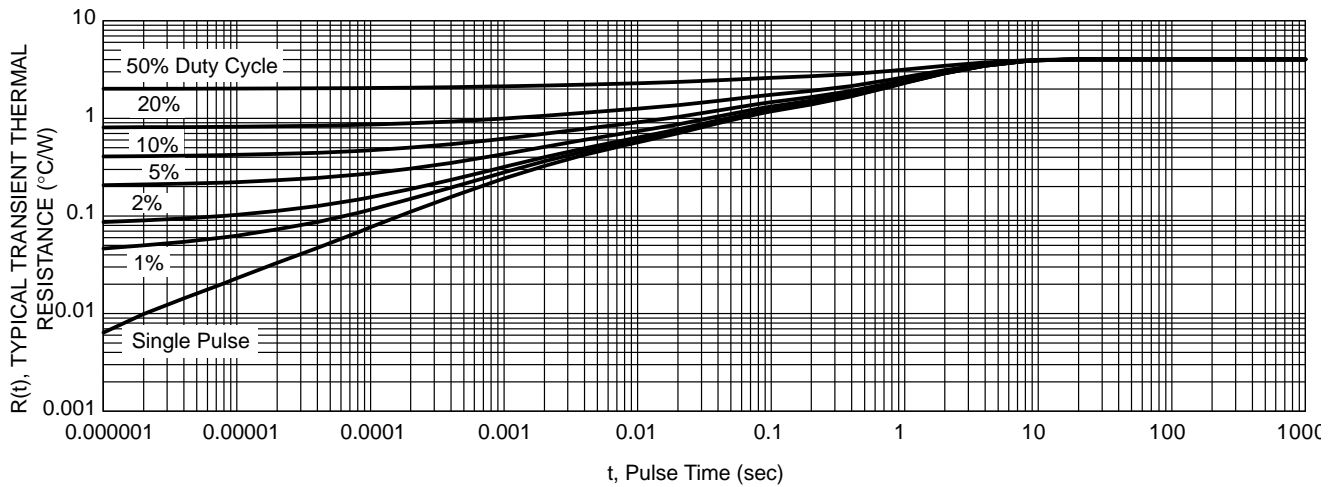
**Figure 6. Forward Power Dissipation**

**NTST40120CT, NTSJ40120CTG, NTSB40120CT-1G, NTSB40120CTG,  
NTSB40120CTT4G**

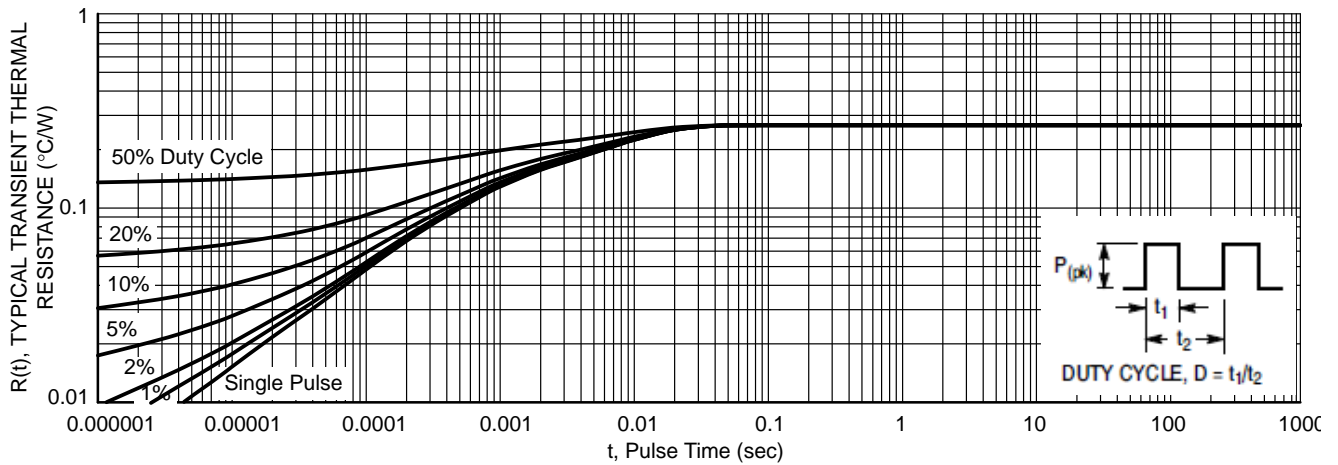
**TYPICAL CHARACTERISTICS**



**Figure 7. Typical Transient Thermal Response for NTST40120CT and NTSB40120CT-1G**



**Figure 8. Typical Transient Thermal Response for NTSJ40120CTG**



**Figure 9. Typical Transient Thermal Response for NTSB40120CTG**

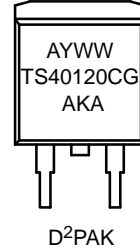
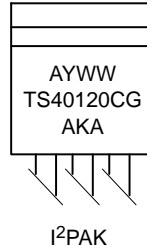
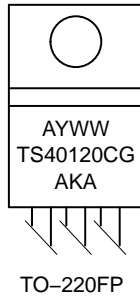
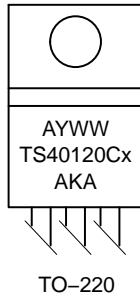
# NTST40120CT, NTSJ40120CTG, NTSB40120CT-1G, NTSB40120CTG, NTSB40120CTT4G

## ORDERING INFORMATION

Device	Package	Shipping†
NTST40120CTG	TO-220 (Pb-Free)	50 Units / Rail
NTST40120CTH	TO-220 (Pb-Free and Halide-Free)	50 Units / Rail
NTSJ40120CTG	TO-220FP (Pb-Free and Halide-Free)	50 Units / Rail
NTSB40120CT-1G	I <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NTSB40120CTG	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NTSB40120CTT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS



- A = Assembly Location
- Y = Year
- WW = Work Week
- AKA = Polarity Designator
- x = G or H
- G = Pb-Free Package
- H = Halide-Free Package

# MECHANICAL CASE OUTLINE

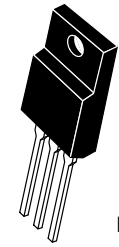
## PACKAGE DIMENSIONS

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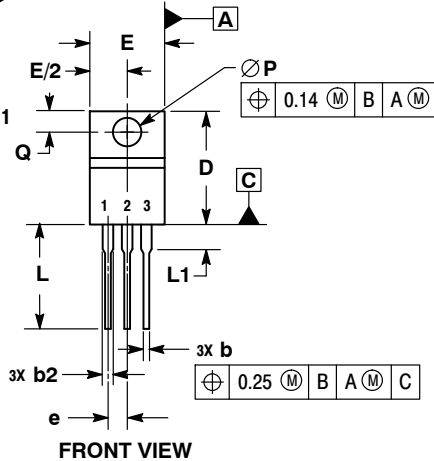


### TO-220 FULLPACK, 3-LEAD CASE 221AH ISSUE F

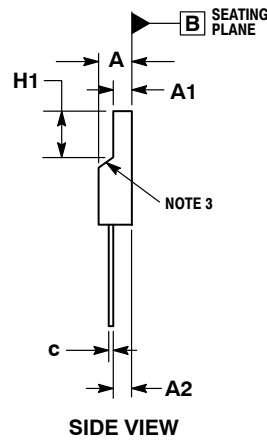
DATE 30 SEP 2014



SCALE 1:1



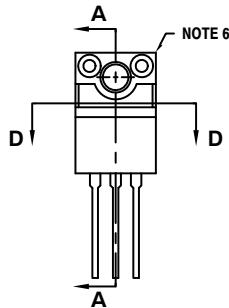
FRONT VIEW



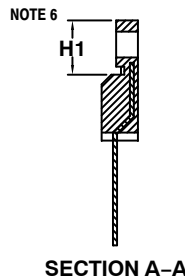
SIDE VIEW



SECTION D-D



ALTERNATE CONSTRUCTION



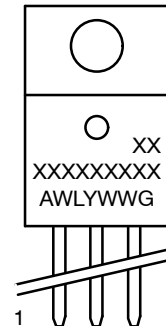
SECTION A-A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

MILLIMETERS		
DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

### GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

STYLE 1:

1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:

1. CATHODE
2. ANODE
3. GATE

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	TO-220 FULLPACK, 3-LEAD	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

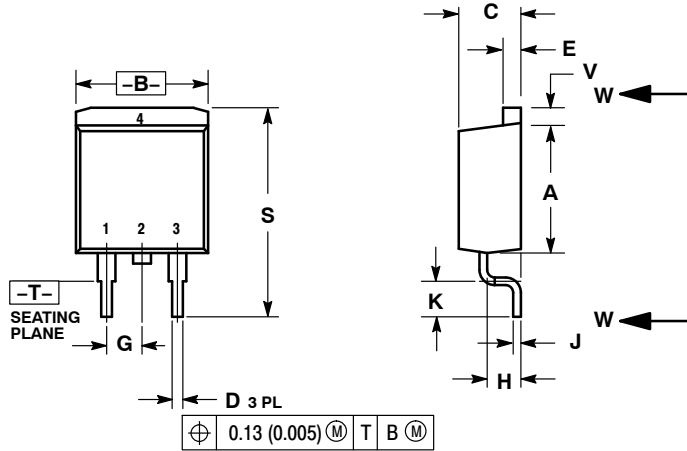
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

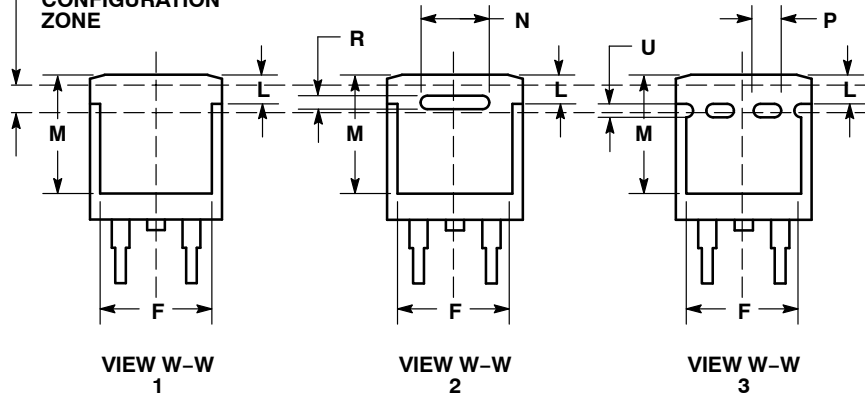


**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**VARIABLE CONFIGURATION ZONE**



- |  |   |   |  |   |  |
|--|---|---|--|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | <b>STYLE 6:</b><br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|--|---|---|--|---|--|

**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**

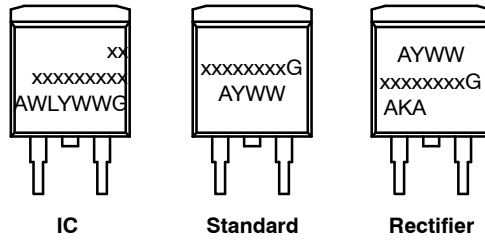
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

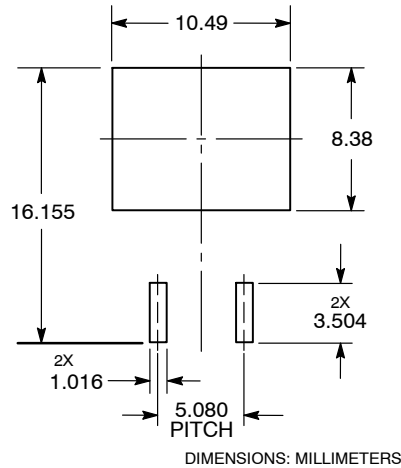
**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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