THE DATASHEET OF

CY62177EV30LL-55ZXI

CY62177EV30 MoBL

32-Mbit (2M × 16/4M × 8) Static RAM

Features

- Thin small outline package TSOP I configurable as 2M × 16 or as 4M × 8 static RAM (SRAM)
- Very high speed
  - ❒ 55 ns
- Wide voltage range
  - ❒ 2.2 V to 3.6 V
- Ultra low standby power
  - ❒ Typical standby current: 3 µA
  - ❒ Maximum standby current: 25 µA
- Ultra low active power
  - ❒ Typical active current: 10 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-pin TSOP I package and 48-ball FBGA package

Functional Description

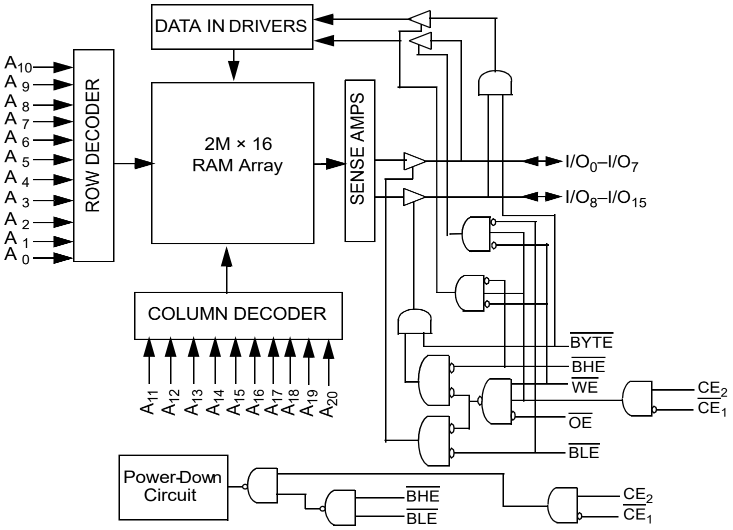
The CY62177EV30 is a high performance CMOS static RAM organized as 2M words by 16 bits and 4M words by 8 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written to the location specified on the address pins (A_0 through A_{20}). To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

Pin #13 of the 48 TSOP I package is an DNU pin that must be left floating at all times to ensure proper application.

For a complete list of related resources, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-pin TSOP I pinout (Front View) [1, 2]

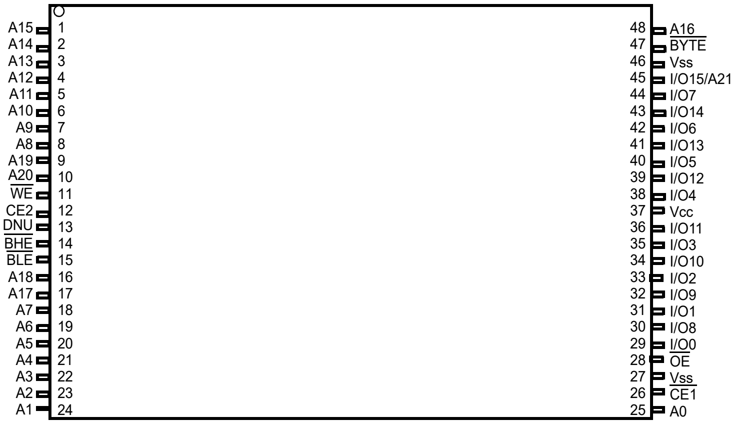
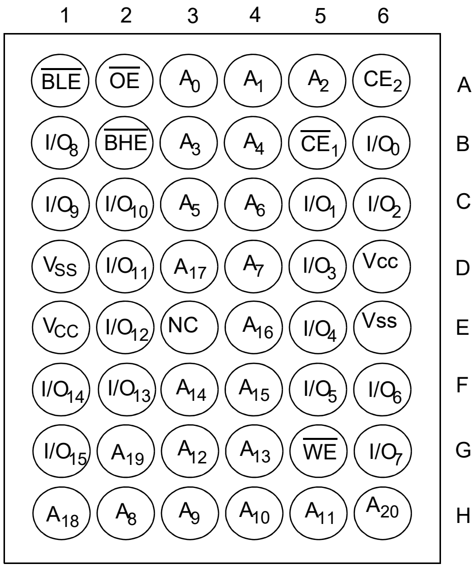


Figure 2. 48-ball FBGA pinout (Top View)



	1	2	3	4	5	6
A	$\overline{\text{BLE}}$	$\overline{\text{OE}}$	A_0	A_1	A_2	CE_2
B	I/O_8	$\overline{\text{BHE}}$	A_3	A_4	$\overline{\text{CE}}_1$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	Vcc
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	Vss
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{\text{WE}}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{20}

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ [3]	Max		Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62177EV30LL	2.2	3.0	3.6	55	10	18	35	45	3	25

Notes

1. DNU Pin# 13 needs to be left floating to ensure proper application.
2. The $\overline{\text{BYTE}}$ pin in the 48-pin TSOP I package has to be tied to V_{CC} to use the device as a 2M × 16 SRAM.

   The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the $\overline{\text{BYTE}}$ signal to V_{SS}. In the 4M × 8 configuration, Pin 45 is A21, while $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, and I/O_8 to I/O_{14} pins are not used.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage to ground potential [4, 5] ....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High Z state [4, 5] ....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [4, 5] ....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [6]
CY62177EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ [7]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20 V	2.0	–	–	V
		I_{OH} = –1.0 mA	V_{CC} = 2.70 V	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20 V	–	–	0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70 V	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.7 [8]	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{Max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$ I_{OUT} = 0 mA CMOS levels	–	35	45	mA
		f = 1 MHz		–	10	18	mA
I_{SB2} [9, 10]	Automatic CE power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.7 V		–	3	25	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
6. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
8. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7 V.
9. The $\overline{BYTE}$ pin in the 48-pin TSOP I package has to be tied to V_{CC} to use the device as a 2M × 16 SRAM.

   The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the $\overline{BYTE}$ signal to V_{SS}. In the 4M × 8 configuration, Pin 45 is A21, while $\overline{BHE}$, $\overline{BLE}$, and I/O_8 to I/O_{14} pins are not used.
10. Chip enables ($\overline{CE}_1$ and CE_2), $\overline{BYTE}$, and Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.

Capacitance

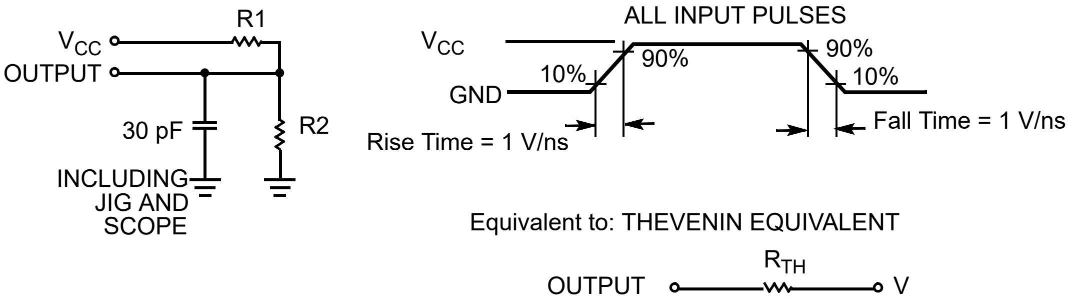
Parameter [11]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\ °C$, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	15	pF
C_{OUT}	Output capacitance		15	pF

Thermal Resistance

Parameter [11]	Description	Test Conditions	FBGA	TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	54.8	54.42	°C/W
Θ_{JC}	Thermal resistance (junction to case)		11.9	9.4	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameter	2.5 V	3.3 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note

11. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [12]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} [13]	Data retention current	V_{CC} = 1.5 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	20	µA
t_{CDR}[14]	Chip deselect to data retention time		0	–	–	ns
t_R[15]	Operation recovery time		55	–	–	ns

Data Retention Waveform

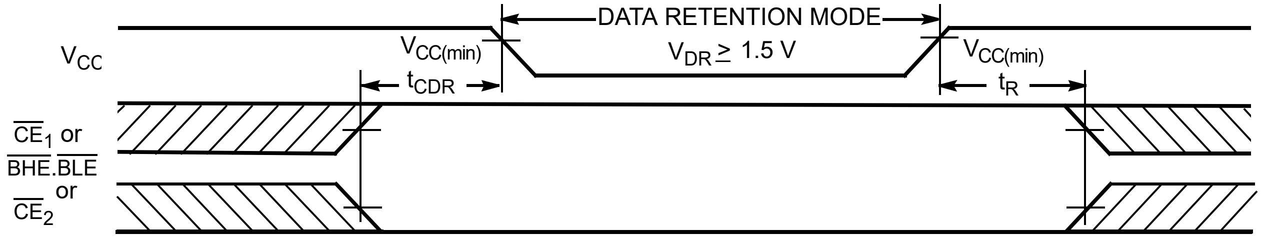


Figure 4. Data Retention Waveform [16]

Notes

12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
13. Chip enables ($\overline{CE_1}$ and CE_2), $\overline{BYTE}$, Address Pin A_{20} and Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
16. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip is deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [17]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	4	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z [18]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [18, 19]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z [18]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z [18, 19]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power down	–	55	ns
t_{DBE}	BLE/BHE LOW to data valid	–	55	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [18]	10	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH Z [18, 19]	–	18	ns
Write Cycle [20, 21]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from Write End	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [18, 19]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [18]	10	–	ns

Notes

[17] Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{TH}, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 3 on page 5.

[18] At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

[19] t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.

[20] The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

[21] The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [22, 23]

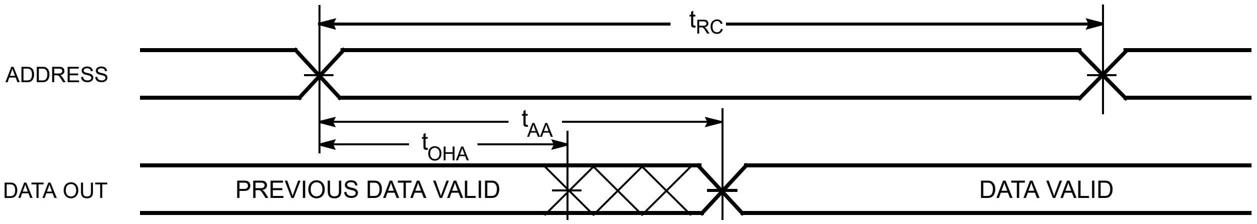
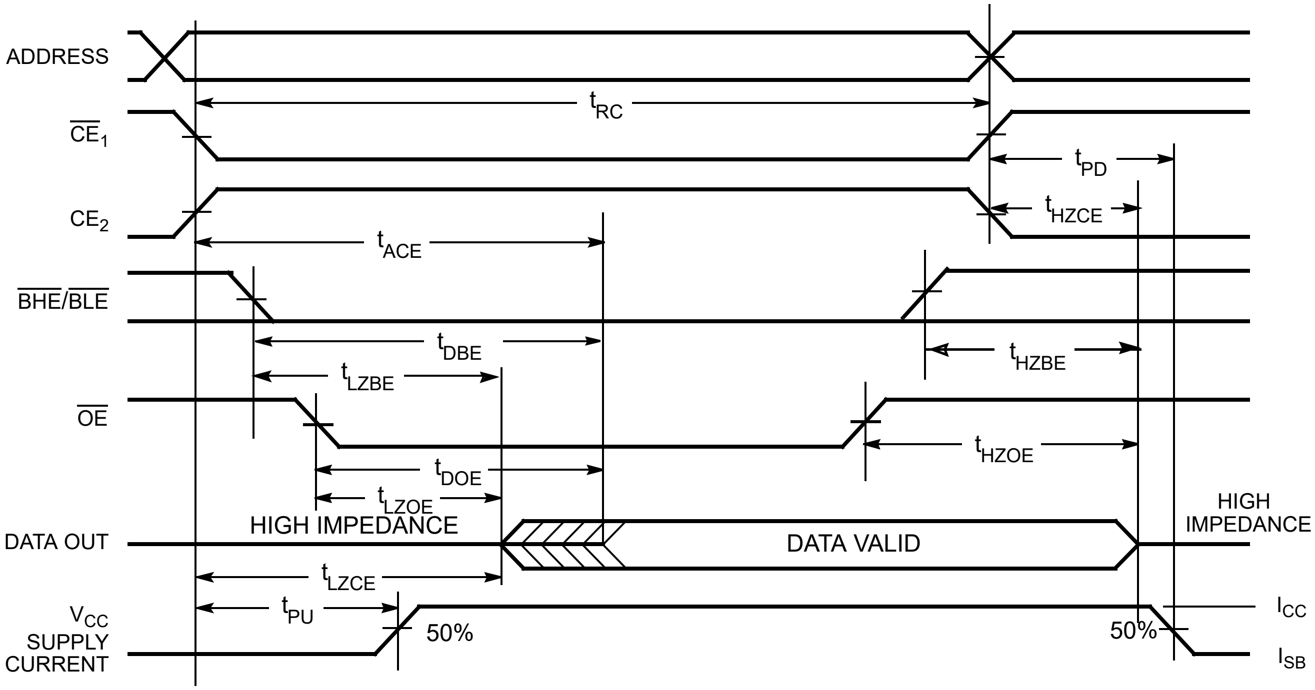


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [23, 24]



Notes

22. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
23. $\overline{WE}$ is HIGH for read cycle.
24. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms *(continued)*

Figure 7. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) [25, 26, 27, 28]

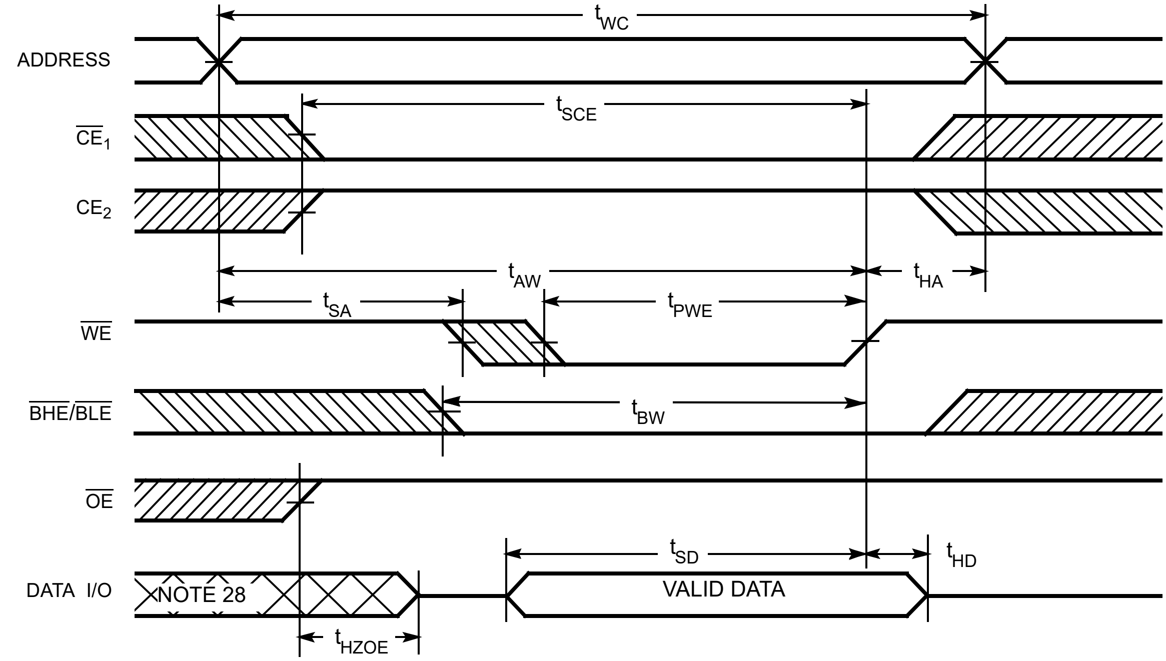
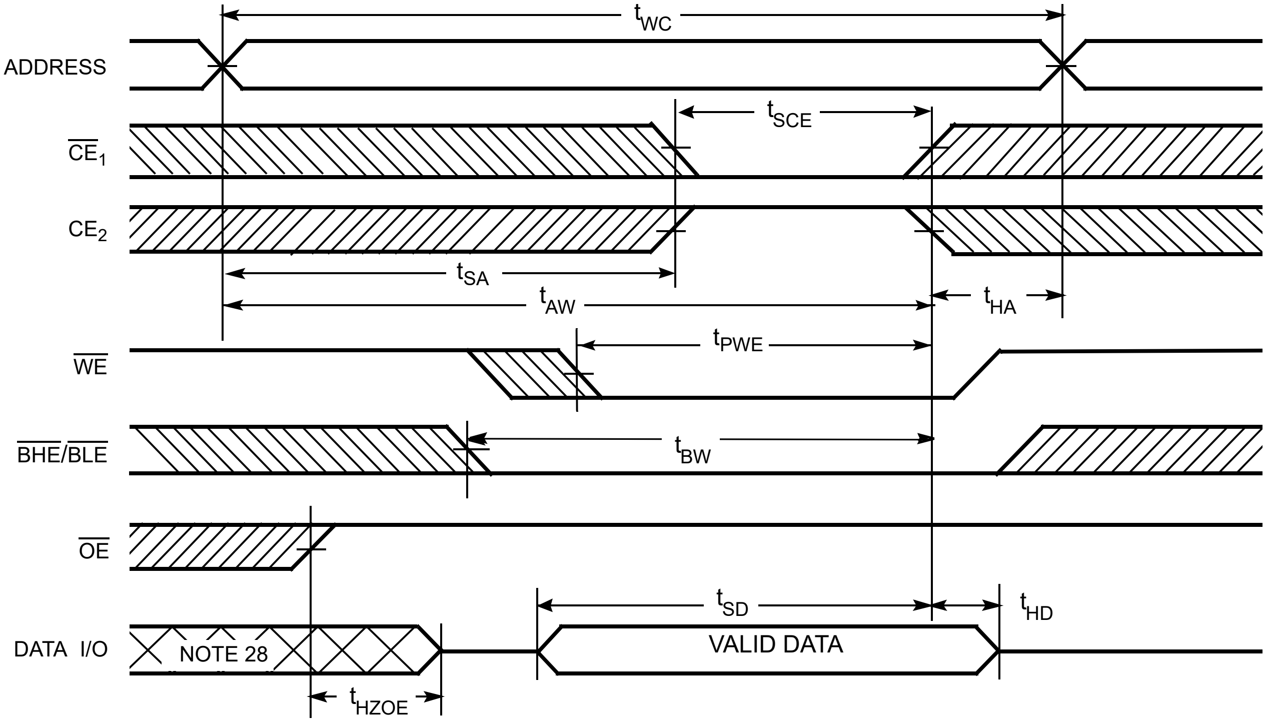


Figure 8. Write Cycle No. 2 ($\overline{\text{CE}}_1$ or CE_2 Controlled) [25, 26, 27, 28]



Notes

25. The internal Write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}}_1 = V_{IL}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IL}$, and $\text{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
27. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
28. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms *(continued)*

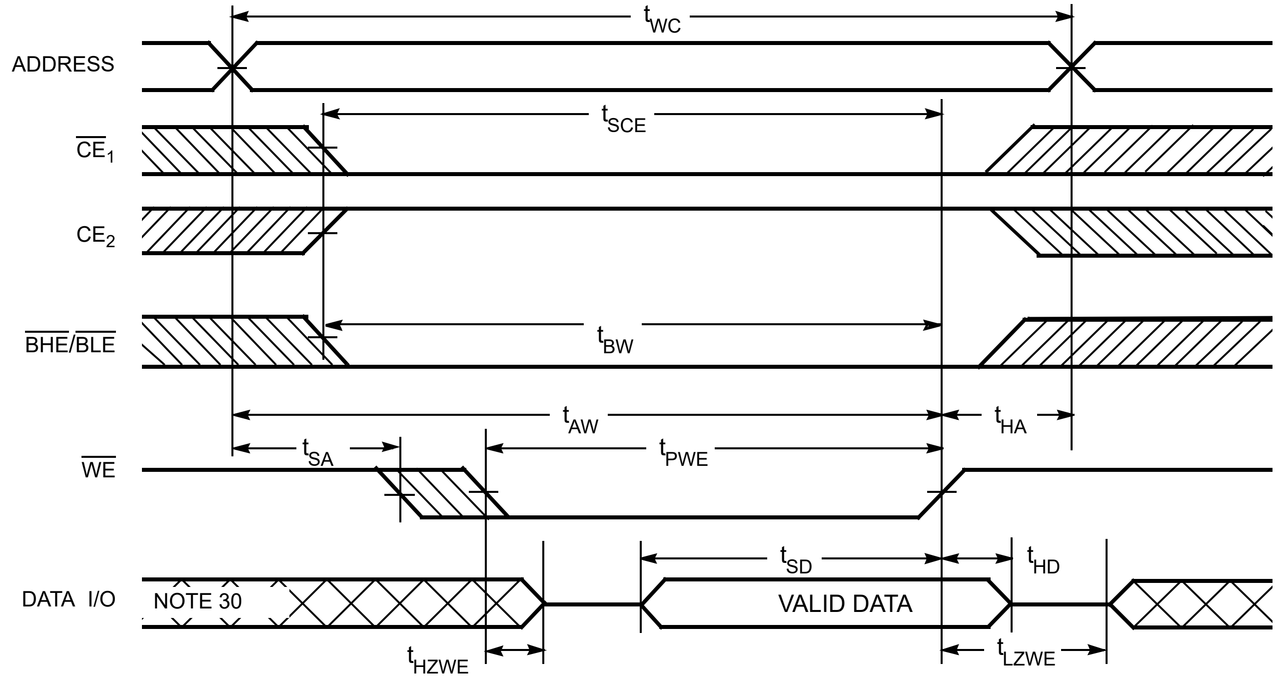


Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [29]

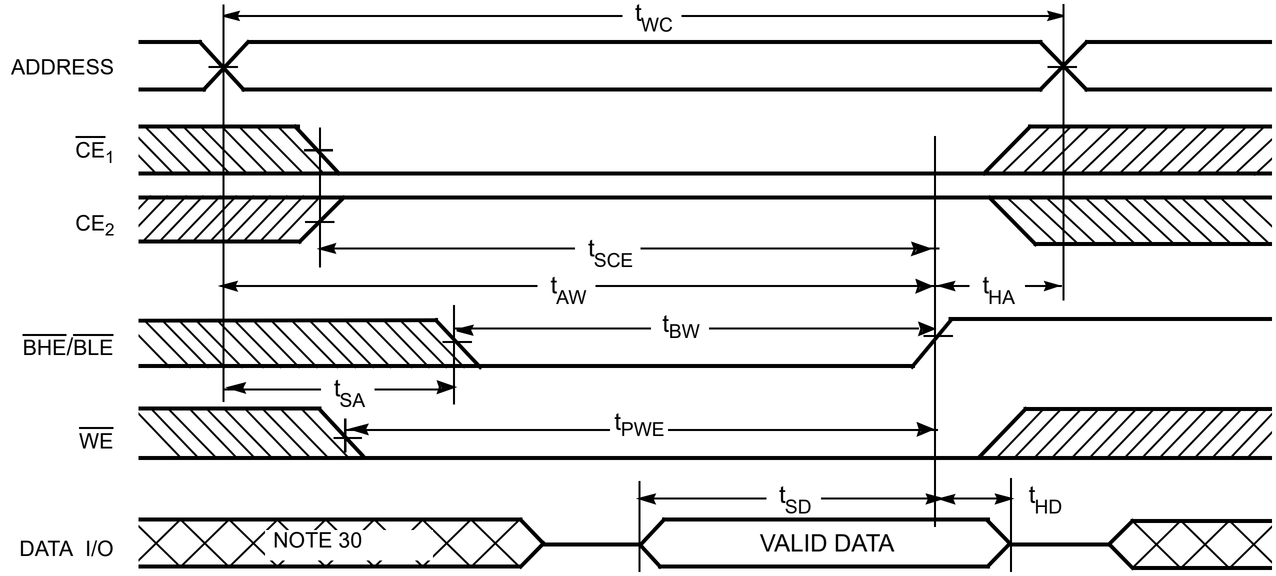


Figure 10. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW) [29, 32]

Notes

[29] If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.

[30] During this period the I/Os are in output state and input signals should not be applied.

[31] The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{\text{CE}}_1$	CE_2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Input/Output	Mode	Power
H	X[32]	X	X	X[32]	X[32]	High Z	Deselect/Power Down	Standby (I_{SB})
X[32]	L	X	X	X[32]	X[32]	High Z	Deselect/Power Down	Standby (I_{SB})
X[32]	X[32]	X	X	H	H	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (I/O_8–I/O_{15}); Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (I/O_8–I/O_{15}); Data In (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})

Note

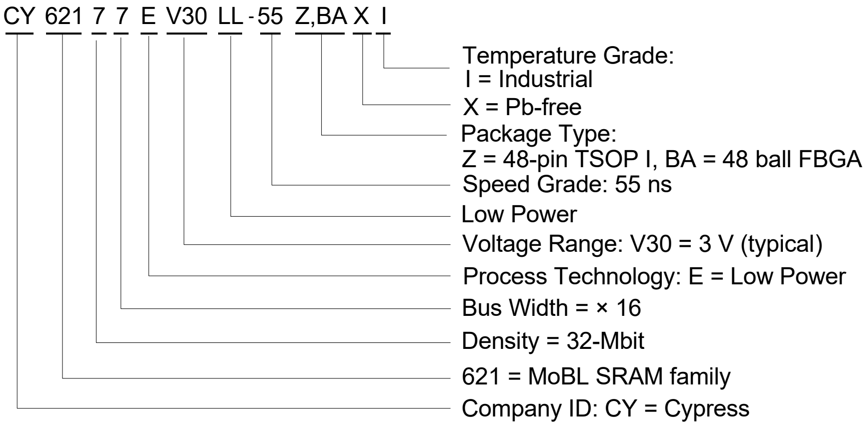
32. The ‘X’ (Don’t care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62177EV30LL-55ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) Pb-free	Industrial
55	CY62177EV30LL-55BAXI	51-85191	48 ball FBGA (8 × 9.5 × 1.2 mm) Pb-free	Industrial

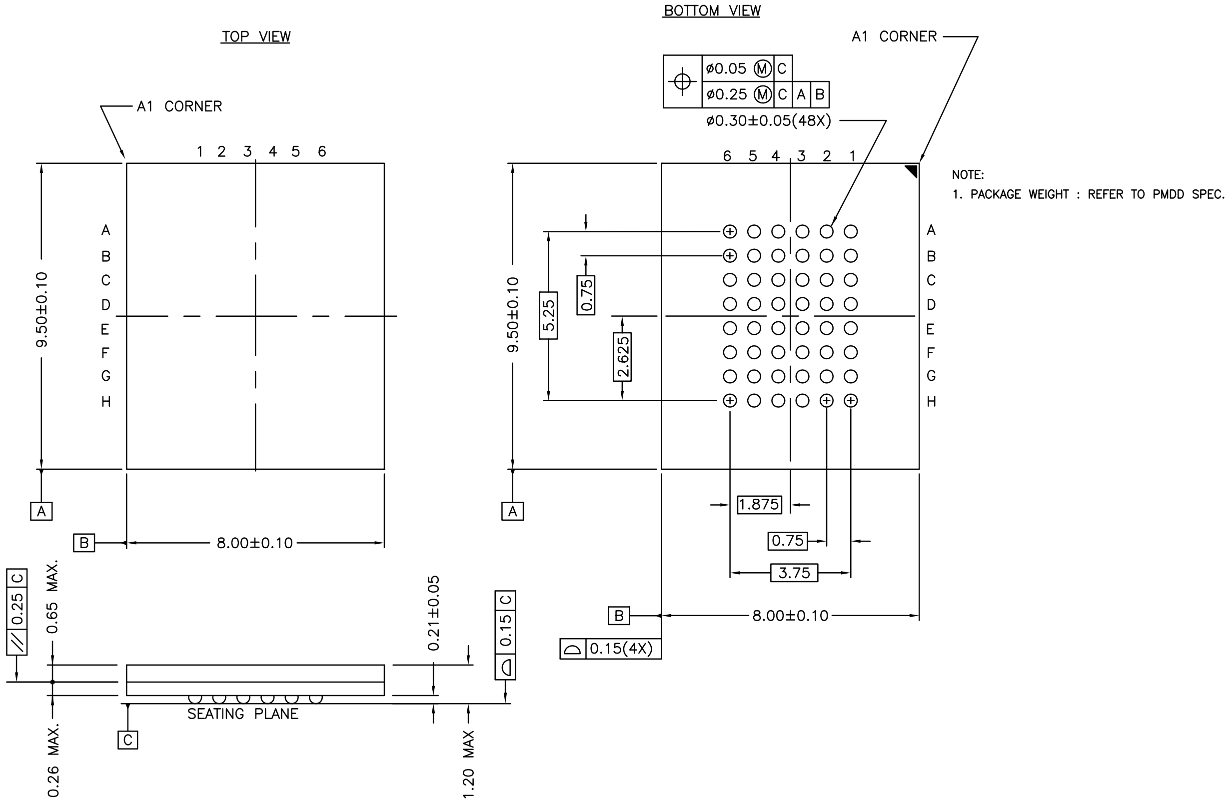
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 11. 48-ball FBGA (8 × 9.5 × 1.2 mm) Package Outline, 51-85191

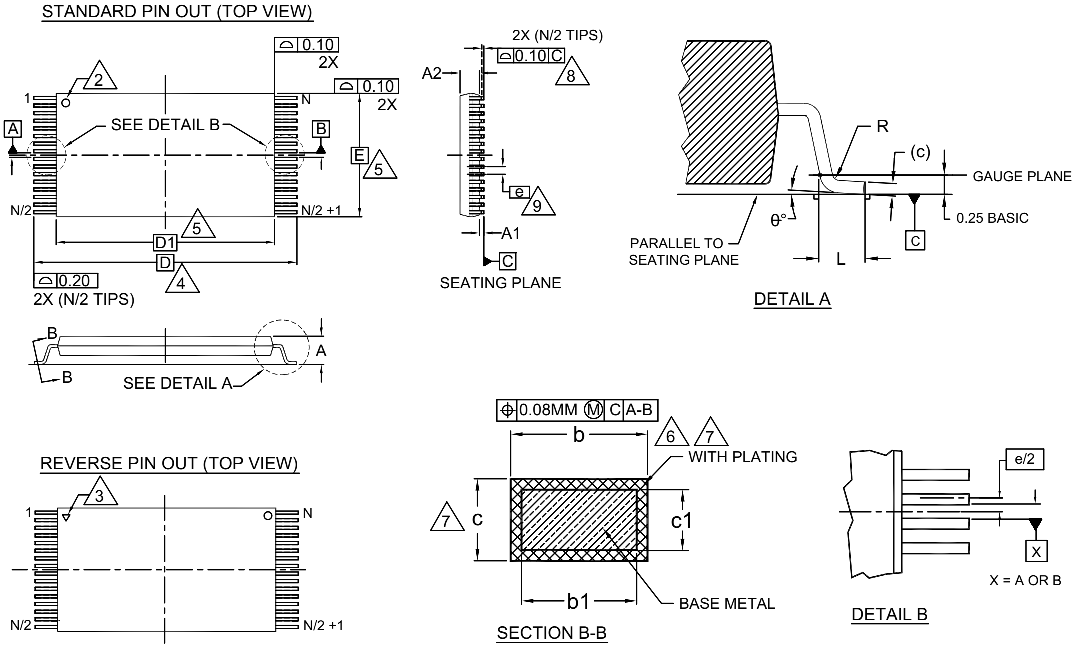


NOTE:
1. PACKAGE WEIGHT : REFER TO PMDD SPEC.

51-85191 *C

Package Diagram *(continued)*

Figure 12. 48-pin TSOP I (12 × 18.4 × 1 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM
Document Number: 001-09880

Revision	ECN	Submission Date	Description of Change
**	498562	08/31/2006	New data sheet.
*A	2544845	07/29/2008	Added 48-pin TSOP I package related information in all instances across the document. Removed 45 ns speed bin related information in all instances across the document. Added 70 ns speed bin related information in all instances across the document. Updated Electrical Characteristics: Added Note 10 and referred the same note in I_{SB2} parameter. Updated Ordering Information: Updated part numbers. Updated Package Diagram: Added spec 51-85183 *A.
*B	2589750	10/15/2008	Updated Pin Configurations: Updated Figure 1 (Changed pin functions of pin 10 from NC to A20 and pin 13 from A20 to DNU).
*C	2668432	03/03/2009	Removed 70 ns speed bin related information in all instances across the document. Added 55 ns speed bin related information in all instances across the document. Replaced 3.6 V with 3.7 V in V_{CC} range in all instances across the document. Updated Electrical Characteristics: Changed maximum value of I_{CC} parameter from 30 mA to 45 mA corresponding to Test Condition “f = $f_{(max)}$”. Changed maximum value of I_{CC} parameter from 2.8 mA to 4.5 mA corresponding to Test Condition “f = 1 MHz”. Removed I_{SB1} parameter and its details. Changed maximum value of I_{SB2} parameter from 17 µA to 25 µA. Referred Note 9 in I_{SB2} parameter. Updated Note 10.
*D	2779867	10/06/2009	Changed status from Preliminary to Final. Updated Electrical Characteristics: Added details of V_{IL} parameter corresponding to Test Condition “For TSOP I Package”. Added Note 8 and referred the same note in maximum value of V_{IL} parameter corresponding to Test Condition “For TSOP I Package”. Changed typical value of I_{CC} parameter from 28 mA to 35 mA corresponding to Test Condition “f = $f_{(max)}$”. Changed typical value of I_{CC} parameter from 2.2 mA to 4.5 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 4.5 mA to 5.5 mA corresponding to Test Condition “f = 1 MHz”. Updated Capacitance: Changed maximum value of C_{OUT} parameter from 10 pF to 15 pF. Updated Thermal Resistance: Replaced TBD with values in FBGA column. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 10 ns to 6 ns. Completing Sunset Review.
*E	2899662	03/26/2010	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85191 – Changed revision from ** to *A. spec 51-85183 – Changed revision from *A to *B.

Document History Page *(continued)*

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM
Document Number: 001-09880

Revision	ECN	Submission Date	Description of Change
*F	2927528	05/04/2010	Updated Electrical Characteristics: Updated Note 10. Updated Truth Table: Added Note 32 and referred the same note in respective places. Added Acronyms. Updated to new template.
*G	3177000	02/18/2011	Removed 48-ball FBGA package related information in all instances in the document. Updated Features (Removed 48-ball FBGA package related information). Updated Pin Configurations: Removed 48-ball FBGA package related information. Updated Note 1 (Replaced NC with DNU). Updated Electrical Characteristics (Updated details in “Test Conditions” column of I_{SB2} parameter). Updated Thermal Resistance (Removed 48-ball FBGA package related information). Updated Data Retention Characteristics (Updated details in “Conditions” column of I_{CCDR} parameter). Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagram: Removed spec 51-85191 *A. Updated Acronyms. Added Units of Measure. Updated to new template.
*H	3295175	06/29/2011	Updated Functional Description: Removed Note “For best practice recommendations, refer to the Cypress application note System Design Guidelines.” and its reference. Updated Package Diagram: spec 51-85183 – Changed revision from *B to *C.
*I	3461953	12/22/2011	Included 48-ball FBGA package related information in all instances in the document. Updated Ordering Information: Updated part numbers. Updated Package Diagram: Added spec 51-85191 *B.
*J	4100342	08/21/2013	Updated Switching Characteristics: Added Note 17 and referred the same note in “Parameter” column. Updated Package Diagram: spec 51-85191 – Changed revision from *B to *C. Updated to new template. Completing Sunset Review.
*K	4111710	09/12/2013	Updated Electrical Characteristics: Updated Note 10. Updated Data Retention Characteristics: Updated Note 13.
*L	4355423	04/29/2014	Updated Electrical Characteristics: Updated Note 10 (Issue is fixed so pin A_{20} can be left floating in standby). Updated Switching Characteristics: Added Note 21 and referred the same note in Write Cycle (for t_{PWE} parameter in $\overline{WE}$ Controlled, $\overline{OE}$ LOW condition). Updated Switching Waveforms: Added Note 31 and referred the same note in Figure 10 (for t_{PWE} parameter in $\overline{WE}$ Controlled, $\overline{OE}$ LOW condition).

Document History Page *(continued)*

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM **Document Number: 001-09880**			
Revision	**ECN**	**Submission Date**	**Description of Change**
*M	4567826	11/12/2014	Updated Features: Included 48-ball FBGA package related information. Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Maximum Ratings: Referred Notes 4, 5 in “Supply voltage to ground potential”. Completing Sunset Review.
*N	5017414	11/17/2015	Updated Thermal Resistance: Replaced “2-layer” with “four-layer” in “Test Conditions” column. Changed value of Θ_{JA} parameter corresponding to TSOP I package from 44.66 °C/W to 55.91 °C/W. Changed value of Θ_{JC} parameter corresponding to TSOP I package from 12.12 °C/W to 9.39 °C/W. Updated Package Diagram: spec 51-85183 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*O	6073315	02/16/2018	Updated Package Diagram: spec 51-85183 – Changed revision from *D to *F. Updated to new template.
*P	6315809	09/26/2018	Updated Maximum Ratings: Changed value of Latch-up current from “> 200 mA” to “> 140 mA”. Updated Operating Range: Replaced “2.2 V to 3.7 V” with “2.2 V to 3.6 V” under “V_{CC}” column. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 4.5 mA to 10 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 5.5 mA to 12 mA corresponding to Test Condition “f = 1 MHz”. Updated Thermal Resistance: Changed value of Θ_{JA} parameter corresponding to FBGA package from 38.1 °C/W to 54.8 °C/W. Changed value of Θ_{JC} parameter corresponding to FBGA package from 7.54 °C/W to 11.9 °C/W. Changed value of Θ_{JA} parameter corresponding to TSOP I package from 55.91 °C/W to 54.42 °C/W. Changed value of Θ_{JC} parameter corresponding to TSOP I package from 9.39 °C/W to 9.4 °C/W. Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 17 µA to 20 µA. Updated Switching Characteristics: Removed Note “In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.” and its reference in “Parameter” column. Changed minimum value of t_{OHA} parameter from 6 ns to 4 ns. Completing Sunset Review.

Document History Page *(continued)*

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM Document Number: 001-09880			
Revision	**ECN**	**Submission Date**	**Description of Change**
*Q	6692046	10/06/2019	Updated Product Portfolio: Changed maximum value of “Operating I_{CC}” under “Power Dissipation” from 12 mA to 18 mA corresponding to “f = 1 MHz”. Updated Electrical Characteristics: Changed maximum value of I_{CC} parameter from 12 mA to 18 mA corresponding to Test Condition “f = 1 MHz”. Updated to new template. Completing Sunset Review.

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