# THE DATASHEET OF

# CY7C1470V33-200BZI

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CY7C1470V33
CY7C1472V33
CY7C1474V33

# 72-Mbit (2M × 36/4M × 18/1M × 72) Pipelined SRAM with NoBL™ Architecture

## Features

- Pin compatible and functionally equivalent to ZBT
- Supports 200 MHz Bus operations with zero wait states
  - Available speed grades are 200 and 167 MHz
- Internally self timed output buffer control to eliminate the need to use asynchronous $\overline{OE}$
- Fully registered (inputs and outputs) for pipelined operation
- Byte write capability
- Single 3.3 V power supply
- 3.3 V/2.5 V I/O power supply
- Fast clock-to-output time
  - 3.0 ns (for 200 MHz device)
- Clock enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self timed writes
- CY7C1470V33 available in JEDEC-standard Pb-free 100-pin TQFP, and non Pb-free 165-ball FBGA package. CY7C1472V33 available in JEDEC-standard Pb-free 100-pin TQFP. CY7C1474V33 available in non Pb-free 209-ball FBGA package
- IEEE 1149.1 JTAG boundary scan compatible
- Burst capability – linear or interleaved burst order
- "ZZ" sleep mode option and stop clock option

## Functional Description

The CY7C1470V33, CY7C1472V33, and CY7C1474V33 are 3.3 V, 2M × 36/4M × 18/1M × 72 synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read/write operations with no wait states. The CY7C1470V33, CY7C1472V33, and CY7C1474V33 are equipped with the advanced (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write/read transitions. The CY7C1470V33, CY7C1472V33, and CY7C1474V33 are pin compatible and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

Write operations are controlled by the byte write selects ($\overline{BW_a}$–$\overline{BW_h}$ for CY7C1474V33, $\overline{BW_a}$–$\overline{BW_d}$ for CY7C1470V33 and $\overline{BW_a}$–$\overline{BW_b}$ for CY7C1472V33) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tristate control. In order to avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

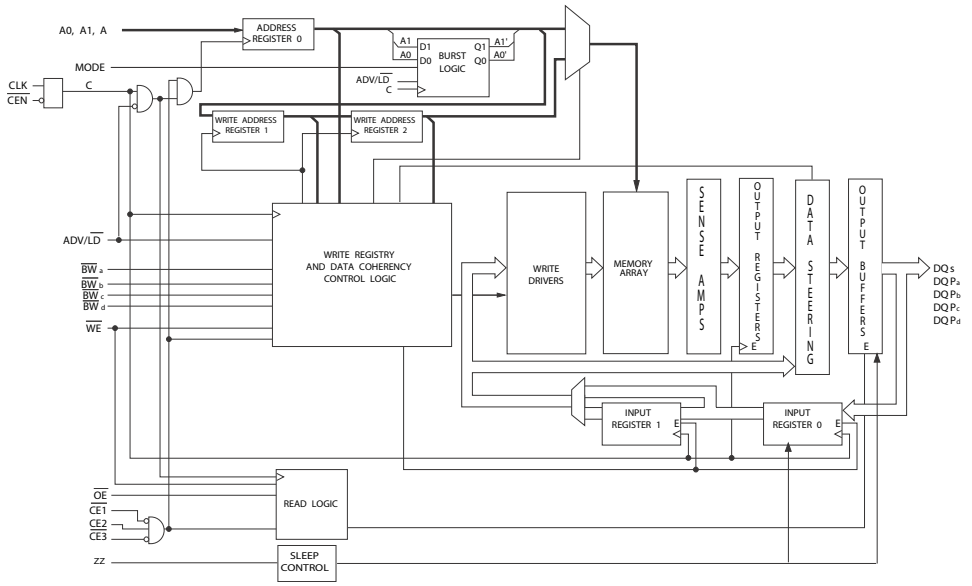
For a complete list of related documentation, click here.

## Selection Guide

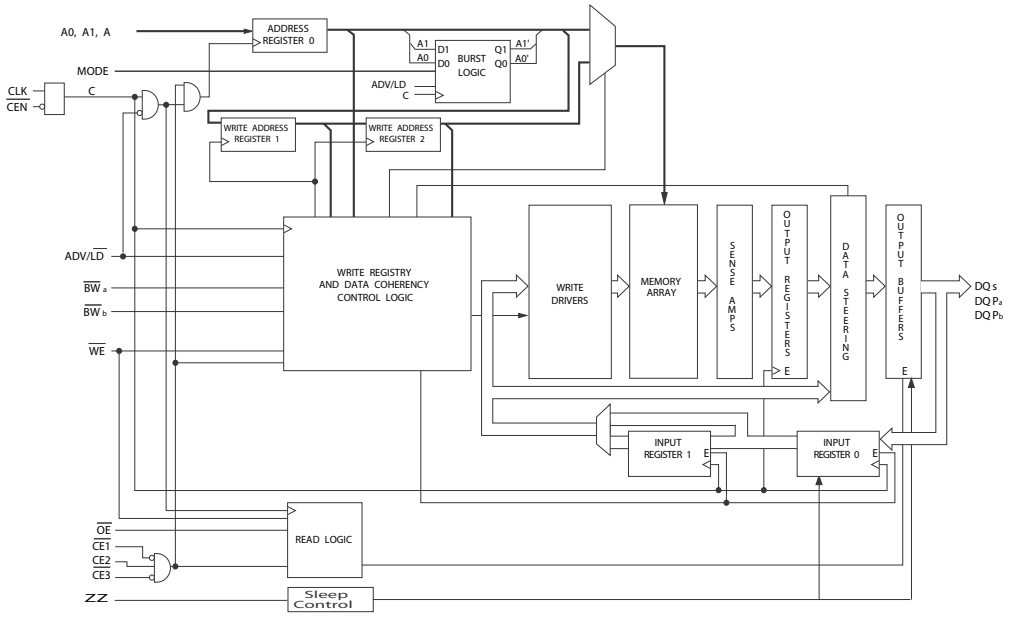
| Description | 200 MHz | 167 MHz | Unit |
|---|---|---|---|
| Maximum access time | 3.0 | 3.4 | ns |
| Maximum operating current | 500 | 450 | mA |
| Maximum CMOS standby current | 120 | 120 | mA |

Errata: For information on silicon errata, see Errata on page 35. Details include trigger conditions, devices affected, and proposed workaround.

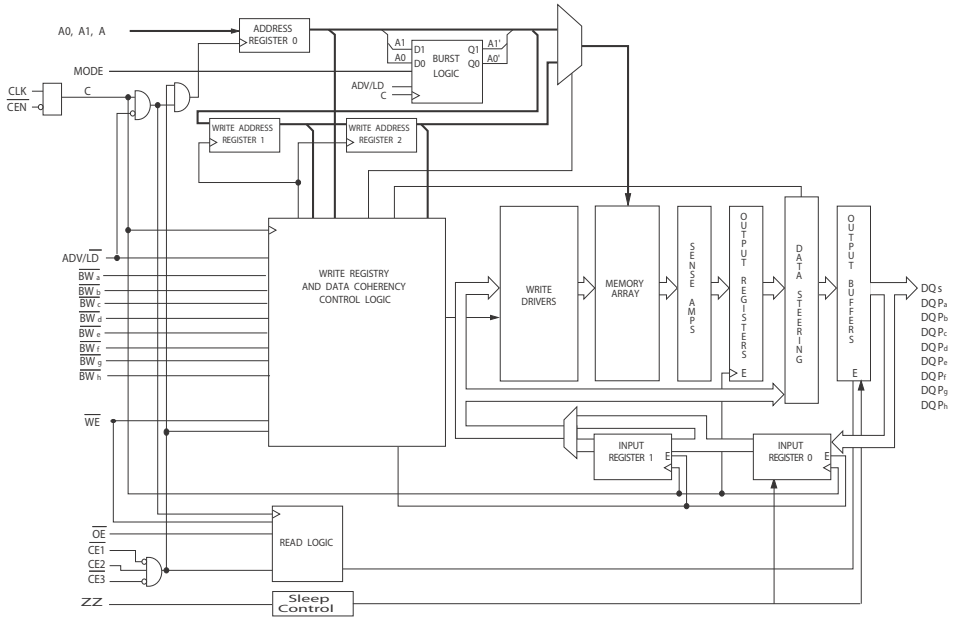
## Logic Block Diagram – CY7C1470V33




## Logic Block Diagram – CY7C1472V33



## Logic Block Diagram – CY7C1474V33



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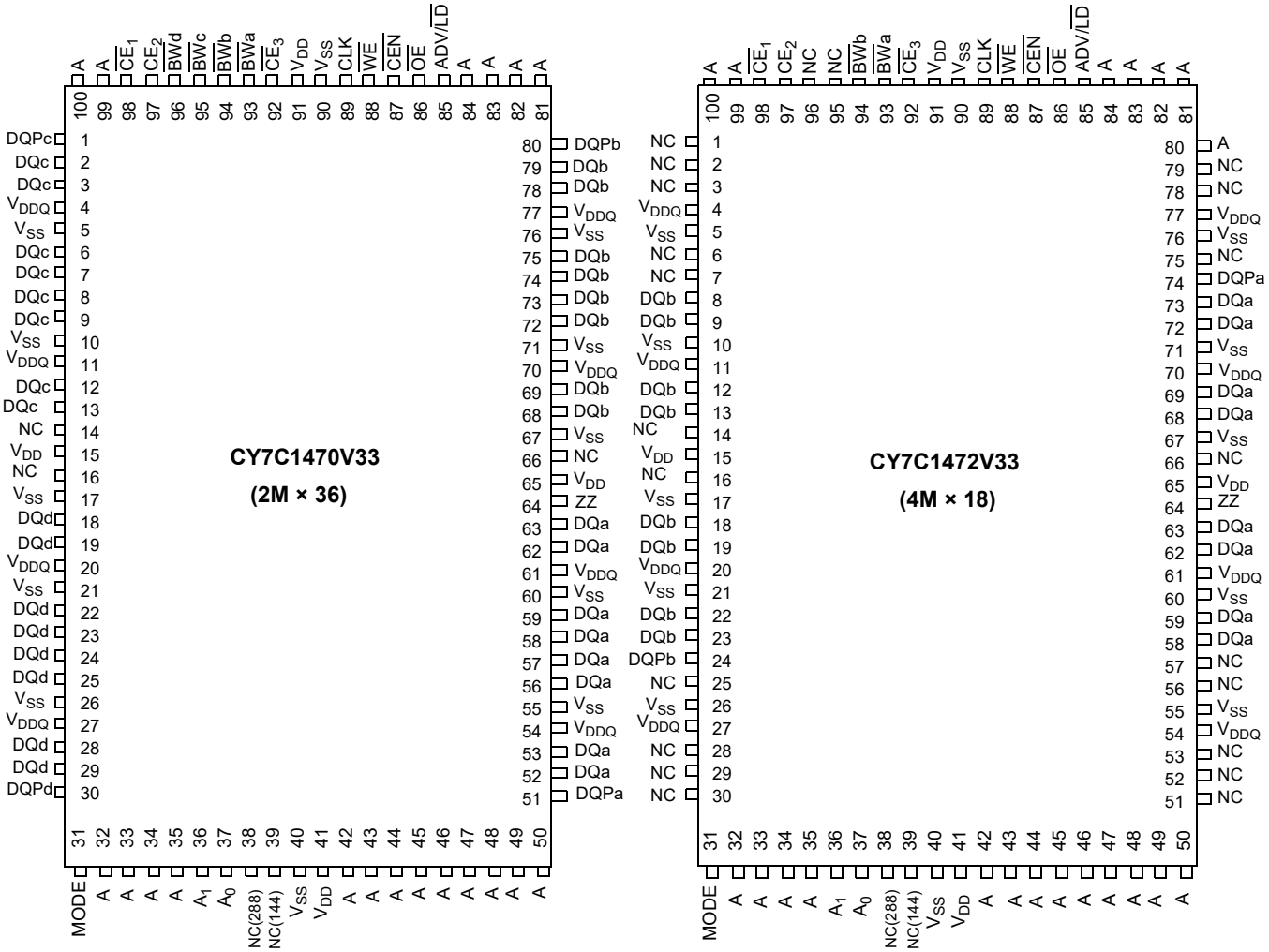
## Pin Configurations

**Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout** [1]




**Note**
1. Errata: The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see Errata on page 35.

## Pin Configurations *(continued)*

**Figure 2. 165-ball FBGA (15 × 17 × 1.4 mm) pinout [2]**

**CY7C1470V33 (2M × 36)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC/576M | A | $\overline{CE_1}$ | $\overline{BW_c}$ | $\overline{BW_b}$ | $\overline{CE_3}$ | $\overline{CEN}$ | ADV/$\overline{LD}$ | A | A | NC |
| **B** | NC/1G | A | CE2 | $\overline{BW_d}$ | $\overline{BW_a}$ | CLK | $\overline{WE}$ | $\overline{OE}$ | A | A | NC |
| **C** | $DQP_c$ | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_b$ |
| **D** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **E** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **F** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **G** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **K** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **L** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **M** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **N** | $DQP_d$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_a$ |
| **P** | NC/144M | A | A | A | TDI | A1 | TDO | A | A | A | NC/288M |
| **R** | MODE | A | A | A | TMS | A0 | TCK | A | A | A | A |

**Note**
2. Errata: The ZZ ball (H11) needs to be externally connected to ground. For more information, see Errata on page 35.

## Pin Configurations *(continued)*

**Figure 3. 209-ball FBGA (14 × 22 × 1.76 mm) pinout [3]**

**CY7C1474V33 (1M × 72)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | DQg | DQg | A | $CE_2$ | A | ADV/$\overline{LD}$ | A | $\overline{CE_3}$ | A | DQb | DQb |
| **B** | DQg | DQg | $\overline{BWS_c}$ | $\overline{BWS_g}$ | NC | $\overline{WE}$ | A | $\overline{BWS_b}$ | $\overline{BWS_f}$ | DQb | DQb |
| **C** | DQg | DQg | $\overline{BWS_h}$ | $\overline{BWS_d}$ | NC/576M | $\overline{CE_1}$ | NC | $\overline{BWS_e}$ | $\overline{BWS_a}$ | DQb | DQb |
| **D** | DQg | DQg | $V_{SS}$ | NC | NC/1G | $\overline{OE}$ | NC | NC | $V_{SS}$ | DQb | DQb |
| **E** | DQPg | DQPc | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQPf | DQPb |
| **F** | DQc | DQc | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | DQf | DQf |
| **G** | DQc | DQc | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQf | DQf |
| **H** | DQc | DQc | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | DQf | DQf |
| **J** | DQc | DQc | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQf | DQf |
| **K** | NC | NC | CLK | NC | $V_{SS}$ | $\overline{CEN}$ | $V_{SS}$ | NC | NC | NC | NC |
| **L** | DQh | DQh | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQa | DQa |
| **M** | DQh | DQh | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | DQa | DQa |
| **N** | DQh | DQh | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQa | DQa |
| **P** | DQh | DQh | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | ZZ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | DQa | DQa |
| **R** | DQPd | DQPh | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQPa | DQPe |
| **T** | DQd | DQd | $V_{SS}$ | NC | NC | MODE | NC | NC | $V_{SS}$ | DQe | DQe |
| **U** | DQd | DQd | NC/144M | A | A | A | A | A | NC/288M | DQe | DQe |
| **V** | DQd | DQd | A | A | A | A1 | A | A | A | DQe | DQe |
| **W** | DQd | DQd | TMS | TDI | A | A0 | A | TDO | TCK | DQe | DQe |

**Note**
3. Errata: The ZZ ball (P6) needs to be externally connected to ground. For more information, see Errata on page 35.

## Pin Definitions

| Pin Name | I/O Type | Pin Description |
|---|---|---|
| $A_0$, $A_1$, A | Input-synchronous | **Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK. |
| $\overline{BW_a}$, $\overline{BW_b}$, $\overline{BW_c}$, $\overline{BW_d}$, $\overline{BW_e}$, $\overline{BW_f}$, $\overline{BW_g}$, $\overline{BW_h}$ | Input-synchronous | **Byte write select inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW_a}$ controls $DQ_a$ and $DQP_a$, $\overline{BW_b}$ controls $DQ_b$ and $DQP_b$, $\overline{BW_c}$ controls $DQ_c$ and $DQP_c$, $\overline{BW_d}$ controls $DQ_d$ and $DQP_d$, $\overline{BW_e}$ controls $DQ_e$ and $DQP_e$, $\overline{BW_f}$ controls $DQ_f$ and $DQP_f$, $\overline{BW_g}$ controls $DQ_g$ and $DQP_g$, $\overline{BW_h}$ controls $DQ_h$ and $DQP_h$. |
| $\overline{WE}$ | Input-synchronous | **Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence. |
| ADV/$\overline{LD}$ | Input-synchronous | **Advance/load input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address. |
| CLK | Input-clock | **Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW. |
| $\overline{CE_1}$ | Input-synchronous | **Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE_3}$ to select/deselect the device. |
| $CE_2$ | Input-synchronous | **Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. |
| $\overline{CE_3}$ | Input-synchronous | **Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $CE_2$ to select/deselect the device. |
| $\overline{OE}$ | Input-asynchronous | **Output enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected. |
| $\overline{CEN}$ | Input-synchronous | **Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required. |
| $DQ_S$ | I/O-synchronous | **Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, $DQ_a$–$DQ_d$ are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. |
| $DQP_X$ | I/O-synchronous | **Bidirectional data parity I/O lines**. Functionally, these signals are identical to $DQ_X$. During write sequences, $DQP_a$ is controlled by $\overline{BW_a}$, $DQP_b$ is controlled by $\overline{BW_b}$, $DQP_c$ is controlled by $\overline{BW_c}$, and $DQP_d$ is controlled by $\overline{BW_d}$, $DQP_e$ is controlled by $\overline{BW_e}$, $DQP_f$ is controlled by $\overline{BW_f}$, $DQP_g$ is controlled by $\overline{BW_g}$, $DQP_h$ is controlled by $\overline{BW_h}$. |
| MODE | Input strap pin | **Mode input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order. |
| TDO | JTAG serial output synchronous | **Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. |
| TDI | JTAG serial input Synchronous | **Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. |

## Pin Definitions *(continued)*

| Pin Name | I/O Type | Pin Description |
|---|---|---|
| TMS | Test mode select synchronous | **This pin controls the test access port state machine**. Sampled on the rising edge of TCK. |
| TCK | JTAG clock | **Clock input to the JTAG circuitry**. |
| $V_{DD}$ | Power supply | **Power supply inputs to the core of the device**. |
| $V_{DDQ}$ | I/O power supply | **Power supply for the I/O circuitry**. |
| $V_{SS}$ | Ground | **Ground for the device**. Should be connected to ground of the system. |
| NC | – | **No connects**. This pin is not connected to the die. |
| NC (144M, 288M, 576M, 1G) | – | **These pins are not connected**. They will be used for expansion to the 144M, 288M, 576M, and 1G densities. |
| ZZ[4] | Input-asynchronous | **ZZ "Sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin has to be LOW or left floating.<br>ZZ pin has an internal pull-down. |

**Note**
4. Errata: The ZZ pin needs to be externally connected to ground. For more information, see Errata on page 35.

## Functional Overview

The CY7C1470V33, CY7C1472V33, and CY7C1474V33 are synchronous-pipelined burst NoBL SRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ($t_{CO}$) is 3.0 ns (200 MHz device).

Accesses can be initiated by asserting all three chip enables ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) active at the rising edge of the clock. If clock enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable ($\overline{WE}$). $\overline{BW_{[x]}}$ can be used to conduct byte write operations.

Write operations are qualified by the write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW after the device has been deselected in order to load a new address for the next operation.

### Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are all asserted active, (3) the write enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.0 ns (200 MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will tristate following the next clock rise.

### Burst Read Accesses

The CY7C1470V33, CY7C1472V33, and CY7C1474V33 have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in Single Read Accesses. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

### Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are all asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to the address inputs is loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically tristated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d,e,f,g,h}$/$DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1470V33 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1472V33). In addition, the address for the subsequent access (read/write/deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d,e,f,g,h}$/$DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1470V33 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1472V33) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by $\overline{BW}$ ($\overline{BW_{a,b,c,d,e,f,g,h}}$ for CY7C1474V33, $\overline{BW_{a,b,c,d}}$ for CY7C1470V33 and $\overline{BW_{a,b}}$ for CY7C1472V33) signals. The CY7C1470V33, CY7C1472V33, and CY7C1474V33 provides byte write capability that is described in the Write Cycle Description table. Asserting the write enable input ($\overline{WE}$) with the selected byte write select ($\overline{BW}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self timed Write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1470V33, CY7C1472V33, and CY7C1474V33 are common I/O devices, data should not be driven into the device while the outputs are active. The output enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d,e,f,g,h}$/$DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1470V33 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1472V33) inputs. Doing so will tristate the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d,e,f,g,h}$/$DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1470V33 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1472V33) are automatically tristated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

### Burst Write Accesses

The CY7C1470V33, CY7C1472V33, and CY7C1474V33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in Single Write Accesses on page 10. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct BW ($\overline{BW}_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $\overline{BW}_{a,b,c,d}$ for CY7C1470V33 and $\overline{BW}_{a,b}$ for CY7C1472V33) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$, must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

### Interleaved Burst Address Table

(MODE = Floating or $V_{DD}$)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

### Linear Burst Address Table

(MODE = GND)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

### ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | ZZ $\geq V_{DD} - 0.2$ V | – | 120 | mA |
| $t_{ZZS}$ | Device operation to ZZ | ZZ $\geq V_{DD} - 0.2$ V | – | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | ZZ $\leq 0.2$ V | $2t_{CYC}$ | – | ns |
| $t_{ZZI}$ | ZZ active to sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ Inactive to exit sleep current | This parameter is sampled | 0 | – | ns |

## Truth Table

The Truth Table for parts CY7C1470V33/CY7C1472V33/CY7C1474V33 is as follows. [5, 6, 7, 8, 9, 10, 11]

| Operation | Address Used | $\overline{CE}$ | ZZ | ADV/$\overline{LD}$ | $\overline{WE}$ | $\overline{BW_x}$ | $\overline{OE}$ | $\overline{CEN}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|
| Deselect cycle | None | H | L | L | X | X | X | L | L–H | Tri-state |
| Continue deselect cycle | None | X | L | H | X | X | X | L | L–H | Tri-state |
| Read cycle (begin burst) | External | L | L | L | H | X | L | L | L–H | Data out (Q) |
| Read cycle (continue burst) | Next | X | L | H | X | X | L | L | L–H | Data out (Q) |
| NOP/dummy read (begin burst) | External | L | L | L | H | X | H | L | L–H | Tri-state |
| Dummy read (continue burst) | Next | X | L | H | X | X | H | L | L–H | Tri-state |
| Write cycle (begin burst) | External | L | L | L | L | L | X | L | L–H | Data in (D) |
| Write cycle (continue burst) | Next | X | L | H | X | L | X | L | L–H | Data in (D) |
| NOP/write abort (begin burst) | None | L | L | L | L | H | X | L | L–H | Tri-state |
| Write abort (continue burst) | Next | X | L | H | X | H | X | L | L–H | Tri-state |
| Ignore clock edge (stall) | Current | X | L | X | X | X | X | H | L–H | – |
| Sleep mode | None | X | H | X | X | X | X | X | X | Tri-state |

**Notes**

5. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BW}$x = 0 signifies at least one byte write select is active, $\overline{BW}$x = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
6. Write is defined by $\overline{WE}$ and $\overline{BW}_{[a:d]}$. See Write Cycle Description table for details.
7. When a write cycle is detected, all I/Os are tristated, even during byte writes.
8. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
9. $\overline{CEN}$ = H inserts wait states.
10. Device will power-up deselected and the I/Os in a tristate condition, regardless of $\overline{OE}$.
11. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle $DQ_s$ and $DQP_{[a:d]}$ = tristate when $\overline{OE}$ is inactive or when the device is deselected, and $DQ_s$= data when OE is active.

## Partial Write Cycle Description

The partial write cycle description for part CY7C1470V33 is as follows. [12, 13, 14, 15]

| Function (CY7C1470V33) | $\overline{WE}$ | $\overline{BW_d}$ | $\overline{BW_c}$ | $\overline{BW_b}$ | $\overline{BW_a}$ |
|---|---|---|---|---|---|
| Read | H | X | X | X | X |
| Write – no bytes written | L | H | H | H | H |
| Write byte a – ($DQ_a$ and $DQP_a$) | L | H | H | H | L |
| Write byte b – ($DQ_b$ and $DQP_b$) | L | H | H | L | H |
| Write bytes b, a | L | H | H | L | L |
| Write byte c – ($DQ_c$ and $DQP_c$) | L | H | L | H | H |
| Write bytes c, a | L | H | L | H | L |
| Write bytes c, b | L | H | L | L | H |
| Write bytes c, b, a | L | H | L | L | L |
| Write byte d – ($DQ_d$ and $DQP_d$) | L | L | H | H | H |
| Write bytes d, a | L | L | H | H | L |
| Write bytes d, b | L | L | H | L | H |
| Write bytes d, b, a | L | L | H | L | L |
| Write bytes d, c | L | L | L | H | H |
| Write bytes d, c, a | L | L | L | H | L |
| Write bytes d, c, b | L | L | L | L | H |
| Write all bytes | L | L | L | L | L |

## Partial Write Cycle Description

The partial write cycle description for part CY7C1472V33 is as follows. [12, 13, 14, 15]

| Function (CY7C1472V33) | $\overline{WE}$ | $\overline{BW_b}$ | $\overline{BW_a}$ |
|---|---|---|---|
| Read | H | x | x |
| Write – no bytes written | L | H | H |
| Write byte a – ($DQ_a$ and $DQP_a$) | L | H | L |
| Write byte b – ($DQ_b$ and $DQP_b$) | L | L | H |
| Write both bytes | L | L | L |

**Notes**
12. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BW}$x = 0 signifies at least one byte write select is active, $\overline{BW}$x = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
13. Write is defined by $\overline{WE}$ and $\overline{BW}_{[a:d]}$. See Write Cycle Description table for details.
14. When a write cycle is detected, all I/Os are tristated, even during byte writes.
15. Table only lists a partial listing of the Byte Write combinations. Any combination of $\overline{BW}_{[a:d]}$ is valid. Appropriate write will be done based on which Byte Write is active.

## Partial Write Cycle Description

The partial write cycle description for part CY7C1474V33 is as follows. [16, 17, 18, 19]

| Function (CY7C1474V33) | $\overline{WE}$ | $\overline{BW_X}$ |
|---|---|---|
| Read | H | x |
| Write – no bytes written | L | H |
| Write byte X – ($DQ_X$ and $DQP_{X)}$ | L | L |
| Write all bytes | L | All $\overline{BW}$ = L |

**Notes**
16. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for all chip enables active. $\overline{BW}$x = 0 signifies at least one byte write select is active, $\overline{BW}$x = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
17. Write is defined by $\overline{WE}$ and $\overline{BW}_{[a:d]}$. See Write Cycle Description table for details.
18. When a write cycle is detected, all I/Os are tristated, even during byte writes.
19. Table only lists a partial listing of the Byte Write combinations. Any combination of $\overline{BW}_{[a:d]}$ is valid. Appropriate write will be done based on which Byte Write is active.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1470V33, and CY7C1474V33 incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1470V33, and CY7C1474V33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ($V_{SS}$) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to $V_{DD}$ through a pull up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

### Test Access Port (TAP)

*Test Clock (TCK)*

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

*Test Mode Select (TMS)*

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

*Test Data-In (TDI)*

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram on page 17. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

*Test Data-Out (TDO)*

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Identification Codes on page 21). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A RESET is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

*Instruction Register*

Three bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 18. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

*Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

*Boundary Scan Register*

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Exit Order on page 22 and Boundary Scan Exit Order on page 23 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

*Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### TAP Instruction Set

*Overview*

Eight different instructions are possible with the three bit instruction register. All combinations are listed in Identification

Codes on page 21. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

*EXTEST*

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high Z state.

*IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

*SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high Z state.

*SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time ($t_{CS}$ plus $t_{CH}$).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

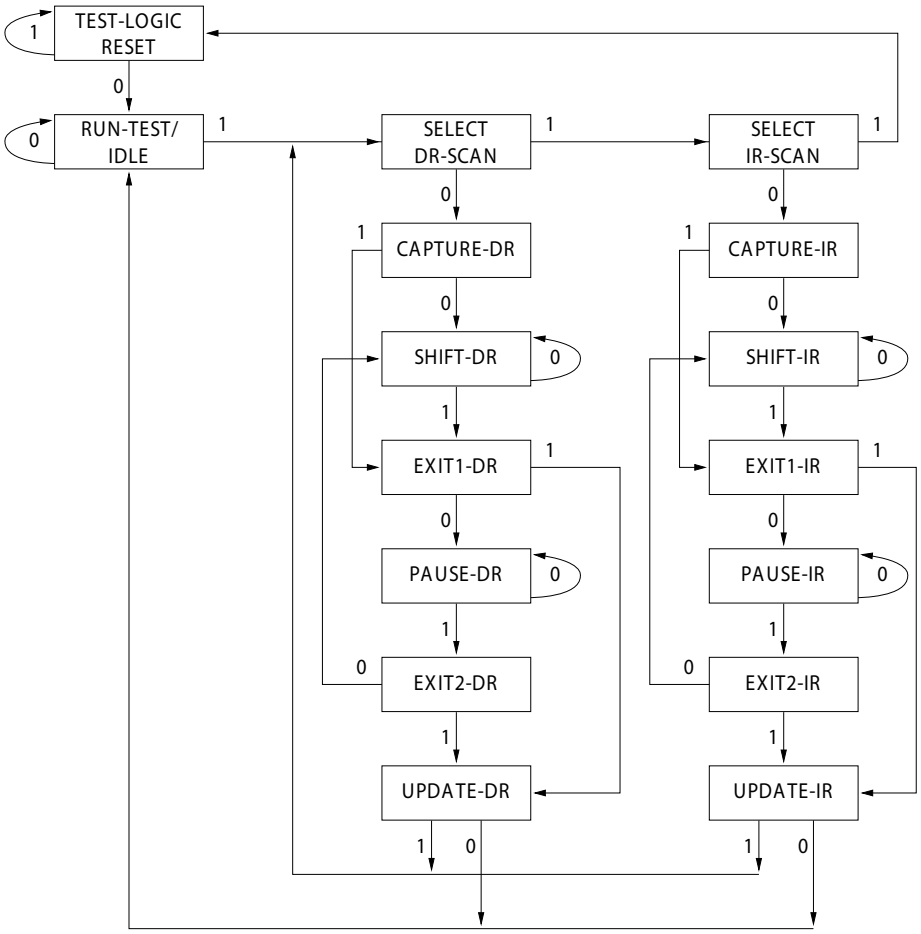
*BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

*Reserved*

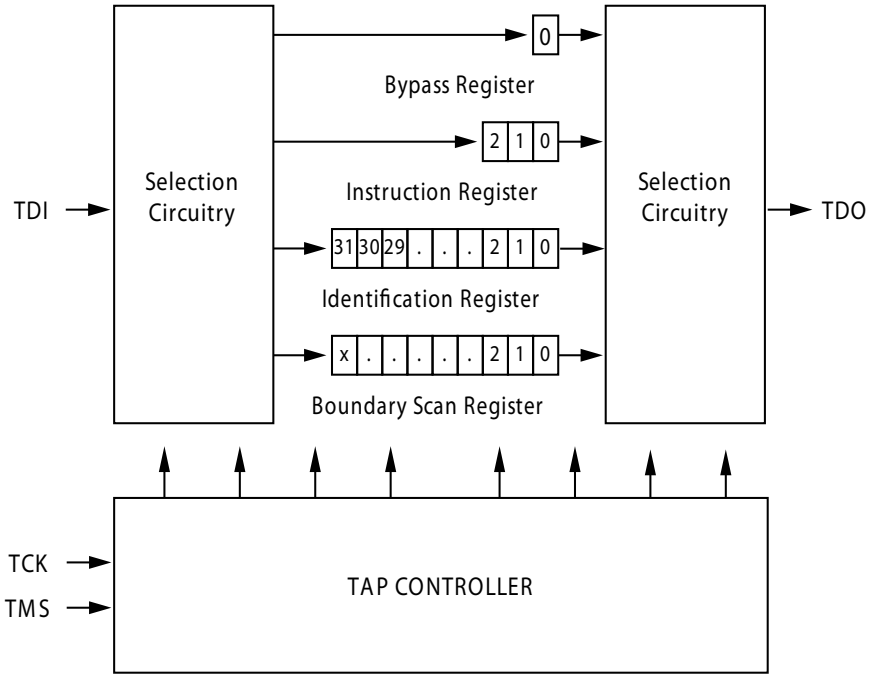
These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Controller State Diagram

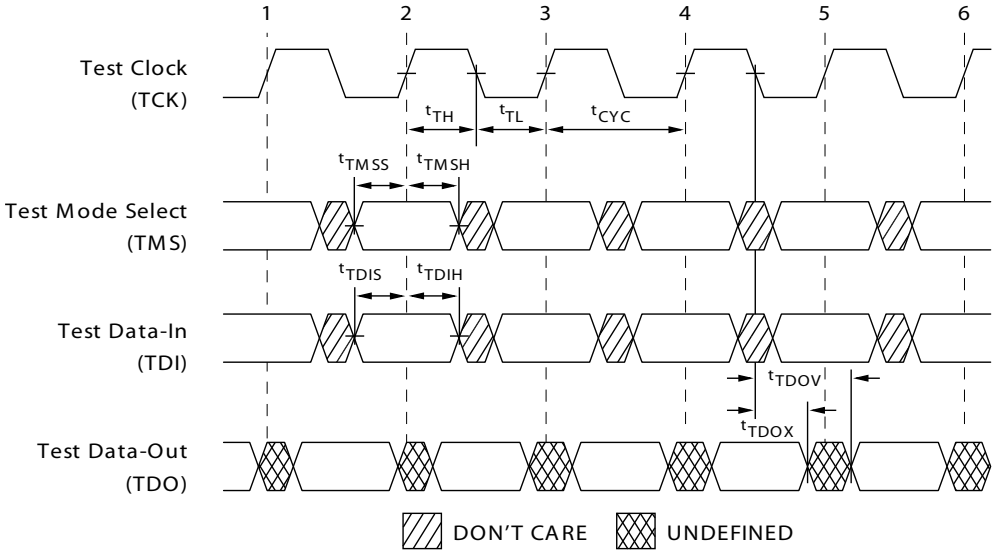



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

## TAP Controller Block Diagram




## TAP Timing Diagram



## TAP AC Switching Characteristics

Over the Operating Range

| Parameter [20, 21] | Description | Min | Max | Unit |
|---|---|---|---|---|
| **Clock** | | | | |
| $t_{TCYC}$ | TCK clock cycle time | 50 | – | ns |
| $t_{TF}$ | TCK clock frequency | – | 20 | MHz |
| $t_{TH}$ | TCK clock HIGH time | 20 | – | ns |
| $t_{TL}$ | TCK clock LOW time | 20 | – | ns |
| **Output Times** | | | | |
| $t_{TDOV}$ | TCK clock LOW to TDO valid | – | 10 | ns |
| $t_{TDOX}$ | TCK clock LOW to TDO invalid | 0 | – | ns |
| **Setup Times** | | | | |
| $t_{TMSS}$ | TMS setup to TCK clock rise | 5 | – | ns |
| $t_{TDIS}$ | TDI setup to TCK clock rise | 5 | – | ns |
| $t_{CS}$ | Capture setup to TCK rise | 5 | – | ns |
| **Hold Times** | | | | |
| $t_{TMSH}$ | TMS hold after TCK clock rise | 5 | – | ns |
| $t_{TDIH}$ | TDI hold after clock rise | 5 | – | ns |
| $t_{CH}$ | Capture hold after clock rise | 5 | – | ns |

**Notes**
20. $t_{CS}$ and $t_{CH}$ refer to the setup and hold time requirements of latching data from the boundary scan register.
21. Test conditions are specified using the load in TAP AC Test Conditions. $t_R/t_F$ = 1 ns.

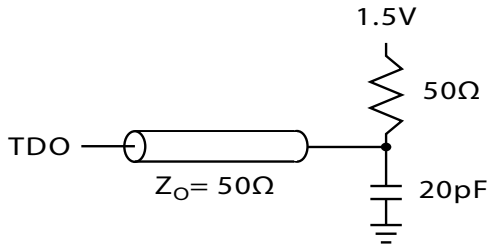
## 3.3 V TAP AC Test Conditions

Input pulse levels ..... $V_{SS}$ to 3.3 V
Input rise and fall times ..... 1 ns
Input timing reference levels ..... 1.5 V
Output reference levels ..... 1.5 V
Test load termination supply voltage ..... 1.5 V

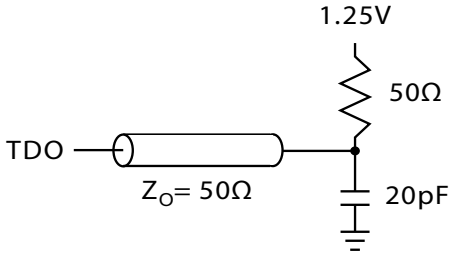
## 2.5 V TAP AC Test Conditions

Input pulse levels ..... $V_{SS}$ to 2.5 V
Input rise and fall time ..... 1 ns
Input timing reference levels ..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

## 3.3 V TAP AC Output Load Equivalent




## 2.5 V TAP AC Output Load Equivalent




## TAP DC Electrical Characteristics and Operating Conditions

(0 °C < $T_A$ < +70 °C; $V_{DD}$ = 3.135 V to 3.6 V unless otherwise noted)

| Parameter [22] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH voltage | $I_{OH}$ = –4.0 mA, $V_{DDQ}$ = 3.3 V | | 2.4 | – | V |
| | | $I_{OH}$ = –1.0 mA, $V_{DDQ}$ = 2.5 V | | 2.0 | – | V |
| $V_{OH2}$ | Output HIGH voltage | $I_{OH}$ = –100 µA | $V_{DDQ}$ = 3.3 V | 2.9 | – | V |
| | | | $V_{DDQ}$ = 2.5 V | 2.1 | – | V |
| $V_{OL1}$ | Output LOW voltage | $I_{OL}$ = 8.0 mA | $V_{DDQ}$ = 3.3 V | – | 0.4 | V |
| | | $I_{OL}$ = 1.0 mA | $V_{DDQ}$ = 2.5 V | – | 0.4 | V |
| $V_{OL2}$ | Output LOW voltage | $I_{OL}$ = 100 µA | $V_{DDQ}$ = 3.3 V | – | 0.2 | V |
| | | | $V_{DDQ}$ = 2.5 V | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage | | $V_{DDQ}$ = 3.3 V | 2.0 | $V_{DD}$ + 0.3 | V |
| | | | $V_{DDQ}$ = 2.5 V | 1.7 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | | $V_{DDQ}$ = 3.3 V | –0.3 | 0.8 | V |
| | | | $V_{DDQ}$ = 2.5 V | –0.3 | 0.7 | V |
| $I_X$ | Input load current | GND ≤ $V_{IN}$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |

**Note**
22. All voltages referenced to $V_{SS}$ (GND).

## Identification Register Definitions

| Instruction Field | CY7C1470V33 (2M × 36) | CY7C1474V33 (1M × 72) | Description |
|---|---|---|---|
| Revision number (31:29) | 000 | 000 | Describes the version number |
| Device depth (28:24) [23] | 01011 | 01011 | Reserved for internal use |
| Architecture/memory type (23:18) | 001000 | 001000 | Defines memory type and architecture |
| Bus width/density (17:12) | 100100 | 110100 | Defines width and density |
| Cypress JEDEC ID code (11:1) | 00000110100 | 00000110100 | Allows unique identification of SRAM vendor |
| ID register presence indicator (0) | 1 | 1 | Indicates the presence of an ID register |

## Scan Register Sizes

| Register Name | Bit Size (× 36) | Bit Size (× 72) |
|---|---|---|
| Instruction | 3 | 3 |
| Bypass | 1 | 1 |
| ID | 32 | 32 |
| Boundary scan order – 165-ball FBGA | 71 | – |
| Boundary scan order – 209-ball FBGA | – | 110 |

## Identification Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state. This instruction is not 1149.1 compliant. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |

**Note**
23. Bit #24 is “1” in the ID Register Definitions for both 2.5 V and 3.3 V versions of this device.

## Boundary Scan Exit Order

(2M × 36)

| Bit # | 165-ball ID |
|---|---|
| 1 | C1 |
| 2 | D1 |
| 3 | E1 |
| 4 | D2 |
| 5 | E2 |
| 6 | F1 |
| 7 | G1 |
| 8 | F2 |
| 9 | G2 |
| 10 | J1 |
| 11 | K1 |
| 12 | L1 |
| 13 | J2 |
| 14 | M1 |
| 15 | N1 |
| 16 | K2 |
| 17 | L2 |
| 18 | M2 |
| 19 | R1 |
| 20 | R2 |

| Bit # | 165-ball ID |
|---|---|
| 21 | R3 |
| 22 | P2 |
| 23 | R4 |
| 24 | P6 |
| 25 | R6 |
| 26 | R8 |
| 27 | P3 |
| 28 | P4 |
| 29 | P8 |
| 30 | P9 |
| 31 | P10 |
| 32 | R9 |
| 33 | R10 |
| 34 | R11 |
| 35 | N11 |
| 36 | M11 |
| 37 | L11 |
| 38 | M10 |
| 39 | L10 |
| 40 | K11 |

| Bit # | 165-ball ID |
|---|---|
| 41 | J11 |
| 42 | K10 |
| 43 | J10 |
| 44 | H11 |
| 45 | G11 |
| 46 | F11 |
| 47 | E11 |
| 48 | D10 |
| 49 | D11 |
| 50 | C11 |
| 51 | G10 |
| 52 | F10 |
| 53 | E10 |
| 54 | A9 |
| 55 | B9 |
| 56 | A10 |
| 57 | B10 |
| 58 | A8 |
| 59 | B8 |
| 60 | A7 |

| Bit # | 165-ball ID |
|---|---|
| 61 | B7 |
| 62 | B6 |
| 63 | A6 |
| 64 | B5 |
| 65 | A5 |
| 66 | A4 |
| 67 | B4 |
| 68 | B3 |
| 69 | A3 |
| 70 | A2 |
| 71 | B2 |

## Boundary Scan Exit Order

(1M × 72)

| Bit # | 209-ball ID |
|---|---|
| 1 | A1 |
| 2 | A2 |
| 3 | B1 |
| 4 | B2 |
| 5 | C1 |
| 6 | C2 |
| 7 | D1 |
| 8 | D2 |
| 9 | E1 |
| 10 | E2 |
| 11 | F1 |
| 12 | F2 |
| 13 | G1 |
| 14 | G2 |
| 15 | H1 |
| 16 | H2 |
| 17 | J1 |
| 18 | J2 |
| 19 | L1 |
| 20 | L2 |
| 21 | M1 |
| 22 | M2 |
| 23 | N1 |
| 24 | N2 |
| 25 | P1 |
| 26 | P2 |
| 27 | R2 |
| 28 | R1 |

| Bit # | 209-ball ID |
|---|---|
| 29 | T1 |
| 30 | T2 |
| 31 | U1 |
| 32 | U2 |
| 33 | V1 |
| 34 | V2 |
| 35 | W1 |
| 36 | W2 |
| 37 | T6 |
| 38 | V3 |
| 39 | V4 |
| 40 | U4 |
| 41 | W5 |
| 42 | V6 |
| 43 | W6 |
| 44 | V5 |
| 45 | U5 |
| 46 | U6 |
| 47 | W7 |
| 48 | V7 |
| 49 | U7 |
| 50 | V8 |
| 51 | V9 |
| 52 | W11 |
| 53 | W10 |
| 54 | V11 |
| 55 | V10 |
| 56 | U11 |

| Bit # | 209-ball ID |
|---|---|
| 57 | U10 |
| 58 | T11 |
| 59 | T10 |
| 60 | R11 |
| 61 | R10 |
| 62 | P11 |
| 63 | P10 |
| 64 | N11 |
| 65 | N10 |
| 66 | M11 |
| 67 | M10 |
| 68 | L11 |
| 69 | L10 |
| 70 | P6 |
| 71 | J11 |
| 72 | J10 |
| 73 | H11 |
| 74 | H10 |
| 75 | G11 |
| 76 | G10 |
| 77 | F11 |
| 78 | F10 |
| 79 | E10 |
| 80 | E11 |
| 81 | D11 |
| 82 | D10 |
| 83 | C11 |
| 84 | C10 |

| Bit # | 209-ball ID |
|---|---|
| 85 | B11 |
| 86 | B10 |
| 87 | A11 |
| 88 | A10 |
| 89 | A7 |
| 90 | A5 |
| 91 | A9 |
| 92 | U8 |
| 93 | A6 |
| 94 | D6 |
| 95 | K6 |
| 96 | B6 |
| 97 | K3 |
| 98 | A8 |
| 99 | B4 |
| 100 | B3 |
| 101 | C3 |
| 102 | C4 |
| 103 | C8 |
| 104 | C9 |
| 105 | B9 |
| 106 | B8 |
| 107 | A4 |
| 108 | C6 |
| 109 | B7 |
| 110 | A3 |

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on $V_{DD}$ relative to GND .....–0.5 V to +4.6 V

Supply voltage on $V_{DDQ}$ relative to GND ..... –0.5 V to +$V_{DD}$

DC to outputs in tri-state .....–0.5 V to $V_{DDQ}$ + 0.5 V

DC input voltage .....–0.5 V to $V_{DD}$ + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) .....> 2001 V

Latch-up current .....> 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0 °C to +70 °C | 3.3 V – 5% / + 10% | 2.5 V – 5% to $V_{DD}$ |
| Industrial | –40 °C to +85 °C | | |

## Neutron Soft Error Immunity

| Parameter | Description | Test Conditions | Typ | Max* | Unit |
|---|---|---|---|---|---|
| LSBU | Logical single bit upsets | 25 °C | 361 | 394 | FIT/ Mb |
| LMBU | Logical multi bit upsets | 25 °C | 0 | 0.01 | FIT/ Mb |
| SEL | Single event latch-up | 85 °C | 0 | 0.1 | FIT/ Dev |

* *No LMBU or SEL events occurred during testing*; this column represents a statistical $\chi^2$, 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

## Electrical Characteristics

Over the Operating Range

| Parameter [24, 25] | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 3.135 | 3.6 | V |
| $V_{DDQ}$ | I/O supply voltage | for 3.3 V I/O | 3.135 | $V_{DD}$ | V |
| | | for 2.5 V I/O | 2.375 | 2.625 | V |
| $V_{OH}$ | Output HIGH voltage | for 3.3 V I/O, $I_{OH}$ = –4.0 mA | 2.4 | – | V |
| | | for 2.5 V I/O, $I_{OH}$= –1.0 mA | 2.0 | – | V |
| $V_{OL}$ | Output LOW voltage | for 3.3 V I/O, $I_{OL}$= 8.0 mA | – | 0.4 | V |
| | | for 2.5 V I/O, $I_{OL}$= 1.0 mA | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage [24] | for 3.3 V I/O | 2.0 | $V_{DD}$ + 0.3 | V |
| | | for 2.5 V I/O | 1.7 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage [24] | for 3.3 V I/O | –0.3 | 0.8 | V |
| | | for 2.5 V I/O | –0.3 | 0.7 | V |
| $I_X$ | Input leakage current except ZZ and MODE | GND ≤ $V_I$ ≤ $V_{DDQ}$ | –5 | 5 | µA |
| | Input current of MODE | Input = $V_{SS}$ | –30 | – | µA |
| | | Input = $V_{DD}$ | – | 5 | µA |
| | Input current of ZZ | Input = $V_{SS}$ | –5 | – | µA |
| | | Input = $V_{DD}$ | – | 30 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_I$ ≤ $V_{DDQ}$, output disabled | –5 | 5 | µA |

**Notes**

24. Overshoot: $V_{IH(AC)}$ < $V_{DD}$ +1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than $t_{CYC}/2$).
25. $T_{power\ up}$: Assumes a linear ramp from 0 V to $V_{DD(Min)}$ within 200 ms. During this time $V_{IH}$ < $V_{DD}$ and $V_{DDQ}$ ≤ $V_{DD}$.

## Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter [24, 25] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ operating supply | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{CYC}$ | 5.0 ns cycle, 200 MHz | – | 500 | mA |
| | | | 6.0 ns cycle, 167 MHz | – | 450 | mA |
| $I_{SB1}$ | Automatic CE power-down current – TTL inputs | Max $V_{DD}$, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = $f_{MAX}$ = $1/t_{CYC}$ | 5.0 ns cycle, 200 MHz | – | 245 | mA |
| | | | 6.0 ns cycle, 167 MHz | – | 245 | mA |
| $I_{SB2}$ | Automatic CE power-down current – CMOS inputs | Max $V_{DD}$, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0 | All speed grades | – | 120 | mA |
| $I_{SB3}$ | Automatic CE power-down current – CMOS inputs | Max $V_{DD}$, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = $f_{MAX}$ = $1/t_{CYC}$ | 5.0 ns cycle, 200 MHz | – | 245 | mA |
| | | | 6.0 ns cycle, 167 MHz | – | 245 | mA |
| $I_{SB4}$ | Automatic CE power-down current – TTL inputs | Max $V_{DD}$, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0 | All speed grades | – | 135 | mA |

## Capacitance

| Parameter [26] | Description | Test Conditions | 100-pin TQFP Max | 165-ball FBGA Max | 209-ball FBGA Max | Unit |
|---|---|---|---|---|---|---|
| $C_{ADDRESS}$ | Address input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 3.3 V, $V_{DDQ}$ = 2.5 V | 6 | 6 | 6 | pF |
| $C_{DATA}$ | Data input capacitance | | 5 | 5 | 5 | pF |
| $C_{CTRL}$ | Control input capacitance | | 8 | 8 | 8 | pF |
| $C_{CLK}$ | Clock input capacitance | | 6 | 6 | 6 | pF |
| $C_{I/O}$ | Input/output capacitance | | 5 | 5 | 5 | pF |

## Thermal Resistance

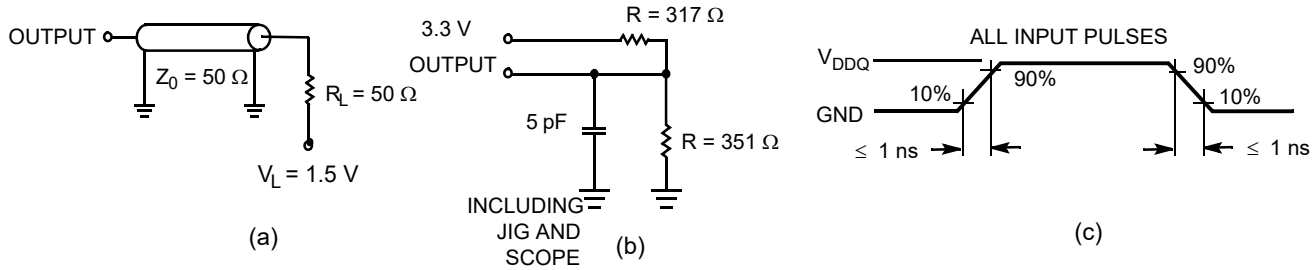
| Parameter [26] | Description | Test Conditions | 100-pin TQFP Package | 165-ball FBGA Package | 209-ball FBGA Package | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 24.63 | 16.3 | 15.2 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 2.28 | 2.1 | 1.7 | °C/W |

**Note**
26. Tested initially and after any design or process changes that may affect these parameters.

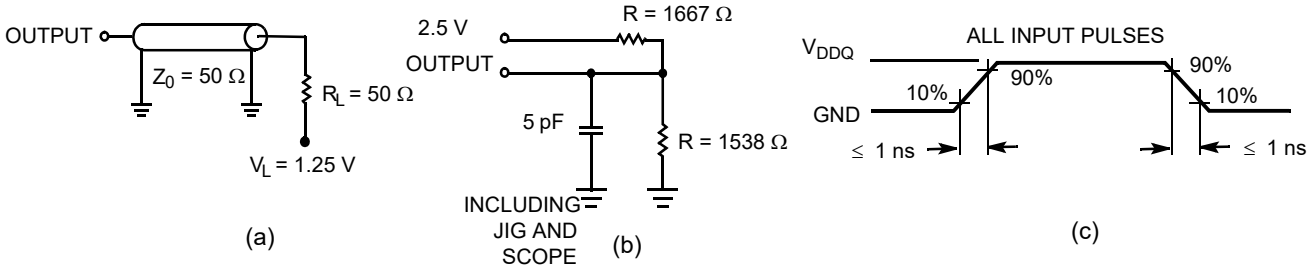
## AC Test Loads and Waveforms

**Figure 4. AC Test Loads and Waveforms**

**3.3 V I/O Test Load**




**2.5 V I/O Test Load**



## Switching Characteristics

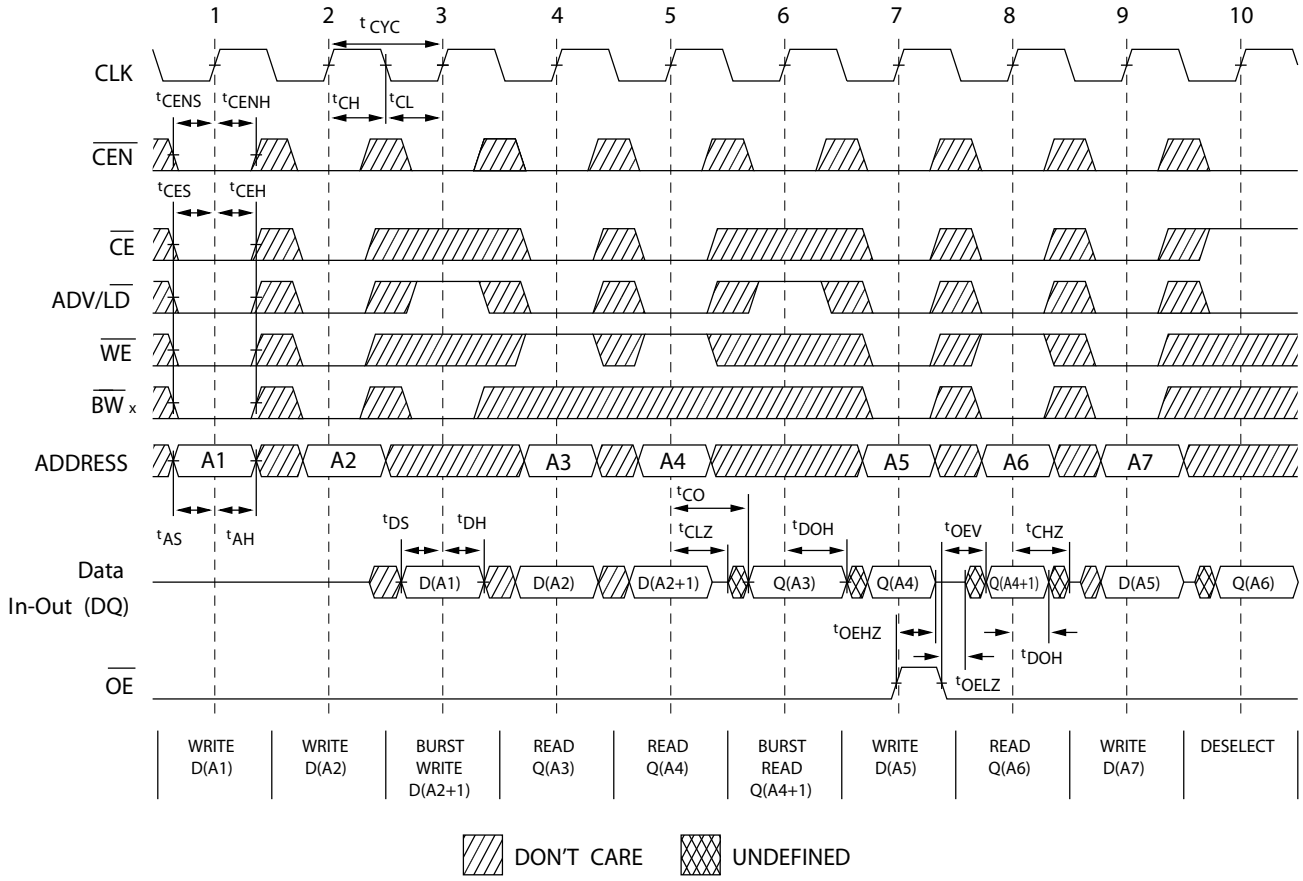
Over the Operating Range

| Parameter [27, 28] | Description | -200 | | -167 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{Power}$ [29] | $V_{CC(typical)}$ to the first access read or write | 1 | – | 1 | – | ms |
| **Clock** | | | | | | |
| $t_{CYC}$ | Clock cycle time | 5.0 | – | 6.0 | – | ns |
| $F_{MAX}$ | Maximum operating frequency | – | 200 | – | 167 | MHz |
| $t_{CH}$ | Clock HIGH | 2.0 | – | 2.2 | – | ns |
| $t_{CL}$ | Clock LOW | 2.0 | – | 2.2 | – | ns |
| **Output Times** | | | | | | |
| $t_{CO}$ | Data output valid after CLK rise | – | 3.0 | – | 3.4 | ns |
| $t_{OEV}$ | $\overline{OE}$ LOW to output valid | – | 3.0 | – | 3.4 | ns |
| $t_{DOH}$ | Data output hold after CLK rise | 1.3 | – | 1.5 | – | ns |
| $t_{CHZ}$ | Clock to high Z [30, 31, 32] | – | 3.0 | – | 3.4 | ns |
| $t_{CLZ}$ | Clock to low Z [30, 31, 32] | 1.3 | – | 1.5 | – | ns |
| $t_{EOHZ}$ | $\overline{OE}$ HIGH to output high Z [30, 31, 32] | – | 3.0 | – | 3.4 | ns |
| $t_{EOLZ}$ | $\overline{OE}$ LOW to output low Z [30, 31, 32] | 0 | – | 0 | – | ns |
| **Setup Times** | | | | | | |
| $t_{AS}$ | Address setup before CLK rise | 1.4 | – | 1.5 | – | ns |
| $t_{DS}$ | Data input setup before CLK rise | 1.4 | – | 1.5 | – | ns |
| $t_{CENS}$ | $\overline{CEN}$ setup before CLK rise | 1.4 | – | 1.5 | – | ns |
| $t_{WES}$ | $\overline{WE}$, $\overline{BW_X}$ setup before CLK rise | 1.4 | – | 1.5 | – | ns |
| $t_{ALS}$ | ADV/$\overline{LD}$ setup before CLK rise | 1.4 | – | 1.5 | – | ns |
| $t_{CES}$ | Chip select setup | 1.4 | – | 1.5 | – | ns |
| **Hold Times** | | | | | | |
| $t_{AH}$ | Address hold after CLK rise | 0.4 | – | 0.5 | – | ns |
| $t_{DH}$ | Data input hold after CLK rise | 0.4 | – | 0.5 | – | ns |
| $t_{CENH}$ | $\overline{CEN}$ hold after CLK rise | 0.4 | – | 0.5 | – | ns |
| $t_{WEH}$ | $\overline{WE}$, $\overline{BW_X}$ hold after CLK rise | 0.4 | – | 0.5 | – | ns |
| $t_{ALH}$ | ADV/$\overline{LD}$ hold after CLK rise | 0.4 | – | 0.5 | – | ns |
| $t_{CEH}$ | Chip select hold after CLK rise | 0.4 | – | 0.5 | – | ns |

**Notes**
27. Timing reference is 1.5 V when $V_{DDQ}$ = 3.3 V and is 1.25 V when $V_{DDQ}$ = 2.5 V.
28. Test conditions shown in (a) of Figure 4 on page 26 unless otherwise noted.
29. This part has a voltage regulator internally; $t_{power}$ is the time power needs to be supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
30. $t_{CHZ}$, $t_{CLZ}$, $t_{EOLZ}$, and $t_{EOHZ}$ are specified with AC test conditions shown in (b) of Figure 4 on page 26. Transition is measured ±200 mV from steady-state voltage.
31. At any voltage and temperature, $t_{EOHZ}$ is less than $t_{EOLZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
32. This parameter is sampled and not 100% tested.

## Switching Waveforms

**Figure 5. Read/Write/Timing** [33, 34, 35]




**Notes**
33. For this waveform ZZ is tied LOW.
34. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.
35. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1= Interleaved). Burst operations are optional.

## Switching Waveforms *(continued)*

**Figure 6. NOP, STALL and DESELECT Cycles** [36, 37, 38]

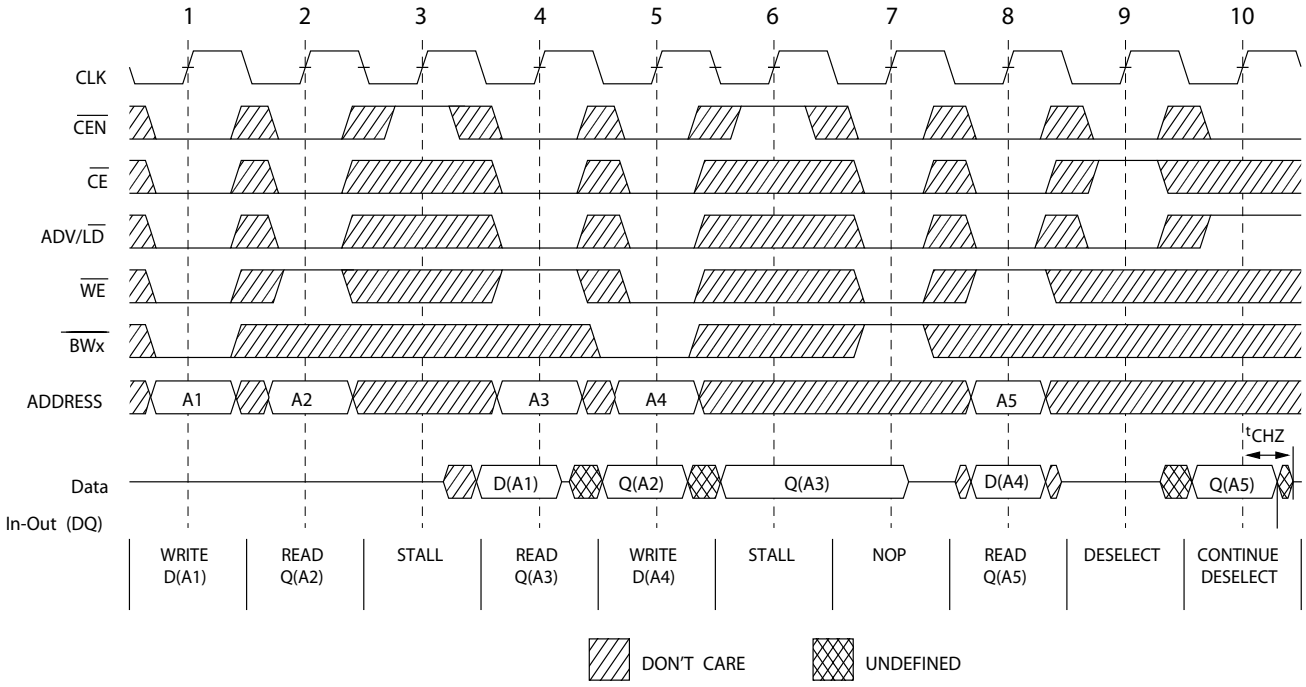
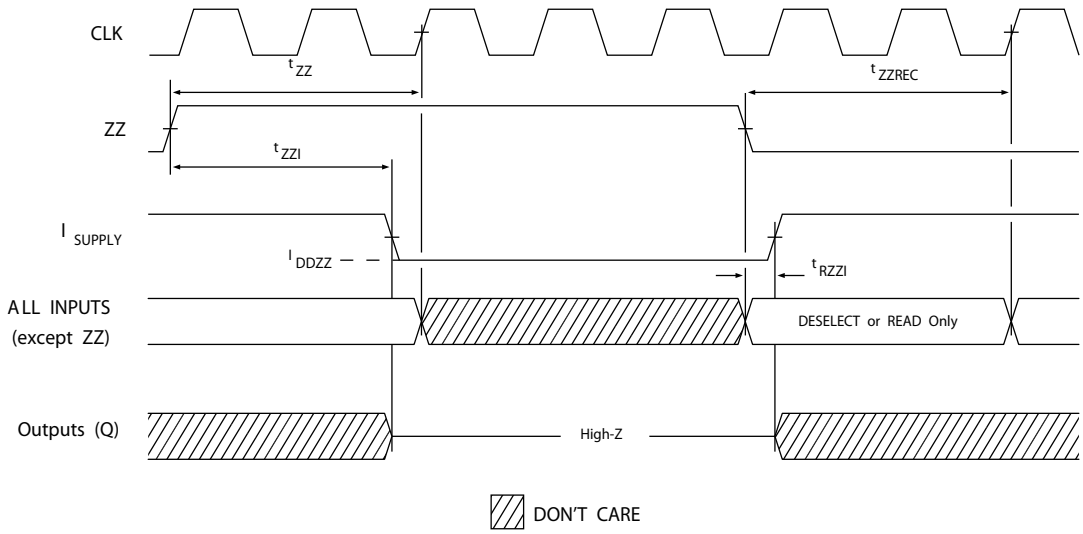



**Figure 7. ZZ Mode Timing** [39, 40]




**Notes**
36. For this waveform ZZ is tied LOW.
37. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, $CE_2$ is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or $CE_2$ is LOW or $\overline{CE_3}$ is HIGH.
38. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.
39. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
40. I/Os are in high Z when exiting ZZ sleep mode.

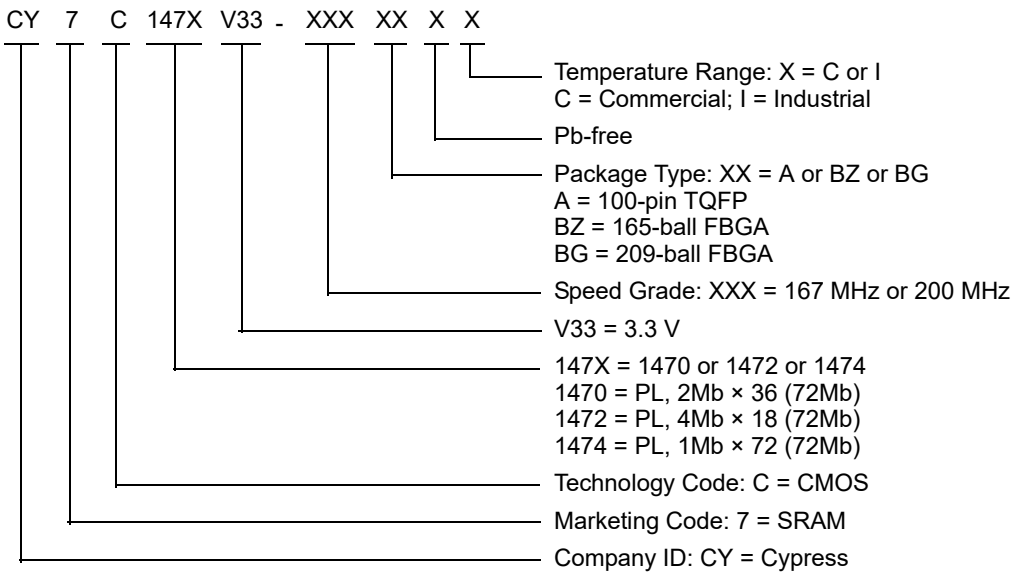
## Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices

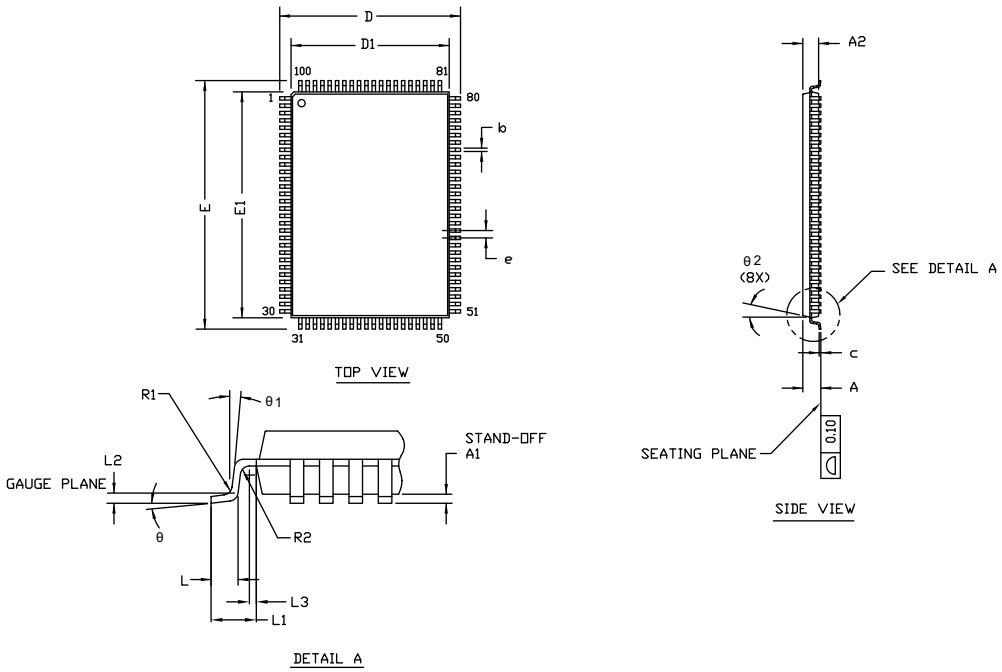
| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|---|---|---|---|---|
| 167 | CY7C1470V33-167AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| | CY7C1470V33-167BZC | 51-85165 | 165-ball FBGA (15 × 17 × 1.4mm) | |
| | CY7C1474V33-167BGC | 51-85167 | 209-ball FBGA (14 × 22 × 1.76 mm) | |
| | CY7C1470V33-167AXI | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Industrial |
| | CY7C1470V33-167BZI | 51-85165 | 165-ball FBGA (15 × 17 × 1.4mm) | |
| 200 | CY7C1472V33-200AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| | CY7C1474V33-200BGC | 51-85167 | 209-ball FBGA (14 × 22 × 1.76 mm) | |
| | CY7C1470V33-200BZI | 51-85165 | 165-ball FBGA (15 × 17 × 1.4mm) | Industrial |

### Ordering Code Definitions



## Package Diagrams

**Figure 8. 100-pin TQFP (16 × 22 × 1.6 mm) Package Outline, 51-85050**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| R1 | 0.08 | — | 0.20 |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | — | 7° |
| θ1 | 0° | — | — |
| θ2 | 11° | 12° | 13° |
| c | — | — | 0.20 |
| b | 0.22 | 0.30 | 0.38 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 BSC | | |
| L3 | 0.20 | — | — |
| e | 0.65 TYP | | |

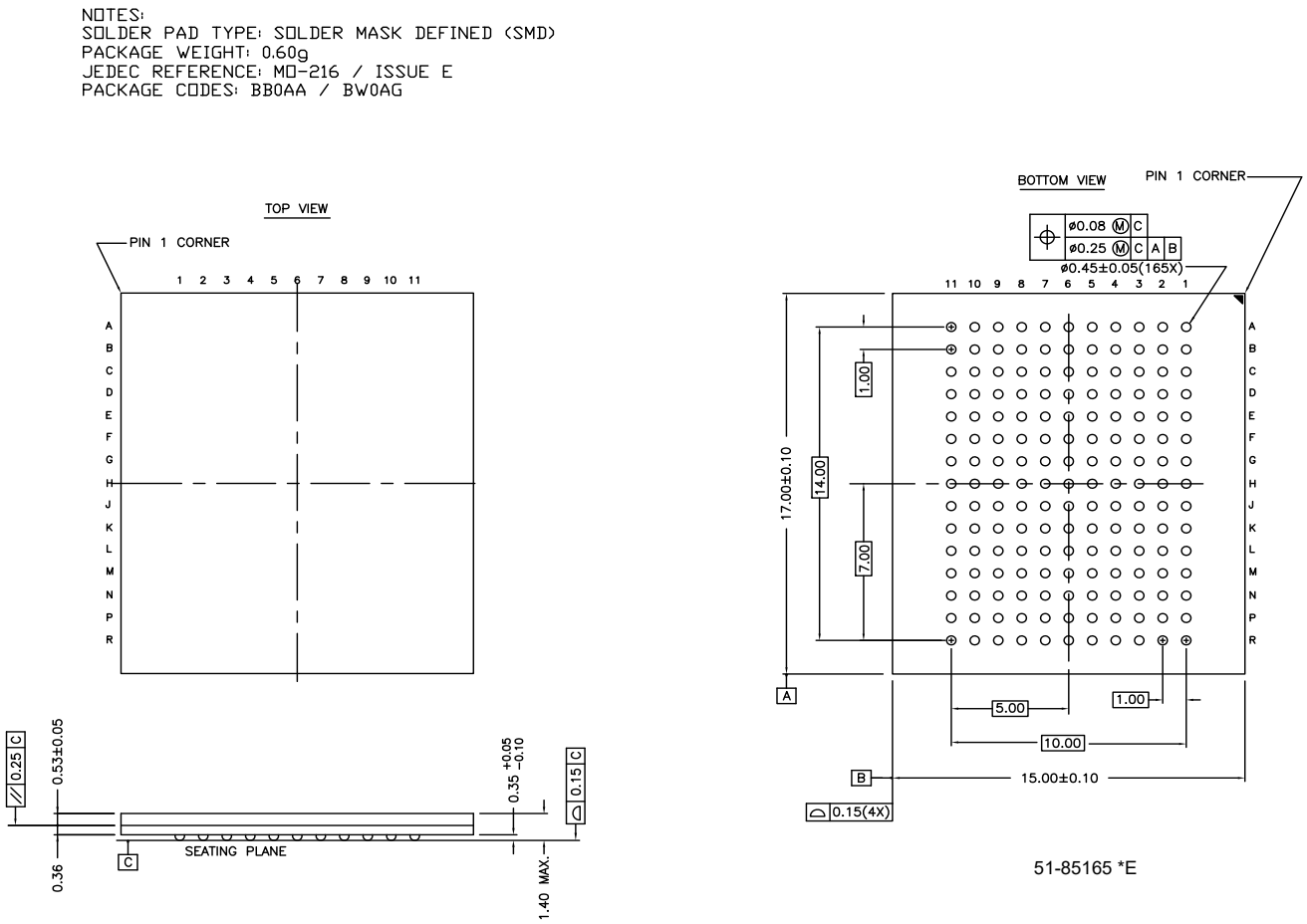
NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *G

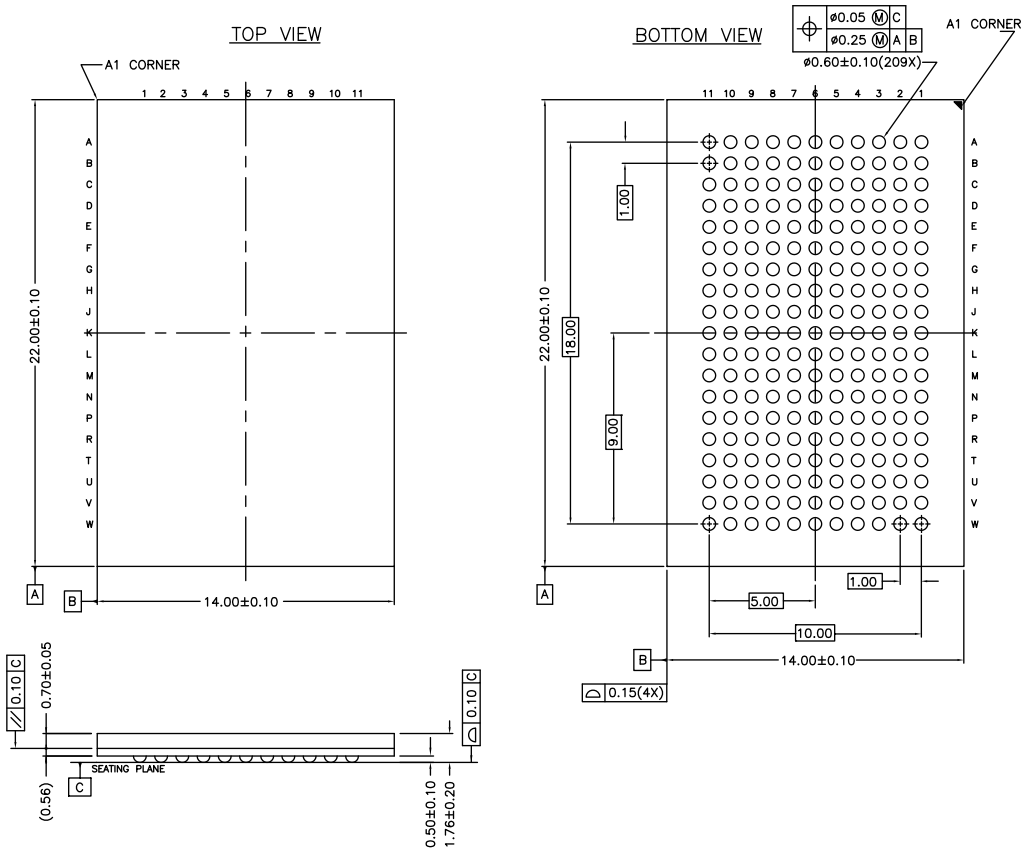
## Package Diagrams *(continued)*

**Figure 9. 165-ball FBGA ((15 × 17 × 1.40 mm) 0.45 Ball Diameter) Package Outline, 51-85165**



## Package Diagrams *(continued)*

**Figure 10. 209-ball FBGA (14 × 22 × 1.76 mm) Package Outline, 51-85167**




51-85167 *C

## Acronyms

| Acronym | Description |
|---|---|
| BGA | Ball Grid Array |
| CMOS | Complementary Metal Oxide Semiconductor |
| $\overline{CE}$ | Chip Enable |
| $\overline{CEN}$ | Clock Enable |
| FBGA | Fine-Pitch Ball Grid Array |
| I/O | Input/Output |
| JTAG | Joint Test Action Group |
| NoBL | No Bus Latency |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TCK | Test Clock |
| TDI | Test Data Input |
| TMS | Test Mode Select |
| TDO | Test Data Output |
| TQFP | Thin Quad Flat Pack |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| ns | nanosecond |
| pF | picofarad |
| V | volt |
| W | watt |

# Errata

This section describes the Ram9 NoBL ZZ pin issues. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

## Part Numbers Affected

| Density & Revision | Package Type | Operating Range |
|---|---|---|
| 72Mb-Ram9 NoBL SRAMs: CY7C147*V33 | 100-pin TQFP | Commercial/ Industrial |
| | 165-ball FBGA | |
| | 209-ball FBGA | Commercial |

## Product Status

All of the devices in the Ram9 72Mb NoBL family are qualified and available in production quantities.

## Ram9 NoBL ZZ Pin Issues Errata Summary

The following table defines the errata applicable to available Ram9 72Mb NoBL family devices.

| Item | Issues | Description | Device | Fix Status |
|---|---|---|---|---|
| 1. | ZZ Pin | When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved.The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation. | 72M-Ram9 (90 nm) | For the 72M Ram9 (90 nm) devices, this issue was fixed in the new revision. Please contact your local sales rep for availability. |

### 1. ZZ Pin Issue

- PROBLEM DEFINITION
  The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

- TRIGGER CONDITIONS
  Device operated with ZZ pin left floating.

- SCOPE OF IMPACT
  When the ZZ pin is left floating, the device delivers incorrect data.

- WORKAROUND
  Tie the ZZ pin externally to ground.

- FIX STATUS
  Fix was done for the 72M RAM9 NoBL SRAMs devices. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

**Table 1. List of Affected Devices and the new revision**

| Revision before the Fix | New Revision after the Fix |
|---|---|
| CY7C147*V33 | CY7C147*BV33 |

## Document History Page

| Document Title: CY7C1470V33/CY7C1472V33/CY7C1474V33, 72-Mbit (2M × 36/4M × 18/1M × 72) Pipelined SRAM with NoBL™ Architecture<br>Document Number: 38-05289 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 114676 | PKS | 08/06/2002 | New data sheet. |
| *A | 121520 | CJM | 01/27/2003 | Changed status from Advanced Information to Preliminary.<br>Updated Features (Updated package offering, removed 300 MHz frequency related information).<br>Updated Selection Guide (Removed 300 MHz frequency related information).<br>Updated Functional Overview (Removed 300 MHz frequency related information).<br>Updated Electrical Characteristics (Removed 300 MHz frequency related information).<br>Updated Switching Characteristics (Removed 300 MHz frequency related information, changed maximum value of $t_{CO}$, $t_{EOV}$, $t_{CHZ}$, $t_{EOHZ}$ parameters from 2.4 ns to 2.6 ns for 250 MHz frequency, changed minimum value of $t_{DOH}$, $t_{CLZ}$ parameters from 0.8 ns to 1.0 ns for 250 MHz frequency, changed minimum value of $t_{DOH}$, $t_{CLZ}$ parameters from 1.0 ns to 1.3 ns for 200 MHz frequency).<br>Updated Ordering Information (Updated part numbers).<br>Updated Package Diagrams:<br>spec 51-85115 – Changed revision from *A to *B.<br>spec 51-85143 – Changed revision from *A to *B. |
| *B | 223721 | NJY | 05/14/2004 | Updated Features (Removed 250 MHz frequency related information and included 225 MHz frequency related information).<br>Updated Functional Description (Updated description).<br>Updated Logic Block Diagram (Splitted Logic Block Diagram into three Logic Block Diagrams).<br>Updated Functional Overview (Updated description).<br>Updated Boundary Scan Exit Order (Replaced TBD with values for all packages).<br>Updated Electrical Characteristics (Removed 250 MHz frequency related information and included 225 MHz frequency related information, replaced TBD with values for maximum values of $I_{DD}$, $I_{SB1}$, $I_{SB2}$, $I_{SB3}$, $I_{SB4}$ parameters).<br>Updated Capacitance (Replaced TBD with values for all packages).<br>Updated Thermal Resistance (Replaced TBD with values for all packages).<br>Updated Switching Characteristics (Removed 250 MHz frequency related information and included 225 MHz frequency related information).<br>Updated Switching Waveforms.<br>Updated Package Diagrams:<br>spec 51-85165 – Changed revision from ** to *A.<br>Added spec 51-85167 **.<br>Removed spec 51-85115 *B.<br>Removed spec 51-85143 *B. |
| *C | 235012 | RYQ | 06/17/2004 | Minor Change (To match on the spec system and external web). |
| *D | 243572 | NJY | 07/20/2004 | Updated Pin Configurations (Updated Figure 2 (Changed ball C11, D11, E11, F11, G11 from $DQP_b$, $DQ_b$, $DQ_b$, $DQ_b$, $DQ_b$ to $DQP_a$, $DQ_a$, $DQ_a$, $DQ_a$, $DQ_a$ (corresponding to CY7C1472V33))).<br>Updated Capacitance (Splitted $C_{IN}$ parameter into $C_{ADDRESS}$, $C_{DATA}$, $C_{CLK}$ parameters and also updated the values). |

## Document History Page *(continued)*

| Document Title: CY7C1470V33/CY7C1472V33/CY7C1474V33, 72-Mbit (2M × 36/4M × 18/1M × 72) Pipelined SRAM with NoBL™ Architecture<br>Document Number: 38-05289 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *E | 299511 | SYT / VBL | 12/14/2004 | Updated Features (Removed 225 MHz frequency related information and included 250 MHz frequency related information).<br>Updated Selection Guide (Removed 225 MHz frequency related information and included 250 MHz frequency related information).<br>Updated Electrical Characteristics (Removed 225 MHz frequency related information and included 250 MHz frequency related information).<br>Updated Thermal Resistance (Changed value of $\Theta_{JA}$ from 16.8 °C/W to 24.63 °C/W, and changed value of $\Theta_{JC}$ from 3.3 °C/W to 2.28 °C/W for 100-pin TQFP Package).<br>Updated Switching Characteristics (Removed 225 MHz frequency related information and included 250 MHz frequency related information, changed minimum value of $t_{CYC}$ from 4.4 ns to 4.0 ns for 250 MHz frequency).<br>Updated Ordering Information (Updated part numbers (Removed 225 MHz frequency related information and included 250 MHz frequency related information, added Pb-free information for 100-pin TQFP Package and 165-ball FBGA Package, added Industrial Temperature Range part numbers), added comment of 'Pb-free BG packages availability' below the Ordering Information). |
| *F | 323039 | PCI | 02/23/2005 | Changed status from Preliminary to Final.<br>Updated Selection Guide (Unshaded 250 MHz frequency related information).<br>Updated Pin Configurations (Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard, updated Figure 3 (Changed package name from 209-ball PBGA to 209-ball FBGA)).<br>Updated Pin Definitions (Added Address Expansion pins).<br>Updated Electrical Characteristics (Updated Test Conditions of $V_{OL}$, $V_{OH}$ parameters, unshaded 250 MHz frequency related information).<br>Updated Switching Characteristics (Unshaded 250 MHz frequency related information).<br>Updated Ordering Information (Updated part numbers, unshaded all shaded areas, removed comment of 'Pb-free BG packages availability' below the Ordering Information). |
| *G | 351937 | PCI | 04/19/2005 | Updated Ordering Information (Updated part numbers). |
| *H | 416221 | RXU | 12/22/2005 | Changed address of Cypress Semiconductor Corporation from "3901 North First Street" to "198 Champion Court".<br>Updated Electrical Characteristics (Updated Note 25 (Changed $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$), changed description of $I_X$ parameter from Input Load Current except ZZ and MODE to Input Leakage Current except ZZ and MODE, changed minimum value of $I_X$ parameter (corresponding to Input Current of MODE (Input = $V_{SS}$)) from –5 µA to –30 µA, changed maximum value of $I_X$ parameter (corresponding to Input Current of MODE (Input = $V_{DD}$)) from 30 µA to 5 µA, changed minimum value of $I_X$ parameter (corresponding to Input Current of ZZ (Input = $V_{SS}$)) from –30 µA to –5 µA, changed maximum value of $I_X$ parameter (corresponding to Input Current of ZZ (Input = $V_{DD}$)) from 5 µA to 30 µA).<br>Updated Ordering Information (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table).<br>Replaced Three-state with Tri-state in all instances across the document.<br>Updated to new template. |

## Document History Page *(continued)*

| Document Title: CY7C1470V33/CY7C1472V33/CY7C1474V33, 72-Mbit (2M × 36/4M × 18/1M × 72) Pipelined SRAM with NoBL™ Architecture<br>Document Number: 38-05289 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *I | 472335 | VKN | 06/27/2006 | Updated Pin Configurations (Updated Figure 3 (Corrected the ball name for H9 from $V_{SSQ}$ to $V_{SS}$).<br>Updated TAP AC Switching Characteristics (Changed minimum value of $t_{TH}$, $t_{TL}$ parameters from 25 ns to 20 ns, changed maximum value of $t_{TDOV}$ parameter from 5 ns to 10 ns).<br>Updated Maximum Ratings (Added Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND).<br>Updated Ordering Information (Updated part numbers).<br>Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *A to *B. |
| *J | 2756998 | VKN | 08/28/2009 | Added Neutron Soft Error Immunity.<br>Updated Ordering Information (Updated part numbers (Including parts that are available), and modified the disclaimer for the Ordering information).<br>Updated Package Diagrams:<br>spec 51-85165 – Changed revision from *A to *B.<br>Updated to new template. |
| *K | 2903057 | NJY | 04/01/2010 | Updated Ordering Information (Updated part numbers).<br>Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *B to *C.<br>spec 51-85167 – Changed revision from ** to *A. |
| *L | 3033272 | NJY | 09/19/2010 | Updated Ordering Information:<br>No change in part numbers.<br>Added Ordering Code Definitions.<br>Added Acronyms and Units of Measure.<br>Minor edits.<br>Updated to new template.<br>Completing Sunset Review. |
| *M | 3052882 | NJY | 10/08/2010 | Updated Ordering Information (Updated part numbers). |
| *N | 3357114 | PRIT | 08/29/2011 | Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *C to *D.<br>spec 51-85165 – Changed revision from *B to *C.<br>spec 51-85167 – Changed revision from *A to *B.<br>Completing Sunset Review. |
| *O | 3403584 | PRIT | 10/12/2011 | Updated Ordering Information (Updated part numbers).<br>Updated Package Diagrams:<br>spec 51-85165 – Changed revision from *C to *D. |
| *P | 3638614 | PRIT | 06/06/2012 | Updated Features (Removed 250 MHz frequency related information, removed 165-ball FBGA package related information (corresponding to CY7C1472V33)).<br>Updated Selection Guide (Removed 250 MHz frequency related information).<br>Updated Pin Configurations (Updated Figure 2 (Removed CY7C1472V33 related information)).<br>Updated Functional Overview (Removed 250 MHz frequency related information).<br>Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1472V33 related information).<br>Updated Identification Register Definitions (Removed CY7C1472V33 related information).<br>Updated Scan Register Sizes (Removed “Bit Size (× 18)” column).<br>Removed Boundary Scan Exit Order (Corresponding to CY7C1472V33). |

## Document History Page *(continued)*

| Document Title: CY7C1470V33/CY7C1472V33/CY7C1474V33, 72-Mbit (2M × 36/4M × 18/1M × 72) Pipelined SRAM with NoBL™ Architecture<br>Document Number: 38-05289 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *P (cont.) | 3638614 | PRIT | 06/06/2012 | Updated Electrical Characteristics (Removed 250 MHz frequency related information).<br>Updated Switching Characteristics (Removed 250 MHz frequency related information).<br>Updated Ordering Information (Updated part numbers). |
| *Q | 3755966 | PRIT | 09/26/2012 | Updated Package Diagrams:<br>spec 51-85167 – Changed revision from *B to *C.<br>Completing Sunset Review. |
| *R | 3971410 | PRIT | 04/18/2013 | Updated Ordering Information (Updated part numbers).<br>Added Errata. |
| *S | 4042037 | PRIT | 06/27/2013 | Added Errata Footnotes.<br>Updated to new template. |
| *T | 4146627 | PRIT | 10/04/2013 | Updated Errata:<br>Removed CY7C147* related information in all instances across the document. |
| *U | 4539205 | PRIT | 10/15/2014 | Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *D to *E.<br>Completing Sunset Review. |
| *V | 4571917 | PRIT | 12/29/2014 | Updated Functional Description:<br>Added “For a complete list of related documentation, click here.” at the end.<br>Updated Package Diagrams:<br>spec 51-85165 – Changed revision from *D to *E. |
| *W | 5513955 | PRIT | 11/08/2016 | Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review. |
| *X | 6015296 | RMES | 01/05/2018 | Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *F to *G.<br>Updated to new template.<br>Completing Sunset Review. |
| *Y | 6524879 | RMES | 03/28/2019 | Updated Ordering Information:<br>Updated part numbers.<br>Updated to new template. |

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