THE DATASHEET OF

UC27131D

UNITRODE

UC17131/2/3
UC27131/2/3
UC37131/2/3

Smart Power Switch

FEATURES

- 300mA Continuous Output Current
- Low Side or High Side Switch Configuration
- 8V to 65V Operation
- Overload and Short Circuit Protection
- Power Interruption Protection
- +6V Regulated Voltage
- 2mA Quiescent Current
- Programmable Overcurrent and Power Interruption Protection
- 1% to 30% Programmable Input Comparator Hysteresis (on UC37132)
- Low and High Side Internal High Current Clamps When Driving Inductive Loads

DESCRIPTION

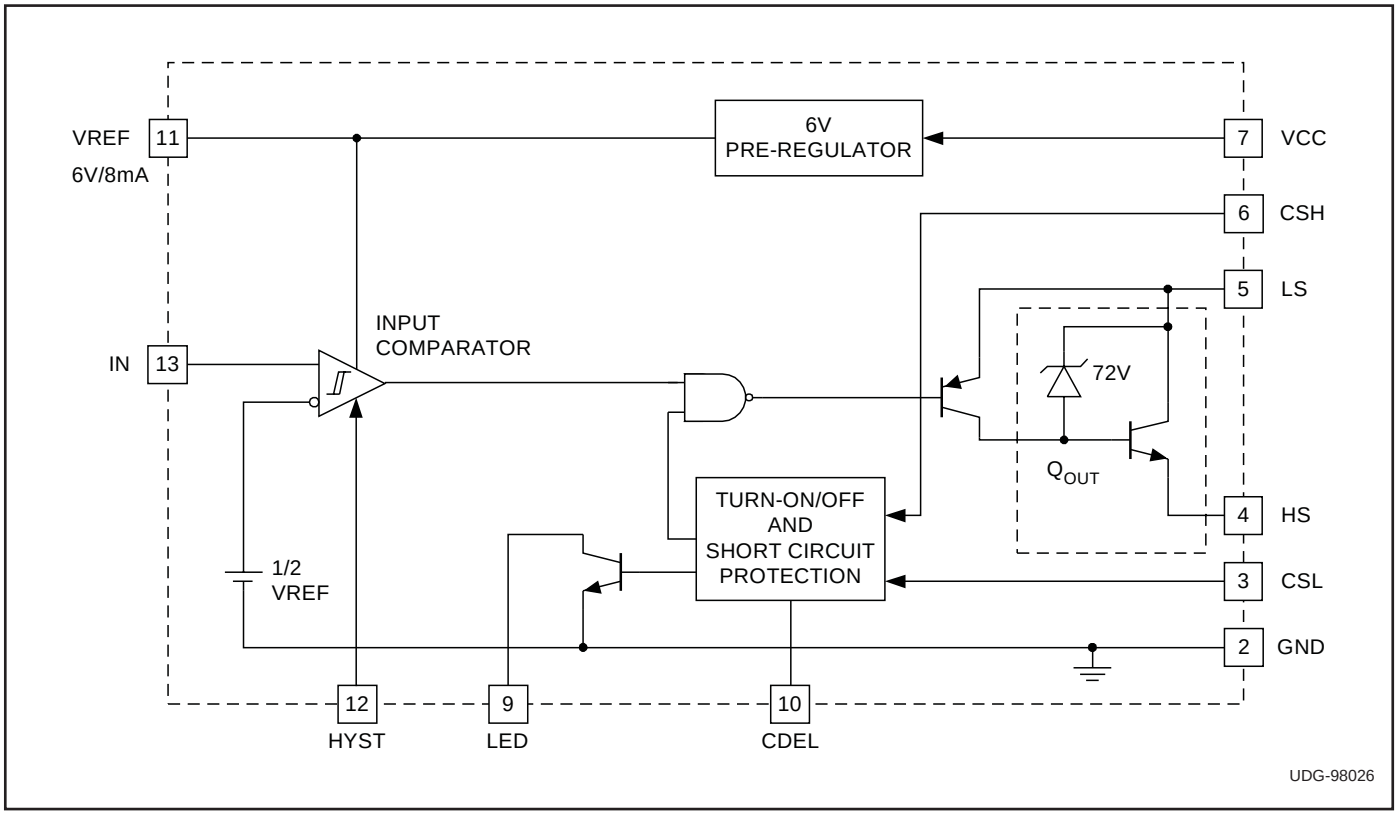
The UC37131, UC37132 and UC37133 are a family of smart power switches which can drive resistive or inductive loads from the high side or low side.

The UC37132 is available in 14 pin (DIP), 16 pin (SOIC), or 20 pin (CLCC) packages and can accommodate both low side (load to VCC) or high side (load to GND) configurations. The UC37131 and UC37133 are exclusively for a low side or a high side configuration respectively and both are available in an 8 pin package. Both high side and low side configurations provide high current switching with low saturation voltages which can drive resistive or inductive loads.

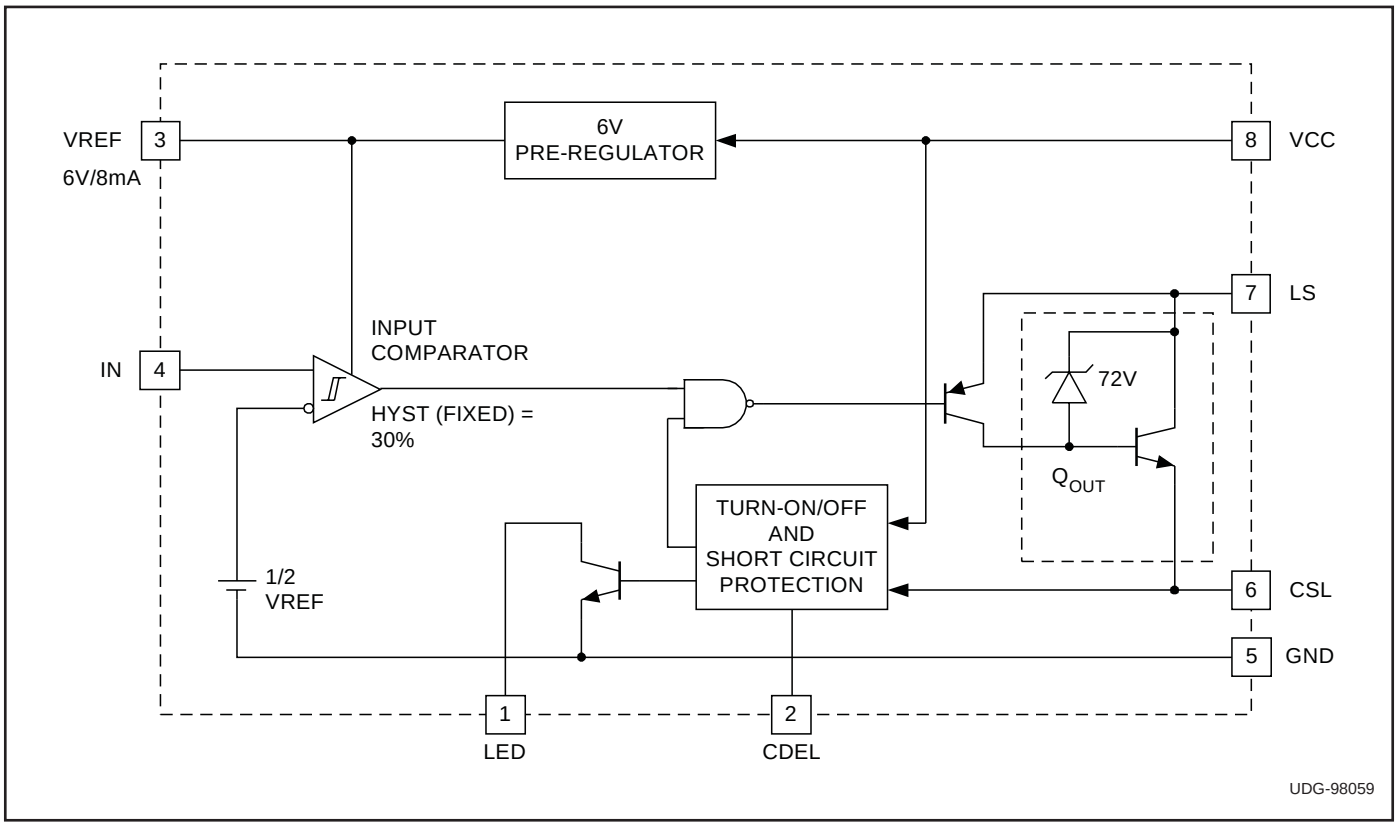
The input to the switch is driven by a low voltage signal, typically 5V. Additionally, UC37132 features adjustable hysteresis. The output of the device can switch a load between 8V and 65V. Output current capability is 300mA continuous or 700mA peak.

The device also has inherent smart features that allow for programmable turn-on delay in enabling the output following startup. The same capacitor that specifies the turn-on delay is also used to program a VCC power interruption time. If VCC drops below a threshold for a time specified by this capacitor, the output is turned off and a new turn-on delay will be re-triggered. Similarly, if high current persists longer than the response delay, the output driver will operate in a very low duty cycle mode to protect the IC.

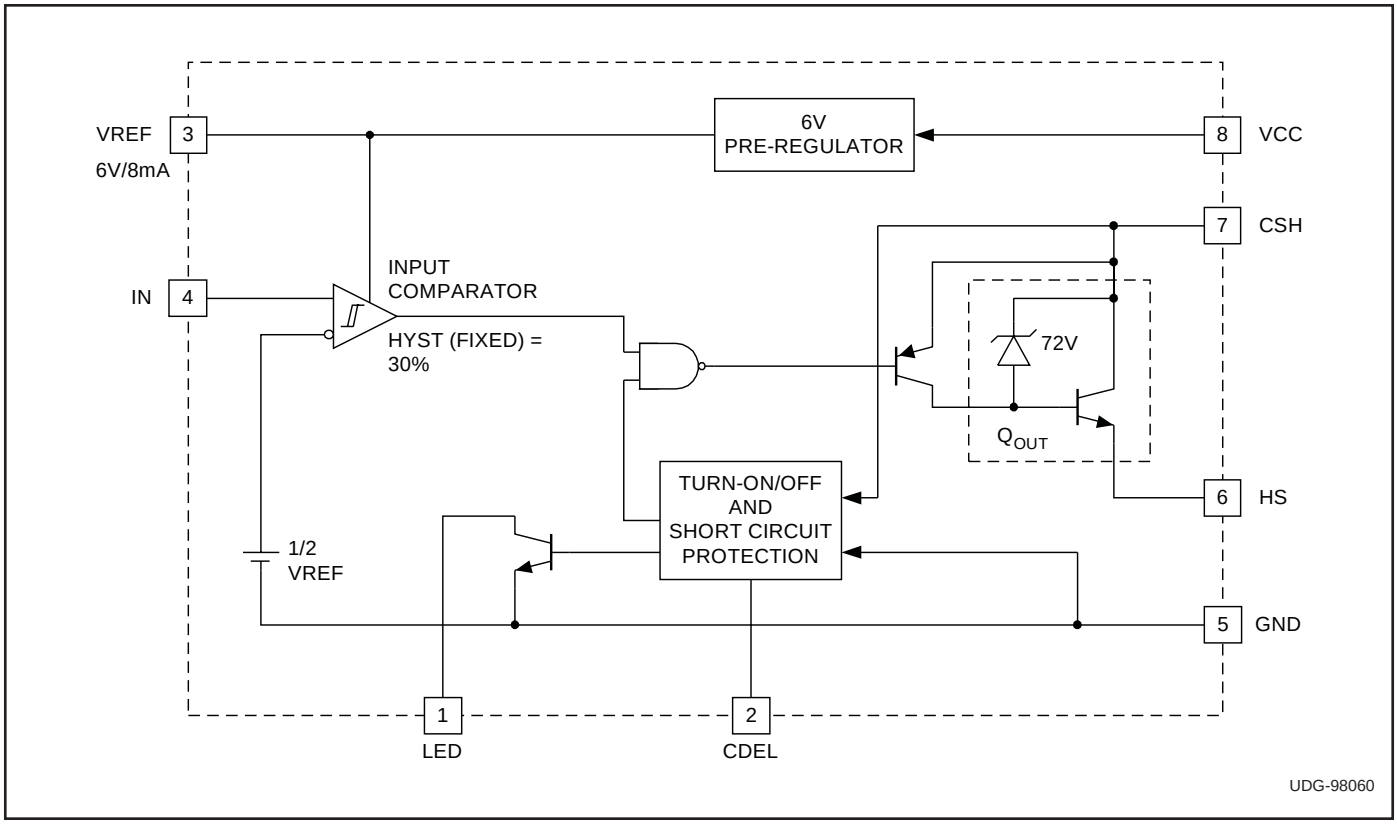
UC37132 BLOCK DIAGRAM



UC37131 BLOCK DIAGRAM



UC37133 BLOCK DIAGRAM

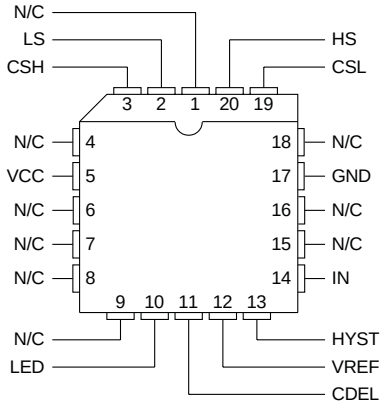


ABSOLUTE MAXIMUM RATINGS

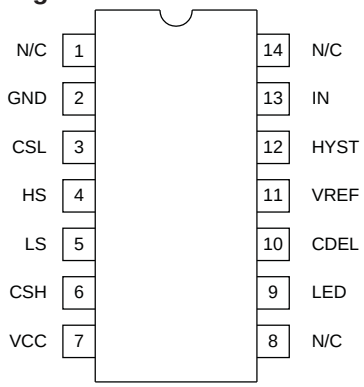
VCC 65V
LS – HS (Clamped by internal circuitry) 78V
CSH, LED 65V
Output Current
  Continuous 400mA
  Peak 900mA
Remaining Pin Voltages . . . . . –0.3V to 9V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

PLCC-20 (Top View)
(for UCX7132)
L Packages

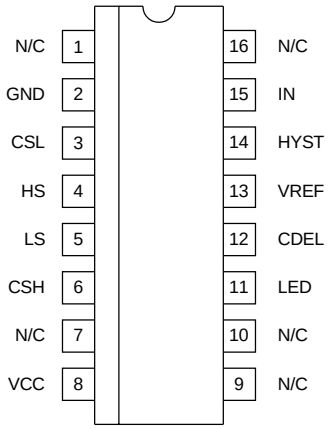


DIL-14 (Top View)
(for UCX7132)
J, or N Packages

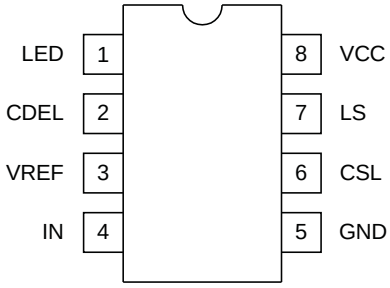


CONNECTION DIAGRAMS

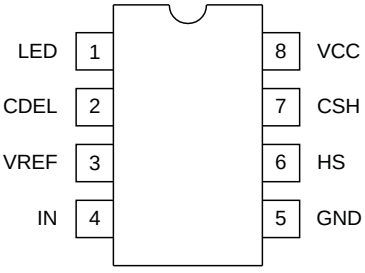
SOIC-16 (Top View)
(for UCX7132)
D Package



DIL-8, SOIC-8 (Top View)
(for UCX7131)
J, N, or D Packages



DIL-8, SOIC-8 (Top View)
(for UCX7133)
J, N, or D Packages



PRODUCT SELECTION TABLES

PART NUMBER	CONFIGURATIONS	PACKAGE PIN COUNT
UCX7131	Low Side Only	8
UCX7132	Low Side or High Side	14, 16, 20
UCX7133	High Side Only	8

PART NUMBER	TEMPERATURE RANGE	AVAILABLE PACKAGES
UC1713X	–55°C to +125°C	J, L
UC2713X	–40°C to +85°C	D, N
UC3713X	0°C to +70°C	D, N

ELECTRICAL CHARACTERISTICS Unless otherwise specified, CDEL = 10nF, VCC = 25V, CSL = GND, CSH = LS; R_{CSH} = 0.5Ω (Note 1); IN=0V (for OFF condition) and IN=5V (for ON condition); $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
VREF	25°C	5.8	6	6.2	V
	–55°C to 125°C	5.6	6	6.4	V
Line Regulation	VCC = 8V to 64V		10	35	mV
Load Regulation	0 < I_{REF} < 8mA		10	50	mV
Short Circuit Current	REF = 0V		20	35	mA
Input Comparator					
Turn-On Threshold Voltage		2.7	3	3.3	V
Input Bias Current	V_{IN} = 3.5V			5	µA
Hysteresis	R_{HYST} = GND (Internally for X31, X33)	0.775	0.9	1.025	V
	R_{HYST} = 96.67k for (X32)		30		mV
Output: High Side (UCX7133: CSH = LS and CSL = GND Internally; See Fig. 2a)					
Rise Time (Off to On)	R_{LOAD} = 250Ω to GND		30	80	V/µs
Fall Time (On to Off)	R_{LOAD} = 250Ω to GND		30	80	V/µs
Output Short Circuit	HS = 0.25Ω to GND	500		900	mA
Voltage Clamp	LS–HS	67	72	77	V
Saturation Voltage	25°C, R_{LOAD} = 100Ω to GND			1.2	V
	–40°C, R_{LOAD} = 100Ω to GND			1.3	V
	–55°C, R_{LOAD} = 100Ω to GND			1.4	V
Leakage Current				5	µA
Output: Low Side (UCX7131; CSH = VCC and CSL = HS Internally; See Fig. 2b)					
Rise Time (On to Off)	R_{LOAD} = 250Ω to VCC, R_{CSL} = 0.5Ω		15	50	V/µs
Fall Time (Off to On)	R_{LOAD} = 250Ω to VCC, R_{CSL} = 0.5Ω		25	60	V/µs
Output Short Circuit	LS = 0.25Ω to VCC	500	700	900	mA
Voltage Clamp	LS–HS	67	72	77	V
Saturation Voltage	25°C, R_{LOAD} = 100Ω to VCC, R_{CSL} = 0.5Ω			1.2	V
	–40°C, R_{LOAD} = 100Ω to VCC, R_{CSL} = 0.5Ω			1.3	V
	–55°C, R_{LOAD} = 100Ω to VCC, R_{CSL} = 0.5Ω			1.4	V
Leakage Current				5	µA
VCC Fault Section					
Output Turn-On Delay, $t_{D(ON)}$	Step VCC from 0V to 8V (See Fig. 3a)	9.5	11	13.5	ms
Output Turn-Off Delay, $t_{D(OFF)}$	Pulse VCC from 25V to VCC Turn-Off Threshold	300	500	700	µs
VCC Turn-Off Threshold	Pulse VCC Low	6.5	7	7.5	V
CDEL Section					
V_{CDEL_MAX}			5.8		V
V_{FAULT_H}			4.9		V
V_{FAULT_L}			1.0		V
Overcurrent Fault Section (See Fig. 3c)					
Short Circuit Turn-Off Delay, t_{SC}	Step $I_{LOAD:}$ 0mA to 400mA		75		µs
Short Circuit Recovery Time, t_{ROFF}	I_{LOAD} = 400mA, 100µs		10		ms
High Side Current Threshold, I_{TH-H}	R_{CSH} = 0.5Ω	250	325	400	mA
Low Side Current Threshold, I_{TH-L}	R_{CSL} = 0.5Ω	250	325	400	mA
Overcurrent Duty Cycle	R_{LOAD} = 0.25Ω to GND	0.6	0.8	1.0	%

ELECTRICAL CHARACTERISTICS Unless otherwise specified, CDEL = 10nF, VCC = 25V, CSL = GND, CSH = LS; R_{CSH} = 0.5Ω (Note 1); IN=0V (for OFF condition) and IN=5V (for ON condition); $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LED Output					
I_{SINK}, t_{DOFF}, t_{ROFF}	V_{LED} = 7V	5.0	8.0	11.0	mA
$I_{LEAKAGE}$			1	5	µA
Overall					
Delay to Output			3	6	µs
ICC	Output Off		2.0	2.8	mA
	I_L = 1mA, 250mA (High Side)		2.3	3	mA
	I_L = 1mA, 250mA (Low Side)		2.5	4	mA

Note 1: All test conditions are for a high side configuration as in Fig. 2a, unless otherwise specified.

PIN DESCRIPTIONS

CDEL: A capacitor connected to this pin is used to program both VCC pulse interruption time and power turn-on delay. The capacitor discharge time corresponds to VCC interruption and the charge time to VCC turn-on delay. The ratio between turn-on delay and turn-off delay will be fixed based on internal charge and discharge currents and voltage thresholds.

The same fault circuitry and capacitor is used for short circuit and overload protection. If an overcurrent or short circuit is detected, the capacitor starts charging and turns off the output if the condition persists at the end of its charge time. The output will then operate in a low-duty cycle mode to protect the IC. After short circuit recovery, the output will be reactivated in order to check if the short circuit was removed. If the overcurrent persists the chip will continue in this pulsing mode.

CSH: (For UC37132 and UC37133) This high side current sense pin is used to program the current limit for high side applications by connecting a resistor between VCC and CSH. An over load current is detected when the voltage drop between VCC and CSH exceeds 150mV. For the UC37132, in a high side application, the CSH pin must be tied to the LS pin; in a low side application, the CSH pin must be tied to VCC

CSL: (For UC37131 and UC37132) This low side current sense pin is used to program the current limit for low side applications by connecting a resistor between CSL and GND. An over load current is detected when the voltage drop between CSL and GND exceeds 150mV. For the UC37132, in a high side application, the CSL pin must be tied to GND; in a low side application, the CSL pin must be tied to the HS pin.

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device.

HS: (For UC37132 and UC37133) The output of the switching transistor in the high side configuration. The emitter of the output transistor is the HS pin which is connected to the load. For the UC37132, the HS pin must be tied to the CSL pin in a low side application.

HYST: (For UC37132) The pin used to program the input comparator hysteresis by connecting a resistor to ground. The hysteresis defaults to 30% with HYST grounded (internally for UC37131 and UC37133).

$$V_{HYST} = \frac{3000}{(3330 + R_{HYST})}$$

IN: The input to the comparator that detects when the output transistor should be turned on. The input threshold is 3.0V (1/2 VREF) and the input voltage range is 0V to VREF.

LED: Open collector output intended to drive an LED. This pin is driven low whenever the output is turned off and is externally pulled high when the output is turned on (see Fig. 3b and 3c).

LS: (For UC37131 and UC37132) The output of the switching transistor in the low side configuration. The collector of the output transistor is the LS pin which is connected to the load. For the UC37132, the LS pin must be tied to the CSH pin in a high side application.

VREF: The 6V regulated reference capable of supplying up to 8mA. The recommended decoupling capacitor is 1nF.

VCC: The supply voltage for the chip. Decouple this pin with a good quality ceramic capacitor to ground.

DESCRIPTION OF OPERATION

Reference

The UC37131/2/3 family of devices features a 6V bandgap reference that is used to bias on-chip logic. Although the 6V reference is not trimmed, this bandgap reference provides less than 200ppm/°C. It is also used to generate the on-chip 3V input comparator threshold and is needed for the programmable hysteresis. The on-chip reference has 8mA maximum current sourcing capacity that is designed to power up external circuitry.

Input Comparator

The input comparator is a high gain comparator with hysteresis that fully switches with either a small signal (30mV, minimum for 1% hysteresis) or a logic signal (0 to 6V max). Only a 5mV overdrive of the 3V threshold is needed to switch the driver.

The hysteresis is set to 30% on the UC37131 and UC37133. (This is 30% of 3V equating to 0.9V of hysteresis.) On the UC37132 it is programmable from 1% to 30%.

Fault Logic

The output of the comparator is logic ANDed with the output of the fault logic. If a fault, either a power interrupt or an overcurrent condition, persists longer than it takes for the CDEL to discharge from its V_{CDEL_MAX} level of 5.8V to its V_{FAULT_L} of 1.3V, the fault protection block will output a logic 0 to the NAND gate and turn off the output driver. If the fault goes away prior to CDEL being discharged to 1.3V, the chip will resume normal operation without going through a turn-on delay.

The power interrupt normal operation consists of the chip turning the driver immediately back on if the interrupt goes away prior to CDEL reaching its lower threshold as described above. The CDEL capacitor is chosen based upon the maximum power interrupt time (t_{INT}) allowed without the output experiencing a turn-on delay. This interrupt time must be less than $t_{D(OFF)}$ where $t_{D(OFF)}$ is equal to the time it takes the CDEL capacitor to discharge from V_{CDEL_MAX} (5.8V) to V_{FAULT_L} (1.3V) with a discharge current of approximately 94µA. If the power stays off only as long as $t_{D(OFF)}$, the minimum power up delay will be equal to the time it takes to charge CDEL from V_{FAULT_L} (1.3V) to V_{FAULT_H} (4.9V) with a charge current of approximately 4µA. If the power stays off longer than this time, then a power up delay will be initialized once power is resumed. This delay is the time it takes for CDEL to charge from 0V to V_{FAULT_H} of 4.9V.

The overcurrent fault normal operation consists of the chip staying off until CDEL fully recharges to V_{FAULT_H} of 4.9V. This is $t_{R(OFF)}$. Once CDEL reaches 4.9V, the driver will turn back on. If the overcurrent fault is still present, the chip will operate in a very low duty cycle (approximately 0.7%) based on the discharge (driver on) and charge time (driver off) of the CDEL capacitor. This overcurrent timing makes the chip act "smart" by allowing very high currents needed to drive large capacitive loads without setting off an overcurrent fault.

The overcurrent and current limit thresholds are programmed with the resistor R_{CSH} from CSH to VCC (high side) or R_{CSL} from CSL to GND (low side). For example, a 150mV ($I_{LOAD} \bullet R_{CSH}$) threshold will set the high side overcurrent fault threshold. An overall short circuit protection threshold is set at 300mV. Therefore, the recommended R_{CSH} of 0.5Ω will result in the 600mA short circuit. By changing the R_{CSH} value the user can optimally set the overcurrent and short circuit current limits.

Output Driver

Once the turn-on signal is gated through from the input comparator, the output transistor is turned on. The output drive transistor is a composite PNP, NPN structure. This is a specially designed structure that keeps all the drive current needed for the load to be sourced through the LS pin. This keeps the overall power dissipation to less than 4mA independent of the load.

The output driver also has a 72V zener diode wired between its base and collector. This allows the output to swing and clamp to 72V above ground when discharging an inductive load in a low side application. The inductive zener clamp can discharge the 250mA to 400mA full load current. This consequently allows the LS pin to safely swing above VCC. Similarly, the 72V zener diode will allow the HS pin to safely swing and clamp 72V below LS/VCC when discharging an inductive load in a high side application. This 72V zener diode simplifies the user application by eliminating the need for external clamp diodes.

APPLICATION INFORMATION

Choosing The CDEL Capacitor

The maximum amount of time that VCC power can be interrupted and not require the outputs to go through a turn-on delay cycle is user programmable by the CDEL capacitor value. While VCC is interrupted, the outputs will be in an indeterminate state and they may turn off during this interval, t_{INT}. However, as long as the programmed interruption time is not exceeded, the outputs will immediately turn back on with the return of VCC.

For example:

$$t_{INT} \approx 500\mu s \text{ (User specified)}$$

CDEL is selected such that the time it takes for this capacitor to discharge from V_{CDEL_MAX} (5.8V) to V_{FAULT_L} (1.3V) with a discharge current of 94µA is just greater than this t_{INT}. This time is referred to as $t_{D(OFF)}$ in Fig. 3b.

$$CDEL = \frac{I_{DISCHARGE} \bullet t_{D(OFF)}}{V_{CDEL\_MAX} - V_{FAULT\_L}}$$

If $t_{D(OFF)}$ is set equal to t_{INT}, which the user has selected to be 500µs, the minimum CDEL capacitor is calculated:

$$CDEL = \frac{94\mu A \bullet 500\mu s}{5.8V - 1.3V}$$

For this application, the CDEL capacitor value calculates to 10.4nF. By using a 10nF capacitor on CDEL, VCC can be interrupted for up to 478µs and the outputs will experience an indeterminate state during this interruption, but resume normal operation when VCC power returns to normal.

If the VCC power is interrupted for a time equal to or longer than $t_{D(OFF)}$ then the following relationships apply. As the CDEL capacitor discharges past the V_{FAULT_L} threshold, the output is fully disabled and must cycle through a power up delay equal to $t_{D(ON)}$. The charge current for the CDEL capacitor is equal to 4µA. The outputs will turn on when the CDEL capacitor charges up to the V_{FAULT_H} threshold of 4.9V. The minimum turn-on delay the outputs will experience will occur if t_{INT} is exactly equal to the $t_{D(OFF)}$ time and the CDEL capacitor has only discharged to V_{FAULT_L}. This would be the minimum turn-on delay time and is calculated with the following equation:

$$t_{D(ON)_{min}} = \frac{CDEL \bullet \left| V_{FAULT\_L} - V_{FAULT\_H} \right|}{I_{CHARGE}}$$

Using the 10nF CDEL capacitor, for example, the minimum turn-on delay calculates to 9ms. If the CDEL capacitor discharges completely to zero, then the 10nF CDEL capacitor would cause a turn-on delay of 12.25ms. The outputs would be off for this amount of time after VCC power is restored. The total amount of time the outputs could be disabled is equal to the t_{INT} time, which may include the indeterminate time of $t_{D(OFF)}$, and the $t_{D(ON)}$ time, as shown in Fig. 3b.

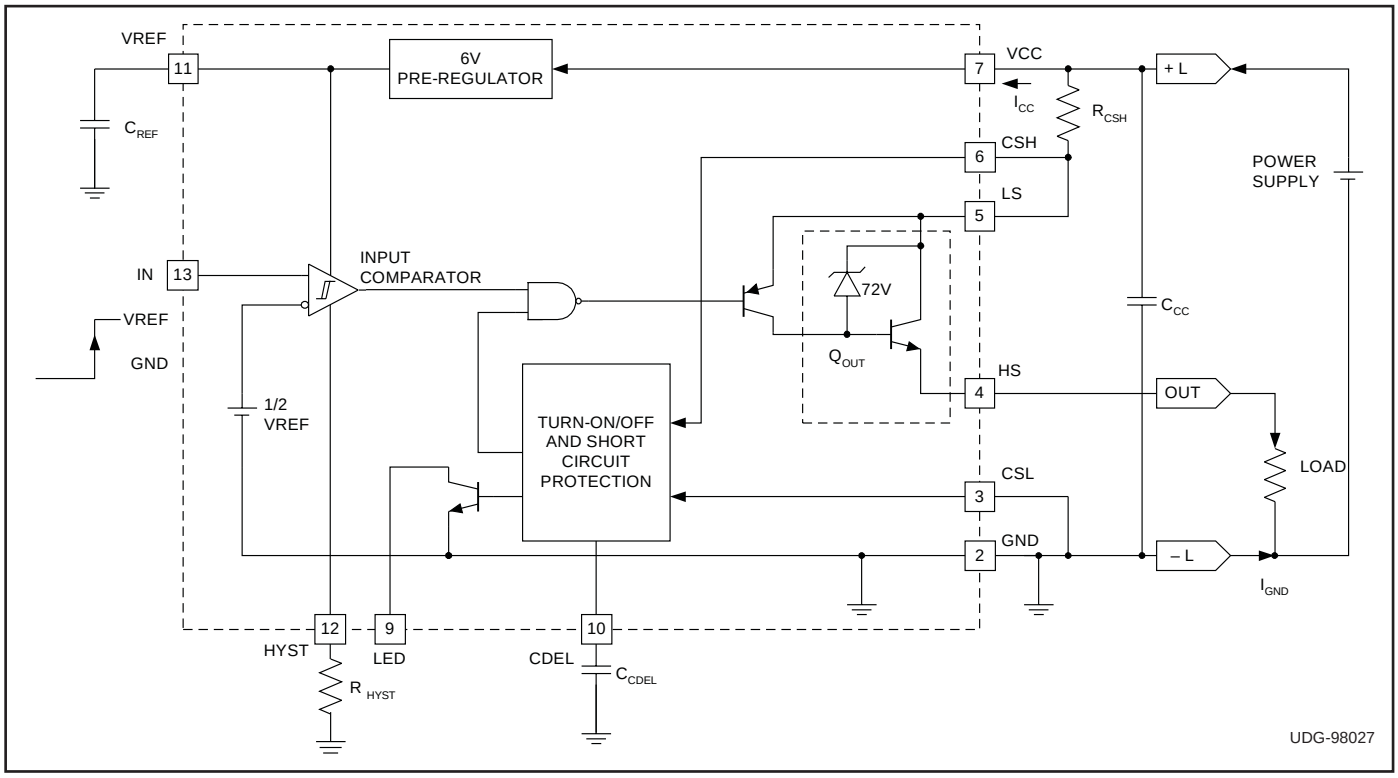


Figure 2a. High side application.

APPLICATION INFORMATION (cont.)

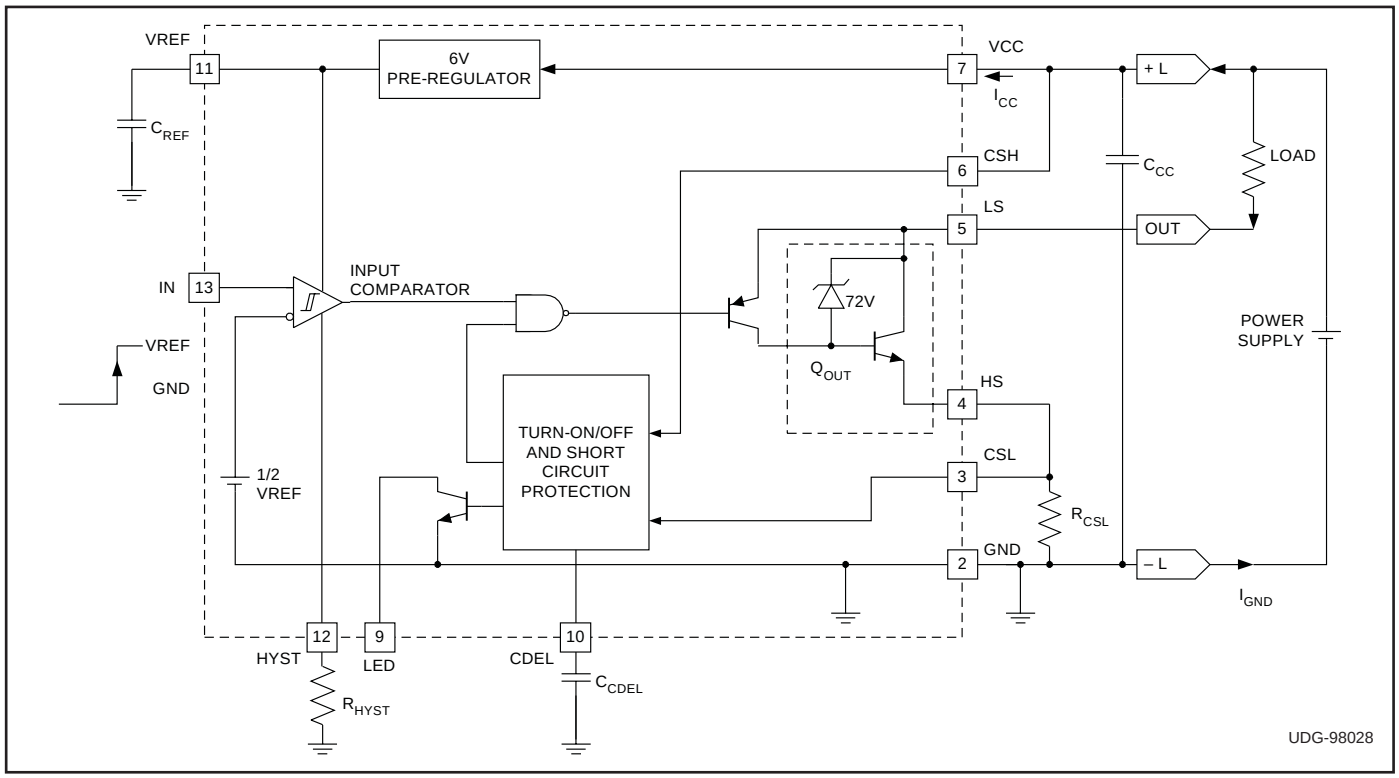


Figure 2b. Low side application.

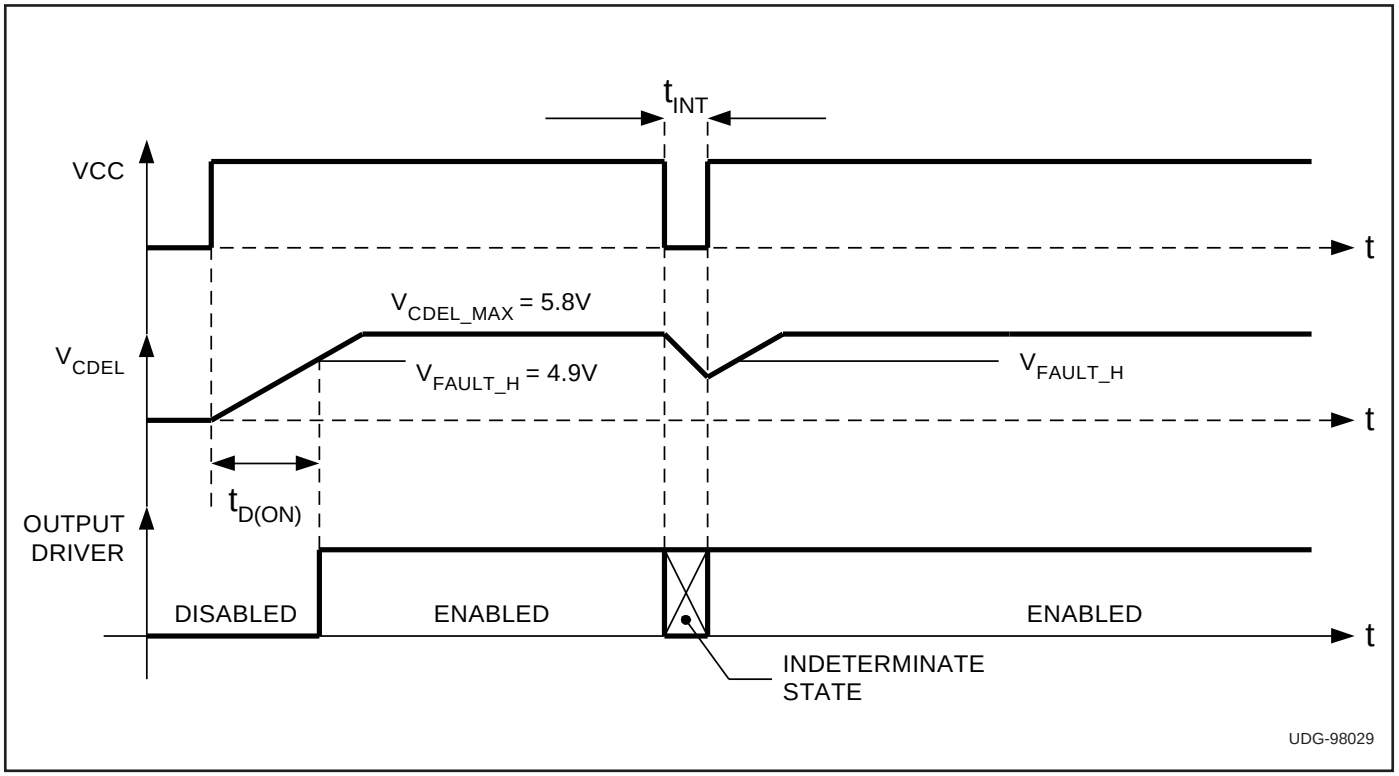


Figure 3a. Power interrupt ignore operation, high side configuration, V_{IN} = 5VDC.

APPLICATION INFORMATION (cont.)

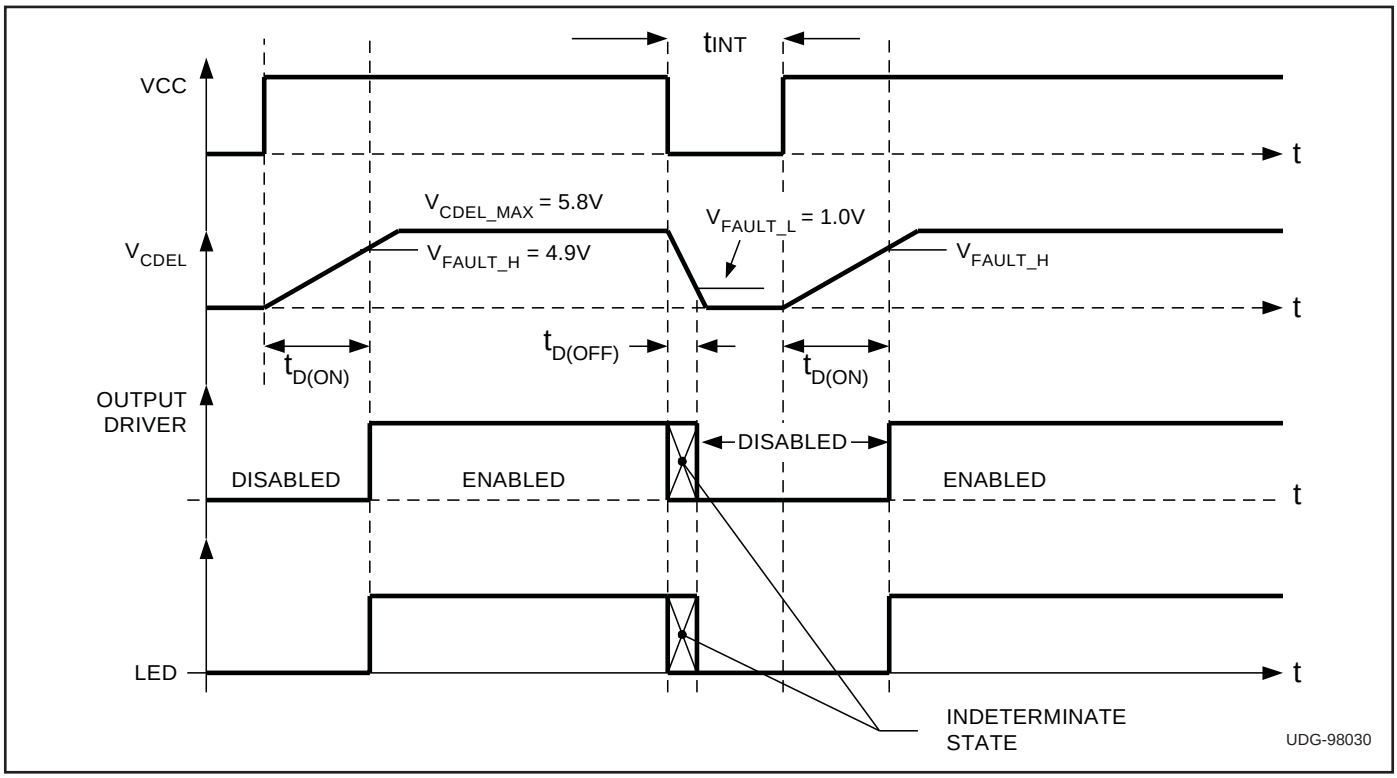


Figure 3b. Power interrupt fault operation, high side configuration, V_{IN} = 5VDC.

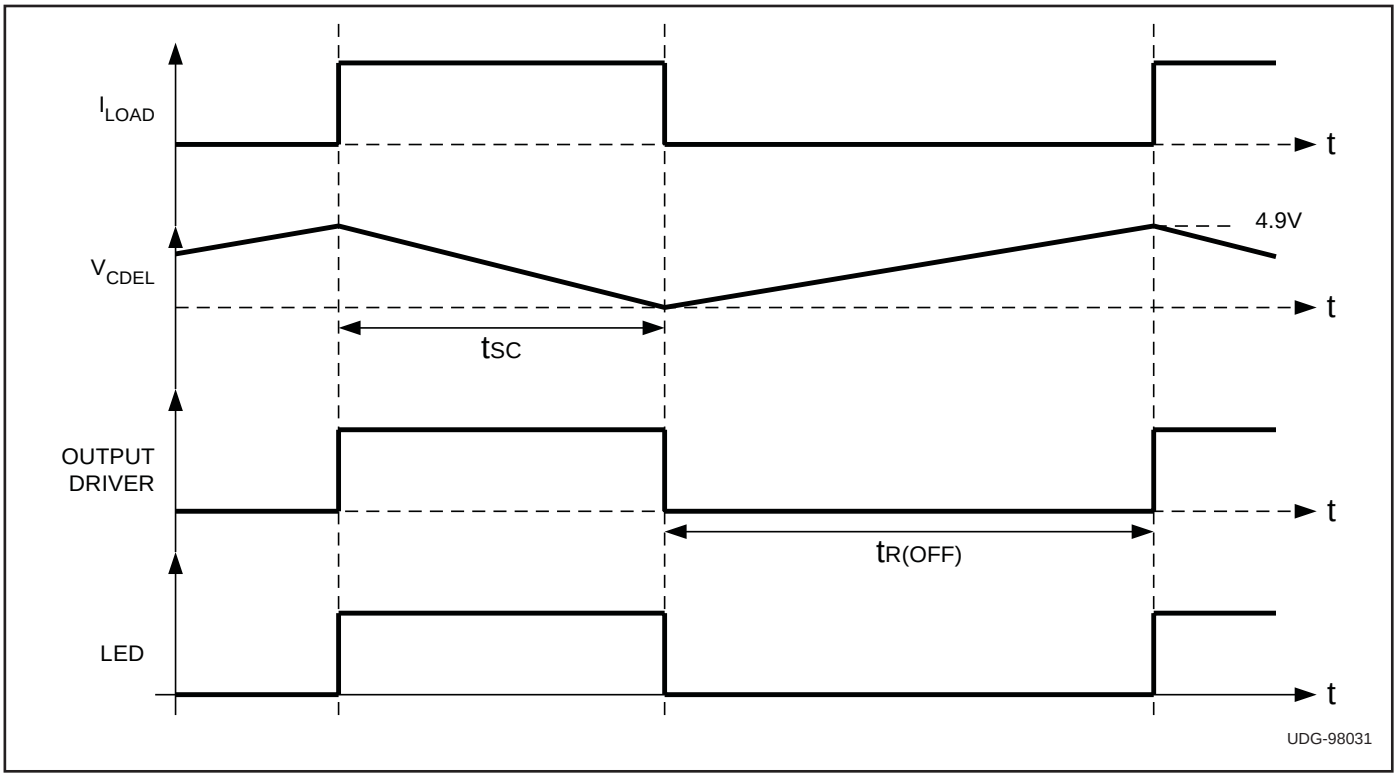


Figure 3c. Overcurrent fault operation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC27131D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC27131	Samples
UC27131DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC27131	Samples
UC27133D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC27133	Samples
UC27133DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC27133	Samples
UC37133D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC37133	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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