



**THE DATASHEET OF  
SKY13296-340LF**



**DATA SHEET**

# SKY13296-340LF: GaAs SP4T Absorptive Switch

## 20 MHz–2.5 GHz

### Features

- Positive voltage control (0/3 V to 0/5 V)
- High isolation 35 dB at 1 GHz
- Integrated silicon CMOS driver
- Isolated ports are absorptive
- Use of external DC blocks to allow good return loss to low frequency
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

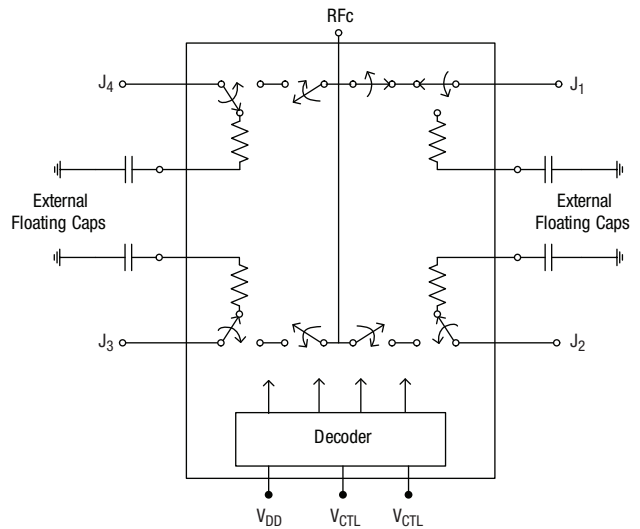
### Description

The SKY13296-340LF is a pHEMT GaAs FET IC high isolation, absorptive single-pole four-throw switch packaged in a lead (Pb)-free, 4 x 4 mm, 20-lead exposed-pad plastic package for low-cost commercial applications. The use of external DC blocking capacitors on the RF ports and in series with the internal RF terminations enables the user to extend the range of good return loss to arbitrarily low frequency. This switch is an ideal building block for filter bank switching.

**NEW** Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.



### Functional Diagram



### Electrical Specifications

**$V_{CTL} = 0\text{ V}/3\text{ V}$ ,  $T = 25\text{ °C}$ ,  $P_{INPUT} = 0\text{ dBm}$ ,  $Z_0 = 50\text{ }\Omega$ ,  $C_{BLOCK} = 1000\text{ pF}$ ,  $C_{BYPASS} = 1000\text{ pF}$ , unless otherwise noted**

| Parameter  | Frequency     | Min. | Typ. | Max. | Unit |
|--|---------------|------|------|------|------|
| Insertion loss   | 0.02–1.00 GHz |      | 0.4  | 0.6  | dB   |
|  | 1.00–2.00 GHz |      | 0.6  | 0.8  | dB   |
|  | 2.00–2.50 GHz |      | 0.7  | 1.1  | dB   |
| Isolation  | 0.02–1.00 GHz | 35   | 40   |      | dB   |
|  | 1.00–2.00 GHz | 25   | 30   |      | dB   |
|  | 2.00–2.50 GHz | 21   | 26   |      | dB   |
| Return loss (Insertion loss state)<br>Lower freq. return loss is dependent on DC blocks              | 0.02–1.00 GHz | 12   | 18   |      | dB   |
|  | 1.00–2.00 GHz | 9    | 13   |      | dB   |
|  | 2.00–2.50 GHz | 7    | 13   |      | dB   |
| Return loss (Isolation state)<br>Lower freq. return loss is dependent on DC blocks and floating caps | 0.02–1.00 GHz | 9.5  | 14   |      | dB   |
|  | 1.00–2.00 GHz | 8.0  | 11   |      | dB   |
|  | 2.00–2.50 GHz | 7.0  | 9    |      | dB   |

### Operating Characteristics

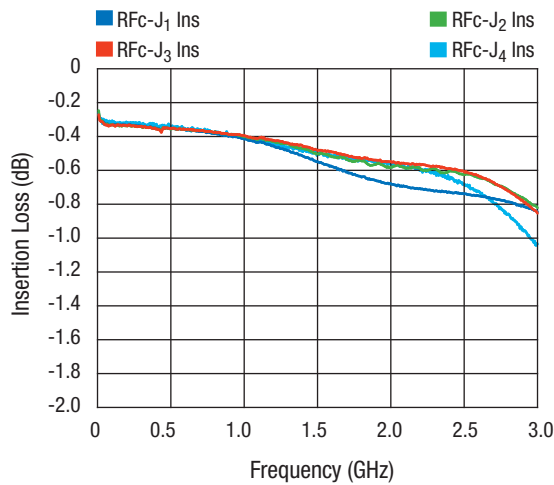
**V<sub>CTL</sub> = 0 V/3V, T = 25 °C, P<sub>INPUT</sub> = 0 dBm, Z<sub>0</sub> = 50 Ω, C<sub>BLOCK</sub> = 1000 pF, C<sub>BYPASS</sub> = 1000 pF, unless otherwise noted**

| Parameter                             | Condition   | Frequency | Min.      | Typ.   | Max.                   | Unit     |
|---------------------------------------|---|-----------|-----------|--------|------------------------|----------|
| Switching characteristics             |   |           |           |        |                        |          |
| Rise/fall time                        | 10/90% or 90/10% RF   |           |           | 25     |                        | ns       |
| On/Off time                           | 50% V <sub>CTL</sub> to 90/10% RF   |           |           | 50     |                        | ns       |
| Input power for 0.1 dB compression    | V <sub>DD</sub> = 3 V   | 870 MHz   | 13        | 16     |                        | dBm      |
| Intermodulation intercept point (IP3) | For two tone input power 8 dbm/tone<br>1 MHz spacing, V <sub>DD</sub> = 3 V | 900 MHz   |           | 40     |                        | dBm      |
| Control voltages <sup>(1)</sup>       | V <sub>CTL</sub> LOW<br>V <sub>CTL</sub> HIGH                               |           | 0<br>2.75 |        | 0.2<br>V <sub>DD</sub> | V<br>V   |
| Supply voltage (V <sub>DD</sub> )     |   |           | 3         |        | 5.5                    | V        |
| Supply currents                       | V <sub>DD</sub> = 3 V<br>V <sub>CTL</sub> LOW, V <sub>CTL</sub> HIGH        |           |           | 5<br>5 |                        | µA<br>µA |

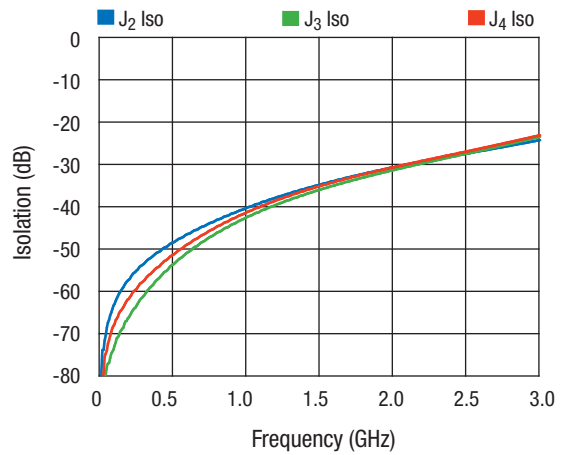
1. Control voltages switch the V<sub>DD</sub> voltage to the GaAs switch.  
V<sub>DD</sub> must be powered on prior to a V<sub>CTL</sub> high signal. A latch up condition may occur if a logic high signal is applied prior to the V<sub>DD</sub> voltage.

### Typical Performance Data

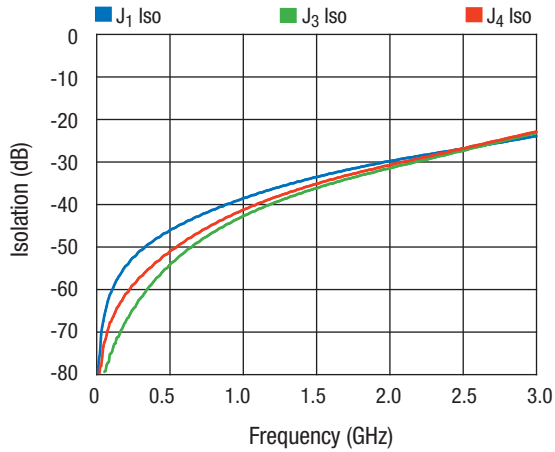
**V<sub>CTL</sub> = 0 V/3V, T = 25 °C, P<sub>INPUT</sub> = 0 dBm, Z<sub>0</sub> = 50 Ω, C<sub>BLOCK</sub> = 1000 pF, C<sub>BYPASS</sub> = 1000 pF, unless otherwise noted**



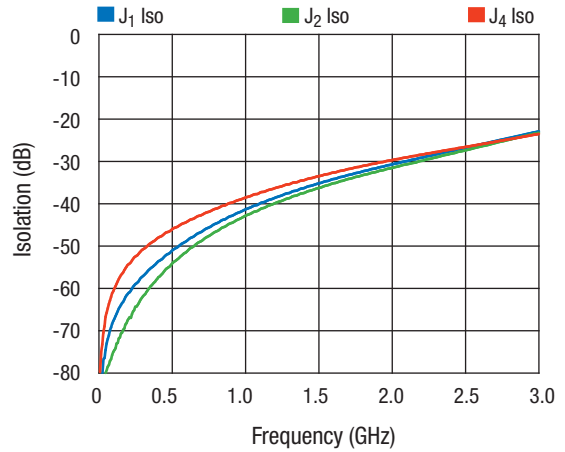
Typical Insertion Loss



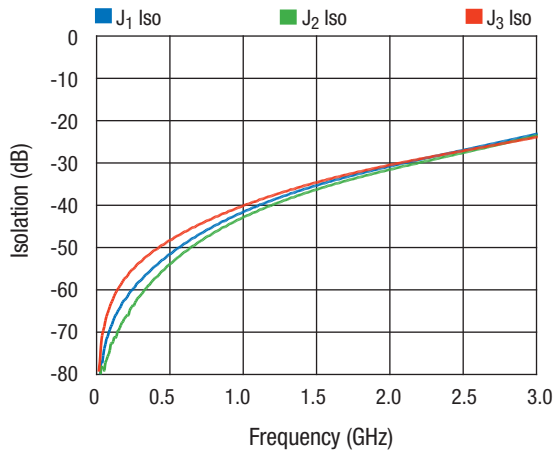
Typical Isolation RFC-J1 Path On



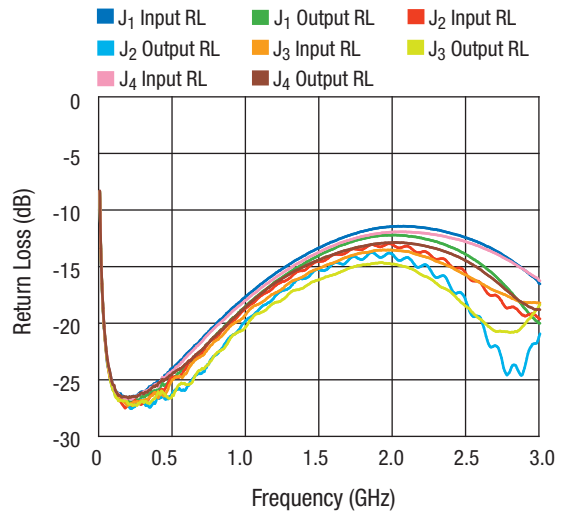
**Typical Isolation RFC-J<sub>2</sub> Path On**



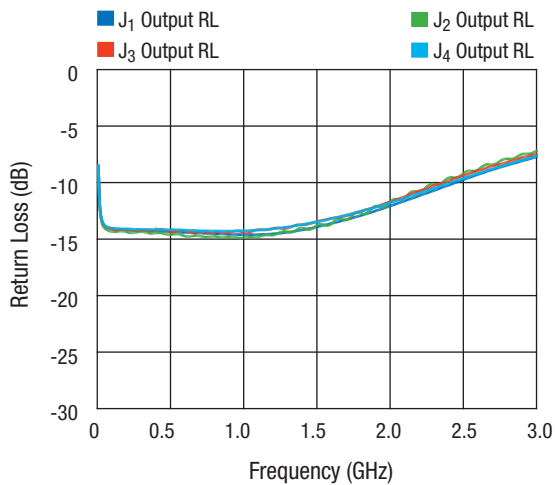
**Typical Isolation RFC-J<sub>3</sub> Path On**



**Typical Isolation RFC-J<sub>4</sub> Path On**

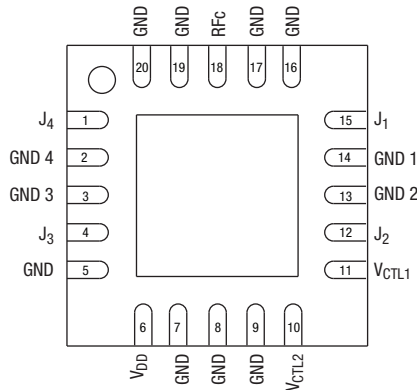


**Typical Return Loss  
Insertion Loss States**



**Typical Return Loss  
Isolation States**

### Pin Out (Top View X-ray of Pads on Bottom of Package)



DC blocks are required on RFC, J<sub>1</sub>, J<sub>2</sub>, J<sub>3</sub>, J<sub>4</sub>.  
Floating caps are required on Gnd 1, Gnd 2, Gnd 3, Gnd 4.

### Truth Table

| V <sub>DD</sub> | V <sub>CTL 1</sub> | V <sub>CTL 2</sub> | RFc-J <sub>1</sub> | RFc-J <sub>2</sub> | RFc-J <sub>3</sub> | RFc-J <sub>4</sub> |
|-----------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 1               | 0                  | 0                  | Ins. Loss          | Isolation          | Isolation          | Isolation          |
| 1               | 1                  | 0                  | Isolation          | Ins. Loss          | Isolation          | Isolation          |
| 1               | 0                  | 1                  | Isolation          | Isolation          | Ins. Loss          | Isolation          |
| 1               | 1                  | 1                  | Isolation          | Isolation          | Isolation          | Ins. Loss          |

V<sub>DD</sub> must be powered on prior to a VCTL high signal.  
"0" = 0 to 0.2 V.  
"1" = 2.75 to V<sub>DD</sub> V.  
V<sub>DD</sub> = 3 V to 5 V.

### Absolute Maximum Ratings

| Characteristic                | Value                          |
|-------------------------------|--------------------------------|
| V <sub>DD</sub> voltage range | 2.75 ≤ V <sub>DD</sub> ≤ 5.5 V |
| RF input power @ 5.5 V        | 1 W, f > 500 MHz               |
| Operating temperature         | -40 °C to +85 °C               |
| Storage temperature           | -65 °C to +150 °C              |

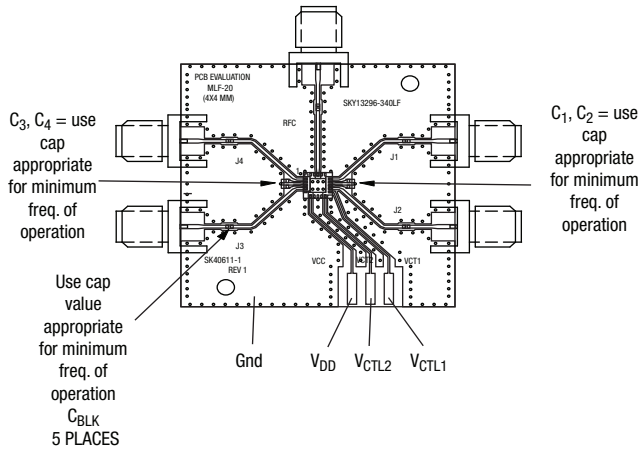
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

### Pin Assignments

| Pin            | Symbol             | Description   |
|----------------|--------------------|---|
| 1              | J <sub>4</sub>     | RF port. Must be DC blocked with a capacitor appropriate for lowest frequency of operation  |
| 2              | GND 4              | AC Ground for J <sub>4</sub> RF port. Must be DC blocked using a capacitor appropriate for lowest frequency of desired input return loss on J <sub>4</sub> port |
| 3              | GND 3              | AC Ground for J <sub>3</sub> RF port. Must be DC blocked using a capacitor appropriate for lowest frequency of desired input return loss on J <sub>3</sub> port |
| 4              | J <sub>3</sub>     | RF port. Must be DC blocked with a capacitor appropriate for lowest frequency of operation  |
| 5              | GND                | DC Ground   |
| 6              | V <sub>DD</sub>    | Supply voltage for decoder  |
| 7              | GND                | DC Ground   |
| 8              | GND                | DC Ground   |
| 9              | GND                | DC Ground   |
| 11             | V <sub>CTL 1</sub> | DC control voltage applied to decoder   |
| 10             | V <sub>CTL 2</sub> | DC control voltage applied to decoder   |
| 12             | J <sub>2</sub>     | RF port. Must be DC blocked with a capacitor appropriate for lowest frequency of operation  |
| 13             | GND 2              | AC Ground for J <sub>2</sub> RF port. Must be DC blocked using a capacitor appropriate for lowest frequency of desired input return loss on J <sub>2</sub> port |
| 14             | GND 1              | AC Ground for J <sub>1</sub> RF port. Must be DC blocked using a capacitor appropriate for lowest frequency of desired input return loss on J <sub>1</sub> port |
| 15             | J <sub>1</sub>     | RF port. Must be DC blocked with a capacitor appropriate for lowest frequency of operation  |
| 16             | GND                | DC Ground   |
| 17             | GND                | DC Ground   |
| 18             | RFc                | RF common port. Must be DC blocked with a capacitor appropriate for lowest frequency of operation   |
| 19             | GND                | DC Ground   |
| 20             | GND                | DC Ground   |
| Exposed Paddle |                    | DC Ground   |

### Evaluation Board



$C_{BLOCK} = 1000 \text{ pF}$  for operating frequency > 20 MHz.  
 $C_{BYPASS} C_1-C_4 = 1000 \text{ pF}$  for operating frequency > 20 MHz.

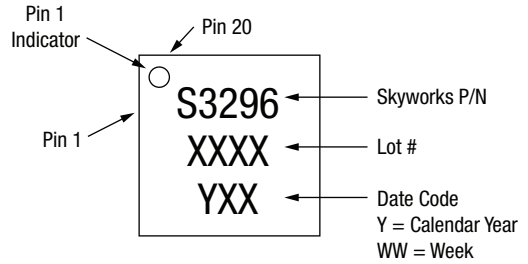
### Recommended Solder Reflow Profiles

Refer to the [“Recommended Solder Reflow Profile”](#) Application Note.

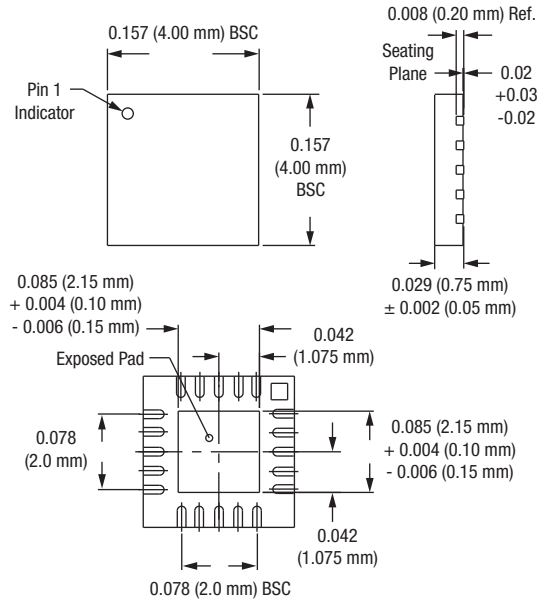
### Tape and Reel Information

Refer to the [“Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation”](#) Application Note.

### Part Marking



### QFN-20 (4 x 4)



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