THE DATASHEET OF

LMH0026MH/NOPB

LMH0026 SD SDI Reclocker with Dual Differential Outputs

Check for Samples: LMH0026

FEATURES

- **Supports SMPTE 259M (C) Serial Digital Video Standard**
- **Supports 270 Mbps Serial Data Rate Operation**
- **Supports DVB-ASI at 270 Mbps**
- **Single 3.3V Supply Operation**
- **330 mW Typical Power Consumption**
- **Two Differential, Reclocked Outputs**
- **Choice of Second Reclocked Output or Low-Jitter, Differential, Data-Rate Clock Output**
- **Single 27 MHz External Crystal or Reference Clock Input**
- **Lock Detect Indicator Output**
- **Output Mute Function for Data and Clock**
- **Auto/Manual Reclocker Bypass**
- **Differential LVPECL Compatible Serial Data Inputs and Outputs**
- **LVCMOS Control Inputs and Indicator Outputs**
- **20-Pin HTSSOP Package**
- **Industrial Temperature Range: -40°C to +85°C**
- **Footprint Compatible with the LMH0046 and LMH0346**

APPLICATIONS

- **SDTV Serial Digital Video Interfaces for:**
  - **Digital Video Routers and Switchers**
  - **Digital Video Processing and Editing Equipment**
  - **DVB-ASI Equipment**
  - **Video Standards and Format Converters**

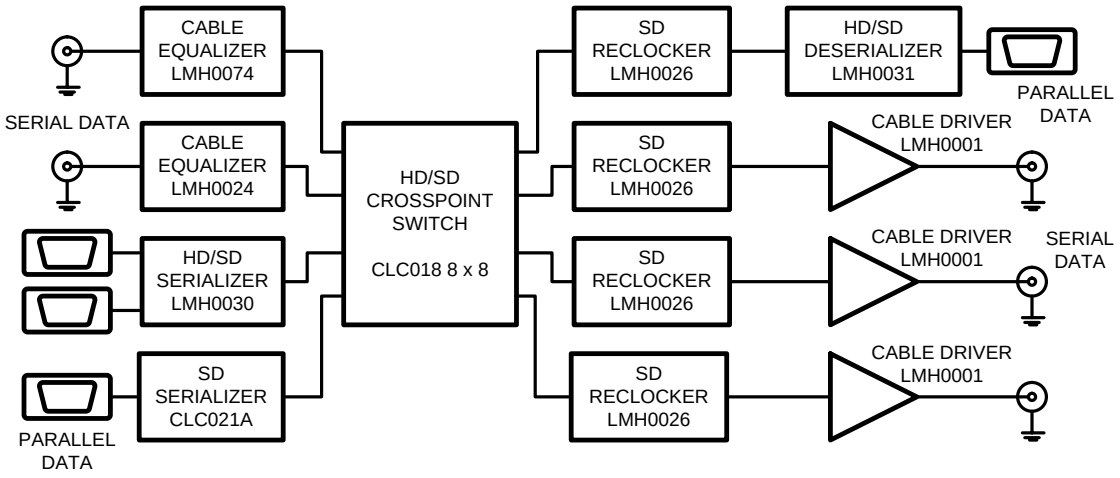
DESCRIPTION

The LMH0026 SD SDI Reclocker retimes serial digital video data conforming to the SMPTE 259M (C) standard. The LMH0026 operates at the serial data rate of 270 Mbps and also supports DVB-ASI operation at 270 Mbps.

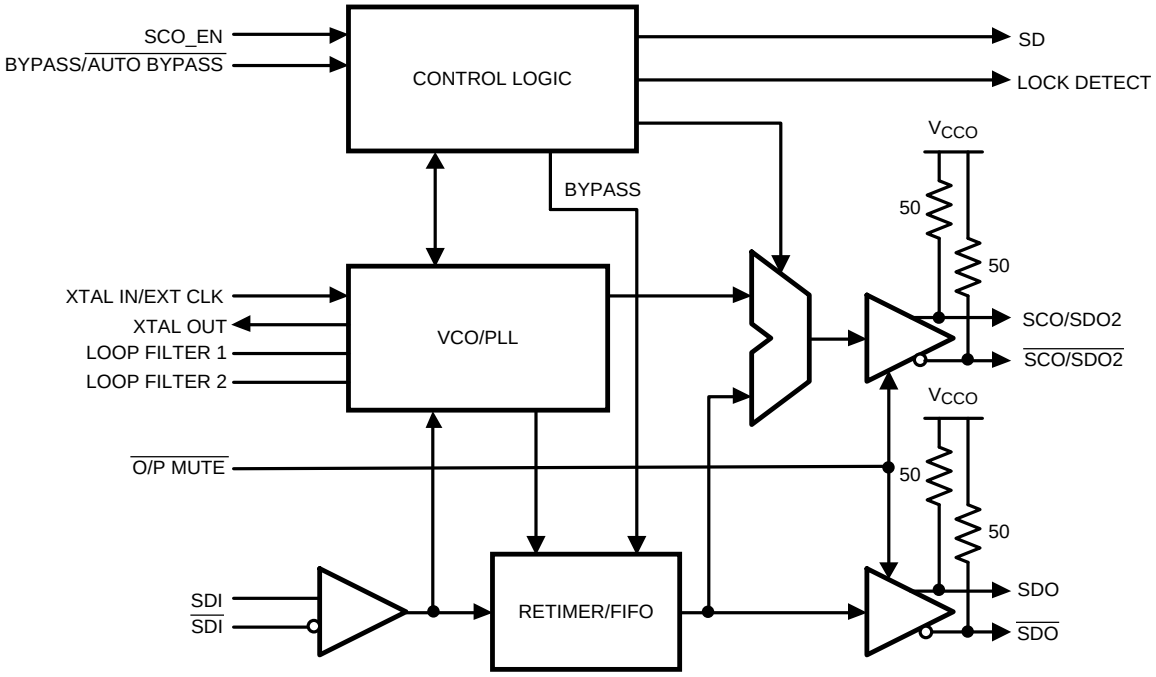
The LMH0026 retimes the incoming data to suppress accumulated jitter. The LMH0026 recovers the serial data-rate clock and optionally provides it as an output. The LMH0026 has two differential serial data outputs; the second output may be selected as a low-jitter, data-rate clock output. Controls and indicators are: serial clock or second serial data output select, SD indicator output, lock detect output, auto/manual data bypass, and output mute. The serial data inputs, outputs, and serial data-rate clock outputs are differential LVPECL compatible. The CML serial data and serial data-rate clock outputs are suitable for driving 100Ω differentially terminated networks. The control logic inputs and outputs are LVCMOS compatible.

The LMH0026 is powered from a single 3.3V supply. Power dissipation is typically 330 mW. The device is housed in a 20-pin HTSSOP package.

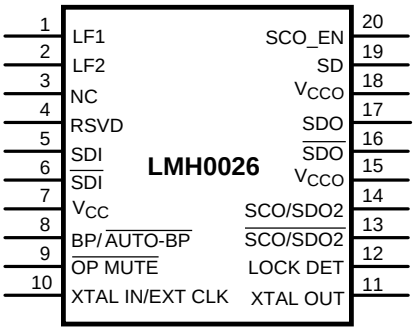
TYPICAL APPLICATION



Block Diagram



CONNECTION DIAGRAM



The exposed die attach pad is the negative electrical terminal for this device. It must be connected to the negative power supply voltage.

Figure 1. 20-Pin HTSSOP

PIN DESCRIPTIONS

Pin	Name	Description
1	LF1	Loop Filter.
2	LF2	Loop Filter.
3	NC	No Connect. Not bonded internally.
4	RSVD	Reserved. Do not connect or connect to ground.
5	SDI	Data Input true.
6	$\overline{SDI}$	Data Input complement.
7	V_{CC}	Positive power supply input.
8	BYPASS/$\overline{AUTO\ BYPASS}$	Bypass/Auto Bypass mode select. Bypasses reclocking when high. This pin has an internal pulldown.
9	OUTPUT $\overline{MUTE}$	Data and Clock Output Mute input. Mutes the output when low. This pin has an internal pullup.
10	XTAL IN/EXT CLK	Crystal or External Oscillator input.
11	XTAL OUT	Crystal Oscillator output.
12	LOCK DETECT	PLL Lock Detect output (active high).
13	$\overline{SCO/SDO2}$	Serial Clock or Serial Data Output 2 complement.
14	SCO/SDO2	Serial Clock or Serial Data Output 2 true.
15	V_{CCO}	Positive power supply input (Output Driver).
16	$\overline{SDO}$	Data Output complement.
17	SDO	Data Output true.
18	V_{CCO}	Positive power supply input (output driver).
19	SD	SD indicator output. Output is high when locked to 270 Mbps.
20	SCO_EN	Serial Clock or Serial Data 2 Output select. Sets second output to output the clock when high and the data when low. This pin has an internal pulldown.
DAP	V_{EE}	Connect exposed DAP to negative power supply (ground).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (V_{CC}–V_{EE})		4.0V
Logic Supply Voltage (Vi)		V_{EE}−0.15V to V_{CC}+0.15V
Logic Input Current (single input):	Vi = V_{EE}−0.15V	−5 mA
	Vi = V_{CC}+0.15V	+5 mA
Logic Output Voltage (Vo)		V_{EE}−0.15V to V_{CC}+0.15V
Logic Output Source/Sink Current		±8 mA
Serial Data Input Voltage (V_{SDI})		V_{CC} to V_{CC}−2.0V
Serial Data Output Sink Current (I_{SDO})		24 mA
Package Thermal Resistance, HTSSOP	θ_{JA}	26.6°C/W
	θ_{JC}	2.4°C/W
Storage Temp. Range		−65°C to +150°C
Junction Temperature		+150°C
Lead Temperature (Soldering 4 Sec)		+260°C (Pb-free)
ESD Rating (HBM)		7 kV
ESD Rating (MM)		350V
ESD Rating (CDM)		1250V

(1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. DC ELECTRICAL CHARACTERISTICS and AC ELECTRICAL CHARACTERISTICS specify acceptable device operating conditions.

(2) **It is anticipated that this device will not be offered in a military qualified version.** If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC}–V_{EE})		3.3V ±5%
Logic Input Voltage		V_{EE} to V_{CC}
Differential Serial Input Voltage		800 mV ±10%
Serial Data or Clock Output Sink	Current (I_{SO})	16 mA max.
Operating Free Air Temperature (T_A)		−40°C to +85°C

DC ELECTRICAL CHARACTERISTICS

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (1)(2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic level inputs	2		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.8	V
I_{IH}	Input Current High Level	V_{IH} = V_{CC}			47	65	µA
I_{IL}	Input Current Low Level	V_{IL} = V_{EE}			−18	−25	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA	All logic level outputs	2			V
V_{OL}	Output Voltage Low Level	I_{OL} = +2 mA				V_{EE} + 0.6	V
V_{SDID}	Serial Input Voltage, Differential		SDI	200		1600	mV_{P-P}
V_{CMI}	Input Common Mode Voltage	V_{SDID} = 200 mV		V_{EE}+1.2		V_{CC}−0.2	V

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are referenced to V_{EE} (equal to zero volts).

(2) Typical values are stated for: V_{CC} = +3.3V, T_A = +25°C.

DC ELECTRICAL CHARACTERISTICS (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (1)(2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{SDOD}	Serial Output Voltage, Differential	100Ω differential load	SDO, SCO	720	800	880	mV_{P-P}
V_{CMO}	Output Common Mode Voltage	100Ω differential load			V_{CC} – V_{SDOD}		V
I_{CC}	Power Supply Current, 3.3V supply, Total	270 Mbps			100		mA

AC ELECTRICAL CHARACTERISTICS

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (1)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{SD}	Serial Data Rate	SMPTE 259M-C	SDI, SDO		270		Mbps
TOL_{JIT}	Serial Input Jitter Tolerance	270 Mbps, (2) (3) (4)	SDI	>6			UI_{P-P}
TOL_{JIT}	Serial Input Jitter Tolerance	270 Mbps, (2) (3) (5)		>0.6			UI_{P-P}
t_{JIT}	Serial Data Output Jitter	270 Mbps, (3) (6)	SDO		0.02	0.08	UI_{P-P}
BW_{LOOP}	Loop Bandwidth	270 Mbps, <0.1dB Peaking			300		kHz
F_{CO}	Serial Clock Output Frequency	270 Mbps data rate	SCO		270		MHz
t_{JIT}	Serial Clock Output Jitter				2	3	ps_{RMS}
	Serial Clock Output Alignment with respect to Data Interval		SDO, SCO	40		60	%
	Serial Clock Output Duty Cycle		SCO	45		55	%
T_{ACQ}	Acquisition Time					(7)(8)15	ms
t_r, t_f	Input rise/fall time	10%–90%	Logic inputs		1.5	3	ns
t_r, t_f	Input rise/fall time	20%–80%	SDI			1500	ps
t_r, t_f	Output rise/fall time	10%–90%	Logic outputs		1.5	3	ns
t_r, t_f	Output rise/fall time	20%–80%, (9)	SDO, SCO		90	130	ps
F_{REF}	Reference Clock Frequency				27		MHz
F_{TOL}	Reference Clock Frequency Tolerance				±50		ppm

(1) Typical values are stated for: V_{CC} = +3.3V, T_A = +25°C.
(2) Peak-to-peak amplitude with sinusoidal modulation per SMPTE RP 184-1996 paragraph 4.1. The test data signal shall be color bars.
(3) This parameter is ensured by characterization over voltage and temperature limits.
(4) Refer to “A1” in Figure 1 of SMPTE RP 184-1996.
(5) Refer to “A2” in Figure 1 of SMPTE RP 184-1996.
(6) Serial Data Output Jitter is total output jitter with 0.2 UI_{P-P} input jitter.
(7) Specification is ensured by design.
(8) Measured from first SDI transition until Lock Detect (LD) output goes high (true).
(9) R_L = 100Ω differential.

DEVICE DESCRIPTION

The LMH0026 SD SDI Reclocker is used in many types of digital video signal processing equipment. The LMH0026 supports the SMPTE 259M (C) serial digital video standard, with a corresponding serial data rate of 270 Mbps. DVB-ASI data at 270 Mbps may also be retimed. The LMH0026 retimes the serial data stream to suppress accumulated jitter. It provides two low-jitter, differential, serial data outputs. The second output may be selected to output either serial data or a low-jitter serial data-rate clock. Controls and indicators are: serial data-rate clock or second serial data output select, SD indicator output, lock detect output, auto/manual data bypass, and output mute.

Serial data inputs are CML and LVPECL compatible. Serial data and data-rate clock outputs are differential CML and produce LVPECL compatible levels. The output buffer design can drive AC or DC-coupled, terminated 100Ω differential loads. The differential output level is 800 mV_{P-P} ±10% into 100Ω AC or DC-coupled differential loads. Logic inputs and outputs are LVCMOS compatible.

The device package is an HTSSOP-20 with an exposed die attach pad. The exposed die attach pad is electrically connected to device ground (V_{EE}) and is the negative electrical terminal for the device. This terminal must be connected to the negative power supply or circuit ground.

Serial Data Inputs, Serial Data and Clock Outputs

SERIAL DATA INPUT AND OUTPUTS

The differential serial data input, SDI, accepts 270 Mbps serial digital video data. The serial data input is differential LVPECL compatible. The input is intended to be DC interfaced to devices such as the LMH0074 adaptive cable equalizer. The input is not internally terminated or biased. The input may be AC-coupled if a suitable input bias voltage is provided. Figure 2 shows the equivalent input circuit for SDI and $\overline{\text{SDI}}$.

The LMH0026 has two, retimed, differential, serial data outputs, SDO and SCO/SDO2. These outputs provide low jitter, differential, retimed data to devices such as the LMH0001 or LMH0002 cable driver. Output SCO/SDO2 is multiplexed and can provide either a second serial data output or a serial data-rate clock output. Figure 3 shows the equivalent output circuit for SDO, $\overline{\text{SDO}}$, SCO/SDO2, and $\overline{\text{SCO/SDO2}}$.

The SCO_EN input controls the operating mode for the SCO/SDO2 output. When the SCO_EN input is high the SCO/SDO2 output provides a serial data-rate clock. When SCO_EN is low, the SCO/SDO2 output provides retimed serial data.

Both differential serial data outputs, SDO and SCO/SDO2, are muted when the OUTPUT $\overline{\text{MUTE}}$ input is a logic low level. SCO/SDO2 also mutes when the Bypass mode is activated when this output is operating as the serial clock output. When muted, SDO and $\overline{\text{SDO}}$ (or SDO2 and $\overline{\text{SDO2}}$) will assume opposite differential output levels. The CML serial data outputs are differential LVPECL compatible. These outputs have internal 50Ω pull-ups and are suitable for driving AC or DC-coupled, 100Ω center-tapped, AC grounded or 100Ω un-center-tapped, differentially terminated networks.

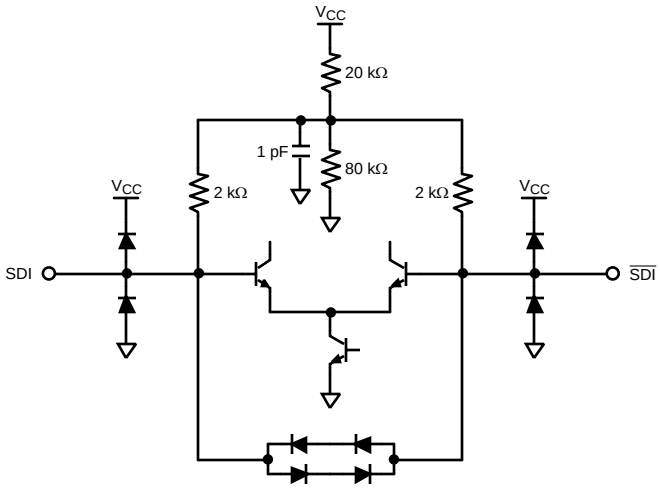


Figure 2. Equivalent SDI input Circuit (SDI, $\overline{\text{SDI}}$)

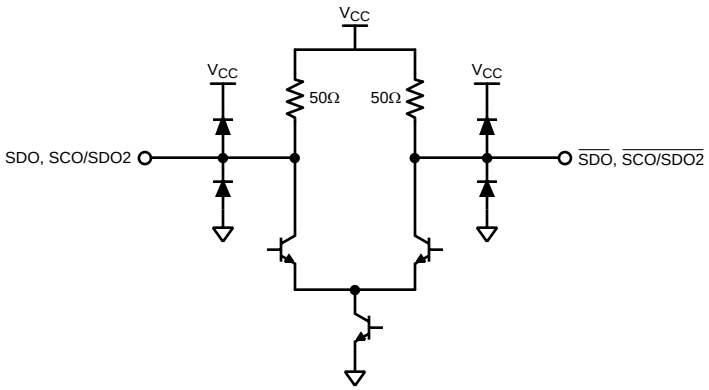


Figure 3. Equivalent SDO Output Circuit (SDO, $\overline{\text{SDO}}$, SCO/SDO2, $\overline{\text{SCO/SDO2}}$)

SERIAL DATA CLOCK/SERIAL DATA 2 OUTPUT

The Serial Data Clock/Serial Data 2 Output is controlled by the SCO_EN input and provides either a second retimed serial data output or a low jitter differential clock output appropriate to the serial data rate being processed. When operating as a serial clock output, the rising edge of the clock will be positioned within the corresponding serial data bit interval within 10% of the center of the data interval.

Differential output SCO/SDO2 functions as the second serial data output when the SCO_EN input is a logic-low level. This output functions as the serial data-rate clock output when the SCO_EN input is a logic-high level. The SCO_EN input has an internal pull-down device and the default state of SCO_EN is low (serial data output 2 enabled). SCO/SDO2 is muted when the OUTPUT $\overline{\text{MUTE}}$ input is a logic low level. When the Bypass mode is activated and this output is functioning as a serial clock output, the output will also be muted. If an unsupported data rate is used while in Auto Bypass mode with this output functioning as a serial clock output, the output is invalid.

Control Inputs and Indicator Outputs

LOCK DETECT

The Lock Detect (LD) output, when high, indicates that data is being received and the PLL is locked. LD may be connected to the OUTPUT $\overline{\text{MUTE}}$ input to mute the data and clock outputs when no data signal is being received. Note that when the Bypass/Auto Bypass input is set high, Lock Detect will remain low. See Table 1.

OUTPUT $\overline{\text{MUTE}}$

The OUTPUT $\overline{\text{MUTE}}$ input, when low, mutes the serial data and clock outputs. It may be connected to Lock Detect or externally driven to mute or un-mute the outputs. If OUTPUT $\overline{\text{MUTE}}$ is connected to LD, then the data and clock outputs are muted when the PLL is not locked. This function overrides the Bypass function: see Table 1. OUTPUT $\overline{\text{MUTE}}$ has an internal pull-up device to enable the output by default.

BYPASS/$\overline{\text{AUTO BYPASS}}$

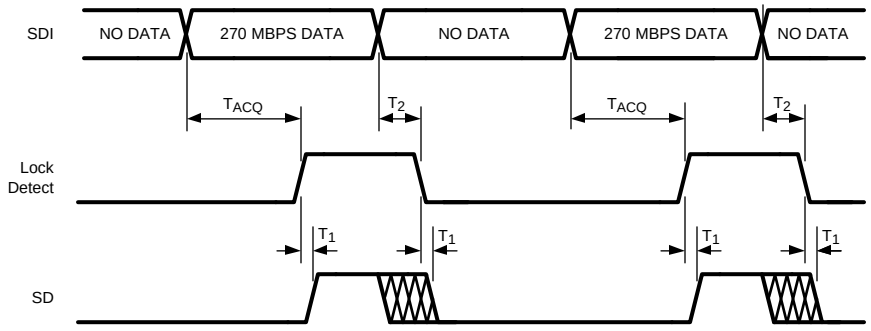
The Bypass/$\overline{\text{Auto Bypass}}$ input, when high, forces the device to output the data without reclocking it. When this input is low, the device automatically bypasses the reclocking function when the device is in an unlocked condition or the detected data rate is a rate which the device does not support. Note that when the Bypass/$\overline{\text{Auto Bypass}}$ input is set high, Lock Detect will remain low. See Table 1. BYPASS/$\overline{\text{AUTO BYPASS}}$ has an internal pull-down device.

Table 1. Control Functionality

LOCK DETECT	OUTPUT $\overline{\text{MUTE}}$	BYPASS/$\overline{\text{AUTO BYPASS}}$	DEVICE STATUS
0	1	X	PLL unlocked, reclocker bypassed
1	1	0	PLL locked to supported data rate, reclocker not bypassed
X	0	X	Outputs muted
0	LOCK DETECT	X	Outputs muted
1	LOCK DETECT	0	PLL locked to supported data rate, reclocker not bypassed

SD

The SD output indicates that the LMH0026 is locked and processing SD data rates. It may be used to control another device such as the LMH0002 cable driver. When this output is high it indicates that the data rate is 270 Mbps. The SD output is a registered function and is only valid when the PLL is locked and the Lock Detect output is high. When the PLL is not locked (the Lock Detect output is low), the SD output defaults to low. The SD output is undefined for a short time after lock detect assertion or de-assertion due to a data change on SDI. See Figure 4 for a timing diagram showing the relationship between SDI, Lock Detect, and SD.



T_{ACQ} = Acquisition Time, defined in the AC Electrical Characteristics Table
T_1 = Time from Lock Detect assertion or deassertion until SD output is valid, typically 37 ns (one 27 MHz clock period)
T_2 = Time from SDI input change until Lock Detect de-assertion, 1 ms maximum. SD output is not valid during this time.

Figure 4. SDI, Lock Detect, and SD Timing

SCO_EN

Input SCO_EN enables the SCO/SDO2 differential output to function either as a serial data-rate clock or second serial data output. SCO/SDO2 functions as a serial data-rate clock when SCO_EN is high. This pin has an internal pull-down device. The default state (low) enables the SCO/SDO2 output as a second serial data output.

CRYSTAL OR EXTERNAL CLOCK REFERENCE

The LMH0026 uses a 27 MHz crystal or external clock signal as a timing reference input. A 27 MHz parallel resonant crystal and load network may be connected to the XTAL IN/EXT CLK and XTAL OUT pins. Alternatively, a 27 MHz LVCMOS compatible clock signal may be input to XTAL IN/EXT CLK. Parameters for a suitable crystal are given in Table 2.

Table 2. Crystal Parameters

Parameter	Value
Frequency	27 MHz
Frequency Stability	±50 ppm @ recommended drive level
Operating Mode	Fundamental mode, Parallel Resonant
Load Capacitance	20 pF
Shunt Capacitance	7 pF
Series Resistance	40Ω max.
Recommended Drive Level	100 µW
Maximum Drive Level	500 µW
Operating Temperature Range	−10°C to +60°C

APPLICATION INFORMATION

Figure 5 shows an application circuit for the LMH0026 along with the LMH0074 SMPTE 259M / 344M Adaptive Cable Equalizer and LMH0001 SMPTE 259M / 344M Cable Driver.

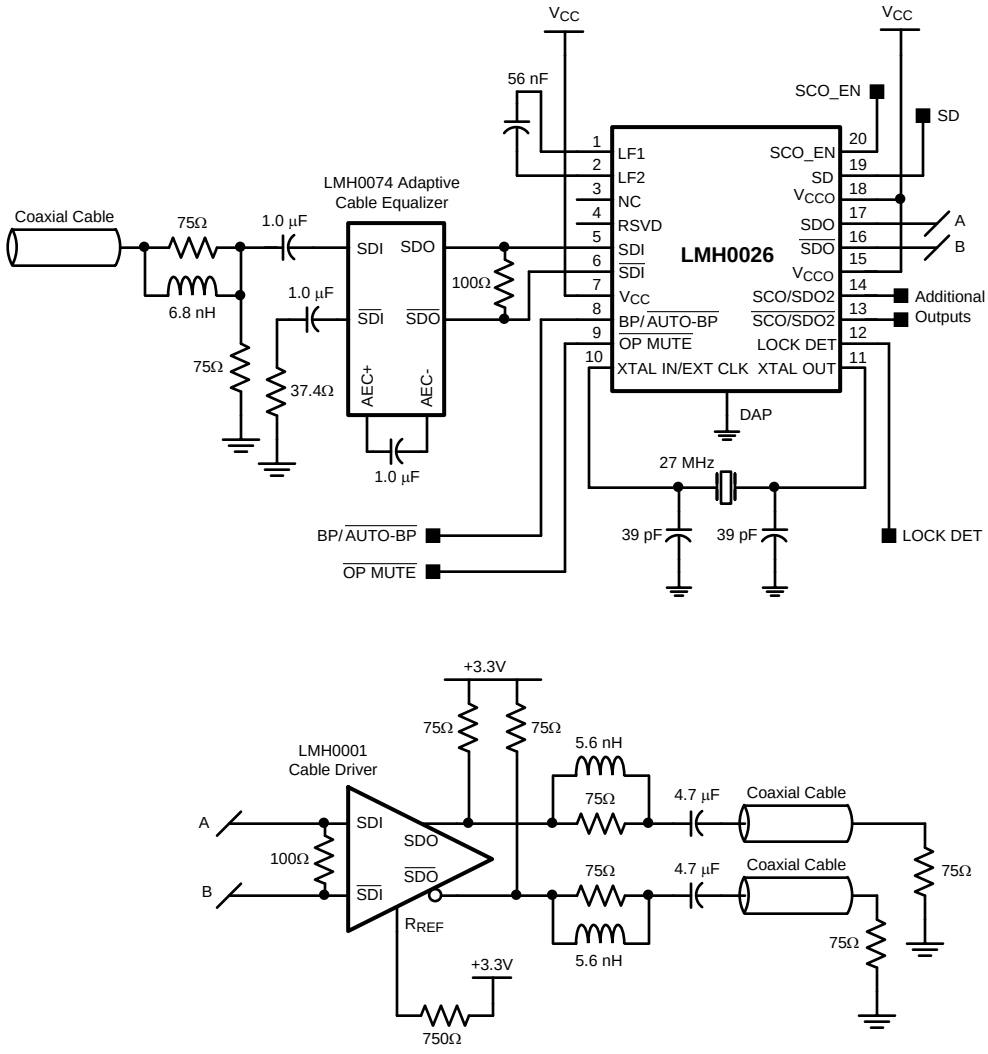


Figure 5. Application Circuit

The LMH0026 inputs are LVPECL compatible. The LMH0026 has a wide input common mode range and in most cases the input should be DC coupled. For DC coupling, the inputs must be kept within the common mode range specified in DC ELECTRICAL CHARACTERISTICS. Figure 5 shows an example of a DC coupled interface between the LMH0074 cable equalizer and the LMH0026. The LMH0074 output common mode voltage and voltage swing are within the range of the input common mode voltage and voltage swing of the LMH0026. All that is required is a 100Ω differential termination as shown. The resistor should be placed as close to the LMH0026 input as possible. If desired, this network may be terminated with two 50Ω resisters and a center tap capacitor to ground in place of the single 100Ω resistor.

The LMH0026 outputs are LVPECL compatible. SDO is the primary data output and SCO/SDO2 is a second output that may be set as the serial clock or a second data output. Both outputs are always active. The LMH0026 output should be DC coupled to the input of the receiving device as long as the common mode ranges of both devices are compatible. Figure 5 shows an example of a DC coupled interface between the LMH0026 and LMH0001 cable driver. All that is required is a 100Ω differential termination as shown. The resistor should be placed as close to the LMH0001 input as possible. If desired, this network may be terminated with two 50Ω resisters and a center tap capacitor to ground in place of the single 100Ω resistor.

The external loop filter capacitor (between LF1 and LF2) should be 56 nF. This is the only supported value; the loop filter capacitor should not be changed.

BYPASS/$\overline{\text{AUTO BYPASS}}$ has an internal pulldown to enable Auto Bypass mode by default. This pin may be pulled high to force the LMH0026 to bypass all data.

OUTPUT $\overline{\text{MUTE}}$ has an internal pullup to enable the outputs by default. This pin may be pulled low to mute the outputs.

The XTAL IN/EXT CLK and XTAL OUT pins are shown with a 27 MHz crystal and the proper loading. The crystal should match the parameters described in Table 2. Alternately, a 27MHz LVCMOS compatible clock signal may be input to XTAL IN/EXT CLK.

The active high LOCK DETECT output provides an indication that proper data is being received and the PLL is locked.

The SD output may be used to drive the SD/$\overline{\text{HD}}$ pin of an SDI cable driver (such as the LMH0002) in order to properly set the cable driver's edge rate for SMPTE compliance. It defaults to low when the LMH0026 is not locked.

SCO_EN has an internal pulldown to set the second output (SCO/SDO2) to output data. This pin may be pulled high to set the second output as a serial clock.

The ground connection for the LMH0026 is through the large exposed DAP. The DAP must be connected to ground for proper operation of the LMH0026.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0026MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L026	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

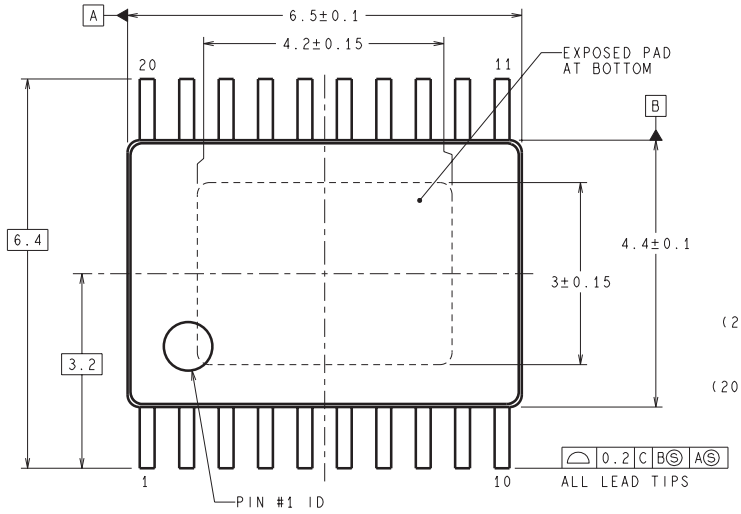
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

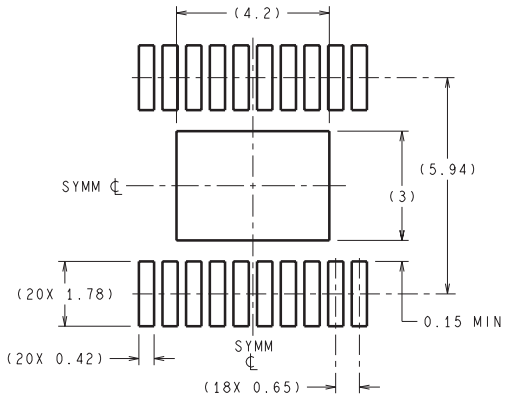
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

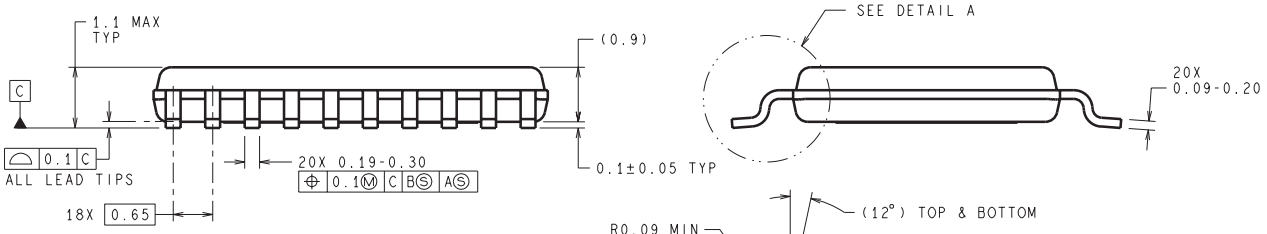
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

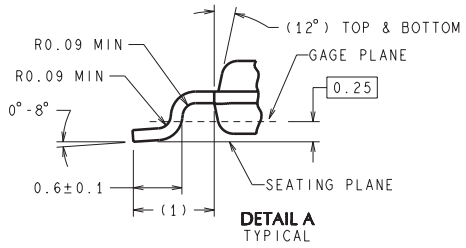
PWP0020A





RECOMMENDED LAND PATTERN





DETAIL A
TYPICAL

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MXA20A (Rev C)

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