THE DATASHEET OF

SI4355-B1A-FM

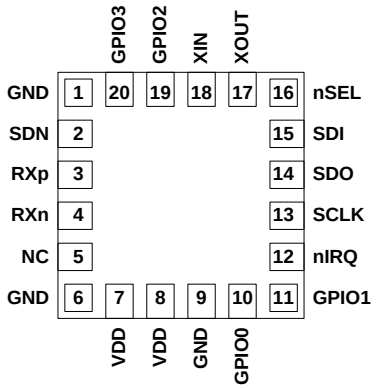
Si4355

EASY-TO-USE, LOW-CURRENT OOK/(G)FSK SUB-GHZ RECEIVER

Features

- Frequency range = 283–960 MHz
- Receive sensitivity = –116 dBm
- Modulation
  - (G)FSK
  - OOK
- Low RX Current = 10 mA
- Low standby current = 50 nA
- Max data rate = 500 kbps
- Power supply = 1.8 to 3.6 V
- 64 byte FIFO
- Auto frequency control (AFC)
- Automatic gain control (AGC)
- Integrated battery voltage sensor
- Packet handling including preamble, sync word detection, and CRC
- Low BOM
- 20-Pin 3x3 mm QFN package

Pin Assignments



Patents pending

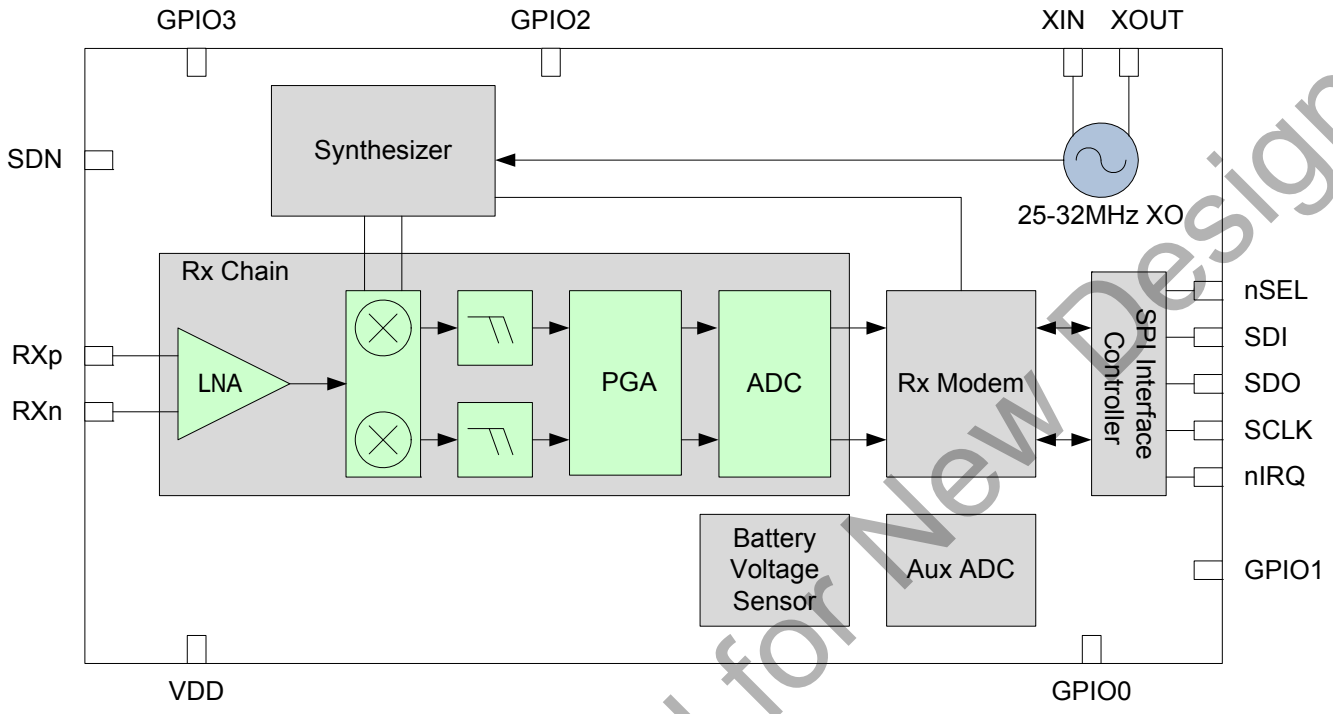
Applications

- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors

Description

Silicon Laboratories' Si4355 is an easy to use, low current, sub-GHz EZRadio® receiver. Covering all major bands, it combines plug-and-play simplicity with the flexibility needed to handle a wide variety of applications. The compact 3x3 mm package size combined with a low external BOM count makes the Si4355 both space efficient and cost effective. Excellent sensitivity of 116 dBm allows for a longer operating range, while the low current consumption of 10 mA active and 50 nA standby, provides for superior battery life. By fully integrating all components from the antenna to the GPIO or SPI interface to the MCU, the Si4355 makes realizing this performance in an application easy. Design simplicity is further exemplified in the Wireless Development Suite (WDS) user interface module. This configuration module provides simplified programming options for a broad range of applications in an easy to use format that results in both a faster and lower risk development. Like all Silicon Laboratories' EZRadio devices, the Si4355 is fully compliant with all worldwide regulatory standards, such as FCC, ETSI, and ARIB.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Supply Voltage	V_{DD}		1.8		3.6	V
I/O Drive Voltage	V_{GPIO}		1.8		3.6	V

Table 2. DC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	V_{DD}		1.8	3.3	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC oscillator, main digital regulator, and low power digital regulator OFF	—	30	—	nA
	$I_{Standby}$	Register values maintained and RC oscillator/WUT OFF	—	50	—	nA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	2	—	mA
	$I_{SPI\ Active}$	SPI Active State		1.35		mA
TUNE Mode Current	I_{Tune_RX}	RX Tune	—	6.5	—	mA
RX Mode Current	I_{RX}		—	10	—	mA

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section of "1.1. Definition of Test Conditions" on page 9.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.

Table 3. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	F_{SYN}		283	—	350	MHz
			425	—	525	MHz
			850	—	960	MHz
Synthesizer Frequency Resolution[2]	$F_{RES-960}$	850–960 MHz	—	114.4	—	Hz
	$F_{RES-525}$	425–525 MHz	—	57.2	—	Hz
	$F_{RES-350}$	283–350 MHz	—	38.1	—	Hz
Synthesizer Settling Time[2]	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency, including VCO Calibration	—	130	—	µs

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.

Table 4. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range	F_{RX}		283	—	350	MHz
			425	—	525	MHz
			850	—	960	MHz
RX Sensitivity	P_{RX-_2}	(BER < 0.1%) (2.4 kbps, GFSK, BT = 0.5, $\Delta f = \pm 30$ kHz)[2] ,114 kHz Rx BW	—	–116	—	dBm
	P_{RX-_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, $\Delta f = \pm 25$ kHz)[2], 114 kHz Rx BW	—	–108	—	dBm
	P_{RX-_128}	(BER < 0.1%) (128 kbps, GFSK, BT = 0.5, $\Delta f = \pm 70$ kHz)[2], 305 kHz Rx BW	—	–103	—	dBm
	P_{RX-_OOK}	BER < 0.1%, 1 kbps, 185 kHz Rx BW, OOK, PN15 data	—	–113	—	dBm
		BER < 0.1%, 40 kbps, 185 kHz Rx BW, OOK, PN15 data	—	–102	—	dBm
RX Channel Bandwidth[2]	BW		40	—	850	kHz

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.

Table 4. Receiver AC Electrical Characteristics[1] (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
BER Variation vs Power Level[2]	P_{RX_RES}	Up to +5 dBm Input Level	—	0	0.1	ppm
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB
±1-Ch Offset Selectivity[2]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW and desired modulated with 1.2 kbps ΔF = 5.2 kHz GFSK with BT = 0.5, Rx BW = 58 kHz, channel spacing = 100 kHz	—	–56	—	dB
±2-Ch Offset Selectivity[2]	$C/I_{2\text{-}CH}$		—	–59	—	dB
Blocking 200 kHz–1 MHz	$200K_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1% Interferer is CW and desired modulated with 1.2 kbps ΔF = 5.2 kHz GFSK with BT = 0.5, RX BW = 58 kHz	—	–58	—	dB
Blocking 1 MHz Offset[2]	$1M_{BLOCK}$		—	–61	—	dB
Blocking 8 MHz Offset[2]	$8M_{BLOCK}$		—	–79	—	dB
Image Rejection[2]	Im_{REJ}	Rejection at the image frequency. IF = 468 kHz	—	–40	—	dB
Spurious Emissions[2]	P_{OB_RX1}	Measured at RX pins	—	—	–54	dBm

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.

Table 5. Auxiliary Block Specifications[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
XTAL Range[2]	XTAL-RANGE		25	—	32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout	—	250	—	µs
30 MHz XTAL Cap Resolution[3]	$30M_{RES}$		—	70	—	fF
POR Reset Time	t_{POR}		—	—	5	ms

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.
2. XTAL Range tested in production using an external clock source (similar to using a TCXO).
3. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.

Table 6. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	2.3	—	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	0<V_{IN} < V_{DD}	–10	—	10	µA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	10	µA
Drive Strength for Output Low Level[2]	I_{OLL}	DRV<1:0> = LL		2.1		mA
	I_{OLH}	DRV<1:0> = LH		1.5		mA
	I_{OHL}	DRV<1:0> = HL		1.0		mA
	I_{OHH}	DRV<1:0> = HH		0.4		mA
Drive Strength for Output High Level (GPIO1, GPIO2, GPIO3)[2]	I_{OLL}	DRV<1:0> = LL		4.5		mA
	I_{OLH}	DRV<1:0> = LH		3.3		mA
	I_{OHL}	DRV<1:0> = HL		2.1		mA
	I_{OHH}	DRV<1:0> = HH		0.7		mA
Drive Strength for Output High Level (GPIO0)[2]	I_{OLL}	DRV<1:0> = LL		1.9		mA
	I_{OLH}	DRV<1:0> = LH		1.7		mA
	I_{OHL}	DRV<1:0> = HL		1.3		mA
	I_{OHH}	DRV<1:0> = HH		0.6		mA
Logic High Level Output Voltage	V_{OH}	I_{OUT} = 500 µA	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OUT} = 500 µA	—	—	V_{DD} x 0.2	V

Notes:
1. All specifications guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 9.
2. GPIO output current measured at 3.3 VDC VDD with V_{OH} = 2.7 VDC and V_{OL} = 0.66 VDC.

Table 7. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	30	°C/W
Junction Temperature	T_J		125	°C

Table 8. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
Voltage on Digital Control Inputs	–0.3, V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	–40 to +85	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.

1.1. Definition of Test Conditions

Production Test Conditions:

- T_A = +25 °C
- V_{DD} = +3.3 VDC
- Sensitivity measured at 434 MHz using a PN15 modulated input signal and with packet handler mode enabled.
- External reference signal (XIN) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC
- Production test schematic (unless noted otherwise)
- All RF input and output levels referred to the pins of the Si4355 (not the RF module)

Qualification Test Conditions:

- T_A = –40 to +85 °C (typical = 25 °C)
- V_{DD} = +1.8 to +3.6 VDC (typical = 3.3 VDC)
- Using reference design or production test schematic
- All RF input and output levels referred to the pins of the Si4355 (not the RF module)

2. Typical Applications Circuit

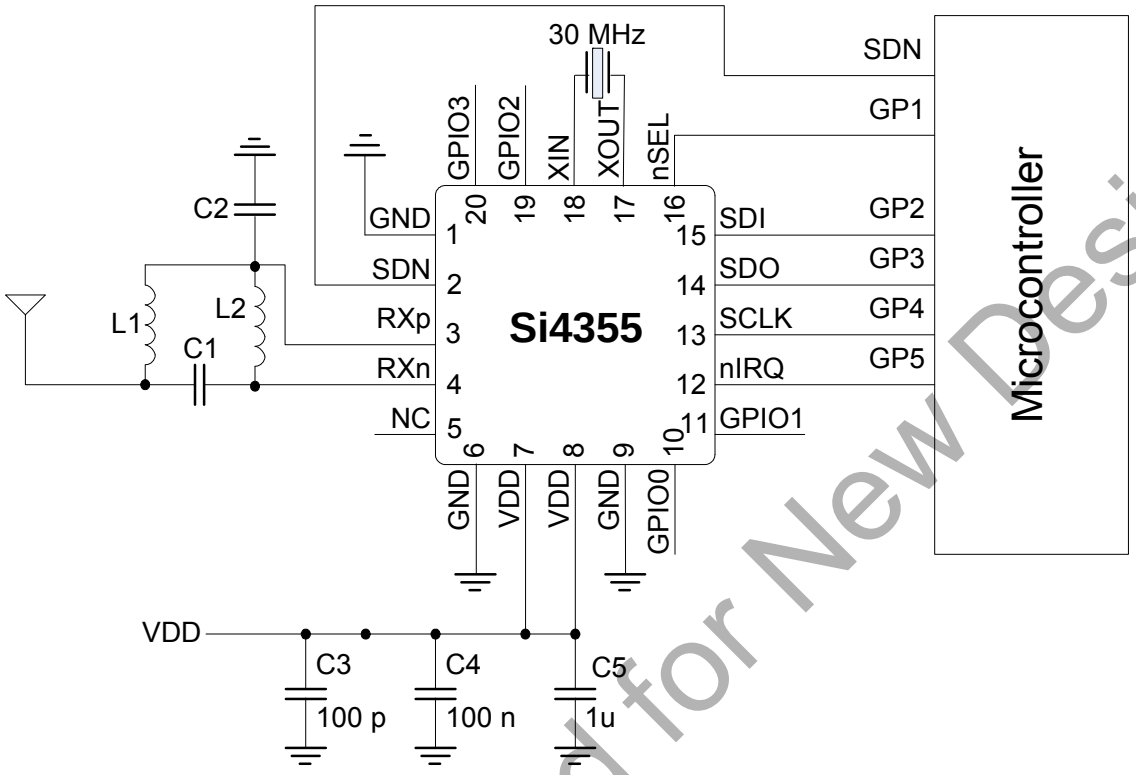


Figure 1. Si4355 Applications Circuit

3. Functional Description

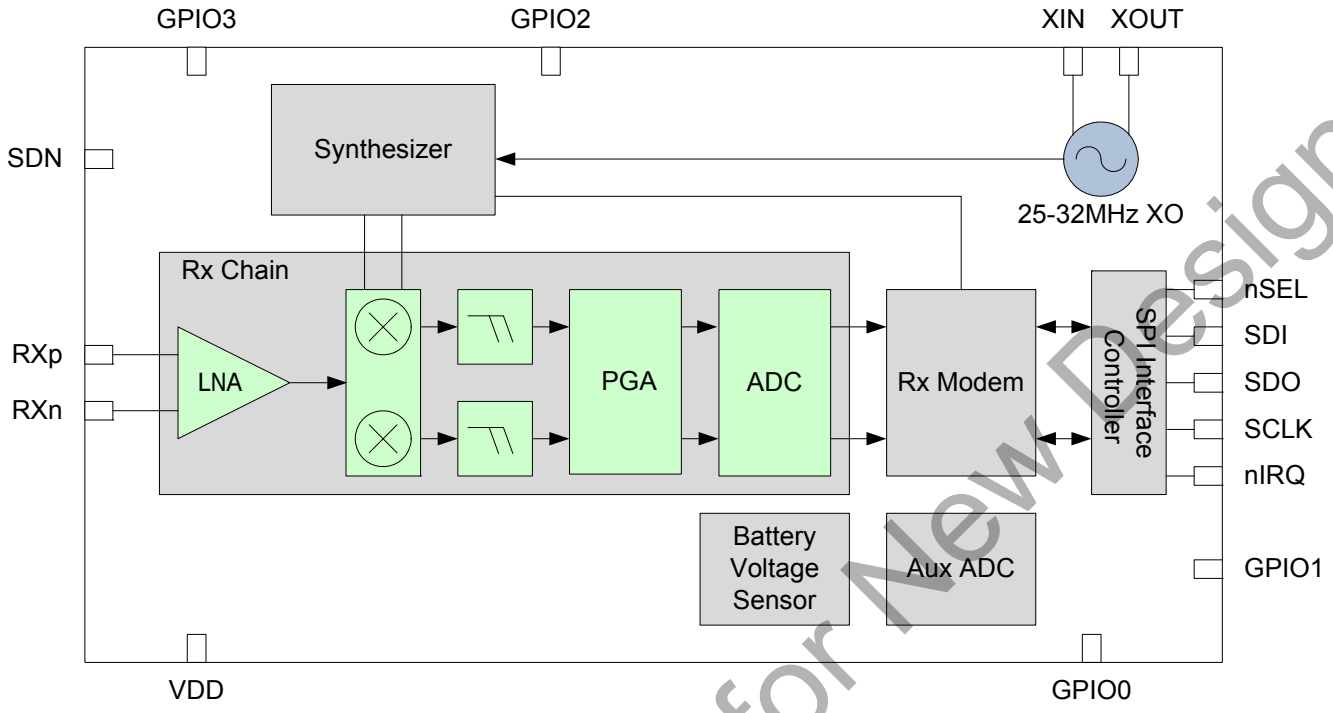


Figure 2. Si4355 Functional Block Diagram

3.1. Overview

The Si4355 is an easy-to-use, size efficient, low current wireless ISM receiver that covers the sub-GHz bands. The wide operating voltage range of 1.8–3.6 V and low current consumption make the Si4355 an ideal solution for battery powered applications. The Si4355 uses a single-conversion mixer to downconvert the FSK/GFSK or OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP, increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte Rx FIFO.

A high precision local oscillator (LO) is used and is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The Si4355 operates in the frequency bands of 283–350, 425–525, and 850–960 MHz.

Additional system features, such as 64 byte Rx FIFO, preamble detection, sync word detector and CRC, reduce overall current consumption, and allow for the use of lower-cost system MCUs. Power-on-reset (POR), and GPIOs further reduce overall system cost and size. The Si4355 is designed to work with an MCU, crystal, and a few passives to create a very compact and low-cost system.

3.2. Receiver Chain

The internal low-noise amplifier (LNA) is designed to be a wide-band LNA that can be matched with three external discrete components to cover any common range of frequencies in the sub-GHz band. The LNA has extremely low noise to suppress the noise of the following stages and achieve optimal sensitivity; so, no external gain or front-end modules are necessary. The LNA has gain control, which is controlled by the internal automatic gain control (AGC) algorithm. The LNA is followed by an I-Q mixer, filter, programmable gain amplifier (PGA), and ADC. The I-Q mixers downconvert the signal to an intermediate frequency. The PGA then boosts the gain to be within dynamic range of the ADC. The ADC rejects out-of-band blockers and converts the signal to the digital domain where filtering, demodulation, and processing is performed. Peak detectors are integrated at the output of the LNA and PGA for use in the AGC algorithm.

3.3. Receiver Modem

Using high-performance ADCs allows channel filtering, image rejection, and demodulation to be performed in the digital domain, which allows for flexibility in optimizing the device for particular applications. The digital modem performs the following functions:

- Channel selection filter
- Preamble detection
- Invalid preamble detection
- RX demodulation
- Automatic gain control (AGC)
- Automatic frequency compensation (AFC)
- Radio signal strength indicator (RSSI)
- Cyclic redundancy check (CRC)

The digital channel filter and demodulator are optimized for ultra-low-power consumption and are highly configurable. Supported modulation types are GFSK, FSK, and OOK. The channel filter can be configured to support bandwidths ranging from 850 kHz down to 40 kHz. A large variety of data rates are supported ranging from 500 kbps up to 500 kbps. The configurable preamble detector is used with the synchronous demodulator to improve the reliability of the sync-word detection. Preamble detection can be skipped using only sync detection, which is a valuable feature of the asynchronous demodulator when very short preambles are used. The received signal strength indicator (RSSI) provides a measure of the signal strength received on the tuned channel. The resolution of the RSSI is 0.5 dB. This high-resolution RSSI enables accurate channel power measurements for clear channel assessment (CCA), carrier sense (CS), and listen before talk (LBT) functionality. A wireless communication channel can be corrupted by noise and interference, so it is important to know if the received data is free of errors. A cyclic redundancy check (CRC) is used to detect the presence of erroneous bits in each packet. A CRC is computed and appended at the end of each transmitted packet and verified by the Si4355 receiver to confirm that no errors have occurred. The packet handler and CRC can significantly reduce the load on the system microcontroller allowing for a simpler and cheaper microcontroller. The default bandwidth-time product (BT) is 0.5 for all programmed data rates.

3.3.1. Received Signal Strength Indicator

The received signal strength indicator (RSSI) is an estimate of the signal strength in the channel to which the receiver is tuned. The RSSI measurement is done after the channel filter, so it is only a measurement of the desired or undesired in-band signal power. The Si4355 uses a fast response register to read RSSI and so can complete the read in 16 SPI clock cycles with no requirement to wait for CTS. The RSSI value is read using the RSSI_READ command. The RSSI value reported by this API command can be converted to dBm using the following equation:

$$RSSI_{dBm} = \frac{RSSI\_value}{2} - RSSI_{cal}$$

RSSIcal in this formula is dependent on the matching network, modem settings, and external LNA gain (if present). It can be obtained through lab measurements using a signal generator connected to the antenna input to provide a known RSSI level. Without an external LNA, the RSSIcal will be approximately 130.

3.4. Synthesizer

The Si4355 includes an integrated Sigma Delta ($\Delta\Sigma$) Fractional-N PLL synthesizer capable of operating over the bands from 283–350, 425–525, and 850–960 MHz. The synthesizer has many advantages; it provides flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The frequency resolution is (2/3)Freq_xo/(2^{19}) for 283–350 MHz, Freq_xo/(2^{19}) for 425–525 MHz, and Freq_xo/(2^{18}) for 850–960 MHz. The nominal reference frequency to the PLL is 30 MHz, but any XTAL frequency from 25 to 32 MHz may be used. The modem configuration calculator in WDS will automatically account for the XTAL frequency being used. The PLL utilizes a differential LC VCO with integrated on-chip inductors. The output of the VCO is followed by a configurable divider, which will divide the signal down to the desired output frequency band.

3.4.1. Synthesizer Frequency Control

The frequency is set by changing the integer and fractional settings to the synthesizer. The WDS calculator will automatically provide these settings, but the synthesizer equation is shown below for convenience. Initial frequency settings are configured in the EZConfig setup and can also be modified using the API commands: FREQ_CONTROL_INTE, FREQ_CONTROL_FRAC2, FREQ_CONTROL_FRAC1, and FREQ_CONTROL_FRAC0.

$$RF\_channel = \left(fc\_inte + \frac{fc\_frac}{2^{19}}\right) \times \frac{4 \times freq\_xo}{outdiv}(Hz)$$

Note: The fc_frac/2^{19} value in the above formula must be a number between 1 and 2. The LSB of fc_frac must be "1".

Table 9. Output Divider (Outdiv) Values

Outdiv	Lower (MHz)	Upper (MHz)
12	284	350
8	425	525
4	850	960

3.4.1.1. EZ Frequency Programming

EZ frequency programming allows for easily changing radio frequency using a single API command. The base frequency is first set using the EZConfig setup. This base frequency will correspond to channel 0. Next, a channel step size is also programmed within the EZConfig setup. The resulting frequency will be:

$$RF\ Frequency = Base\ Frequency + Channel \times Step\ Size$$

The second argument of the START_RX is CHANNEL, which sets the channel number for EZ frequency programming. For example, if the channel step size is set to 1 MHz, the base frequency is set to 900 MHz, and a CHANNEL number of 5 is programmed during the START_RX command, the resulting frequency will be 905 MHz. If no CHANNEL argument is written as part of the START_RX command, it will default to the previous value. The initial value of CHANNEL is 0 and so will be set to the base frequency if this argument is never used.

3.5. Crystal Oscillator

The Si4355 includes an integrated crystal oscillator with a fast start-up time of less than 250 µs. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the crystal. The default crystal is 30 MHz, but the circuit is designed to handle any XTAL from 25 to 32 MHz, set in the EZConfig setup. The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the GLOBAL_XO_TUNE API property. The total internal capacitance is 11 pF and is adjustable in 127 steps (70 fF/step). The crystal frequency adjustment can be used to compensate for crystal production tolerances. The frequency offset characteristics of the capacitor bank are demonstrated in Figure 3.

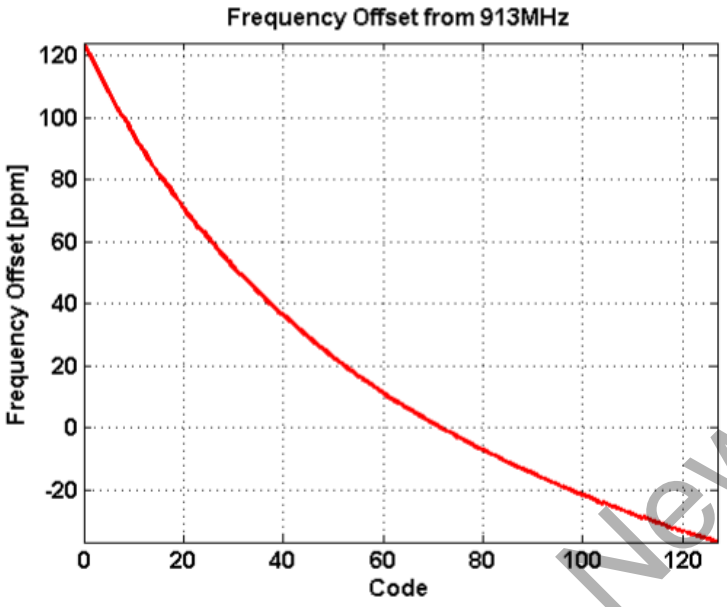


Figure 3. Capacitor Bank Frequency Offset Characteristics

3.6. Battery Voltage and Auxiliary ADC

The Si4355 contains an integrated auxiliary 11-bit ADC used for the internal battery voltage detector or an external component via GPIO. The Effective Number of Bits (ENOB) is 9 bits. When measuring external components, the input voltage range is 1 V, and the conversion rate is between 300 Hz to 2.44 kHz. The ADC value is read by first sending the GET_ADC_READING command and enabling the desired inputs. When the conversion is finished and all the data is ready, CTS will go high, and the data can be read out. Refer to application note, “AN691: EZRadio API Guide”, for details on this command and the formulas needed to interpret the results.

4. Configuration Options and User Interface

4.1. EZConfig GUI

The EZConfig Setup GUI is part of the Wireless Development Suite (WDS) program. This setup interface provides an easy path for quickly selecting and loading the desired configuration for the device. The EZConfig Setup allows for three different methods for device setup. One option is the configuration wizard, which easily identifies the optimal setup based on a few questions about the application. Another option is the configuration table, which provides a list of preloaded, common configurations. Lastly, EZConfig allows for custom configuration to be loaded using the radio configuration application. After the desired configuration is selected, the EZConfig setup automatically creates the configuration array that will be passed to the chip for setup. The program then gives the option to load a sample project with the selected configuration onto the evaluation board, or launch IDE with the new configuration array preloaded into the user program. For more complete information on EZConfig usage, refer to the application note, “AN692: Si4x55 Programming Guide & Sample Codes”.

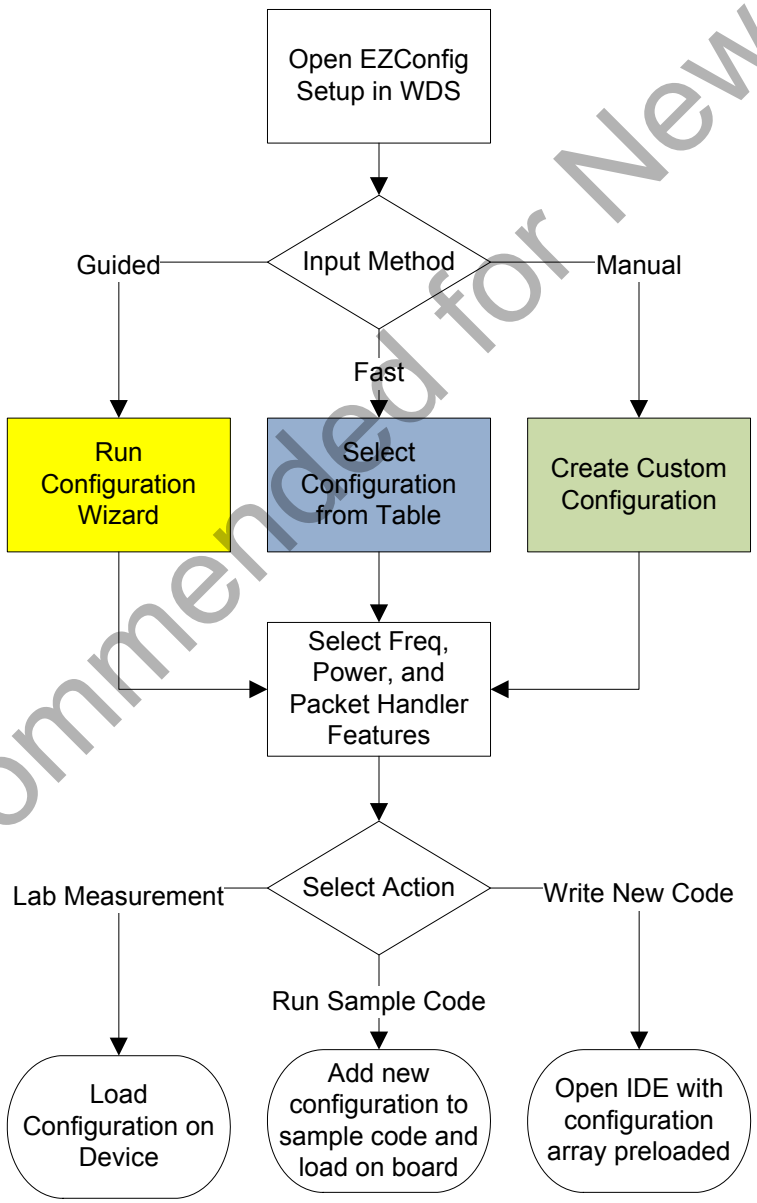


Figure 4. Device Configuration Steps

4.1.1. Configuration Wizard

The configuration wizard is available to easily identify the optimal device setup based on a few questions about the desired application. Within this wizard, the user is able to define their system requirements and can see some potential trade-offs for various settings. The wizard then provides a recommended configuration that is optimized for the given application. This configuration can be further modified if needed to provide the desired setup.

4.1.2. Configuration Table

The configuration table is a list of predefined configurations that have been optimized for performance and validated by Silicon Labs. These configurations are listed for many common application conditions and so most users will be able to find the configuration they need in this table. These configurations are set to provide optimized performance for a given application and can be implemented with low design risk. Once the list item is selected, the specific frequency, and packet handler features can also be applied.

4.1.3. Radio Configuration Application

The Radio Configuration Application provides an intuitive interface for directly modifying the device configuration. Using this control panel, the device parameters such as modulation type, data rate, and frequency deviation, can be set. The EZConfig Setup then takes these parameters and automatically determines the appropriate device register settings. This method allows the user to have complete flexibility in determining the configuration of the device without the need to translate the system requirements into device specific properties. As with the other EZConfig methods, the resulting configuration array is automatically generated and available for use in the user's program.

4.2. Configuration Options

4.2.1. Frequency Band

The Si4355 can operate in the 283–350 MHz, 425–525 MHz, or 850–960 MHz bands. One of these three bands will be selected during the configuration setup and then the specific receive frequency that will be used within this band can be selected.

4.2.2. Modulation Type

The Si4355 can operate using On/Off Keying (OOK), Frequency Shift Keying (FSK), or Gaussian Frequency Shift Keying (GFSK). OOK modulation is the most basic modulation type available. It is the most power efficient method and does not require as high oscillator accuracy as FSK. FSK provides the best sensitivity and, therefore, range performance but generally requires more precision from the oscillator used. GFSK is a version of FSK where the signal is passed through a Gaussian filter, limiting its spectral width. As a result, the out of band components of the signal are reduced.

The Si4355 also has an option for Manchester coding. This method provides a state transition at each bit and so allows for more reliable clock recovery.

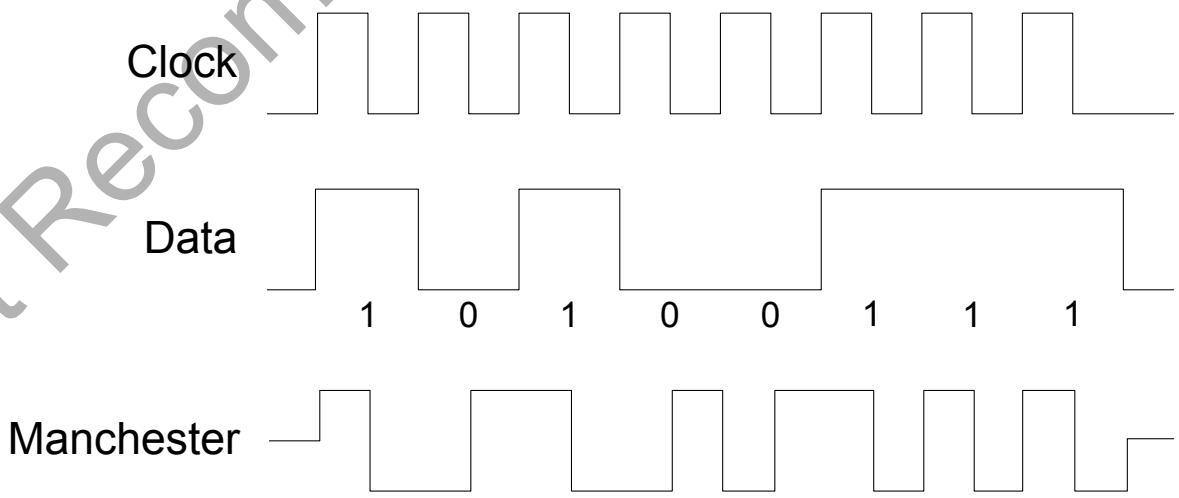


Figure 5. Manchester Code Example

4.2.3. Frequency Deviation

If FSK or GFSK modulation is selected, then a frequency deviation will also need to be selected. The frequency deviation is the maximum instantaneous difference between the FM modulated frequency and the nominal carrier frequency. The Si4455 can operate across a wide range of data rates and frequency deviations. If a frequency deviation needs to be selected, the following guideline might be helpful to build a robust link. A proper frequency deviation is linked to the frequency error between transmitter and receiver. The frequency error can be calculated using the crystal tolerance parameters and the RF operating frequency: (ppm_tx+ppm_rx)*Frf/1E-6. For frequency errors below 50 kHz, the deviation can be about the same as the frequency error. For frequency errors exceeding 50 kHz the frequency deviation can be set to about 0.75 times the frequency error. It is advised to position the modulation index (=2*freq_dev/data_rate) into a range between 1 and 100 for Packet Handling mode and 2 to 100 for direct mode (non-standard preamble). For example, when in Packet Handling mode and the frequency error is smaller than data_rate/2, the frequency deviation is set to about data_rate/2. When the frequency error exceeds 100xdata_rate/2, the frequency deviation is preferred to be set to 100xdata_rate/2.

4.2.4. Data Rate

The Si4355 can be set to communicate at between 1 to 500 kbps in (G)FSK mode and between 0.5 to 120 kbps in OOK mode. Higher data rates allow for faster data transfer while lower data rates result in improved sensitivity and range performance.

4.2.5. Channel Bandwidth

The channel bandwidth sets the bandwidth for the receiver. Since the receiver bandwidth is directly proportional to the noise allowed in the system, this will normally be set as low as possible. The specific channel bandwidth used will usually be determined based upon the precision of the oscillator and the frequency deviation of the transmitted signal. The EZConfig setup can provide the recommended channel bandwidth based upon these two parameters to help optimize the system.

4.2.6. Preamble Length

A preamble is a defined simple bit sequence used to notify the receiver that a data transmission is imminent. The length of this preamble will normally be set as short as possible to minimize power while still insuring that it will be reliably detected given the receiver characteristics, such as duty cycling and packet error rate performance. The Si4355 allows the preamble length to be set between 3 to 255 bytes in length with a default length of 4 bytes. The preamble pattern for the Si4355 will always be 55h with a first bit of "0" if the packet handler capability is used.

4.2.7. Sync Word Length and Pattern

The sync word follows the preamble in the packet structure and is used to identify the start of the payload data and to synchronize the receiver to the transmitted bit stream. The Si4355 allows for sync word lengths of 1 to 4 bytes and the specific pattern can be set within the EZConfig program. The default is a 2 byte length 2d d4 pattern.

4.2.8. Cyclic Redundancy Check (CRC)

CRC is used to verify that no errors have occurred during transmission and the received packet has exactly the same data as it did when transmitted. If this function is enabled in the Si4355, the last byte of transmitted data must include the CRC generated by the transmitter. The Si4355 then performs a CRC calculation on the received packet and compares that to the transmitted CRC. If these two values are the same, the Si4355 will set an interrupt indicating a valid packet has been received and is waiting in the Rx FIFO. If these two CRC values differ, the Si4355 will flag an interrupt indicating that a packet error occurred. The Si4355 uses CRC(16)-IBM: x16+x15+x2+1 with a seed of 0xFFFF.

4.3. Configuration Commands

The EZConfig Setup provides all of the code needed for basic radio configuration. Once the setup is completed in the GUI, the program outputs configuration array(s) that can be sent to the radio via the SPI interface. No additional setup coding is needed. The configuration command process is shown in Figure 6. The EZCONFIG_SETUP passes the configuration array to the device and the EZCONFIG_CHECK insures that all of the configuration data was written correctly. For more information on the setup commands, refer to application note, “AN691: EZRadio API Guide”.

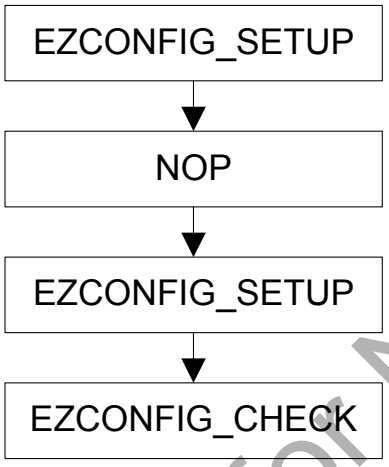


Figure 6. Configuration Command Flowchart

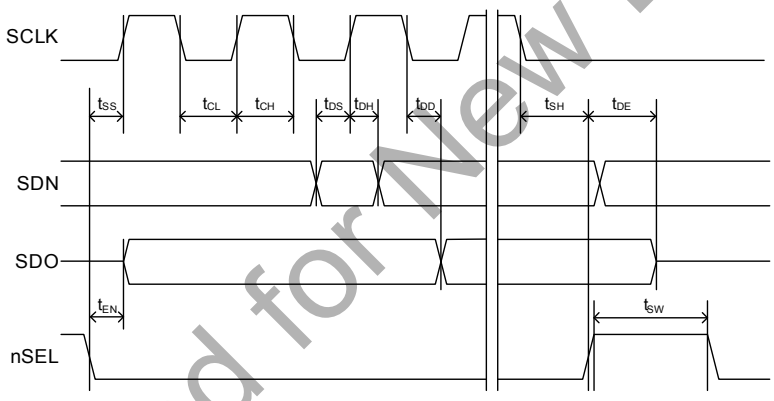
5. Controller Interface

5.1. Serial Peripheral Interface (SPI)

The Si4355 communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI, SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are listed in Table 10. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 7 shows an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the API commands followed by n bytes of parameter data, which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 10. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	



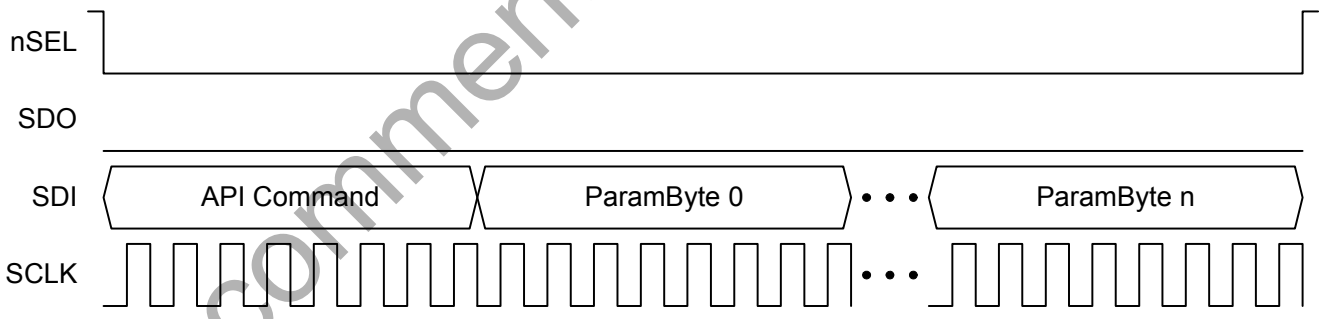


Figure 7. SPI Write Command

The Si4355 contains an internal MCU which controls all the internal functions of the radio. For SPI read commands, a typical communication flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 8 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh, the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 9 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

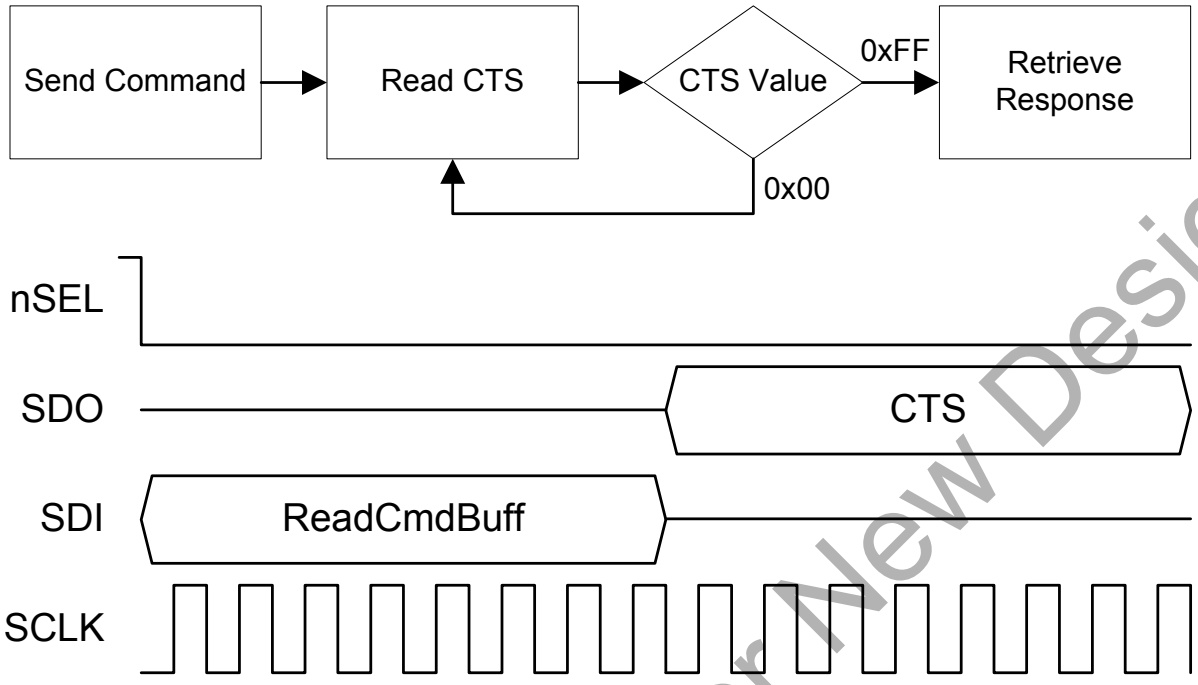


Figure 8. SPI Read Command—Check CTS Value

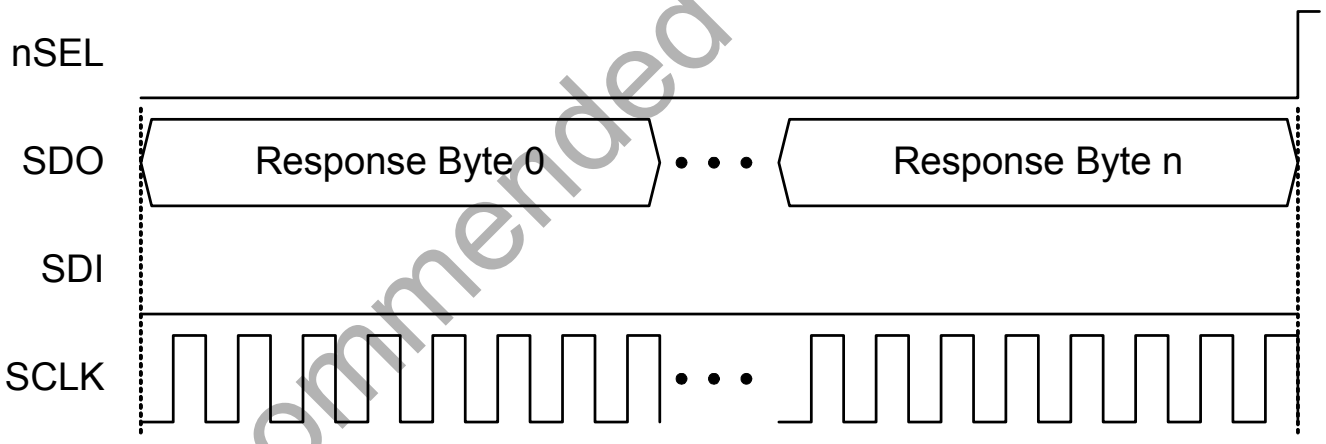


Figure 9. SPI Read Command—Clock Out Read Data

5.2. Operating Modes and Timing

The primary states of the Si4355 are shown in Figure 10. The shutdown state completely shuts down the radio, minimizing current consumption and is controlled using the SDN (pin 2). All other states are controlled using the API commands START_RX and CHANGE_STATE. Table 11 shows each of the operating modes with the time required to reach either RX state as well as the current consumption of each state. The times in Table 11 are measured from the rising edge of nSEL until the chip is in the desired state. This information is included for reference only since an automatic sequencer moves the chip from one state to another and so it is not necessary to manually step through each state. Most applications will utilize the standby mode since this provides the fastest transition response time, maintains all register values, and results in nearly the same current consumption as shutdown.

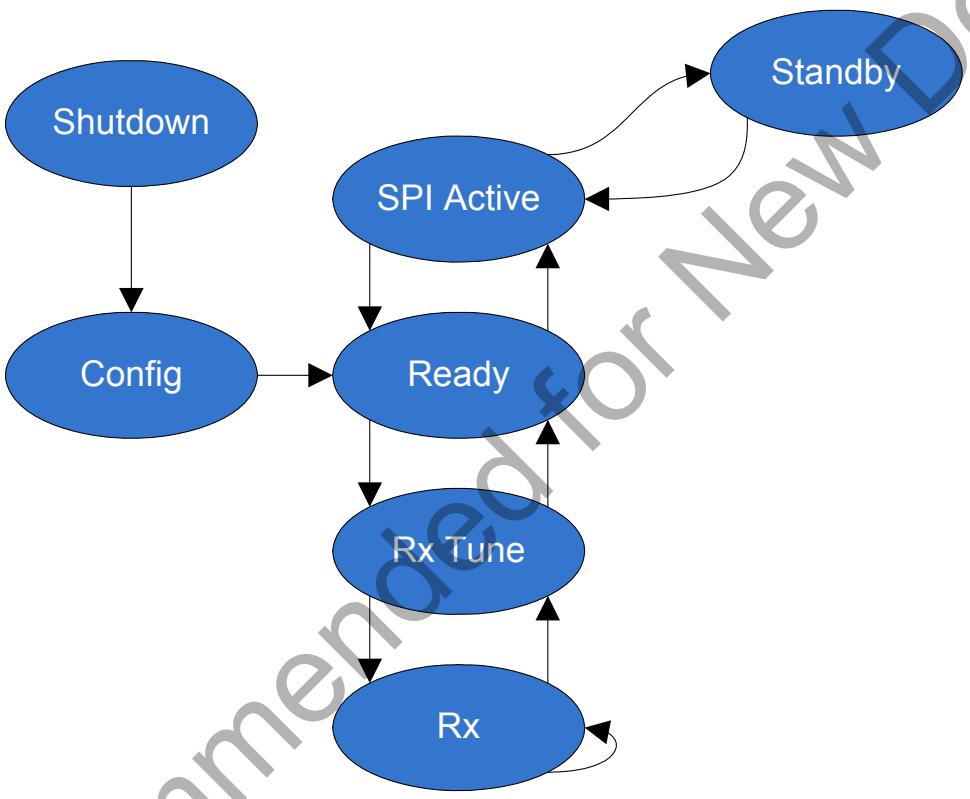


Figure 10. State Machine Diagram

Table 11. Operating State Response Time and Current Consumption

State / Mode	Response Time to Rx	Current in State / Mode
Shutdown	30 ms	30 nA
Standby	460 µs	50 nA
SPI Active	330 µs	1.35 mA
Ready	130 µs	1.8 mA
Rx Tune	75 µs	6.5 mA
Rx	150 µs	10 mA

5.2.1. Shutdown State

The shutdown state is the lowest current consumption state of the device and is entered by driving SDN (Pin 2) high. In this state, all register contents are lost and there is no SPI access. To exit this mode, drive SDN low. The device will then initiate a power on reset (POR) along with internal calibrations. Once this POR period is complete, the POWER_UP command is required to initialize the radio and the configuration can then be loaded into the device. The SDN pin must be held high for at least 10 µs before driving it low again to insure the POR can be executed correctly. The shutdown state can be used to fully reset the part.

5.2.2. Standby State

The standby state has similar current consumption to the shutdown state but retains all register values, allowing for a much faster response time. Because of these benefits, most applications will want to use standby mode rather than shutdown. The standby state is entered by using the CHANGE_STATE API command. While in this state, the SPI is accessible but any SPI event will automatically transition the chip to the SPI active state. After the SPI event, the host will need to re-command the device to standby mode.

5.2.3. SPI Active State

The SPI active state enables the device to process any SPI events, such as API commands. In this state, the SPI and boot up oscillator are enabled. The SPI active state is entered by using the CHANGE_STATE command or automatically through an SPI event while in standby mode. If the SPI active state was entered automatically from standby mode, a CHANGE_STATE command will be needed to return the device to standby mode.

5.2.4. Ready State

Ready state is designed to give a fast transition time to RX state with minimized current consumption. In this mode the crystal oscillator remains enabled to minimize the transition time. Ready state can be entered using the CHANGE_STATE command.

5.2.5. Power On Reset

A Power On Reset (POR) sequence is used to boot the device up from a fully off or shutdown state. To execute this process, VDD must ramp within 1ms and must remain applied to the device for at least 10ms. If VDD is removed, then it must stay below 0.15V for at least 10ms before being applied again. Please see Figure x and Table x for details.

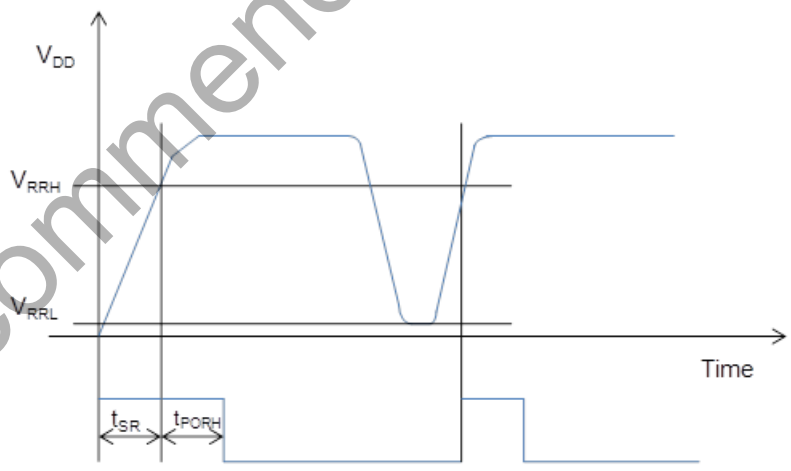


Figure 11. POR Timing Diagram

Table 12. POR Timing

Variable	Description	Min	Typ	Max	Units
t_{PORH}	High time for VDD to fully settle POR circuit.	10			ms
t_{PORL}	Low time for VDD to enable POR.	10			ms
V_{RRH}	Voltage for successful POR.	90%*Vdd			V
V_{RRL}	Starting Voltage for successful POR.	0		150	mV
t_{SR}	Slew rate of VDD for successful POR.			1	ms

5.2.6. RX State

The RX state is used whenever the device is required to receive data. It is entered using either the START_RX or CHANGE_STATE commands. With the START_RX command, the next state can be defined to insure optimal timing. When either command is sent to enter RX state, an internal sequencer automatically takes care of all actions required to move between states with no additional user commands needed. The sequencer controlled events can include enable the digital and analog LDOs, start up the crystal oscillator, enable PLL, calibrate VCO, enable receiver circuits, and enable receive mode. The device will also automatically set up all receiver features such as packet handling based upon the initial configuration of the device.

5.3. Application Programming Interface

An Application Programming Interface (API) is embedded inside the device and is used for communications with the host MCU. API commands are used to configure the device, control the chip during operation, and retrieve its status. Available commands are shown in Table 13. The complete list of commands and their descriptions are provided in application note, “AN691: EZRadio API Guide”.

Table 13. API Commands

#	Name	Description
0x00	NOP	No operation command
0x01	PART_INFO	Reports basic information about the device
0x02	POWER_UP	Boot options and crystal frequency offset
0x10	FUNC_INFO	Returns the function revision information of the device
0x11	SET_PROPERTY	Sets the value of a property
0x12	GET_PROPERTY	Retrieves the value of a property
0x13	GPIO_PIN_CFG	Configures the GPIO pins
0x14	GET_ADC_READING	Performs and retrieves ADC conversion results
0x15	FIFO_INFO	Provides access to the RX FIFO counts and reset
0x19	EZCONFIG_CHECK	Validates the EZConfig array was written correctly
0x20	GET_INT_STATUS	Returns the interrupt status byte
0x32	START_RX	Switches to RX state
0x33	REQUEST_DEVICE_STATE	Request current device state
0x34	CHANGE_STATE	Changes to a specified device state / mode
0x44	READ_CMD_BUFF	Used to read CTS and the command response
0x50	CHIP_STATUS_INT_PEND_READ	CHIP_STATUS_INT_PEND fast response register
0x51	MODEM_INT_PEND_READ	MODEM_INT_PEND fast response register
0x53	PH_INT_PEND_READ	PH_INT_PEND fast response register
0x57	RSSI_READ	RSSI fast response register
0x66	EZCONFIG_SETUP	Configures device using EZConfig array
0x77	READ_RX_FIFO	Reads the RX FIFO

5.4. Interrupts

The Si4355 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Registers. The nIRQ output signal will then be reset until the next change in status is detected.

The interrupt sources are grouped into three categories: packet handler, chip status, and modem. The individual interrupts in these groups can be enabled/disabled in the interrupt property registers, 0x0101, 0x0102, and 0x0103. An interrupt must be enabled for it to trigger an event on the nIRQ pin. The interrupt group must be enabled as well as the individual interrupts in API property 0x0100.

Once an interrupt event occurs and the nIRQ pin is low the interrupts are read and cleared using the GET_INT_STATUS command. By default all interrupts will be cleared once read. The instantaneous status of a specific function may be read if the specific interrupt is enabled or disabled. The status results are provided after the interrupts and can be read with the same commands as the interrupts. The status bits will give the current state of the function whether the interrupt is enabled or not.

5.5. GPIO

Four General Purpose IO (GPIO) pins are available for use in the application. The GPIOs are configured using the GPIO_PIN_CFG command. GPIO pins 0 and 1 should be used for active signals such as data or clock. GPIO pins 2 and 3 have more susceptibility to generating spurious components in the synthesizer than pins 0 and 1. The drive strength of the GPIOs can be adjusted with the GEN_CONFIG parameter in the GPIO_PIN_CFG command. By default, the drive strength is set to the minimum. The default configuration and the state of the GPIO during shutdown are shown in Table 14. For a complete list of the GPIO options, please refer to the API guide application note, “AN691: EZRadio API Guide”.

Table 14. GPIOs

Pin	SDN State	POR Default
GPIO0	0	POR
GPIO1	0	CTS
GPIO2	0	POR
GPIO3	0	POR
nIRQ	Resistive V_{DD} pull-up	nIRQ
SDO	Resistive V_{DD} pull-up	SDO
SDI	High Z	SDI

6. Data Handling and Packet Handler

6.1. RX FIFO

A 64-byte RX FIFO is integrated into the chip. Reading from command register 77h reads data from this RX FIFO.

6.2. Packet Handler

The Si4355 includes integrated packet handler features such as preamble and sync word detection as well as CRC calculation. This allows the chip to qualify and synchronize with legitimate transmissions independent of the microcontroller. These features can be enabled using the EZConfig setup. In this setup, the preamble and sync word length can be modified and the sync word pattern can be selected. The general packet structure is shown in Figure 12.

There is also the option within the EZConfig setup to select a variable packet length. With this setting, the receiver is not required to know the packet length ahead of time. The transmitter sends the length of the packet immediately after the sync word. The packet structure for variable length packets is shown in Figure 13.

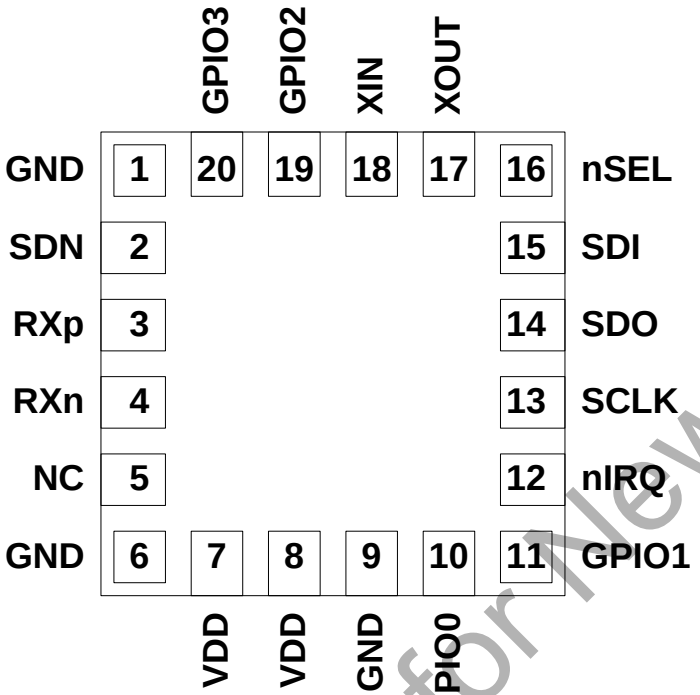
Preamble	Sync Word	Data	CRC
0 – 255 Bytes	1 – 4 Bytes	1 – 64 Bytes	2 Bytes

Figure 12. Packet Structure for Fixed Packet Length

Preamble	Sync Word	Length	Data	CRC
0 – 255 Bytes	1 – 4 Bytes	1 Byte	1 – 64 Bytes	2 Bytes

Figure 13. Packet Structure for Variable Packet Length

7. Pin Descriptions



Pin	Pin Name	I/O	Description
1	GND	GND	Ground
2	SDN	I	Shutdown (0 – V_{DD} V) – SDN = 1, part will be in shutdown mode and contents of all registers are lost. SDN = 0, all other modes.
3	RXp	I	Differential RF receiver input pin
4	RXn	I	Differential RF receiver input pin
5	NC	—	No Connect
6	GND	GND	Ground
7	V_{DD}	V_{DD}	Supply voltage
8	V_{DD}	V_{DD}	Supply voltage
9	GND	GND	Ground
10	GPIO0	I/O	General Purpose Digital I/O
11	GPIO1	I/O	General Purpose Digital I/O
12	nIRQ	O	Interrupt Status Output – nIRQ = 0, interrupt event has occurred. Read interrupt status for event details.
13	SCLK	I	Serial Clock Input (0 – V_{DD} V)—Provides serial data clock for 4-line serial data bus.
14	SDO	O	Serial Data Output (0 – V_{DD} V)— Provides serial data readback function of internal control registers.
15	SDI	I	Serial Data Input (0 – V_{DD} V)—Serial data stream input for 4-line serial data bus

Pin	Pin Name	I/O	Description
16	nSEL	I	Serial Interface Select Input (0 – V_{DD} V) – Provides select/enable function for 4-line serial data bus
17	XOUT	O	Crystal Oscillator Output
18	XIN	I	Crystal Oscillator Input—No DC bias required, but if used, should be set to 7 V.
19	GPIO2	I/O	General Purpose Digital I/O
20	GPIO3	I/O	General Purpose Digital I/O

8. Ordering Information

Part Number*	Description	Package Type	Operating Temperature
Si4355-B1A-FM	EZRadio Receiver	3x3 QFN-20 Pb-free	–40 to 85 °C
***Note:** Add an “R” at the end of the device part number to denote tape and reel option.			

9. Package Outline

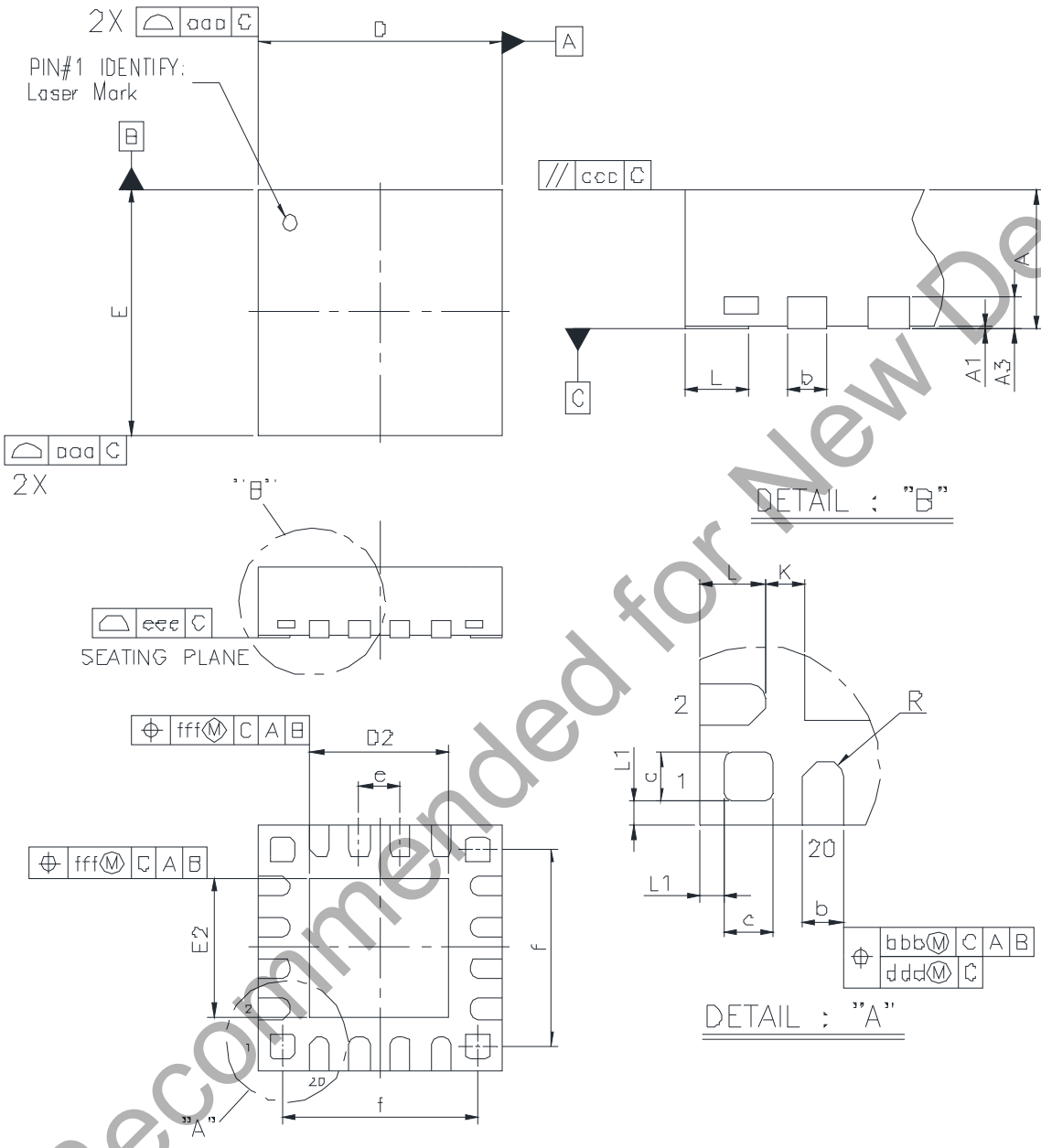


Figure 14. 20-pin QFN Package

Table 15. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D		3.00 BSC.	
D2	1.55	1.70	1.85
e		0.50 BSC.	
E		3.00 BSC.	
E2	1.55	1.70	1.85
f		2.40 BSC.	
L	0.30	0.40	0.50
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note: All dimensions shown are in millimeters (mm) unless otherwise noted.

10. PCB Land Pattern

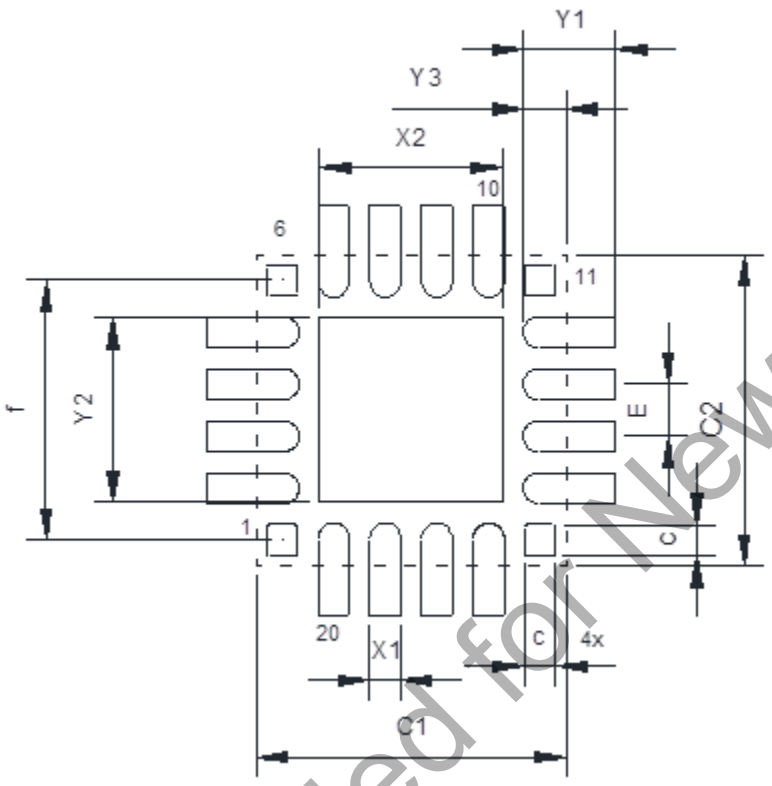


Figure 15. 20-pin QFN PCB Land Pattern

Table 16. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.00	
C2	3.00	
E	0.50 REF	
X1	0.25	0.35
X2	1.65	1.75
Y1	0.85	0.95
Y2	1.65	1.75
Y3	0.37	0.47
f	2.40 REF	
c	0.25	0.35

Note: : All dimensions shown are in millimeters (mm) unless otherwise noted.

11. Top Marking

11.1. Si4355 Top Marking

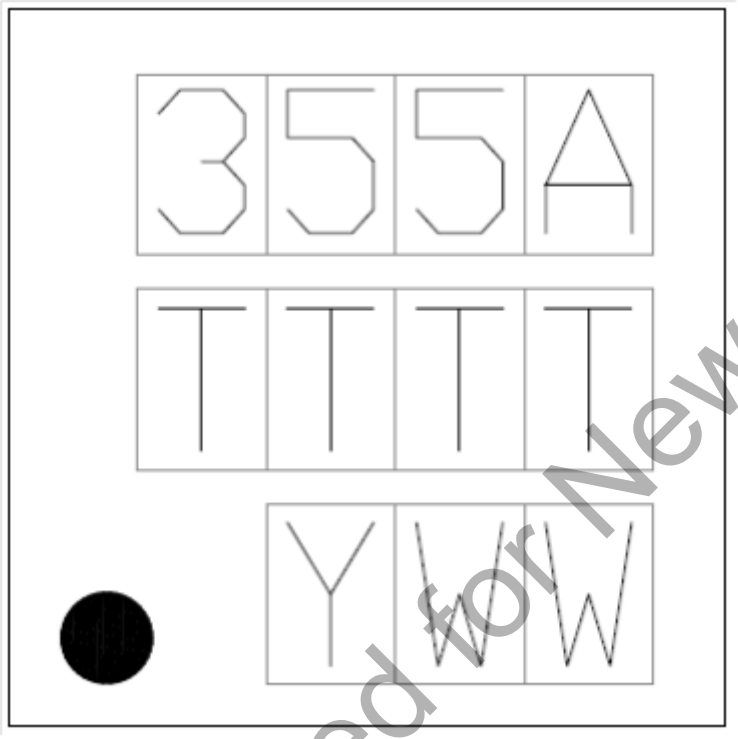


Figure 16. Si4355 Top Marking

11.2. Top Marking Explanation

Mark Method:	Laser	
Line 1 Marking:	Part Number	4355A
	Firmware Revision	
Line 2 Marking:	Die Revision	Internal tracking number
	TTTT = Trace Code	
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and work week of the mold date.

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