THE DATASHEET OF

DAC7678SPWR

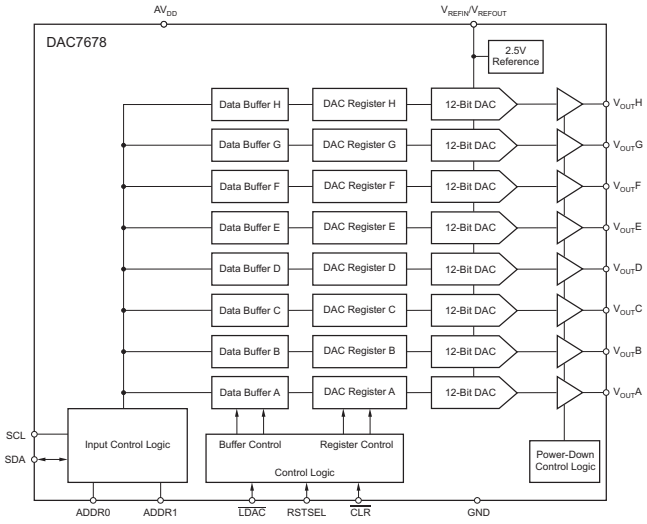
www.win-source.net 0086-755-83957316

12-Bit, Octal-Channel, Ultra-Low Glitch, Voltage Output, Two-Wire Interface Digital-to-Analog Converter with 2.5V Internal Reference

Check for Samples: DAC7678

FEATURES

- **Relative Accuracy:**
  - **1 LSB INL**
- **Glitch Energy: 0.15nV-s**
- **Internal Reference:**
  - **2.5V Reference Voltage (disabled by default)**
  - **±5mV Initial Accuracy (max)**
  - **5ppm/°C Temperature Drift (typ)**
  - **25ppm/°C Temperature Drift (max)**
  - **20mA Sink/Source Capability**
- **Power-On Reset to Zero Scale or Midscale**
  - **Devices in the TSSOP Package Reset to Zero Scale**
  - **Devices in the QFN Package Reset to Zero Scale or Midscale**
- **Ultra-Low Power Operation: 0.13mA/Channel at 5V (without internal reference current)**
- **Wide Power-Supply Range: +2.7V to +5.5V**
- **2-Wire Serial Interface (I^2C™ compatible)**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Temperature Range: –40°C to +125°C**



APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control**
- **Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**

DESCRIPTION

The DAC7678 is a low-power, voltage-output, octal channel, 12-bit digital-to-analog converter (DAC). The DAC7678 includes a 2.5V internal reference (disabled by default), giving a full-scale output voltage range of 5V. The internal reference has an initial accuracy of ±5mV and can source up to 20mA at the V_{REFIN}/V_{REFOUT} pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch).

The DAC7678 uses a versatile, 2-wire serial interface that is I^2C-compatible and operates at clock rates of up to 3.4MHz. Multiple devices can share the same bus.

The DAC7678 incorporates a power-on-reset circuit that ensures the DAC output powers up to either zero-scale or mid-scale until a valid code is written to the device. These devices contain a power-down feature, accessed over the serial interface that reduces the current consumption of the device to typically 0.42µA at 5V. Power consumption (including internal reference) is typically 3.56mW at 3V, reducing to 0.68µW in power-down mode. The low power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment. The DAC7678 is drop-in and functionally compatible with DAC5578, DAC6578, and DAC7578. All devices are available in a 4x4 QFN-24 package and a TSSOP-16 package.

RELATED DEVICES	8-BIT	10-BIT	12-BIT
Pin- and Function-Compatible (w/internal reference)	—	—	DAC7678
Pin- and Function-Compatible	DAC5578	DAC6578	DAC7578

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC7678	±1	±0.25	25	TSSOP-16	PW	–40°C to +125°C	DAC7678
				QFN-24	RGE		

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	DAC7678	UNIT
AV_{DD} to GND	–0.3 to +6	V
Digital input voltage to GND	–0.3 to +AV_{DD} + 0.3	V
V_{OUT} to GND	–0.3 to +AV_{DD} + 0.3	V
V_{REFIN}/V_{REFOUT} to GND	–0.3 to +AV_{DD} + 0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature range (T_J max)	+150	°C
Power dissipation	(T_J max – T_A)/θ_{JA}	W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		DAC7678		UNITS
		PW (16 PINS)	RGE (24 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	111.9	33.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.3	16.9	
θ_{JB}	Junction-to-board thermal resistance	52.4	7.4	
ψ_{JT}	Junction-to-top characterization parameter	2	0.5	
ψ_{JB}	Junction-to-board characterization parameter	51.2	7.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7V to 5.5V, External Reference Used, and over –40°C to +125°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7678			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE(1)					
Resolution		12			Bits
Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.3	±1	LSB
Differential nonlinearity	12-bit monotonic		±0.1	±0.25	LSB
Offset error	Extrapolated from two-point line(2), unloaded		0.5	±4	mV
Offset error drift			3		µV/°C
Full-scale error	DAC register loaded with all '1's		±0.03	±0.2	% of FSR
Full-scale error drift			2		µV/°C
Zero-code error	DAC register loaded with all '0's		1	4	mV
Zero-code error drift			2		µV/°C
Gain error	Extrapolated from two-point line(2), unloaded		±0.01	±0.15	% of FSR
Gain temperature coefficient			±1		ppm of FSR/°C
OUTPUT CHARACTERISTICS(3)					
Output voltage range		0		AV_{DD}	V
Output voltage settling time	DACs unloaded, 1/4 scale to 3/4 scale		7		µs
	R_L = 1MΩ, C_L = 470 pF		12		µs
Slew rate			0.75		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		pF
Code change glitch impulse	1LSB change around major carry		0.15		nV-s
Digital feedthrough	SCL toggling		1.5		nV-s
Power-on glitch	R_L = ∞		3		mV
Channel-to-channel dc crosstalk	Full-scale swing on adjacent channel		0.1		LSB
DC output impedance	At midscale input		4.5		Ω
Short-circuit current	DAC outputs shorted to GND		25		mA
Power-up time (including settling time)	Coming out of power-down mode, AV_{DD} = 5V		50		µs
AC PERFORMANCE(3)					
DAC output noise density	T_A = +25°C, at zero-code input, f_{OUT} = 1kHz		20		nV/√Hz
DAC output noise	T_A = +25°C, at midscale input, 0.1Hz to 10Hz (external reference used)		3		$µV_{PP}$

(1) Linearity calculated using a reduced code range; output unloaded.
(2) 12-bit: 30 and 4050
(3) Specified by design or characterization; not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = 2.7V to 5.5V, External Reference Used, and over –40°C to +125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC7678			UNIT
			MIN	TYP	MAX	
INTERNAL REFERENCE						
Output voltage		T_A = +25°C	2.495	2.5	2.505	V
Initial accuracy		T_A = +25°C	–5	±0.1	5	mV
Output voltage temperature drift(4)				5	25	ppm/°C
Output voltage noise		T_A = +25°C, f = 0.1Hz to 10Hz		15		μV_{PP}
Output voltage noise density (high-frequency noise)		T_A = +25°C, f = 1kHz, C_L = 0µF		250		nV/√Hz
		T_A = +25°C, f = 1MHz, C_L = 0µF		50		
Load regulation(5)		Sourcing, T_A = +25°C		500		µV/mA
		Sinking, T_A = +25°C		200		µV/mA
Output current load capability(4)				±20		mA
Line regulation		T_A = +25°C		80		µV/V
Long-term stability/drift (aging)(5)		T_A = +25°C, time = 0 to 2160 hours		100		ppm
Thermal hysteresis(5)		First cycle		200		ppm
		Additional cycles		50		ppm
Internal reference current consumption		AV_{DD} = 5.5V		420		µA
		AV_{DD} = 3.6V		400		µA
External reference current		External V_{REF} = 2.5V (when internal reference is disabled), all eight channels active		60		µA
V_{REFIN}/V_{REFOUT} pin reference input range			0		AV_{DD}	V
Reference input impedance		Reference disabled		42		kΩ
LOGIC INPUTS(4)						
Input current				±1		µA
$V_{IN}L$	Logic input LOW voltage	2.7V ≤ AV_{DD} ≤ 5.5V	GND–0.3		0.3×AV_{DD}	V
$V_{IN}H$	Logic input HIGH voltage	2.7V ≤ AV_{DD} ≤ 5.5V	0.7×AV_{DD}		AV_{DD}+0.3	V
Pin capacitance				1.5	3	pF
POWER REQUIREMENTS						
AV_{DD}			2.7		5.5	V
I_{DD} (6)	Normal mode, internal reference switched off	AV_{DD} = 3.6V to 5.5V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		1.02	1.4	mA
		AV_{DD} = 2.7V to 3.6V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.86	1.3	mA
	Normal mode, internal reference switched on	AV_{DD} = 3.6V to 5.5V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		1.49	2.2	mA
		AV_{DD} = 2.7V to 3.6V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		1.32	2	mA
	All power-down modes	AV_{DD} = 3.6V to 5.5V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.42	6	µA
		AV_{DD} = 2.7V to 3.6V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.25	4.7	µA
Power dissipation(6)	Normal mode, internal reference switched off	AV_{DD} = 3.6V to 5.5V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		3.67	7.7	mW
		AV_{DD} = 2.7V to 3.6V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		2.32	4.68	mW
	Normal mode, internal reference switched on	AV_{DD} = 3.6V to 5.5V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		5.36	12.1	mW
		AV_{DD} = 2.7V to 3.6V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		3.56	7.2	mW
	All power-down modes	AV_{DD} = 3.6V to 5.5V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		1.51	33	µW
		AV_{DD} = 2.7V to 3.6V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.68	16.92	µW
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(4) Specified by design or characterization; not production tested.
(5) Explained in more detail in the *Application Information* section of this data sheet.
(6) Input code = midscale, no load.

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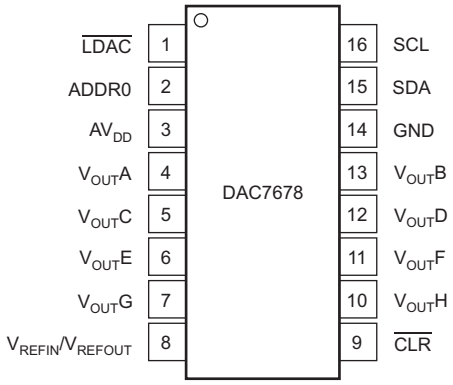
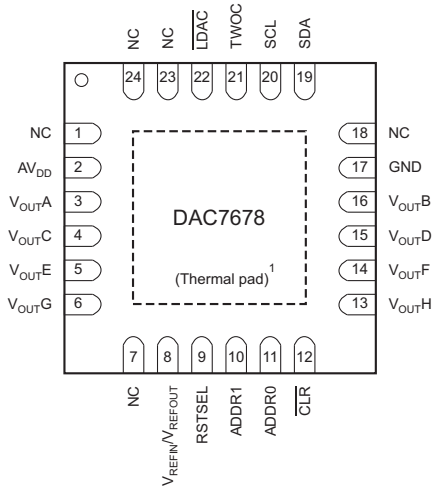
PIN CONFIGURATIONS

PW PACKAGE
TSSOP-16
(TOP VIEW)



RGE PACKAGE
QFN-24
(TOP VIEW)



(1) It is recommended to connect the thermal pad to GND for better thermal dissipation.

PIN DESCRIPTIONS

16-PIN	24-PIN	NAME	DESCRIPTION
1	22	$\overline{\text{LDAC}}$	Load DACs.
2	11	ADDR0	Three-state address input 0
3	2	AV_{DD}	Power-supply input, 2.7V to 5.5V
4	3	$V_{OUT}A$	Analog output voltage from DAC A
5	4	$V_{OUT}C$	Analog output voltage from DAC C
6	5	$V_{OUT}E$	Analog output voltage from DAC E
7	6	$V_{OUT}G$	Analog output voltage from DAC G
8	8	V_{REFIN}/ V_{REFOUT}	Positive reference input or reference output of 2.5V, if internal reference used.
9	12	$\overline{\text{CLR}}$	Asynchronous clear input
10	13	$V_{OUT}H$	Analog output voltage from DAC H
11	14	$V_{OUT}F$	Analog output voltage from DAC F
12	15	$V_{OUT}D$	Analog output voltage from DAC D
13	16	$V_{OUT}B$	Analog output voltage from DAC B
14	17	GND	Ground reference point for all circuitry on the device
15	19	SDA	Serial data input. Data are clocked into or out of the input register. This pin is a bidirectional, open-drain data line that should be connected to the supply voltage with an external pull-up resistor.
16	20	SCL	Serial clock input. Data can be transferred at rates up to 3.4MHz. Schmitt-trigger logic input.
—	1	NC	Not internally connected.
—	7	NC	Not internally connected.
—	9	RSTSEL	Reset select pin. RSTSEL high resets device to mid-scale; RSTSEL low resets device to zero-scale.
—	10	ADDR1	Three-state address input 1
—	18	NC	Not internally connected.
—	21	TWOC	Twos complement select. If the TWOC pin is pulled high, the DAC registers use twos complement format; if TWOC is pulled low, the DAC registers use straight binary format.
—	23	NC	Not internally connected.
—	24	NC	Not internally connected.

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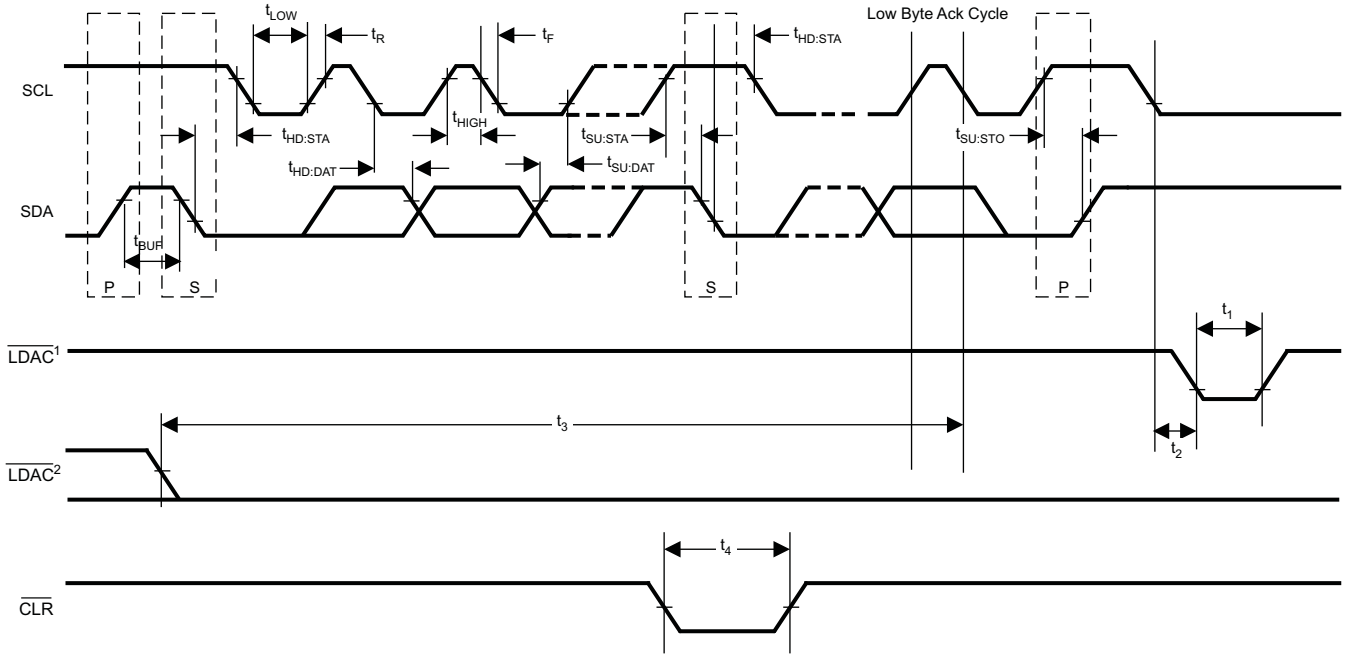
TIMING DIAGRAM



(1) Asynchronous LDAC update mode. For more information and details, see the LDAC Functionality section

(2) Synchronous LDAC update mode. For more information and details, see the LDAC Functionality section

Figure 1. Serial Write Operation

TIMING REQUIREMENTS

At AV_{DD} = 2.7 V to 5.5 V and –40°C to +125°C range (unless otherwise noted).

PARAMETER	STANDARD MODE		FAST MODE		HIGH SPEED MODE		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
SCL frequency, f_{SCL}		0.1		0.4		3.4	MHz
Bus free time between STOP and START conditions, t_{BUF}	4.7		1.3				µs
Hold time after repeated start, t_{HDSTA}	4		0.6		0.16		µs
Repeated Start setup time, t_{SUSTA}	4.7		0.6		0.16		µs
STOP condition setup time, t_{SUSTO}	4		0.6		0.16		µs
Data hold time, t_{HDDAT}	0		0		0		ns
Data setup time, t_{SUDAT}	250		100		10		ns
SCL clock LOW period, t_{LOW}	4700		1300		160		ns
SCL clock HIGH period, t_{HIGH}	4000		600		60		ns
Clock/Data fall time, t_F		300		300		160	ns
Clock/Data rise time, t_R		1000		300		160	ns
LDAC pulse width LOW time, t_1	40		10		1.2		µs
SCL falling edge to LDAC falling edge for asynchronous LDAC update, t_2	20		5		0.6		µs
LDAC falling edge to SCL falling edge for synchronous LDAC update, t_3	360		90		10.5		µs
CLR pulse width LOW time, t_4	40		10		1.2		µs

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TYPICAL CHARACTERISTICS: INTERNAL REFERENCE

At T_A = 25°C, unless otherwise noted

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE

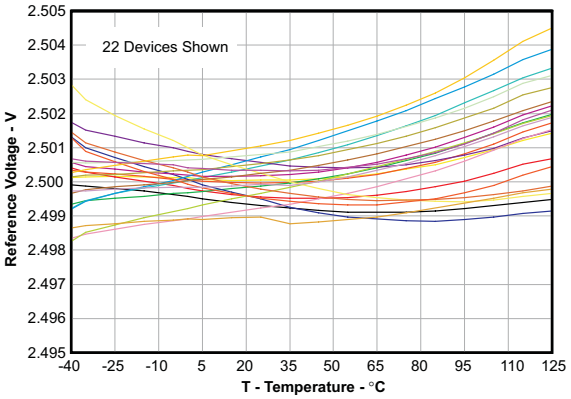

Figure 2.

LONG-TERM STABILITY DRIFT

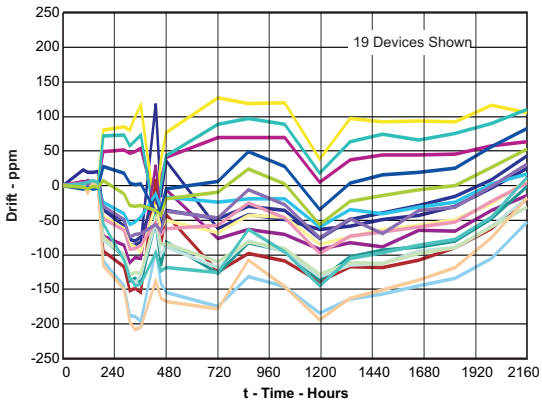

Figure 3.

INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE

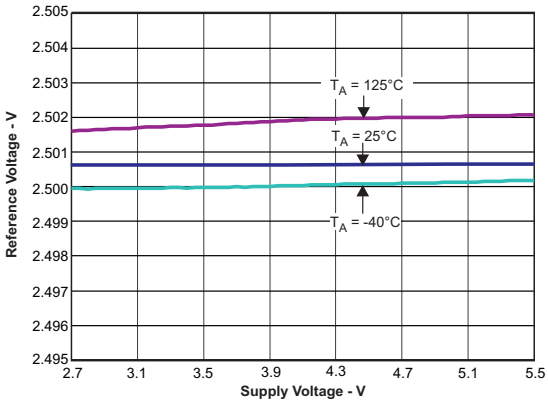

Figure 4.

INTERNAL REFERENCE VOLTAGE vs LOAD CURRENT

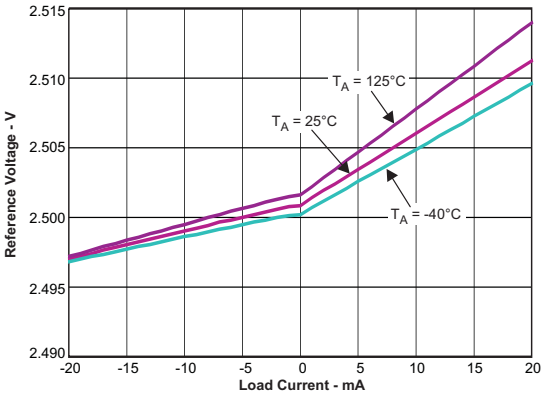

Figure 5.

INTERNAL REFERENCE NOISE DENSITY vs FREQUENCY

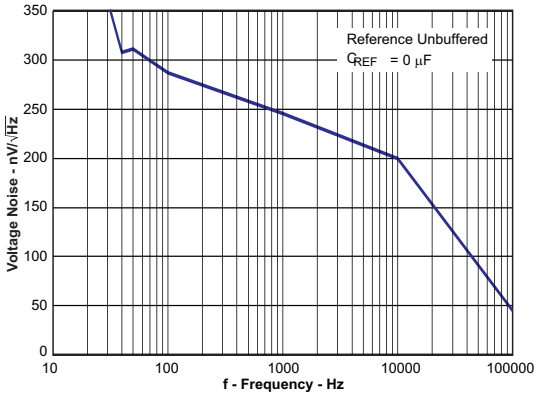

Figure 6.

INTERNAL REFERENCE NOISE 0.1 Hz to 10 Hz

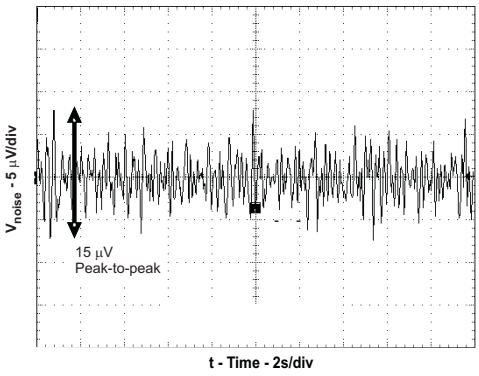

Figure 7.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

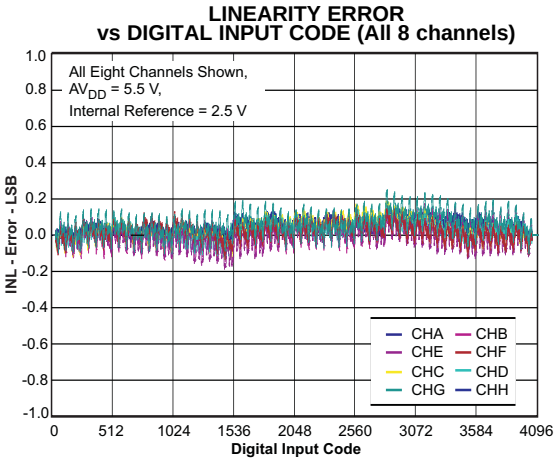

Figure 8.

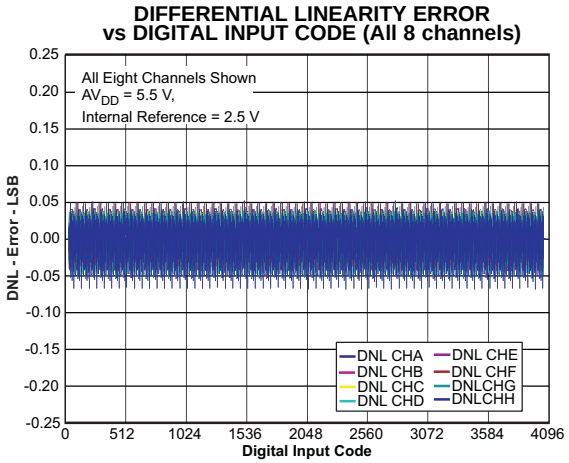

Figure 9.

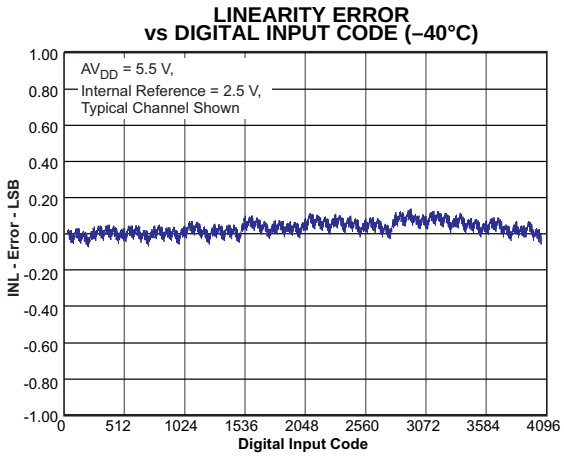

Figure 10.

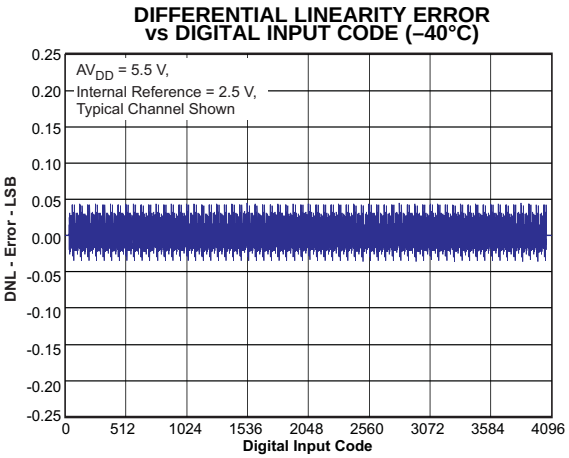

Figure 11.

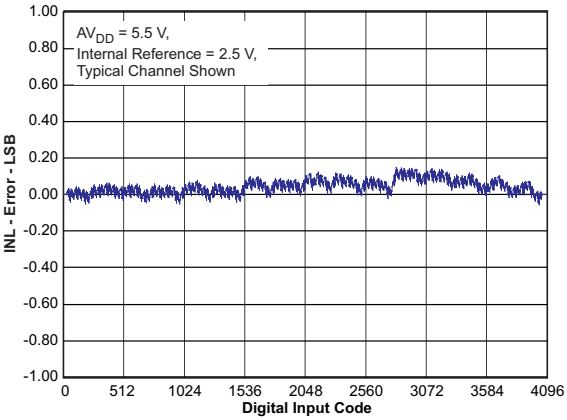

Figure 12.

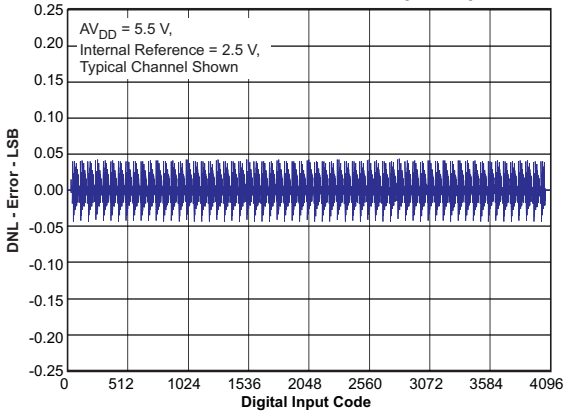

Figure 13.

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TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR vs DIGITAL INPUT CODE (+125°C)

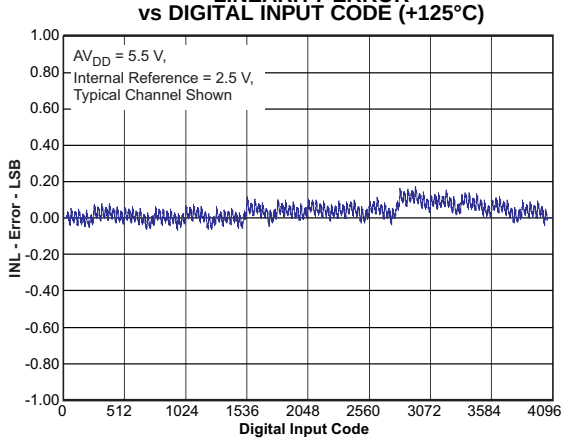

Figure 14.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+125°C)

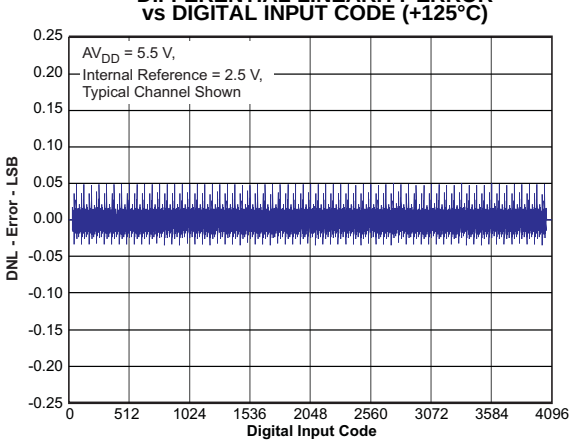

Figure 15.

LINEARITY ERROR vs TEMPERATURE

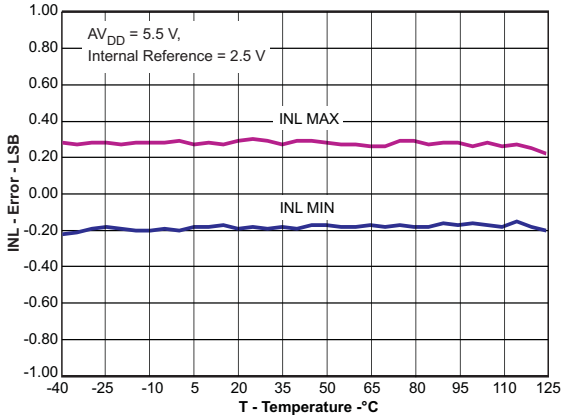

Figure 16.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

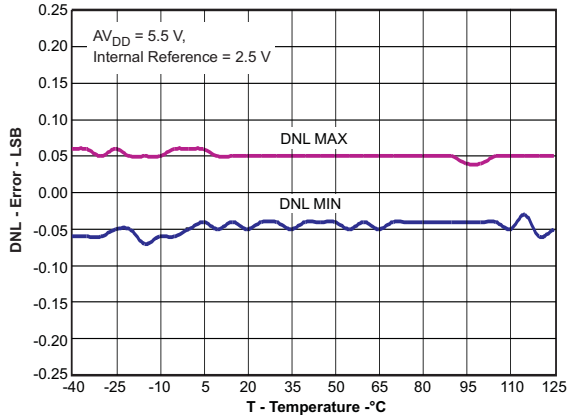

Figure 17.

POWER SUPPLY CURRENT vs TEMPERATURE

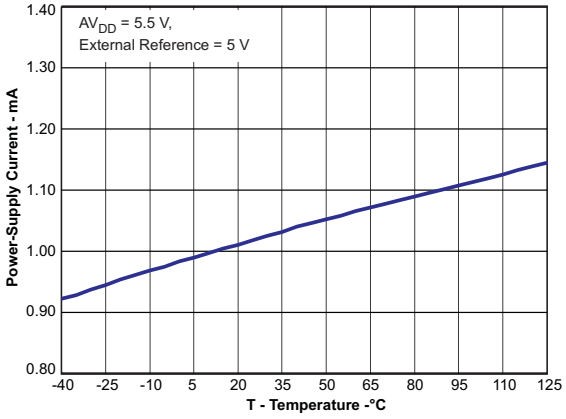

Figure 18.

OFFSET ERROR vs TEMPERATURE

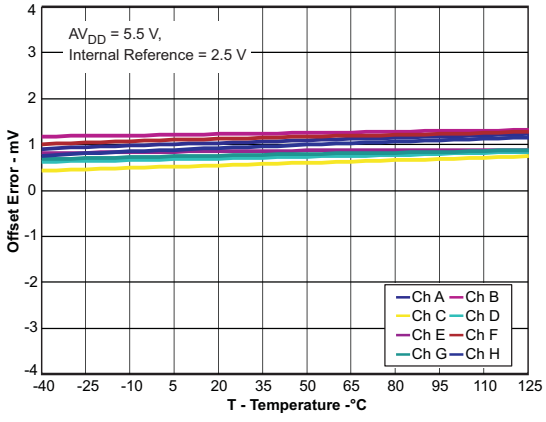

Figure 19.

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TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

POWER SUPPLY CURRENT vs TEMPERATURE

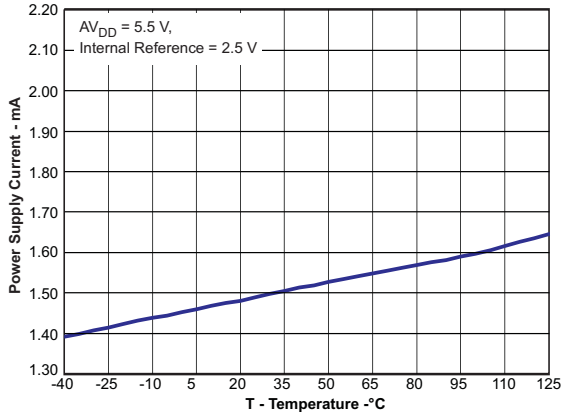

Figure 20.

FULL-SCALE ERROR vs TEMPERATURE

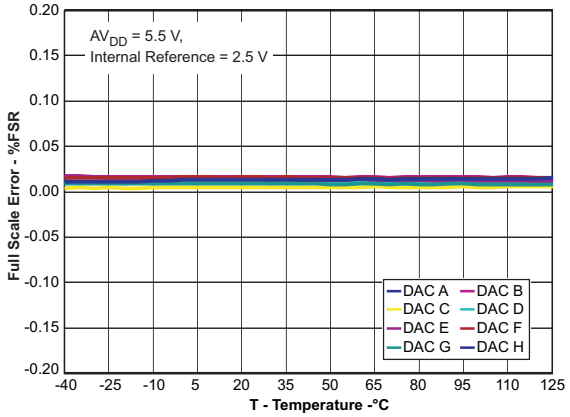

Figure 21.

POWER-DOWN CURRENT vs TEMPERATURE

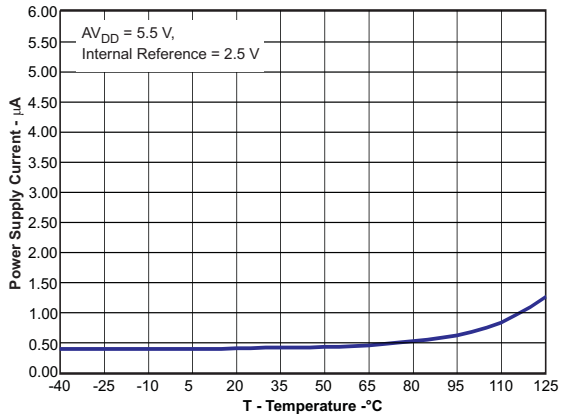

Figure 22.

GAIN ERROR vs TEMPERATURE

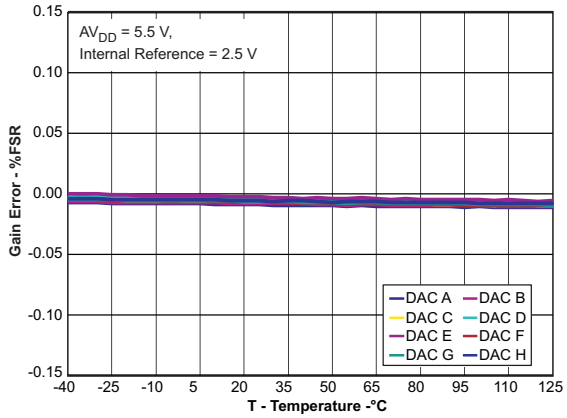

Figure 23.

SOURCE CURRENT AT POSITIVE RAIL

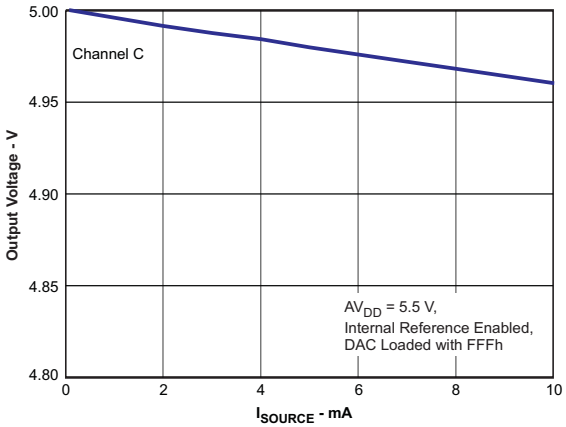

Figure 24.

SINK CURRENT AT NEGATIVE RAIL

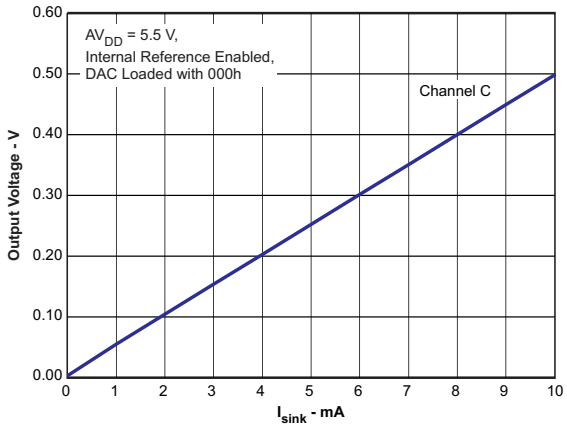

Figure 25.

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TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

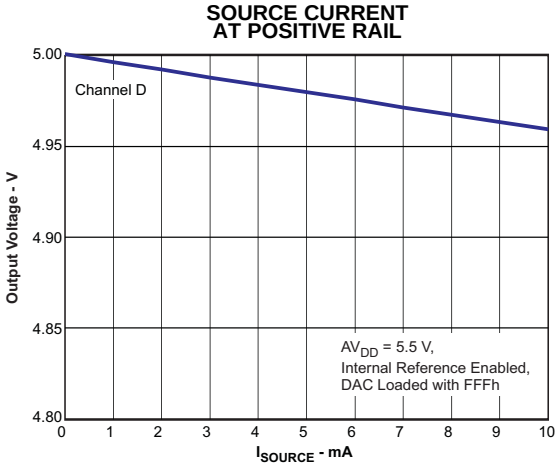

Figure 26.

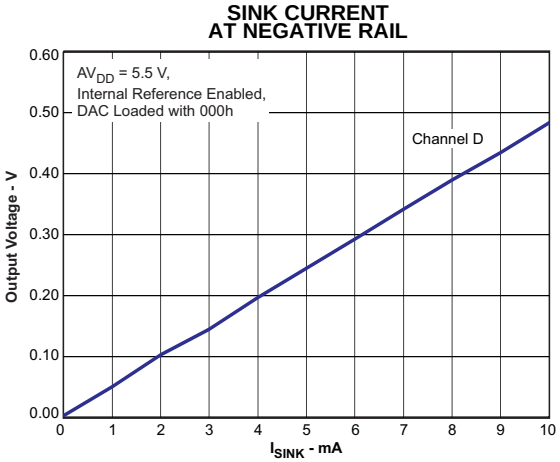

Figure 27.

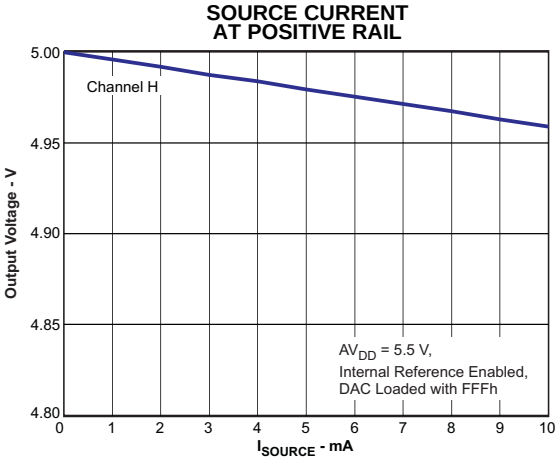

Figure 28.

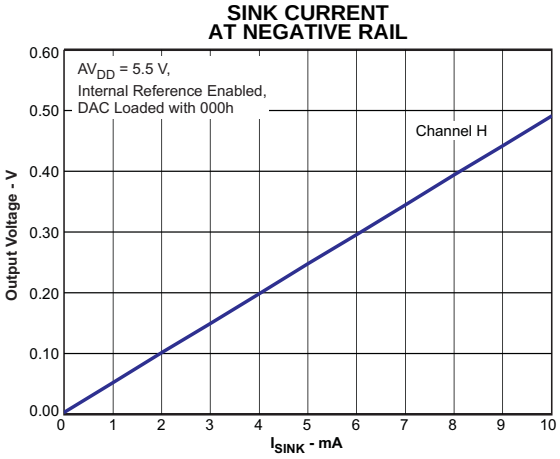

Figure 29.

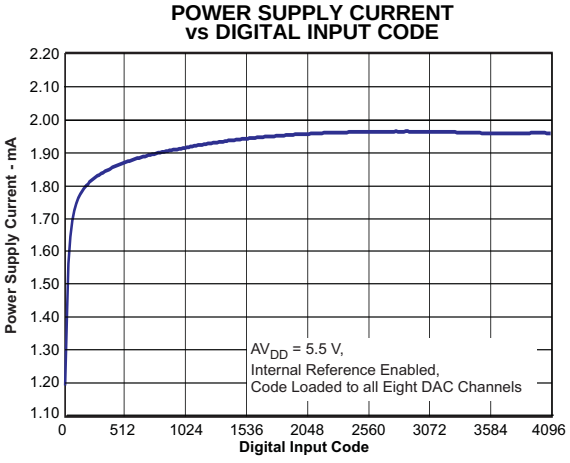

Figure 30.

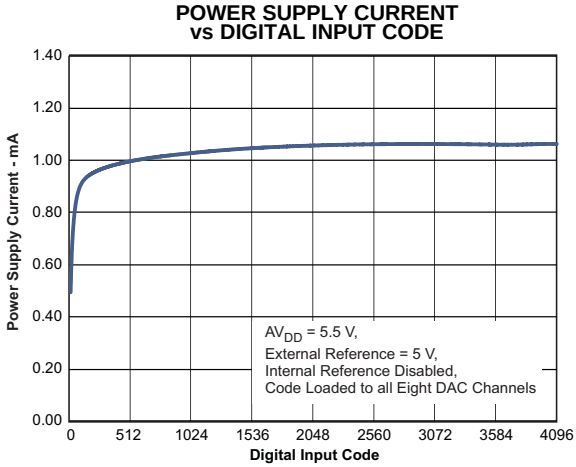

Figure 31.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

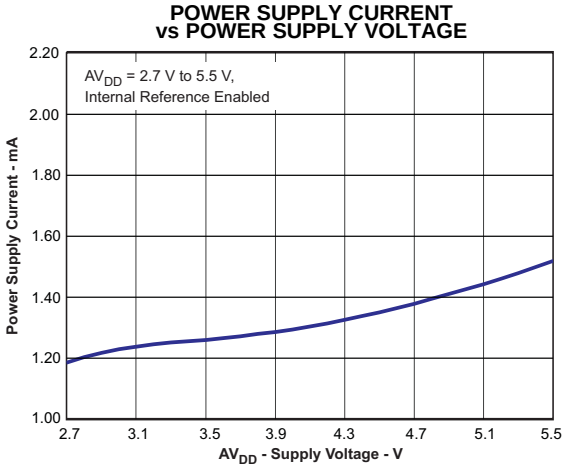

Figure 32.

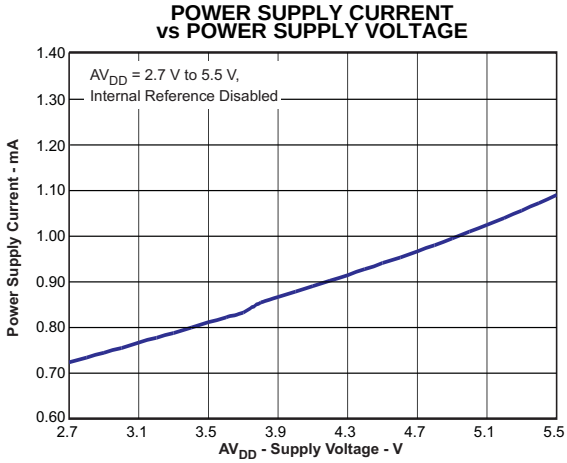

Figure 33.

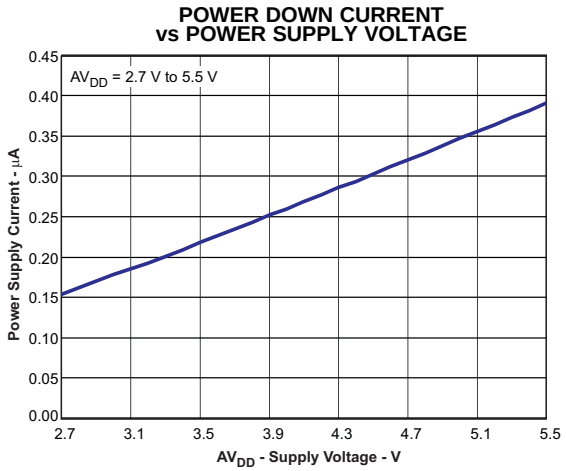

Figure 34.

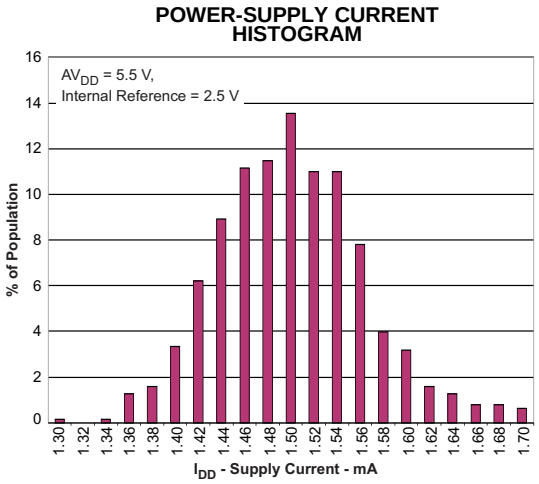

Figure 35.

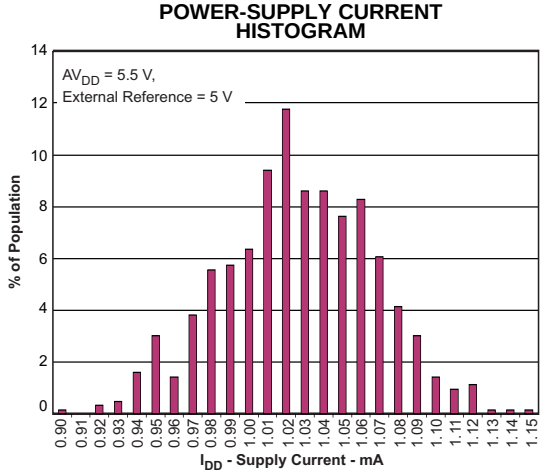

Figure 36.

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TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

FULL-SCALE SETTLING TIME: 5V RISING EDGE

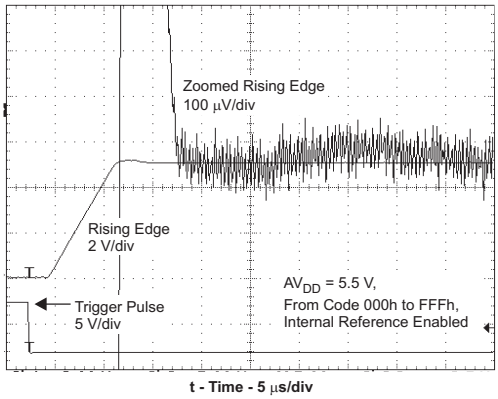

Figure 37.

FULL-SCALE SETTLING TIME: 5V FALLING EDGE

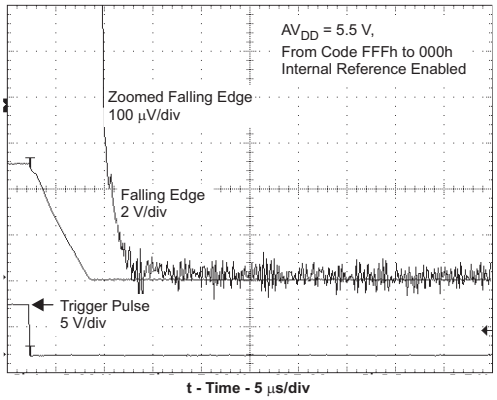

Figure 38.

HALF-SCALE SETTLING TIME: 5V RISING EDGE

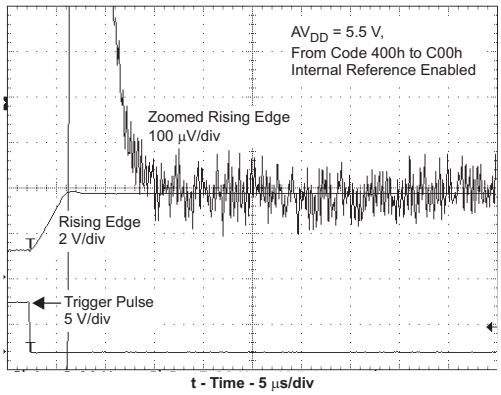

Figure 39.

HALF-SCALE SETTLING TIME: 5V FALLING EDGE

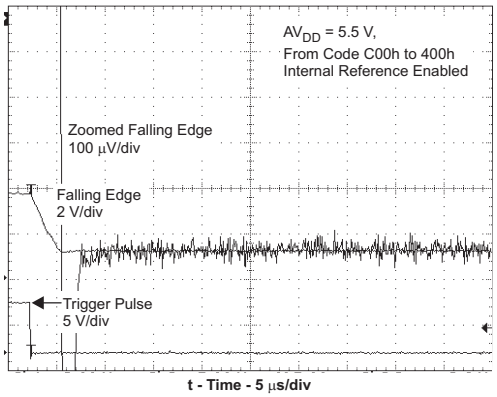

Figure 40.

CLOCK FEEDTHROUGH 400 kHz, MIDSCALE

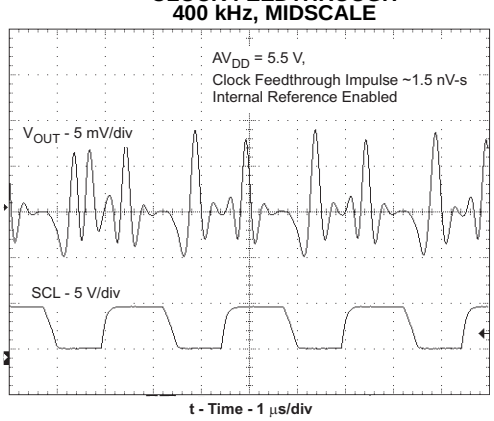

Figure 41.

POWER-ON GLITCH RESET TO ZERO SCALE

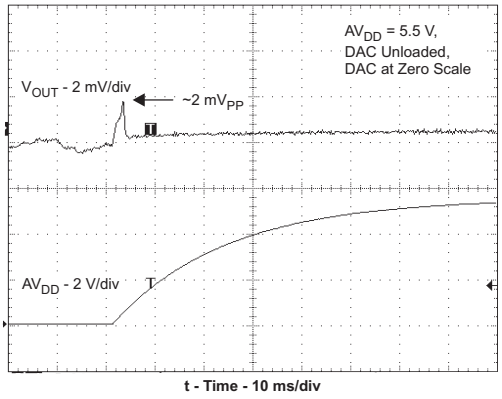

Figure 42.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

POWER-ON GLITCH RESET-TO-MID SCALE

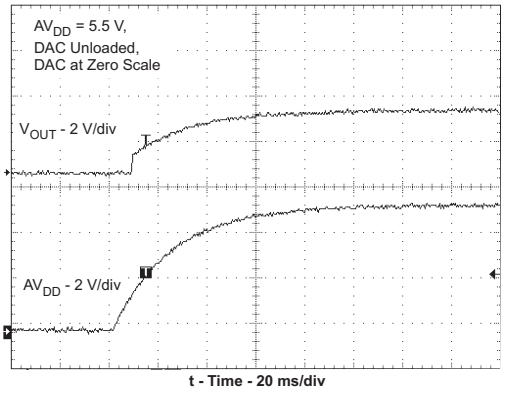

Figure 43.

POWER-OFF GLITCH

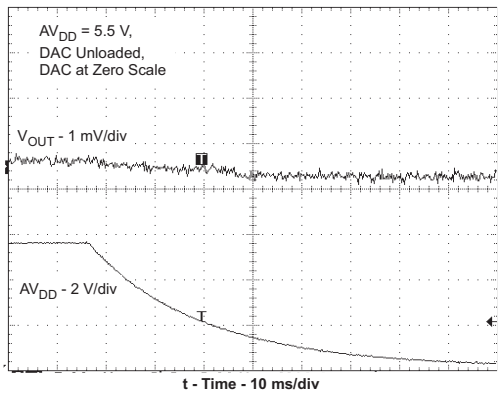

Figure 44.

GLITCH ENERGY: 5V 1LSB STEP, RISING EDGE

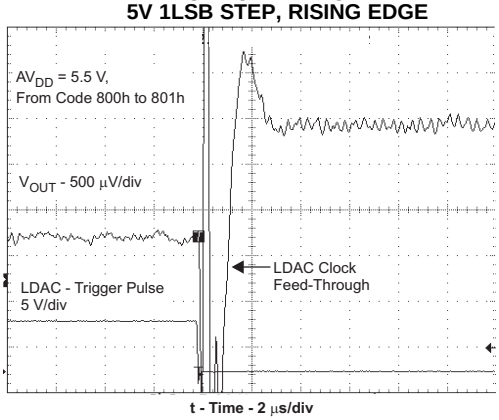

Figure 45.

GLITCH ENERGY: 5V 1LSB STEP, FALLING EDGE

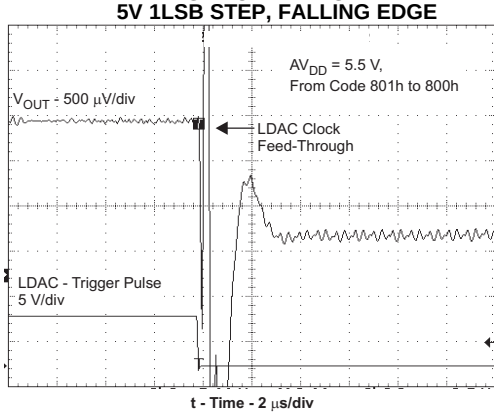

Figure 46.

DAC OUTPUT NOISE DENSITY vs FREQUENCY INTERNAL REFERENCE ENABLED

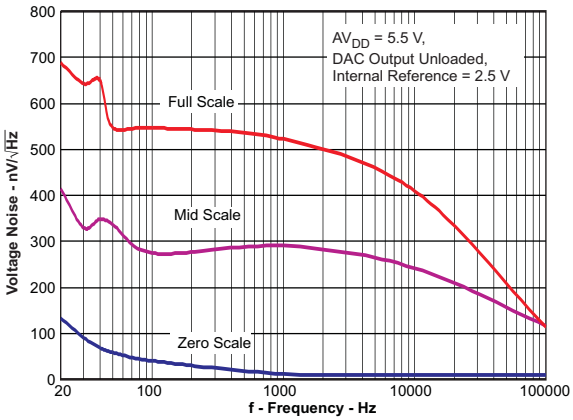

Figure 47.

DAC OUTPUT NOISE DENSITY vs FREQUENCY INTERNAL REFERENCE DISABLED

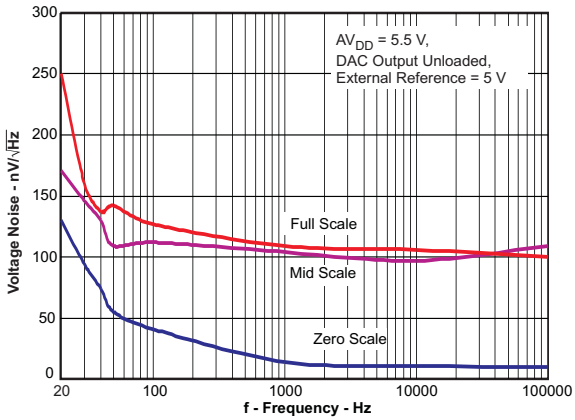

Figure 48.

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TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

DAC OUTPUT NOISE
0.1 Hz to 10 Hz

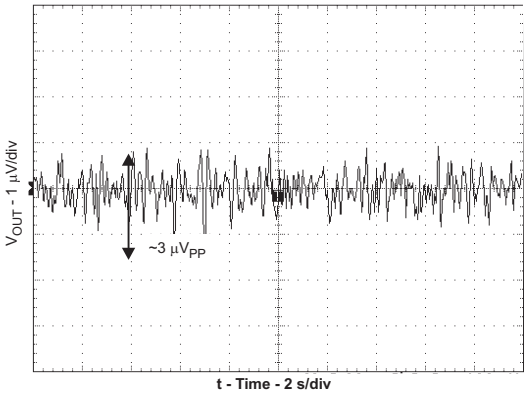

Figure 49.

TYPICAL CHARACTERISTICS: DAC AT AV_{DD} = 3.6 V

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

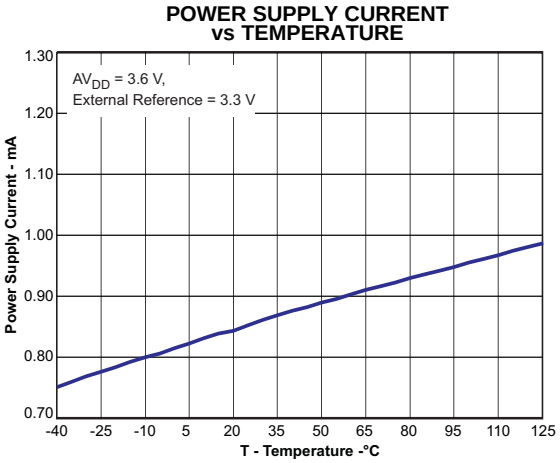

Figure 50.

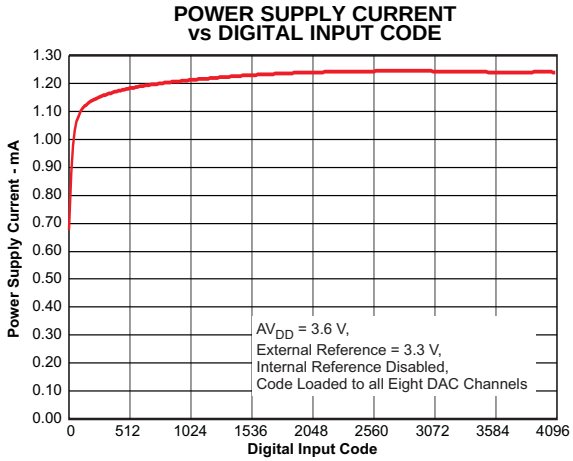

Figure 51.

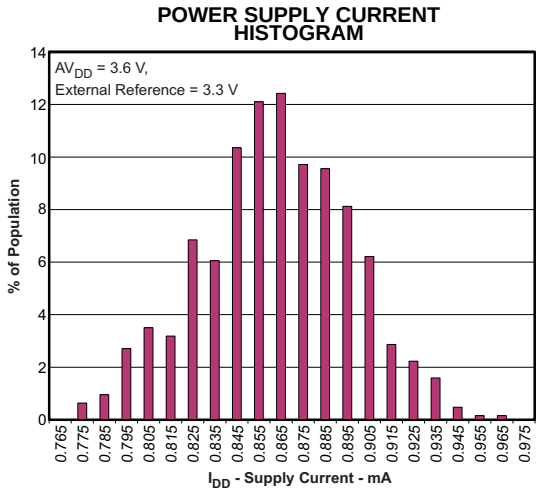

Figure 52.

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TYPICAL CHARACTERISTICS: DAC AT AV_{DD} = 2.7 V

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR vs DIGITAL INPUT CODE (All 8 Channels)

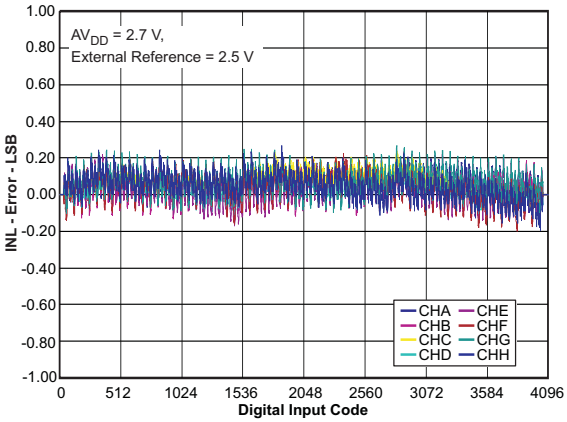

Figure 53.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (All 8 Channels)

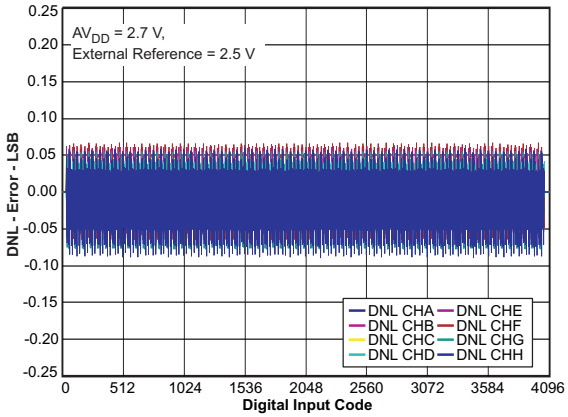

Figure 54.

LINEARITY ERROR vs DIGITAL INPUT CODE (-40°C)

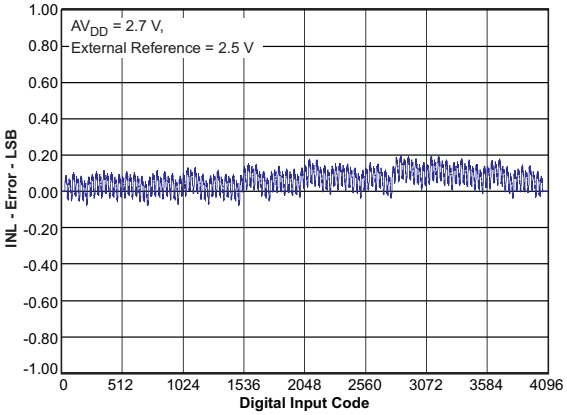

Figure 55.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (-40°C)

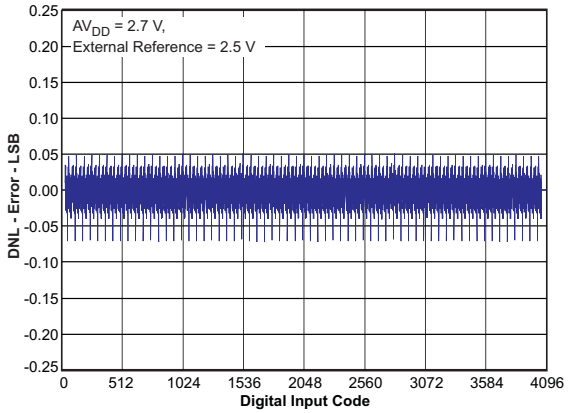

Figure 56.

LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

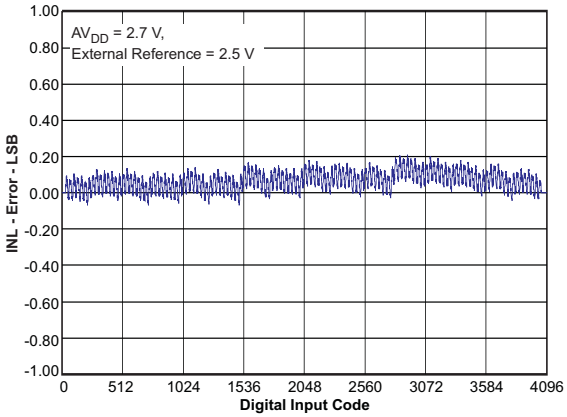

Figure 57.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

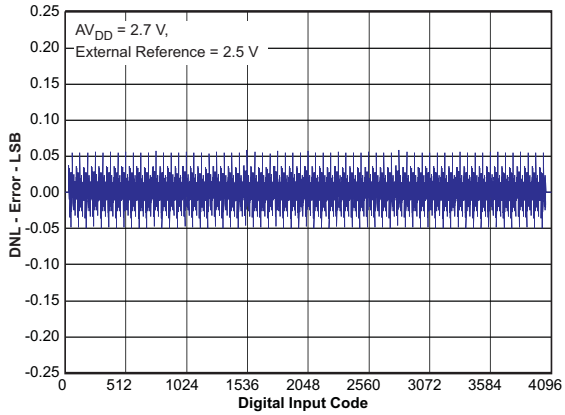

Figure 58.

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TYPICAL CHARACTERISTICS: DAC AT AV_{DD} = 2.7 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

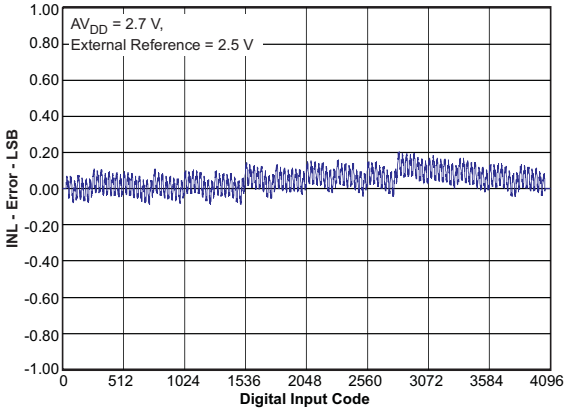

Figure 59.

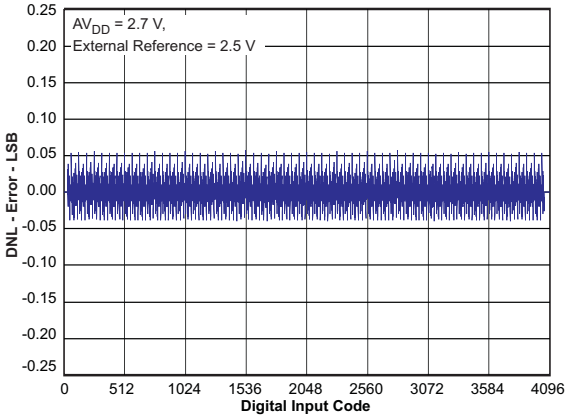

Figure 60.

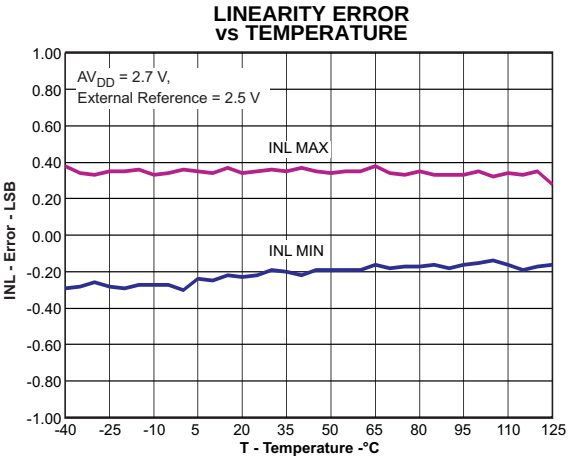

Figure 61.

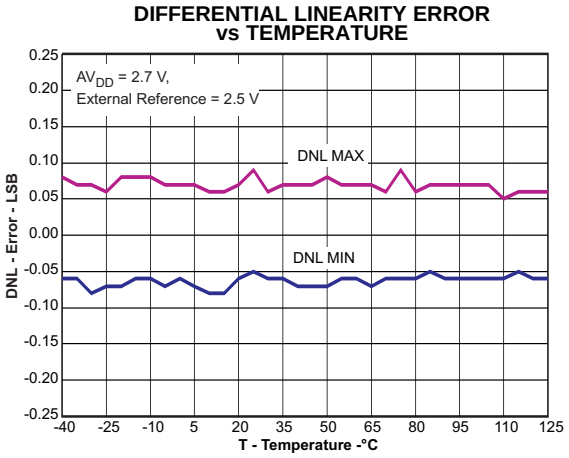

Figure 62.

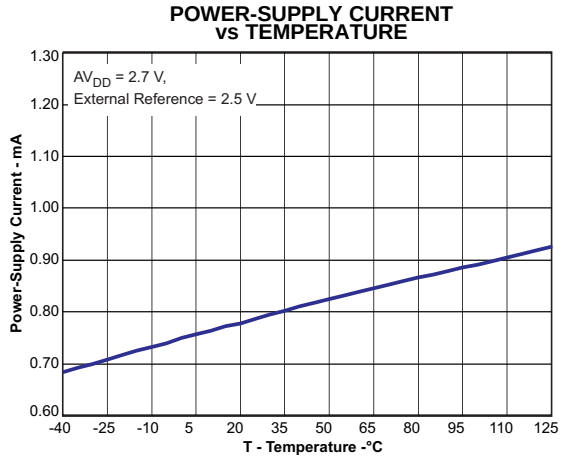

Figure 63.

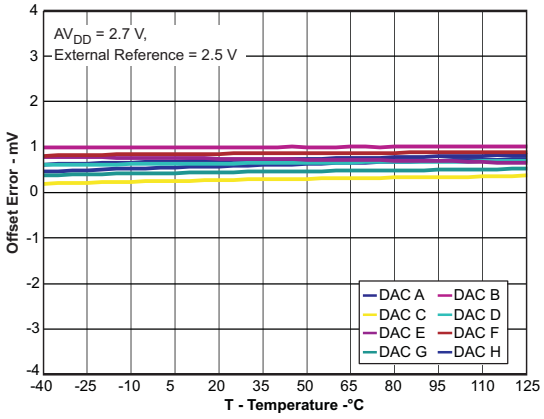

Figure 64.

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TYPICAL CHARACTERISTICS: DAC AT AV_{DD} = 2.7 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

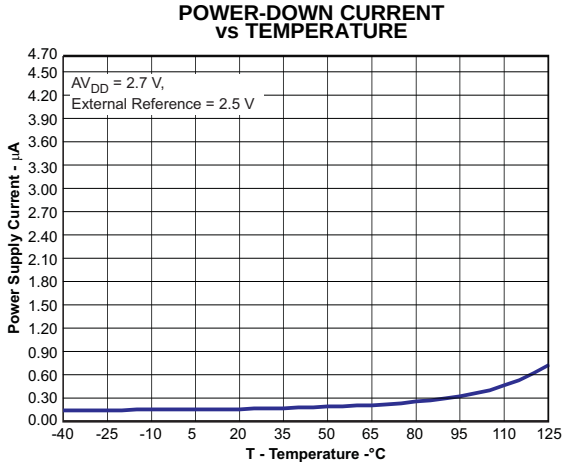

Figure 65.

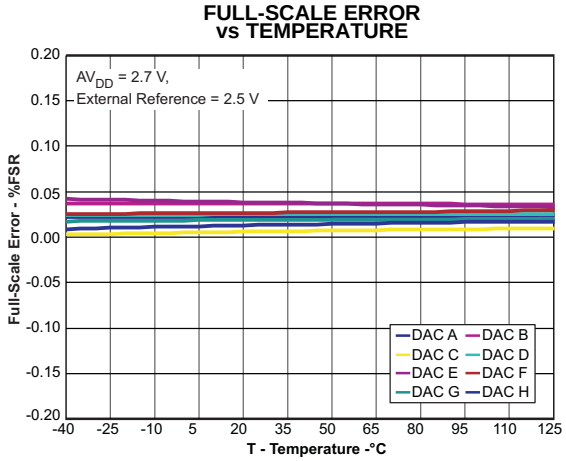

Figure 66.

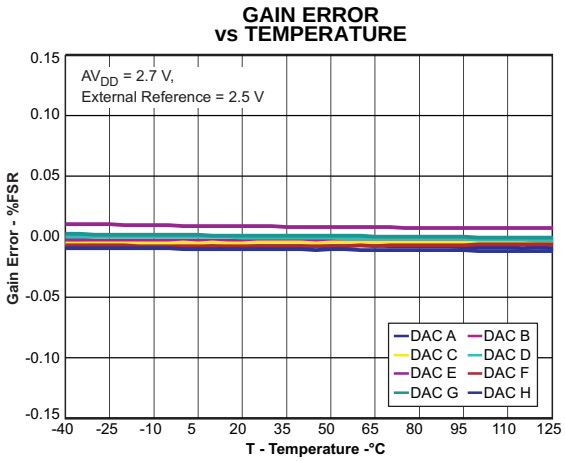

Figure 67.

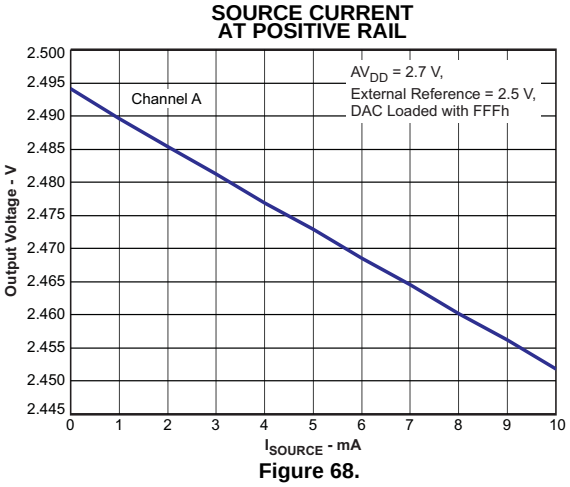

Figure 68.

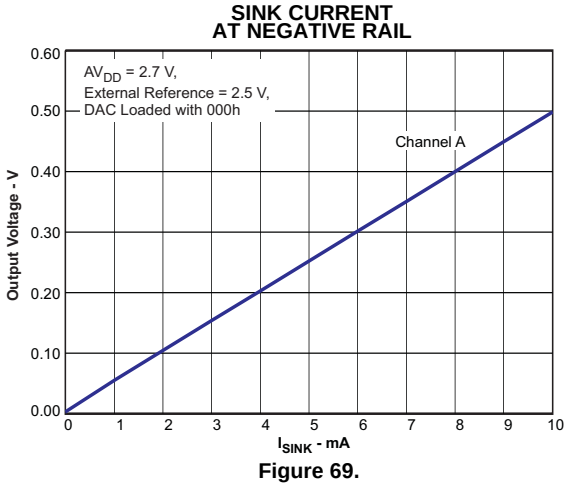

Figure 69.

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TYPICAL CHARACTERISTICS: DAC AT AV_{DD} = 2.7 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

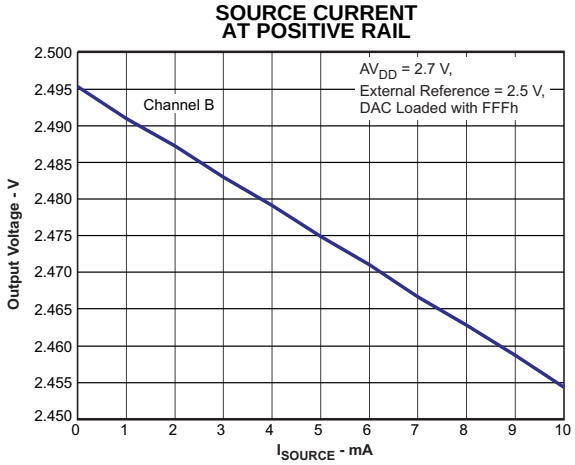

Figure 70.

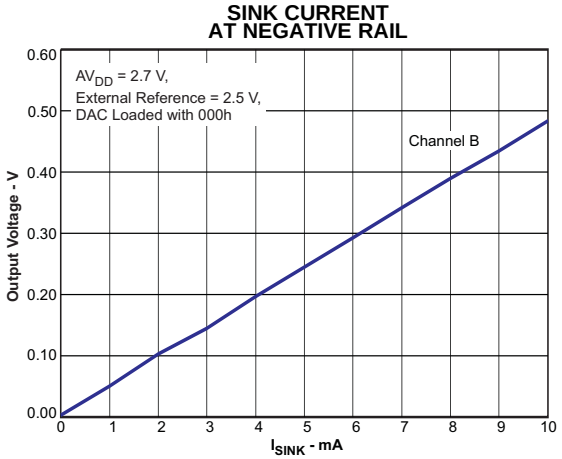

Figure 71.

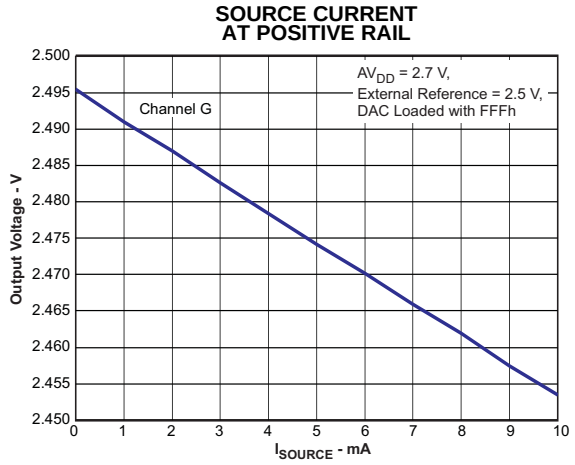

Figure 72.

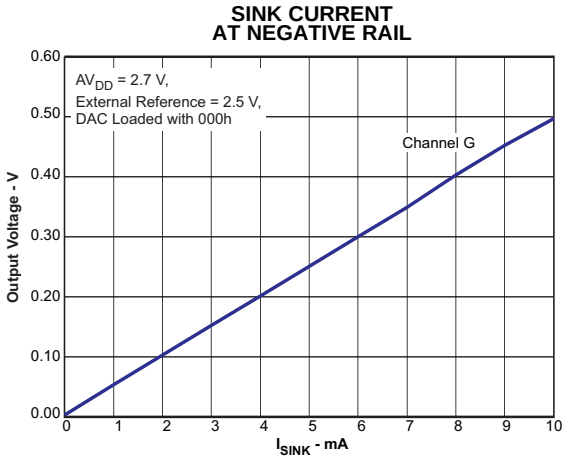

Figure 73.

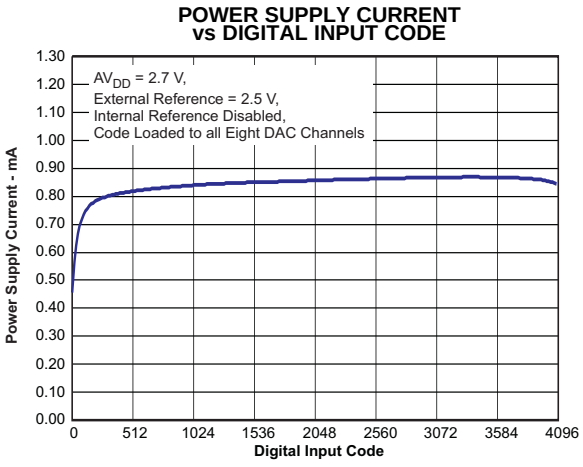

Figure 74.

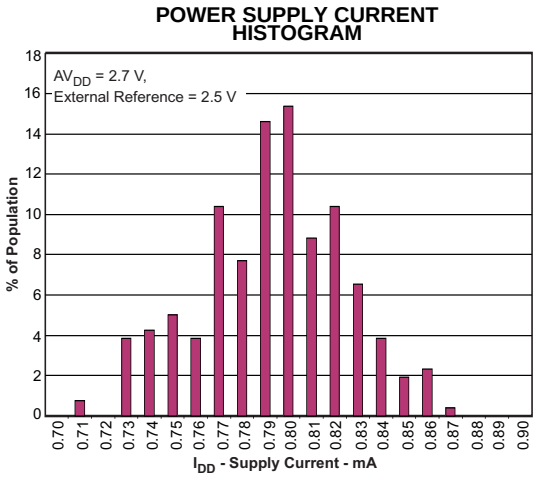

Figure 75.

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TYPICAL CHARACTERISTICS: DAC AT AV_{DD} = 2.7 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

FULL-SCALE SETTLING TIME: 2.7V RISING EDGE

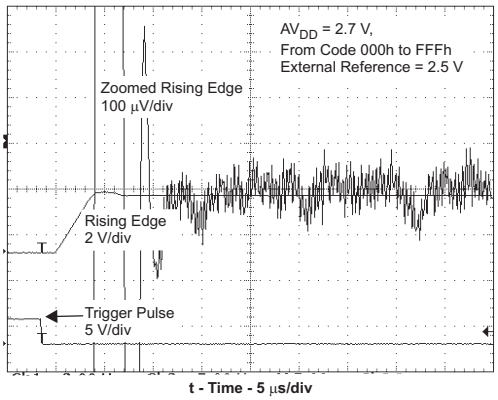

Figure 76.

FULL-SCALE SETTLING TIME: 2.7V FALLING EDGE

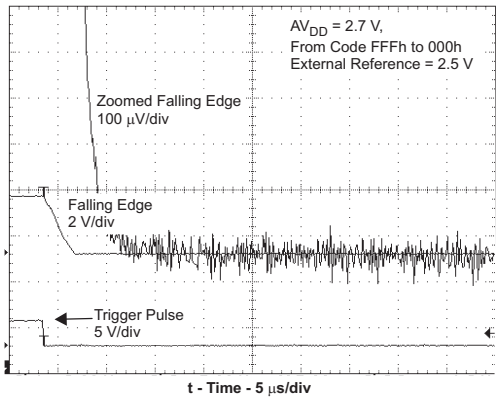

Figure 77.

HALF-SCALE SETTLING TIME: 2.7V RISING EDGE

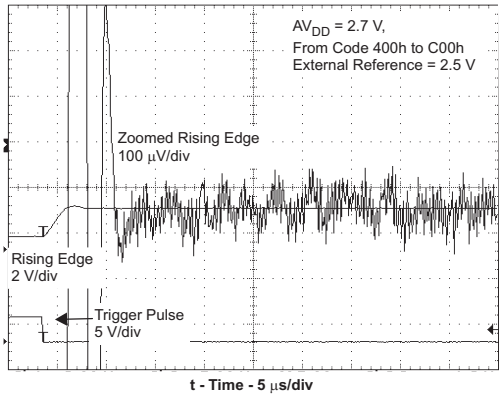

Figure 78.

HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE

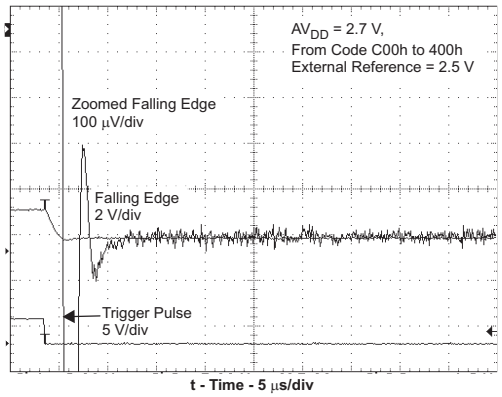

Figure 79.

CLOCK FEEDTHROUGH 400 kHz, MIDSCALE

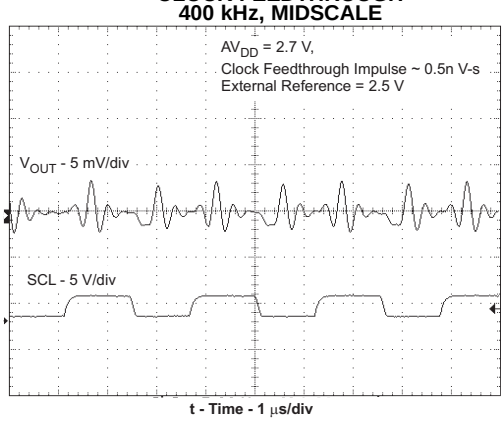

Figure 80.

POWER-ON GLITCH RESET TO ZERO SCALE

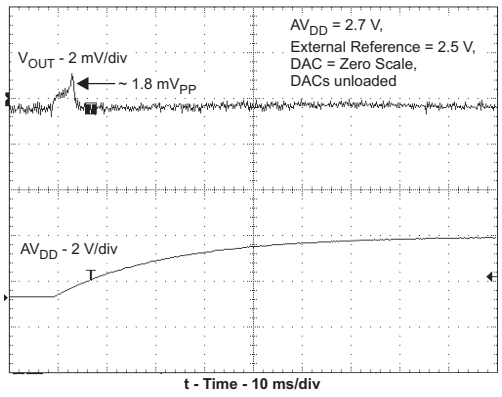

Figure 81.

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TYPICAL CHARACTERISTICS: DAC AT AV_{DD} = 2.7 V (continued)

At T_A = 25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted

POWER-ON GLITCH RESET TO MIDSCALE

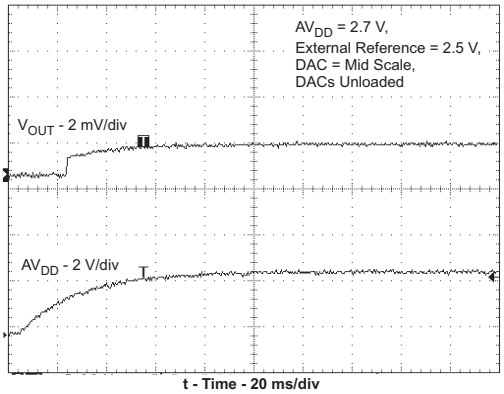

Figure 82.

POWER-OFF GLITCH

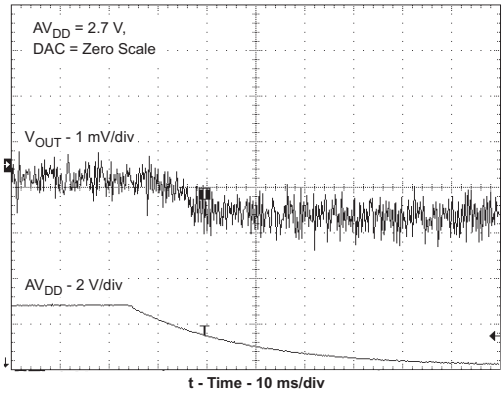

Figure 83.

GLITCH ENERGY: 2.7V 1LSB STEP, RISING EDGE

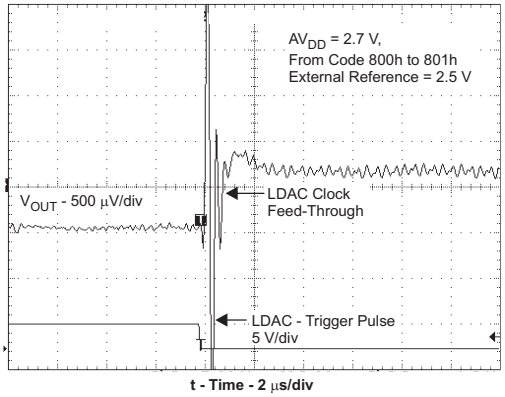

Figure 84.

GLITCH ENERGY: 2.7V 1LSB STEP, FALLING EDGE

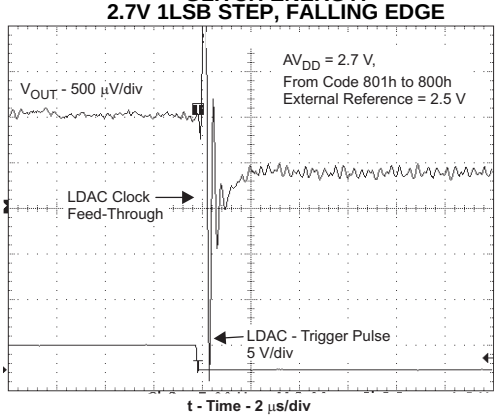

Figure 85.

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THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC7678 architecture consists of eight string DACs each followed by an output buffer amplifier. The DAC7678 also includes an internal 2.5V reference with a maximum 25ppm/°C temperature drift performance, offering a 5V, full-scale output voltage. Figure 86 shows a principal block diagram of the DAC architecture.

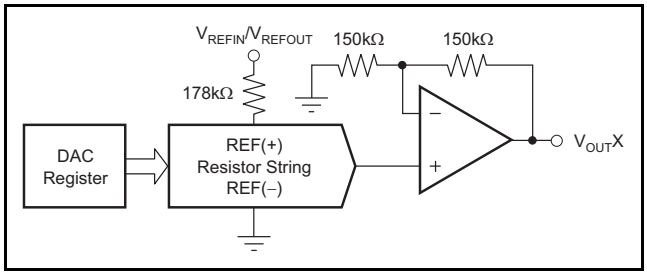

Figure 86. Device Architecture

For the TSSOP package, the input coding to the DAC7678 is straight binary. For the QFN package, the TWOC pin controls the code format.

When using the internal reference, the ideal output voltage is given by Equation 1:

$$V_{OUT} = \frac{D_{IN}}{4096} \times 2 \times V_{REFOUT} \quad (1)$$

When using an external reference, the ideal output voltage is given by Equation 2:

$$V_{OUT} = \frac{D_{IN}}{4096} \times V_{REFIN} \quad (2)$$

Where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 4095.

V_{REFOUT} = internal reference voltage of 2.5V (typ), supplied at the V_{REFIN}/V_{REFOUT} pin.

V_{REFIN} = external reference voltage of 0V to 5V (typ), supplied at the V_{REFIN}/V_{REFOUT} pin.

RESISTOR STRING

The resistor string circuitry is shown in Figure 87. It is a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is monotonic because it is a string of resistors. $R_{DIVIDER}$ will be un-shorted if external reference is used. Thus the overall gain will be one and allows the user to provide an external reference value of 0 to AVDD. If internal reference is used $R_{DIVIDER}$ is shorted and the overall gain will be two.

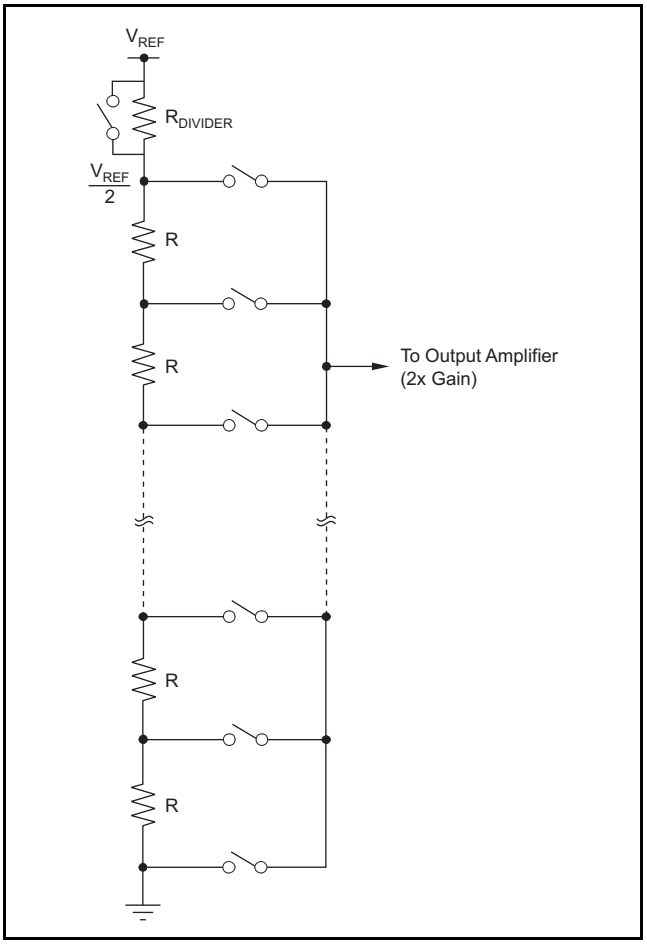

Figure 87. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0V to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The typical slew rate is 0.75V/µs, with a typical full-scale settling time of 7µs with the output unloaded.

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INTERNAL REFERENCE

The DAC7678 includes a 2.5V internal reference that is disabled by default. The internal reference is externally available at the V_{REFIN}/V_{REFOUT} pin. A minimum 100nF capacitor is recommended between the reference output and GND for noise filtering. The internal reference of the DAC7678 is a bipolar-transistor based precision bandgap voltage reference. Figure 88 shows the basic bandgap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages ($V_{BE1} - V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_1. This voltage is gained up and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100mA.

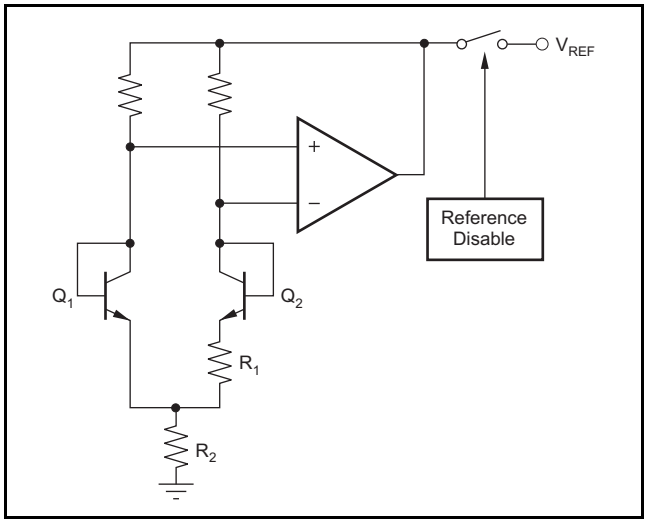

Figure 88. Simplified Schematic of the Bandgap Reference

Enable/Disable Internal Reference

The internal reference in the DAC7678 is disabled by default for debugging, evaluation purposes, or when using an external reference. The internal reference can be powered up and powered down using a serial command that requires a 32-bit write sequence, which consists of 8 bit Address Byte plus 24 bit serial command as shown in Table 1. During the time that the internal reference is disabled, the DAC functions normally using an external reference. However, when switching to the external reference the internal gain is dynamically switched to one. Therefore appropriate value of external reference should be used per the desired output voltage. At this point, the internal reference is disconnected from the V_{REFIN}/V_{REFOUT} pin (3-state output). Do not attempt to drive the V_{REFIN}/V_{REFOUT} pin externally and internally at the same time indefinitely. There are two modes that allow communication with the internal reference: Regular/Static and Flexible. In Flexible mode DB14 needs to be set to '1' as shown in Table 17.

Regular/Static Mode (see Table 1 and Table 2)

Enabling Internal Reference:

To enable the internal reference, write the 24-bit serial command shown in Table 1 after properly addressing the device. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence is applied to power up the internal reference. Setting DB4 to '1' turns on the internal reference.If the internal reference is powered up, it automatically powers down when all DACs power down in any of the power-down modes (see Table 17 and *Power Down Modes* section). The internal reference automatically powers up when any DAC is powered up.

Disabling Internal Reference:

To disable the internal reference, address the device by writing the 8-bit address byte and then writing the 24-bit serial command shown in Table 1. When performing a power cycle to reset the device, the internal reference is put back into the default mode (switched off).

Table 1. Write Sequence for Enabling Internal Reference (Static Mode) (Internal Reference Powered On)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT BYTE							
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X

Table 2. Write Sequence for Disabling Internal Reference (Static Mode) (Internal Reference Powered Off)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT BYTE							
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X

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Flexible Mode (see Table 3, Table 4, Table 5 and Table 6)

Enabling Internal Reference:

Method 1) To enable the internal reference, write the 24-bit serial command shown in Table 3 after properly addressing the device. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence is applied to power up the internal reference. If the internal reference is powered up, it automatically powers down when all DACs power down in any of the power-down modes (see the Power Down Modes section). The internal reference powers up automatically when any DAC is powered up.

Method 2) To always enable the internal reference, write the 24-bit serial command shown in Table 4 after properly addressing the device. When the internal reference is always enabled, any power-down command to the DAC channels does not change the internal reference operating mode. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference remains powered down until a valid write sequence is applied to power up the internal reference. When the internal reference is powered up in flexible mode, it remains powered up, regardless of the state of the DACs.

Disabling Internal Reference:

To disable the internal reference, write the 24-bit serial command shown in Table 5 after properly addressing the device. When performing a power cycle to reset the device, the internal reference is switched off (default mode). When the internal reference is operated in Flexible mode, Static mode is disabled and does not work. To switch from Flexible mode to Static mode, use the command shown in Table 6.

Table 3. Write Sequence for Enabling Internal Reference (Flexible Mode) (Internal Reference Powered On)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT BYTE							
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	X	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X

Table 4. Write Sequence for Enabling Internal Reference (Flexible Mode) (Internal Reference Always Powered On)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT BYTE							
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	X	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X

Table 5. Write Sequence for Disabling Internal Reference (Flexible Mode) (Internal Reference Always Powered Down)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT BYTE							
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	X	X	X	X	X	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X

Table 6. Write Sequence for Switching from Flexible Mode to Static Mode for Internal Reference

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT BYTE							
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X

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TWO-WIRE, I²C-COMPATIBLE INTERFACE

The I²C™ is a 2-wire serial interface developed by Philips Semiconductor (see I²C™-Bus Specification, Rev. 03, June 2007). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C™ compatible devices connect to the I²C™ bus through open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *master*, and the devices that are controlled by the master are called *slaves*. The master device generates the SCL signal. The master device also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is also done by the master. The master device on an I²C bus is usually a microcontroller or a digital signal processor (DSP). The DAC7678 on the other hand, operates as a slave device on the I²C bus. A slave devcie acknowledges master's commands and upon master's control, either receives or transmits data.

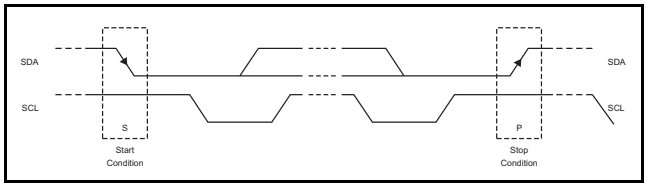

Figure 89. Start and Stop Conditions

The DAC7678 normally operates as a slave receiver. A master device *writes* to the DAC7678, a slave receiver. However, if a master device inquires the DAC7678 internal register data, the DAC7678 operates as a slave transmitter. In this case, the master device *reads* from the DAC7678, a slave transmitter. According to I²C™ terminology, *read* and *write* are with respect to the master device.

The DAC7678 works as a slave and supports the following data transfer modes, as defined in the I²C™ -Bus Specification:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode+ (1.0Mbps) and
- High-Speed mode (3.4 Mbps)

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The fast mode+ protocol is supported in terms of data transfer speed but not output current. The low-level output current would be 3mA similar to the case of standard and fast modes. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as HS-mode. The DAC7678 supports 7-bit addressing. The 10-bit addressing and general call address are **not** supported.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a 9th clock cycle is used to generate/detect an acknowledge signal, *Acknowledge* is when the SDA line is pulled low during the high period of the 9th clock cycle. A *not-acknowledge* is when the SDA line is left high during the high period of the 9th clock cycle as shown in Figure 90.

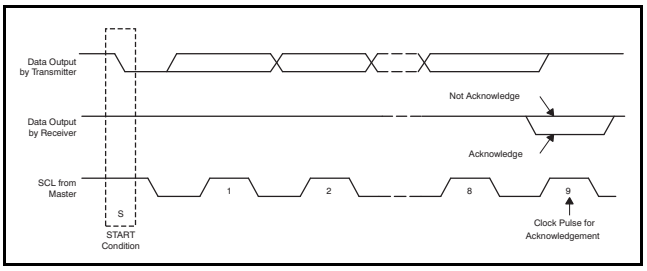

Figure 90. Acknowledge and Not Acknowledge on the I²C Bus

F/S Mode Protocol

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occcurs on the SDA line while SCL is high, as shown in Figure 90. All I²C-compatible devices recognize a start condition.
- The master then generates the SCL pulses, and transmits the 7-bit address and the *read/write direction bit* (R/$\overline{W}$) on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid* data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 91. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* by pulling the SDA line low during the entire high period of the ninth SCL cycle, as shown in Figure 90 by pulling the SDA line low during the entire high period of the 9th SCL cycle. Upon detecting this acknowledge, the master knows the communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/$\overline{W}$ bit 0) or *receive* data from the slave (R/$\overline{W}$ bit 1). In either case, the *receiver* needs to acknowledge the data sent by the *transmitter*. So the acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences, consisting of 8-data bits and 1-bit acknowledge can continue as long as

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necessary.

- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 89). This action releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices recognize the stop condition. Upon receipt of a *stop condition*, the bus is released, and all slave devices then wait for a *start condition* followed by a matching address.

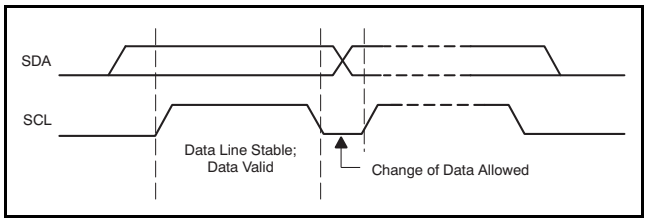

Figure 91. Bit Transfer on the I²C Bus

HS Mode Protocol

- When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up resistors.
- The master generates a start condition followed by a valid serial byte containing H/S master code 00001XXX. This transmission is made in F/S mode at no more than 1.0 Mbps. No device is allowed to acknowledge the H/S master code, but all devices must recognize it and switch their internal setting to support 3.4Mbps operation.
- The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends HS mode and switches all the internal settings of the slave devices to support F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in H/S-mode.

DAC7678 I²C UPDATE SEQUENCE

For a single update, the DAC7678 requires a start condition, a valid I²C address, a command and access (CA) byte, and two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), as shown in Table 7.

After each byte is received, the DAC7678 acknowledges by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 92. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address selects the DAC7678.

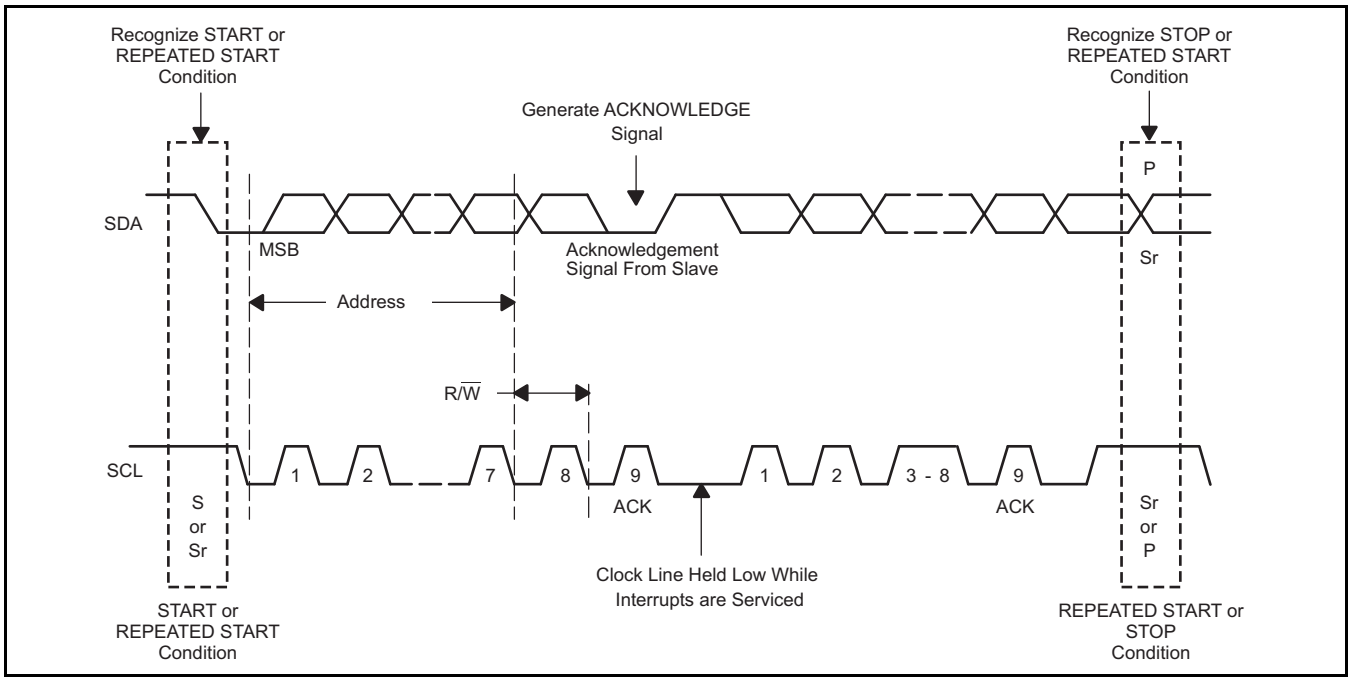

Figure 92. I²C Bus Protocol

Table 7. Update Sequence

MSB	…	LSB	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
Address (A) Byte				Command/Access Byte				MSDB				LSDB			
DB[32:24]				DB[23:16]				DB[15:8]				DB[7:0]			

The CA byte sets the operational mode of the selected DAC7678. When the operational mode is selected by this byte, the DAC7678 must receive two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), for data update to occur. The DAC7678 performs an update on the falling edge of the acknowledge signal that follows the LSDB.

The CA byte does not have to be resent until a change in operational mode is required. The bits of the control byte continuously determine the type of update performed. Thus, for the first update, the DAC7678 requires a start condition, a valid I^2C address, the CA byte, and two data bytes (MSDB and LSDB). For all consecutive updates, the DAC7678 needs only an MSDB and LSDB, as long as the CA byte command remains the same.

When using the I^2C HS mode (clock = 3.4MHz), each 12-bit DAC update other than the first update can be done within 18 clock cycles (MSDB, acknowledge signal, LSDB, acknowledge signal) at 188.88kSPS. When using Fast mode (clock = 400kHz), the maximum DAC update rate is limited to 22.22kSPS. Using the Fast mode plus (clock = 1MHz), the maximum DAC update rate is limited to 55.55kSPS. When a stop condition is received, the DAC7678 releases the I^2C bus and awaits a new start condition.

Address (A) Byte

The address byte, as shown in Table 8, is the first byte received following the START condition from the master device. The first four bits (MSBs) of the address are factory preset to 1001. The next 3 bits of the address are controlled by the ADDR pin(s). The ADDR pin(s) inputs can be connected to AV_{DD}, GND, or left floating. The device address should be determined before device power up. During power up the device latches the values of the address pins and consequently will respond to that particular address according to Table 9 and Table 10. When using the QFN package (DAC7678RGE), up to 8 devices can be connected to the same I^2C bus. When using the TSSOP package (DAC7678PW), up to 3 devices can be connected to the same I^2C bus.

Table 8. Address Byte

MSB							LSB
AD6	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**	**R/$\overline{W}$**
1	0	0	1	See Table 9 or Table 10 Slave Address column			0 or 1

Table 9. Address Format For QFN-24 (RGE) Package

SLAVE ADDRESS	ADDR1	ADDR0
1001 000	0	0
1001 001	0	1
1001 010	1	0
1001 011	1	1
1001 100	Float	0
1001 101	Float	1
1001 110	0	Float
1001 111	1	Float
Not supported	Float	Float

Table 10. Address Format For TSSOP-16 (PW) Package

SLAVE ADDRESS	ADDR0
1001 000	0
1001 010	1
1001 100	Float

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Command and Access (CA) Byte

The Command and Access Byte, as shown in Table 11, controls which command is executed and which register is being accessed when writing to or reading from the DAC7678. See Table 12 for a list of write and read commands.

Table 11. Command and Access Byte

MSB							LSB
C3	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**
Command bits				Access bits			

Table 12. Command and Access Byte Format(1)

C3	C2	C1	C0	A3	A2	A1	A0	DESCRIPTION
Write Sequences								
0	0	0	0	A3	A2	A1	A0	Write to DAC input register channel n
0	0	0	1	A3	A2	A1	A0	Select to update DAC register channel n
0	0	1	0	A3	A2	A1	A0	Write to DAC input register channel n, and update all DAC registers (global software LDAC)
0	0	1	1	A3	A2	A1	A0	Write to DAC input register channel n, and update DAC register channel n
0	1	0	0	X	X	X	X	Power down/on DAC
0	1	0	1	X	X	X	X	Write to clear code register
0	1	1	0	X	X	X	X	Write to LDAC register
0	1	1	1	X	X	X	X	Software reset
1	0	0	0	X	X	X	X	Write to internal reference register
1	0	0	1	X	X	X	X	Write to additional internal reference register
Read Sequences								
0	0	0	0	A3	A2	A1	A0	Read from DAC input register channel n
0	0	0	1	A3	A2	A1	A0	Read from DAC register channel n
0	1	0	0	X	X	X	X	Read from DAC power down register
0	1	0	1	X	X	X	X	Read from clear code register
0	1	1	0	X	X	X	X	Read from LDAC register
1	0	0	0	X	X	X	X	Read from internal reference register
1	0	0	1	X	X	X	X	Read from additional internal reference register
Access Sequences								
C3	C2	C1	C0	0	0	0	0	DAC channel A
C3	C2	C1	C0	0	0	0	1	DAC channel B
C3	C2	C1	C0	0	0	1	0	DAC channel C
C3	C2	C1	C0	0	0	1	1	DAC channel D
C3	C2	C1	C0	0	1	0	0	DAC channel E
C3	C2	C1	C0	0	1	0	1	DAC channel F
C3	C2	C1	C0	0	1	1	0	DAC channel G
C3	C2	C1	C0	0	1	1	1	DAC channel H
C3	C2	C1	C0	1	1	1	1	All DAC channels, broadcast update

(1) Any sequences other than the ones listed are invalid; improper use can cause incorrect device functionality.

Most Significant Data Byte (MSDB) and Least Significant Data Byte (LSDB)

The MSDB and LSDB contain the data that are passed to the register(s) specified by the CA byte, as shown in Table 13 and Table 14. See Table 17 for a complete list of write sequences and Table 18 for a complete list of read sequences. The DAC7678 updates at the falling edge of the acknowledge signal that follows the LSDB[0] bit.

Table 13. MSDB

MSB							LSB
DB15	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**
Most Significant Data Byte (MSDB)							

Broadcast Address Byte

Broadcast addressing, see Table 15, is also supported by DAC7678. Broadcast addressing can be used for synchronously updating or powering down multiple DAC7678 devices. DAC7678 is designed to work with other members of the DACx578 family to support multichannel synchronous update. Using the broadcast address, DAC7678 responds regardless of the states of the address pins. Broadcast is supported only in write mode (Master writes to DAC7678).

DAC7678 I²C READ SEQUENCE

To read any register the following command sequence should be used:

1. Send a start or repeated start command with a slave address and the R/$\overline{W}$ bit set to '0' for writing. The device will acknowledge this event.
2. Then send a command byte for the register to be read. The device will acknowledge this event again.
3. Then send a repeated start with the slave address and the R/$\overline{W}$ bit set to '1' for reading. The device will also acknowledge this event.
4. Then the device writes the MSDB byte of the addressed register. The master should acknowledge this byte. Finally, the device writes out the LSDB of the register as shown in Table 16.

An alternative reading method allows for reading back the value of the last register written. The sequence is a start/repeated start with slave address and the R/$\overline{W}$ bit set to '1', and the two bytes of the last register are read out.

Note that it is not possible to use the broadcast address for reading.

Table 14. LSDB

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**

Least Significant Data Byte (LSDB)

Table 15. Broadcast Address Byte

MSB							LSB
1	0	0	0	1	1	1	0

Table 16. Read Sequence

S	MSB	…	R/$\overline{W}$(0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/$\overline{W}$(1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	Address Byte				Command/Access Byte				Sr	Address Byte				MSDB				LSDB			
From master				Slave	From master			Slave	From master				slave	From Slave			Master	From Slave			Master

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Table 17. Control Matrix for Write Commands

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT DATA BYTE								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Write to DAC Input Register																								
0	0	0	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel A
0	0	0	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel B
0	0	0	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel C
0	0	0	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel D
0	0	0	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel E
0	0	0	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel F
0	0	0	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel G
0	0	0	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel H
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	0	0	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode–write to all DAC channels
Select to Update DAC Register																								
0	0	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel A to be updated
0	0	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel B to be updated
0	0	0	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel C to be updated
0	0	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel D to be updated
0	0	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel E to be updated
0	0	0	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel F to be updated
0	0	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel G to be updated
0	0	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel H to be updated
0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Broadcast mode–selects all DAC channels to be updated
Write to DAC Input Registers and Update DAC Register (Individual Software LDAC)																								
0	0	1	1	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel A DAC register
0	0	1	1	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel B and update channel B DAC register
0	0	1	1	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel C and update channel C DAC register
0	0	1	1	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel D and update channel D DAC register
0	0	1	1	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel E and update channel E DAC register
0	0	1	1	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel F and update channel F DAC register
0	0	1	1	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel G and update channel G DAC register
0	0	1	1	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel H and update channel H DAC register
0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	1	1	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode–write to all input registers and update all DAC registers

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Table 17. Control Matrix for Write Commands (continued)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT DATA BYTE								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Write to Select DAC Input Register and Update All DAC Registers (Global Software LDAC)																								
0	0	1	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel A and update all DAC registers
0	0	1	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel B and update all DAC registers
0	0	1	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel C and update all DAC registers
0	0	1	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel D and update all DAC registers
0	0	1	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel E and update all DAC registers
0	0	1	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel F and update all DAC registers
0	0	1	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel G and update all DAC registers
0	0	1	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register of channel H and update all DAC registers
0	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	1	0	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode–write to all input registers and update all DAC registers
Power-Down Register																								
0	1	0	0	X	X	X	X	X	PD1	PD0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	
0	1	0	0	X	X	X	X	X	0	0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	Each DAC bit set to '1' powers on selected DACs
0	1	0	0	X	X	X	X	X	0	1	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} connected to GND through 1kΩ pull-down resistor
0	1	0	0	X	X	X	X	X	1	0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} connected to GND through 100kΩ pull-down resistor
0	1	0	0	X	X	X	X	X	1	1	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} is High Z
Clear Code Register																								
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CL1	CL0	X	X	X	X	
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X	X	Write to clear code register, CLR pin will clear to zero scale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	X	X	Write to clear code register, CLR pin will clear to midscale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X	X	Write to clear code register, CLR pin will clear to full scale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X	X	Write to clear code register disables $\overline{CLR}$ pin
LDAC Register																								
0	1	1	0	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	X	X	X	When all DAC bits are set to '1', selected DACs ignore the $\overline{LDAC}$ pin. When all DAC bits are set to '0', selected DAC registers update according to the $\overline{LDAC}$ pin.

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Table 17. Control Matrix for Write Commands (continued)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT DATA BYTE								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Software Reset																								
0	1	1	1	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset (default). Equivalent to power-on reset (POR).
0	1	1	1	X	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset that sets device into High-Speed mode
0	1	1	1	X	X	X	X	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset that maintains High-Speed mode state
Internal Reference in Regular/Static Mode																								
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	AR	X	X	X	X	
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	Disable internal reference (Regular/Static mode)
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	Enable internal reference (Regular/Static mode). If any DACs are powered on, the reference is on. If all DACS are powered down, then reference is off.
Internal Reference in Flexible Mode																								
1	0	0	1	X	X	X	X	X	TR2	TR1	TR0	X	X	X	X	X	X	X	X	X	X	X	X	
1	0	0	1	X	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	Reference powers down when all DACs power down. Reference powers on when any DACs are powered on.
1	0	0	1	X	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Reference is powered on regardless of DAC power state
1	0	0	1	X	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	Reference is powered down regardless of DAC power state
1	0	0	1	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reference follows Regular/Static mode reference register

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Table 18. Control Matrix for Read Commands

COMMAND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE								LEAST SIGNIFICANT DATA BYTE								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Input Register																								
0	0	0	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel A
0	0	0	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel B
0	0	0	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel C
0	0	0	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel D
0	0	0	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel E
0	0	0	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel F
0	0	0	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel G
0	0	0	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel H
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code
DAC Register																								
0	0	0	1	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC A DAC register
0	0	0	1	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC B DAC register
0	0	0	1	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC C DAC register
0	0	0	1	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC D DAC register
0	0	0	1	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC E DAC register
0	0	0	1	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC F DAC register
0	0	0	1	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC G DAC register
0	0	0	1	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC H DAC register
0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code
Power Down Register																								
0	1	0	0	X	X	X	X	0	0	0	0	0	0	PD1	PD0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Read power down register
Clear Code Register																								
0	1	0	1	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CL1	CL0	Read clear code register
LDAC Register																								
0	1	1	0	X	X	X	X	0	0	0	0	0	0	0	0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Read LDAC register
Internal Reference in Regular/Static Mode																								
1	0	0	0	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AR	Read reference register
Internal Reference in Flexible Mode																								
1	0	0	1	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	TR2	TR1	TR0	Read additional reference register

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POWER-ON RESET TO ZERO-SCALE OR MID-SCALE

The DAC7678 contains a power-on reset (POR) circuit that controls the output voltage during power-on. For devices housed in the TSSOP package, at power-on, all DAC registers are filled with zeros and the output voltages of all DAC channels are set to zero-scale. For devices housed in the QFN package, all DAC registers are set to have all DAC channels power on depending of the state of the RSTSEL pin.

The RSTSEL pin value is read at power-on and should be set prior to or simultaneously with AV_{DD}. For RSTSEL set to AV_{DD}, the DAC channels are loaded with midscale code. If RSTSEL is set to ground, the DAC channels are loaded with zero-scale code. All DAC channels remain in this state until a valid write sequence and load command are sent to the respective DAC channel. The power-on reset function is useful in applications where it is important to know the output state of each DAC while the device is in the process of powering on.

The internal reference is powered off/down by default, and remains that way until a valid reference-change command is executed.

LDAC FUNCTIONALITY

The DAC7678 offers both software and hardware simultaneous updates and control functions. The DAC double-buffered architecture is designed so that new data can be entered for each DAC without disturbing the analog outputs.

The DAC7678 data updates can be performed either in *synchronous* or *asynchronous* mode.

In *synchronous* mode, data are updated on the falling edge of the acknowledge signal that follows LSDB. For *synchronous* mode updates, the LDAC pin is not required and must be connected to GND permanently.

In *asynchronous* mode, the LDAC pin is used as a negative-edge-triggered timing signal for *asynchronous* DAC updates. Multiple single-channel updates can be performed in order to set different channel buffers to desired values and then make a falling edge on the LDAC pin. The data buffers of all the channels must be loaded with the desired data before an LDAC falling edge. After a high-to-low LDAC transition, all DACs are simultaneously updated with the last contents of the corresponding data buffers. If the contents of a data buffer are not changed by the serial interface, the corresponding DAC output remains unchanged after the LDAC trigger.

Alternatively, all DAC outputs can be updated simultaneously using the built-in LDAC software function. The LDAC register offers additional flexibility and control, giving the ability to select which DAC channel(s) should be updated simultaneously when the hardware LDAC pin is being brought low. The LDAC register is loaded with an 8-bit word (DB15 to DB8) using control bits C3, C2, C1, and C0. The default value for each bit, and therefore each DAC channel, is zero and the external LDAC pin operates in normal mode. If the LDAC register bit for a selected DAC channel is set to '1', that DAC channel ignores the external LDAC pin and updates only through the software LDAC command. If, however, the LDAC register bit is set to '0', the DAC channel is controlled by the external LDAC pin.

This combination of a software and hardware simultaneous update function is particularly useful in applications where only selective DAC channels are to be updated simultaneously, while keeping the other channels unaffected and updating those channels synchronously.

POWER-DOWN MODES

The DAC7678 has two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. For more information on powering down the reference see the *Enable/Disable Internal Reference* section.

DAC Power-Down Commands

The DAC7678 uses four modes of operation. These modes are accessed by using control bits C3, C2, C1, and C0. The control bits must be set to '0100'. When the control bits are set correctly, the four different power-down modes are software programmable by setting bits PD0 (DB13) and PD1 (DB14) in the control register. Table 19 shows how to control the operating mode with data bits PD0 (DB13) and PD1 (DB14). The DAC7678 treats the power-down condition as data; all the operational modes are still valid for power down. It is possible to broadcast a power-down condition to all the DAC7678s in a system. It is also possible to power-down a channel and update data on other channels. Furthermore, it is possible to write to the DAC register/buffer of the DAC channel that is powered down. When the DAC channel is then powered on, it will contain this new value.

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When both the PD0 and PD1 bits are set to '0', the device works normally with its typical consumption of 1.49 mA at 5.5V. The reference is included with the operation of all eight channels. However, for the three power-down modes, the supply current falls to 0.42 µA at 5.5V (0.25 µA at 2.7V). Not only does the supply current fall, but the output stage also switches internally from the output amplifier to a resistor network of known values as shown in Figure 93.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As described in Table 19, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or open-circuited (High-Z). In other words, C3, C2, C1, and C0 = '0100' and DB14 and DB13 = '11' represent a power-down condition with High-Z output impedance for a selected channel. DB14 and DB13 = '01' represents a power-down condition with 1kΩ output impedance and '10' represents a power-down condition with 100kΩ output impedance.

Table 19. DAC Operating Modes

PD1 (DB14)	PD0 (DB13)	DAC OPERATING MODES
0	0	Power on selected DACs
0	1	Power down selected DACs, 1kΩ to GND
1	0	Power down selected DACs, 100kΩ to GND
1	1	Power down selected DACs, High-Z to GND

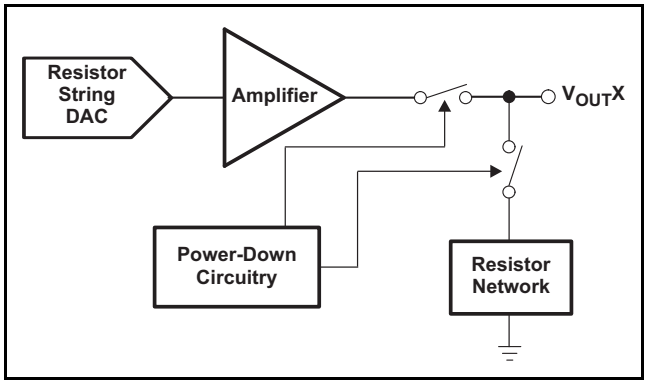

Figure 93. Output Stage During Power-Down

CLEAR CODE REGISTER AND CLR PIN

The DAC7678 contains a clear code register. The clear code register can be accessed via the serial interface (I^2C) and is user configurable. Bringing the CLR pin low clears the contents of all DAC registers and all DAC buffers and replaces the code with the code determined by the clear code register. The clear code register can be written to by applying the commands shown in Table 17. The default setting of the clear code register sets the output of all DAC channels to 0V when the CLR pin is brought low. The CLR pin is falling-edge triggered; therefore, the device exits clear code mode on the falling edge of the acknowledge signal that follows LSDB of the next write sequence. If the CLR pin is executed (brought low) during a write sequence, this write sequence is aborted and the DAC registers and DAC buffers are cleared as described above.

When performing a software reset of the device, the clear code register is reset to the default mode (DB5 = '0', DB4 = '0'). Setting the clear code register to DB4 = '1' and DB5 = '1' ignores any activity on the external CLR pin.

SOFTWARE RESET FUNCTION

The DAC7678 contains a software reset feature. When the software reset feature is executed, the device (all DAC channels) are reset to the power-on reset code. All registers inside the device are reset to the respective default settings. The DAC7678 has an additional feature of switching straight to high speed mode after reset. Table 20 shows all the different modes of the software reset function.

Table 20. Software Reset Modes

DB15	DB14	OPERATING MODES
0	0	Default Software reset. Equivalent to Power-on-Reset
x	1	Software reset and set part in High Speed Mode
1	0	Software reset and maintain High Speed Mode state

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OPERATING EXAMPLES: DAC7678

For the following examples X = don't care; value can be either '0' or '1'.

I²C Standard and Fast mode examples (ADDR0 and LDAC pin tied low) (TSSOP package)

Example 1: Write Mid Scale to Data Buffer A and Update Channel A Output

Start	Address	ACK	Command and Access Byte	ACK	MSDB	ACK	LSDB	ACK	Stop
S	1001 0000		0000 0000		1000 0000		0000 XXXX		P

Channel A updates to Mid Scale after the falling edge of the last ACK cycle

Example 2: Power-Down Channel B, C, and H with Hi-Z Output

Start	Address	ACK	Command and Access Byte	ACK	MSDB	ACK	LSDB	ACK	Stop
S	1001 0000		0100 XXXX		X111 0000		110X XXXX		P

Example 3: Read-back the value of the input register of Channel G

Start	Address	ACK	Command and Access Byte	ACK	Repeated Start	Address	ACK	MSDB (from DAC7678)	ACK	LSDB (from DAC7678)
S	1001 0000		0000 0110		Sr	1001 0001		XXXX XXXX		XXXX 0000

Example 4: Write multiple bytes of data to Channel F
Write Full Scale and then Quarter Scale to Channel F

Start	Address	ACK	Command and Access Byte	ACK	MSDB	ACK	LSDB	ACK*	MSDB	ACK	LSDB	ACK**	Stop
S	1001 0000		0000 0101		1111 1111		1111 XXXX		0100 0000		0000 XXXX		P

Channel F updates to Full Scale after the falling edge of the 4th ACK* cycle and then Channel F updates to quarter scale after falling edge of the last ACK** cycle.

I²C High Speed mode example (ADDR0 and LDAC pin tied low) (TSSOP package)

Example 5: Write Mid Scale and then Full Scale to all DAC channels

Start	HS Master Code	NOT ACK	Repeated Start	Address	ACK	Command and Access Byte	ACK	MSDB	ACK	LSDB	ACK	MSDB	ACK	LSDB	ACK	Stop
S	0000 1000		Sr	1001 0000		0011 1111		1000 0000		0000 XXXX		1111 1111		1111 XXXX		P

All Channels update to Mid Scale after the falling edge of the 4th ACK cycle and then all Channels update to Full scale after falling edge of the last ACK cycle.

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APPLICATION INFORMATION

INTERNAL REFERENCE

The internal reference of the DAC7678 does not require an external load capacitor for stability because it is stable with any capacitive load. However, for improved noise performance, an external load capacitor of 100nF or larger connected to the V_{REFIN}/V_{REFOUT} output is recommended. Figure 94 shows the typical connections required for operation of the DAC7678 internal reference. A supply bypass capacitor at the AV_{DD} input is also recommended.

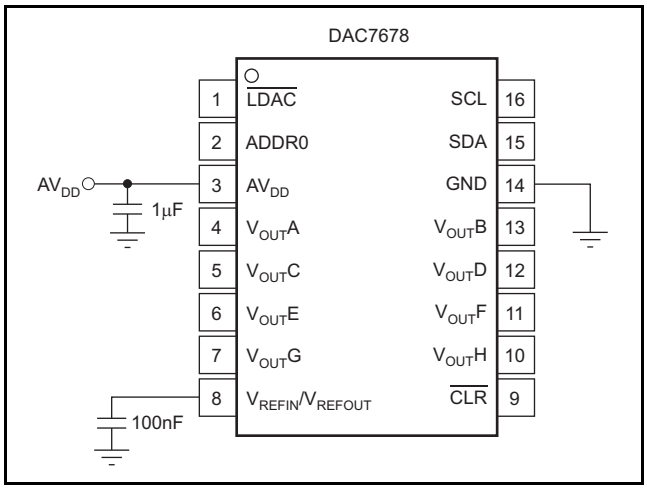

Figure 94. Typical Connections for Operating the DAC7678 Internal Reference

Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5mV above the reference output voltage in an unloaded condition. For loaded conditions, refer to the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, dc PSRR) is also exceptional. Within the specified supply voltage range of 2.7V to 5.5V, the variation at V_{REFIN}/V_{REFOUT} is less than 100 µV/V; see the Typical Characteristics.

Temperature Drift

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the box method described by Equation 3:

$$\text{Drift Error} = \left(\frac{V_{REF_MAX} - V_{REF_MIN}}{V_{REF} \times T_{RANGE}} \right) \times 10^6 \,(\text{ppm/°C}) \quad (3)$$

Where:

V_{REF_MAX} = maximum reference voltage observed within temperature range T_{RANGE}.

V_{REF_MIN} = minimum reference voltage observed within temperature range T_{RANGE}.

V_{REF} = 2.5V, target value for reference output voltage.

The internal reference features an exceptional maximum drift coefficient of 25ppm/°C from –40°C to 125°C. Temperature drift results are summarized in the Typical Characteristics.

Noise Performance

Typical 0.1Hz to 10Hz voltage noise can be seen in Figure 7, Internal Reference Noise. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the ac performance. The output noise spectrum at V_{REFIN}/V_{REFOUT} without any external components is depicted in Figure 6, Internal Reference Noise Density vs Frequency. Internal reference noise impacts the DAC output noise; see the DAC Noise Performance section for more details.

Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 5. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are summarized in the Typical Characteristics. Force and sense lines should be used for applications that require improved load regulation.

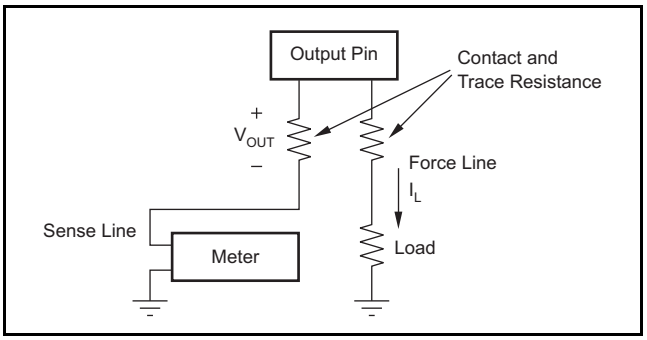

Figure 95. Accurate Load Regulation of the DAC7678 Internal Reference

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Long-Term Stability

Long-term stability/aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses (see Figure 3, the typical long-term stability curve). The typical drift value for the internal reference is 100ppm from 0 hours to 2160 hours. This parameter is characterized by powering-up 19 units and measuring them at regular intervals for a period of 2160 hours.

Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at 25°C, cycling the device through the operating temperature range, and returning to 25°C. Hysteresis is expressed by Equation 4:

$$V_{HYST} = \left(\frac{|V_{REF_PRE} - V_{REF_POST}|}{V_{REF_NOM}} \right) \times 10^6 (ppm/°C) \quad (4)$$

Where:

V_{HYST} = thermal hysteresis
V_{REF_PRE} = output voltage measured at 25°C pre-temperature cycling
V_{REF_POST} = output voltage measured after the device cycles through the temperature range of –40°C to 125°C, and returns to 25°C.

DAC NOISE PERFORMANCE

Typical noise performance for the DAC7678 with the internal reference enabled is shown in Figure 47. Output noise spectral density at the V_{OUTX} pin versus frequency is depicted in Figure 47 for full-scale, midscale, and zero-scale input codes. The typical noise density for midscale code is 290nV/√Hz at 1kHz and 117nV/√Hz at 100 kHz when internal reference is enabled. The typical noise density reduces to 104nV/√Hz at 1kHz for mid scale code with external reference as shown in Figure 48. High-frequency noise can be improved by filtering the reference noise. Integrated output noise between 0.1Hz and 10Hz is close to 3µVPP (midscale), as shown in Figure 49.

BIPOLAR OPERATION USING THE DAC7678

The DAC7678 family of products is designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 96. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated with Equation 5.

$$V_{OUT} = \left(V_{REF} \times Gain \times \left(\frac{D_{IN}}{2^n} \right) \times \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \times \left(\frac{R2}{R1} \right) \right) \quad (5)$$

Where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 4095 (12 bit)
n = resolution in bits
Gain = 1 when External Reference is used and 2 when internal reference is used.

$$V_{OUT} = \left(\frac{10 \times D_{IN}}{2^n} \right) - 5V \quad (6)$$

This result has an output voltage range of ±5V with 000h corresponding to a -5V output and FFFh corresponding to a +5V output for the 12 bit DAC7678.

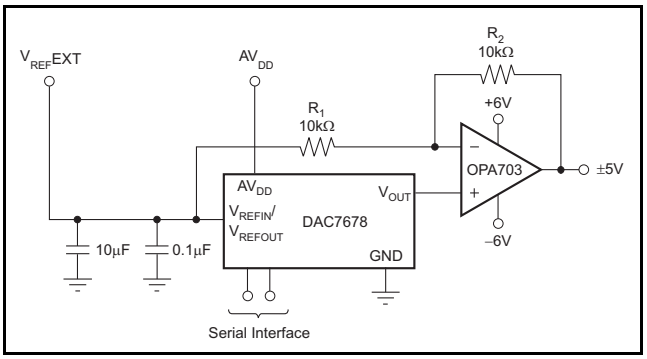

Figure 96. Bipolar Output Range Using External Reference at 5V

MICROPROCESSOR INTERFACING

A basic connection diagram to the SCL and SDA pins of the DAC7678 is shown in Figure 97. The DAC7678 interfaces directly to standard mode, fast mode and high speed mode of 2-Wire compatible serial interfaces. The DAC7678 does not perform clock stretching (pulling SCL low), as a result it is not necessary to provide for this function unless other devices on the same bus require this function. Pull-up resistors are required on both the SDA and SCL lines as the bus-drivers are open-drain. The size of these pull-up resistors depends on the operating speed and capacitance of the bus lines. Higher value resistors consume less power but increase transition time on the bus limiting the bus speed. Long bus lines have higher capacitance and require smaller pull-up resistors to compensate. The resistors should not be too small; if they are, bus drivers may not be able to pull the bus lines low.

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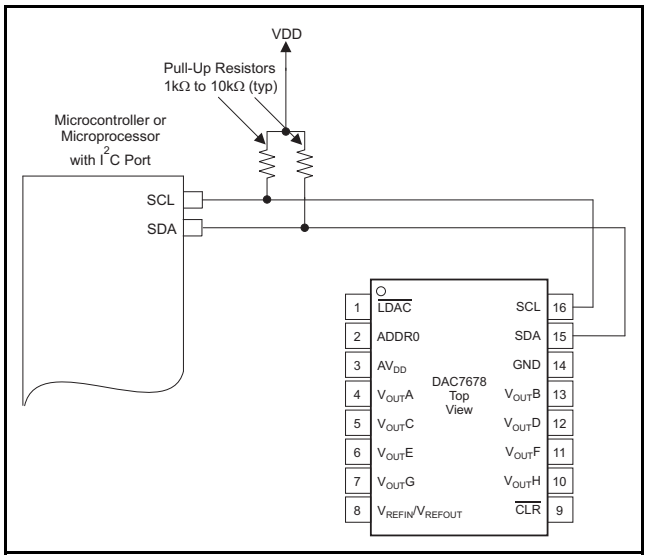

Figure 97. Typical Connections of the DAC7678

CONNECTING MULTIPLE DEVICES

Multiple devices of DAC7678 family can be connected on the same bus. Using the address pin, the DAC7678 can be set to one of three different I^2C addresses for the TSSOP package and one of eight addresses for the QFN package. An example showing three DAC7678 devices in TSSOP package is shown if Figure 98. Note that only one set of pull-up resistors is needed per bus. The pull-up resistor values may need to be lowered slightly to compensate for the additional bus capacitance due to multiple devices and increased bus length.

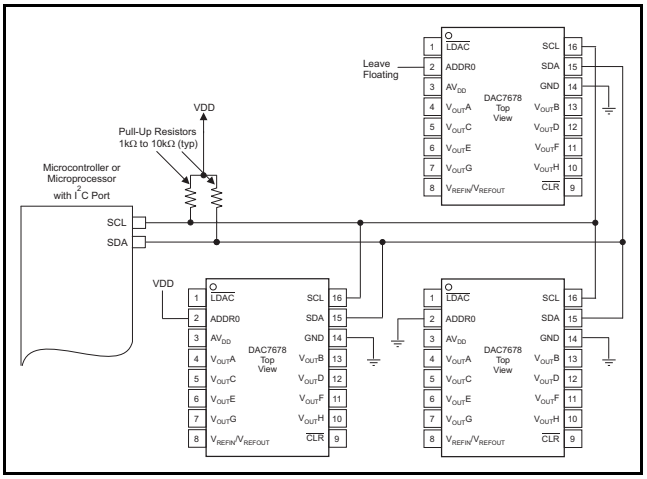

Figure 98. Typical Connections of the Multiple DAC7678 on the Same Bus

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PARAMETER DEFINITIONS

With the increased complexity of many different specifications listed in product data sheets, this section summarizes selected specifications related to digital-to-analog converters.

STATIC PERFORMANCE

Static performance parameters are specifications such as differential nonlinearity (DNL) or integral nonlinearity (INL). These are dc specifications and provide information on the accuracy of the DAC. They are most important in applications where the signal changes slowly and accuracy is required.

Resolution

Generally, the DAC resolution can be expressed in different forms. Specifications such as IEC 60748-4 recognize the numerical, analog, and relative resolution. The numerical resolution is defined as the number of digits in the chosen numbering system necessary to express the total number of steps of the transfer characteristic, where a step represents both a digital input code and the corresponding discrete analogue output value. The most commonly-used definition of resolution provided in data sheets is the numerical resolution expressed in bits.

Least Significant Bit (LSB)

The least significant bit (LSB) is defined as the smallest value in a binary coded system. The value of the LSB can be calculated by dividing the full-scale output voltage by 2^n, where *n* is the resolution of the converter.

Most Significant Bit (MSB)

The most significant bit (MSB) is defined as the largest value in a binary coded system. The value of the MSB can be calculated by dividing the full-scale output voltage by 2. Its value is one-half of full-scale.

Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity (INL) is defined as the maximum deviation between the real transfer function and a straight line passing through the endpoints of the ideal DAC transfer function. INL is measured in LSBs.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is defined as the maximum deviation of the real LSB step from the ideal 1LSB step. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. If the DNL is less than 1LSB, the DAC is said to be monotonic.

Full-Scale Error

Full-scale error is defined as the deviation of the real full-scale output voltage from the ideal output voltage while the DAC register is loaded with the full-scale code (0xFFF). Ideally, the output should be AVDD – 1 LSB. The full-scale error is expressed in percent of full-scale range (%FSR).

Offset Error

The offset error is defined as the difference between actual output voltage and the ideal output voltage in the linear region of the transfer function. This difference is calculated by using a straight line defined by two codes (code 30 and 4050). Since the offset error is defined by a straight line, it can have a negative or positive value. Offset error is measured in mV.

Zero-Code Error

The zero-code error is defined as the DAC output voltage, when all '0's are loaded into the DAC register. Zero-scale error is a measure of the difference between actual output voltage and ideal output voltage (0V). It is expressed in mV. It is primarily caused by offsets in the output amplifier.

Gain Error

Gain error is defined as the deviation in the slope of the real DAC transfer characteristic from the ideal transfer function. Gain error is expressed as a percentage of full-scale range (%FSR).

Full-Scale Error Drift

Full-scale error drift is defined as the change in full-scale error with a change in temperature. Full-scale error drift is expressed in units of µV/°C.

Offset Error Drift

Offset error drift is defined as the change in offset error with a change in temperature. Offset error drift is expressed in µV/°C.

Zero-Code Error Drift

Zero-code error drift is defined as the change in zero-code error with a change in temperature. Zero-code error drift is expressed in µV/°C.

Gain Temperature Coefficient

The gain temperature coefficient is defined as the change in gain error with changes in temperature. The gain temperature coefficient is expressed in ppm of FSR/°C.

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Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is defined as the ratio of change in output voltage to a change in supply voltage for a full-scale output of the DAC. The PSRR of a device indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is measured in decibels (dB).

Monotonicity

Monotonicity is defined as a slope whose sign does not change. If a DAC is monotonic, the output changes in the same direction or remains at least constant for each step increase (or decrease) in the input code.

DYNAMIC PERFORMANCE

Dynamic performance parameters are specifications such as settling time or slew rate, which are important in applications where the signal rapidly changes and/or high frequency signals are present.

Slew Rate

The output slew rate (SR) of an amplifier or other electronic circuit is defined as the maximum rate of change of the output voltage for all possible input signals.

$$SR = \max\left(\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right)$$

Where $\Delta V_{OUT}(t)$ is the output produced by the amplifier as a function of time *t*.

Output Voltage Settling Time

Settling time is the total time (including slew time) for the DAC output to settle within an error band around its final value after a change in input. Settling times are specified to within ±0.003% (or whatever value is specified) of full-scale range (FSR).

Code Change/Digital-to-Analog Glitch Energy

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolt-seconds (nV-s), and is measured when the digital input code is changed by 1LSB at the major carry transition.

Digital Feed-through

Digital feed-through is defined as impulse seen at the output of the DAC from the digital inputs of the DAC. It is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus; that is, from all '0's to all '1's and vice versa.

Channel-to-Channel DC Crosstalk

Channel-to-channel dc crosstalk is defined as the dc change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on one DAC channel while monitoring another DAC channel remains at midscale. It is expressed in LSB.

DAC Output Noise Density

Output noise density is defined as internally-generated random noise. Random noise is characterized as a spectral density (nV/$\sqrt{Hz}$). It is measured by loading the DAC to midscale and measuring noise at the output.

DAC Output Noise

DAC output noise is defined as any voltage deviation of DAC output from the desired value (within a particular frequency band). It is measured with a DAC channel kept at midscale while filtering the output voltage within a band of 0.1Hz to 10Hz and measuring its amplitude peaks. It is expressed in terms of peak-to-peak voltage (Vpp).

Full-Scale Range (FSR)

Full-scale range (FSR) is the difference between the maximum and minimum analog output values that the DAC is specified to provide; typically, the maximum and minimum values are also specified. For an *n*-bit DAC, these values are usually given as the values matching with code 0 and 2^n–1.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC7678 offers single-supply operation, and is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output. As a result of the single ground pin of the DAC7678, all return currents(including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to AVDD should be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and

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analog output. As with the GND connection, AVDD should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1µF to 10µF capacitor and 0.1µF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors – all designed to essentially low-pass filter the supply and remove the high-frequency noise.

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REVISION HISTORY

Changes from Original (February 2010) to Revision A **Page**

- Changed the data sheet From: Product Preview status To : Production 1

Changes from Revision A (August 2010) to Revision B **Page**

- Changed in Table 17, Power-Down Register section, bit DB12 through bit DB5 values have been reversed 32
- Changed in Table 18, Power-Down Register section, bit DB7 through bit DB0 values have been reversed 34

Changes from Revision B (July 2012) to Revision C **Page**

- Changed the formatting so the title would straddle 2 columns, paragraph in first column and Table 13 in second column. lso formatted Table 14 and 15 to be 2 column. 29
- Changed "to read any register other than the power-down register..." to "to read any register..." in the DAC7678 I^2C READ SEQUENCE section. 30

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DAC7678SPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7678	Samples
DAC7678SPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7678	Samples
DAC7678SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7678	Samples
DAC7678SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7678	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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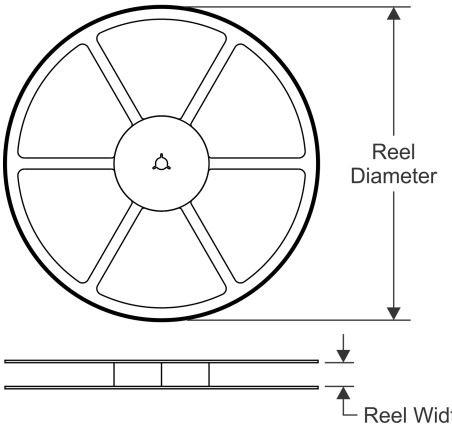
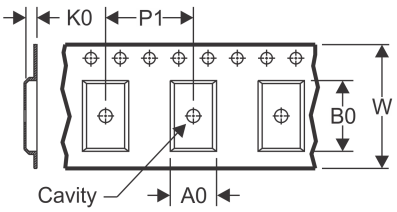
TAPE AND REEL INFORMATION

REEL DIMENSIONS

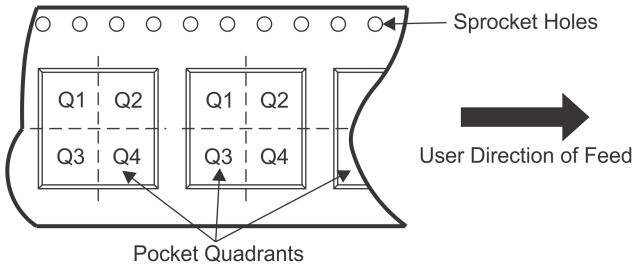


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

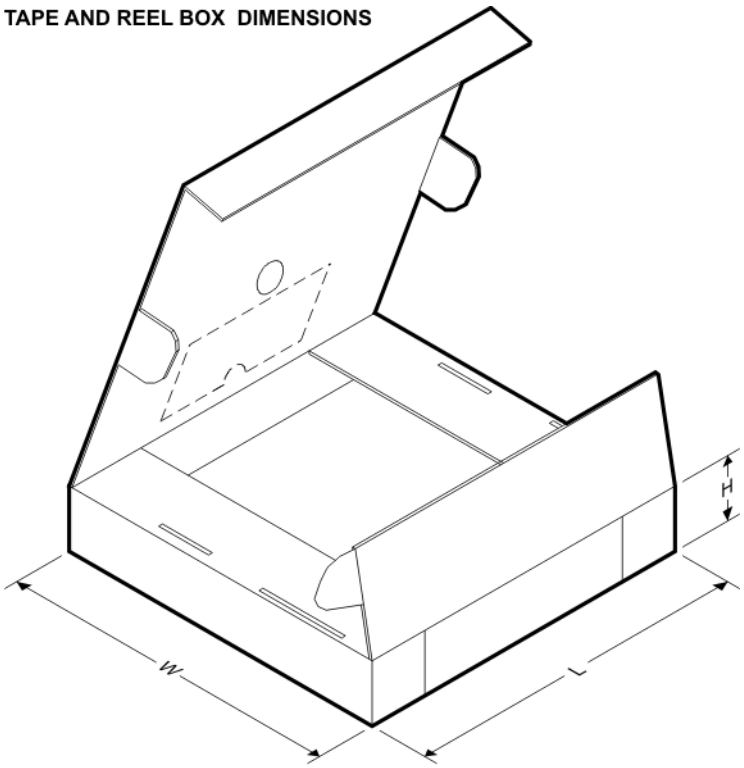
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7678SPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC7678SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DAC7678SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



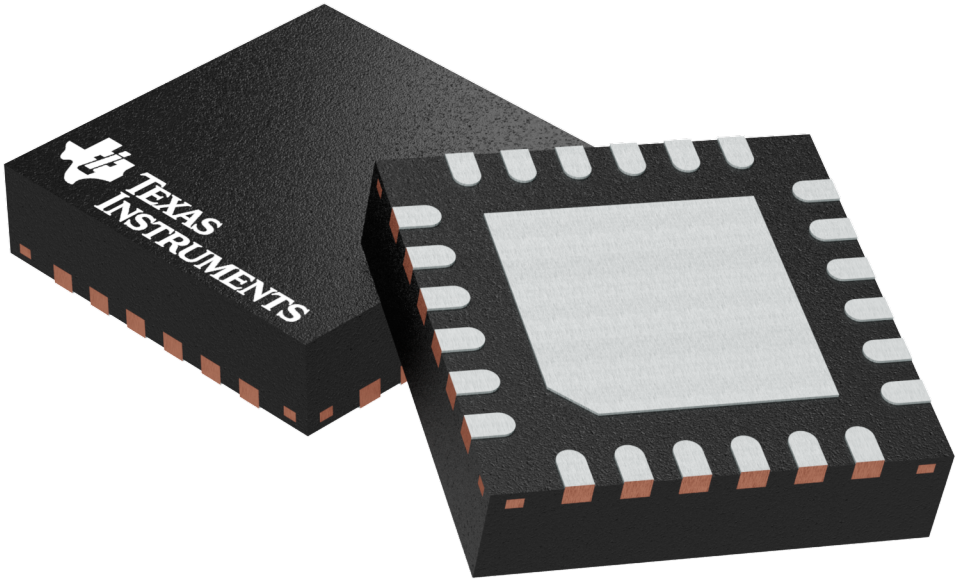
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7678SPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
DAC7678SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DAC7678SRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



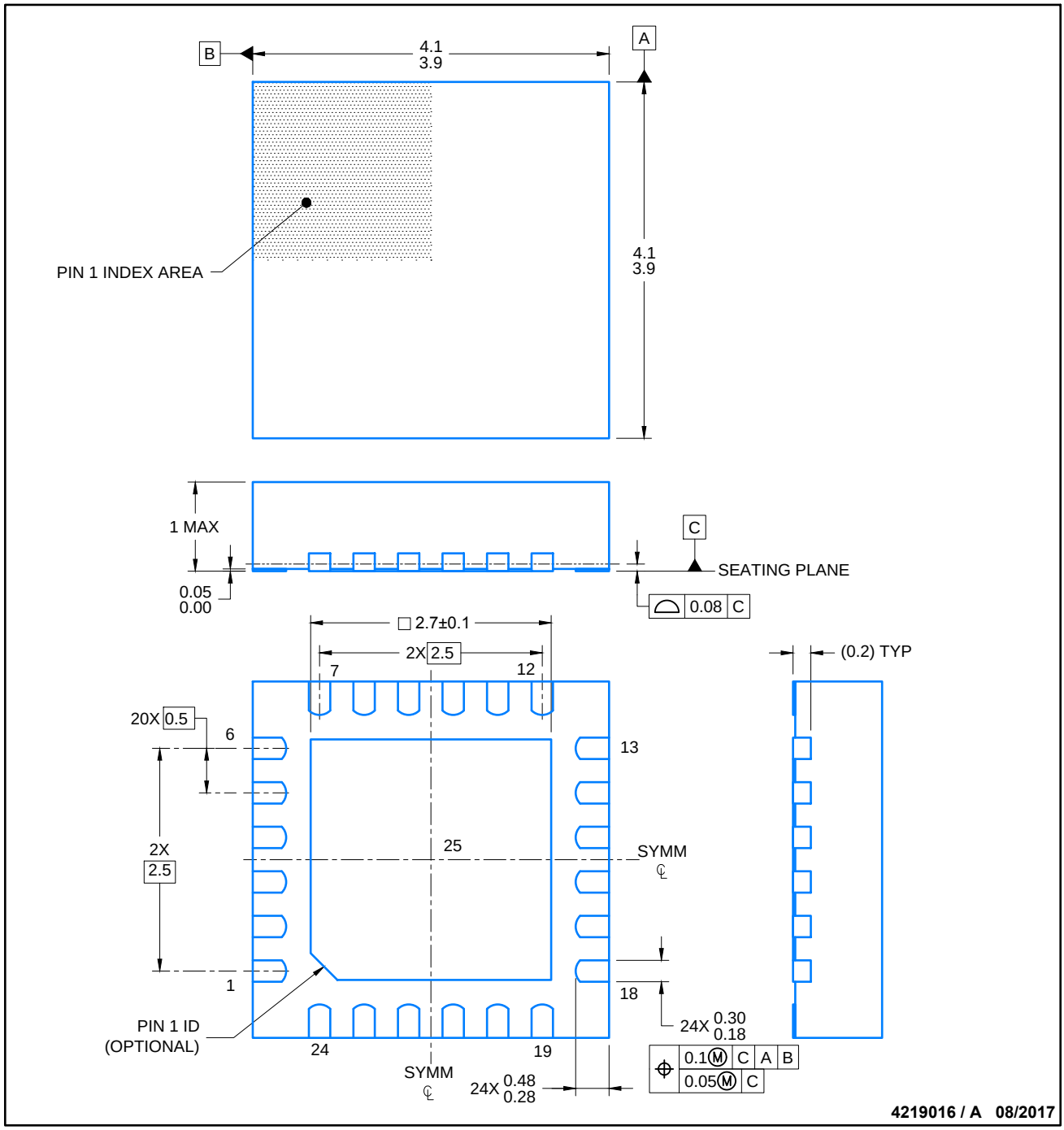
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024H

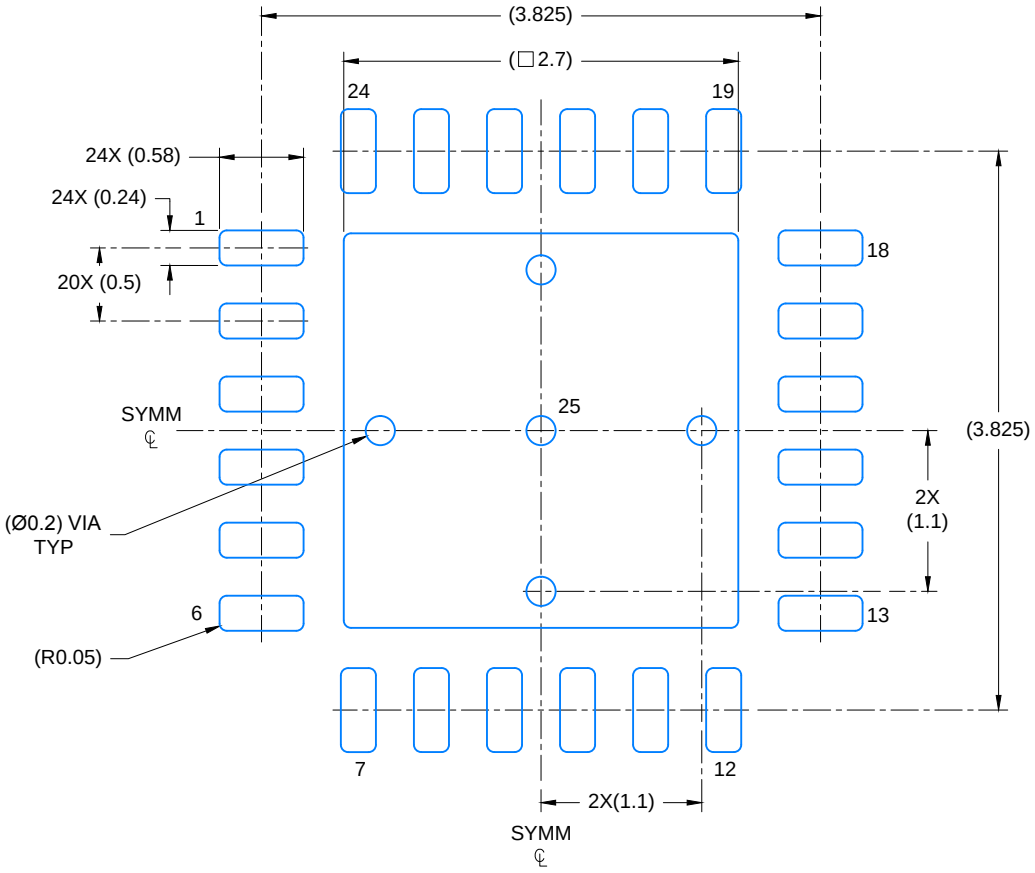
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



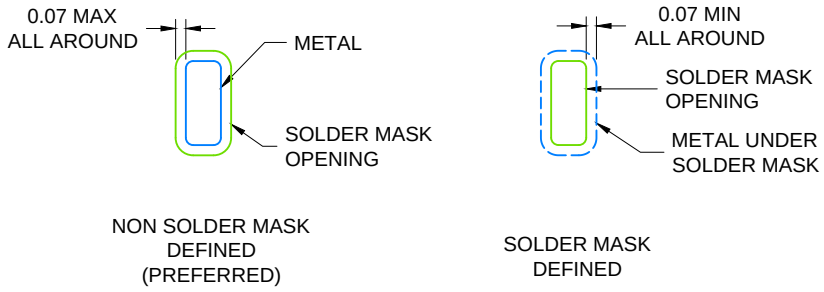
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

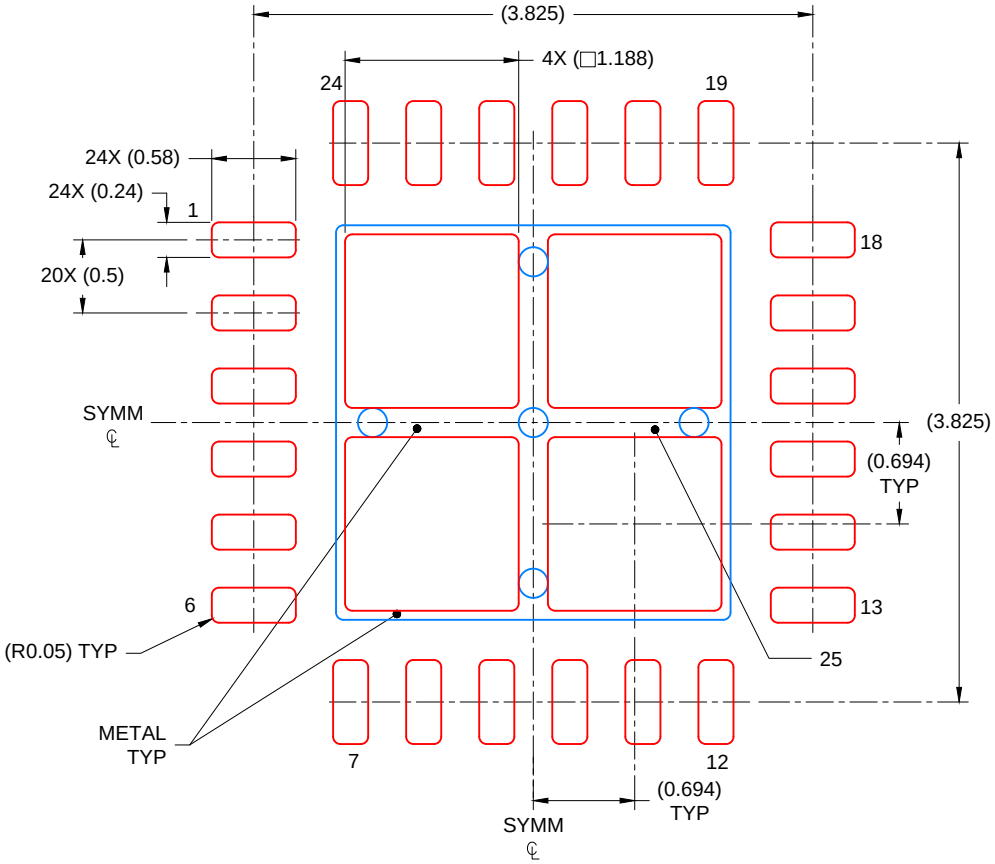


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

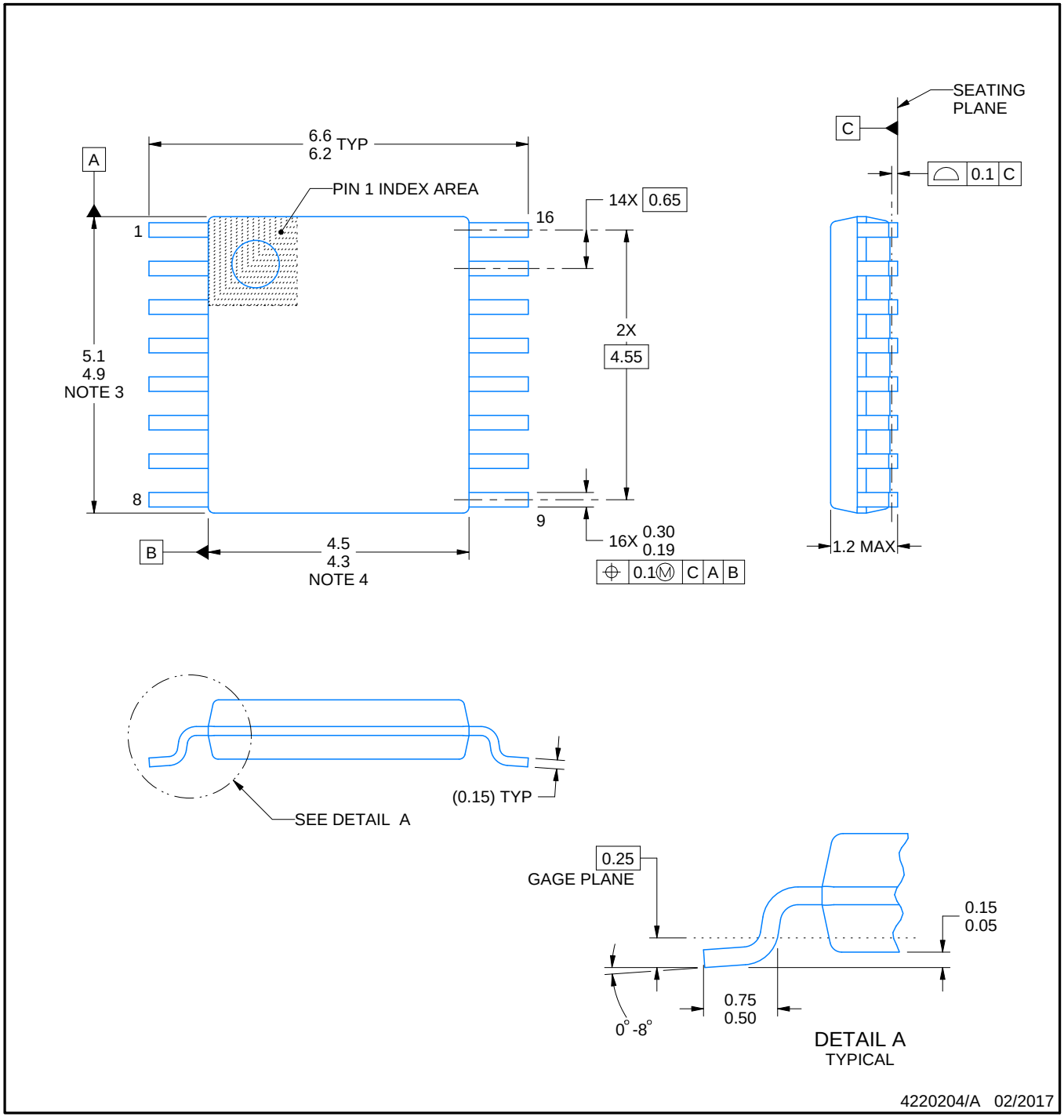
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGE OUTLINE

PW0016A

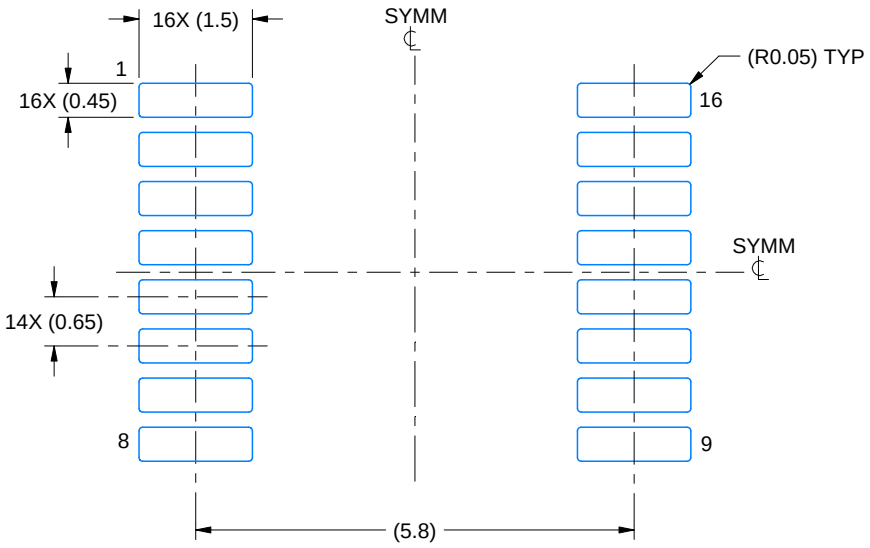
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



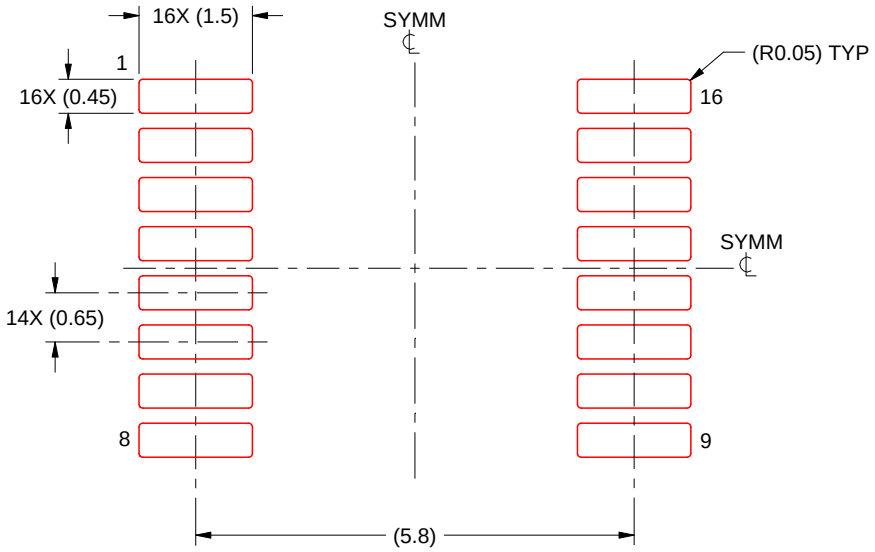
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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