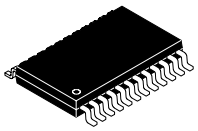
THE DATASHEET OF

TPS2345PW



SLUS503B – MARCH 2002 – REVISED AUGUST 2002

CompactPCI® HOT SWAP POWER MANAGER

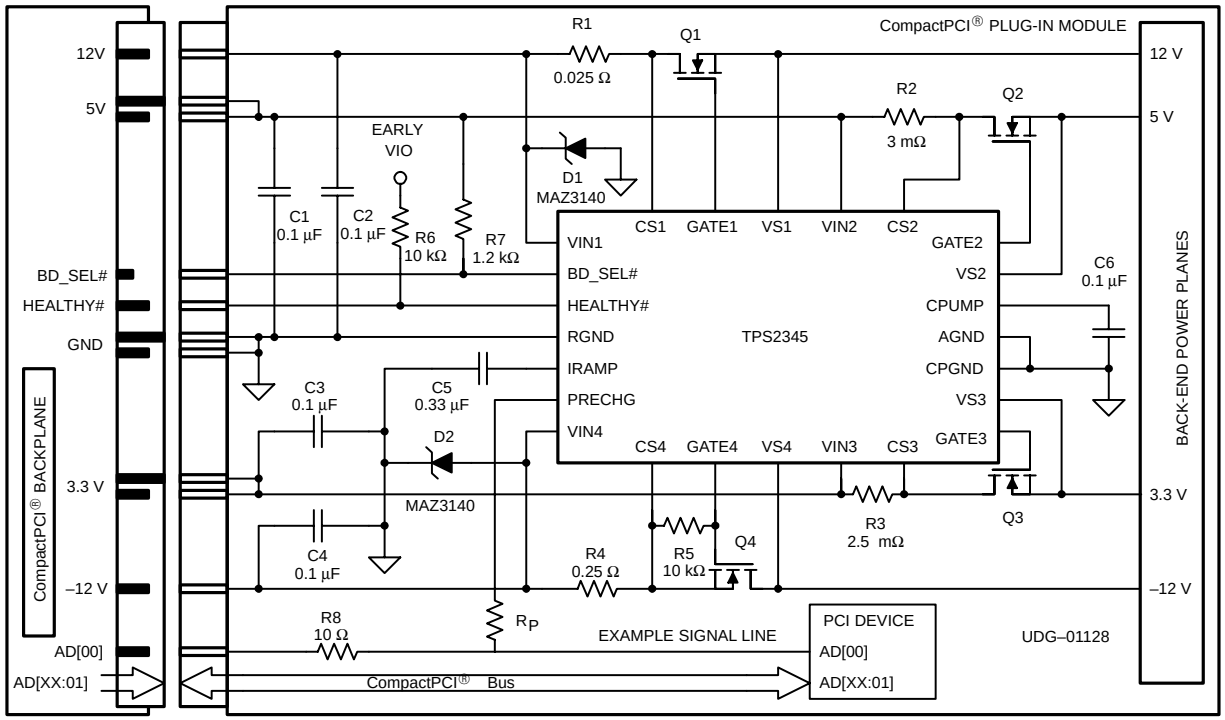
FEATURES

- **Enables Hot Swap in CompactPCI® High Availability Systems**
- **Programmable Current Slew Rate**
- **Power Supply Sequencing**
- **Sense Resistors Set Peak Current (IMAX)**
- **Overcurrent Circuit Breaker at 2× IMAX**
- **Precharge Output**
- **HEALTHY# Signal of Board Power Good**
- **BD_SEL# Signal for Peripheral Enable**
- **On-Chip Charge Pump**
- **Low Sleep Mode Current**
- **Undervoltage Lockout (UVLO)**
- **Minimal External Parts Count**
- **24-pin TSSOP Package**

DESCRIPTION

The TPS2345 CompactPCI® Hot Swap Power Manager (HSPM) provides highly-integrated supply control of three positive (3.3-V, 5-V, and 12-V) and one negative (–12-V) supply rails with a minimum number of external components. A linear current amplifier (LCA) in each of the four device channels provides closed-loop control of load current during insertion and extraction events. This allows the designer to configure the plug-in card's maximum inrush slew rate and magnitude according to the requirements of the CompactPCI® Hot Swap Specification PICMG 2.1.

TYPICAL APPLICATION



description (continued)

Fully programmed sequencing control ramps the back-end plane voltages in order, and during shutdown from a healthy state, turns off the back-end supplies in the reverse order. In addition, electronic circuit breakers provide continuous protection for the system supplies during the plug-in operation. The control and status pins can interface directly to the back-plane BD_SEL# and HEALTHY# signals. A precharge pin (PRECHG) provides a 1-V bias supply for the I/O signals.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range, VIN1, VIN2, VIN3, BD_SEL#, HEALTHY#, PRECHG . . . . . –0.3 V to 15 V
VS1, VS2, VS3, CS1, CS2, CS3 . . . . . –0.3 V to V_{IN} +0.3 V of corresponding channel
CPUMP, GATE1, GATE2, GATE3 . . . . . –0.3 V to 25 V
VIN4, VS4, GATE4, CS4 . . . . . –15 V to 0.3 V
IRAMP . . . . . –0.3 V to $V_{I(VIN1)}$ +0.3 V
Operating junction temperature range, T_J . . . . . –55°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

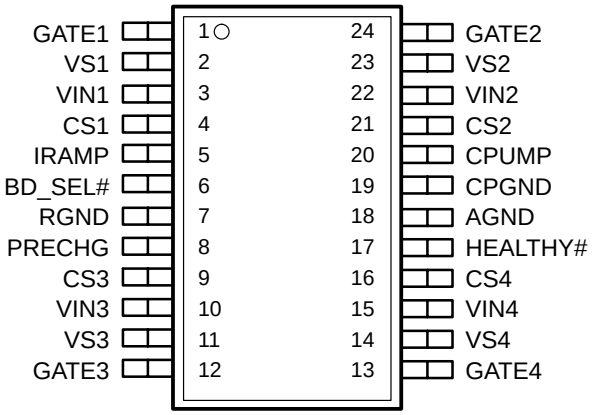
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, and negative out of the specified terminal.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP (PW)
–40°C to 85°C	TPS2345PW

†The PW package is available taped and reeled. Add TR suffix to device type (e.g. TPS2345PWTR) to order quantities of 2,000 devices per reel and 90 units per tube.

PW PACKAGE
(TOP VIEW)



electrical characteristics $V_{I(VIN1)}$ = 12 V, $V_{I(VIN2)}$ = 5 V, $V_{I(VIN3)}$ = 3.3 V, $V_{I(VIN4)}$ = –12 V, T_A = –40°C to 85°C (unless otherwise noted)

input supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, VIN1			6	8	mA
I_{CC2}	Supply current, VIN2			1	2	
I_{CC3}	Input current, VIN3			0.5	1	
I_{CC4}	Input current, VIN4			–1.5	–3	
$I_{CC1(SLP)}$	Sleep mode current, VIN1	$V_{I(BD\_SEL\#)}$ = 5 V		0.5		
$I_{CC2(SLP)}$	Sleep mode current, VIN2	$V_{I(BD\_SEL\#)}$ = 5 V		1		
$I_{CC3(SLP)}$	Sleep mode current, VIN3	$V_{I(BD\_SEL\#)}$ = 5 V		100		µA
$I_{CC4(SLP)}$	Sleep mode current, VIN4	$V_{I(BD\_SEL\#)}$ = 5 V		–400		

charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(MAX)}$	Maximum output voltage	$I_{O(CPUMP)}$ = –25 µA	17		23	V
I_{SOURCE}	Peak output current	$V_{O(CPUMP)}$ = 15 V		–120		µA
Z_O	Charge pump source impedance	$\frac{1\ V}{\left(I_{O\ (CPUMP=17\ V)}\right) - \left(I_{O\ (CPUMP=16\ V)}\right)}$		200		kΩ

precharge output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(PCHG)1}$	Output voltage	$V_{I(VIN2)}$ = 4 V, $V_{I(VIN1/3/4)}$ = 0 V	0.9	1	1.1	V
$V_{O(PCHG)2}$	Output voltage, sourcing	$V_{I(VIN2)}$ = 4 V, $V_{I(VIN1/3/4)}$ = 0 V, $I_{O(PRECHG)}$ = –5 mA	0.8	1	1.2	
$V_{O(PCHG)3}$	Output voltage, sinking	$V_{I(VIN2)}$ = 4 V, $V_{I(VIN1/3/4)}$ = 0 V, $I_{O(PRECHG)}$ = 5 mA	0.8	1	1.2	
t_{START}	Startup time	$V_{I(VIN2)}$ = 4 V, $V_{I(VIN1/3/4)}$ = 0 V		200		µs

linear current amplifiers 1, 2, 3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{MAX1}	IMAX sense voltage (VIN1 – CS1)		16	20	24	mV
V_{MAX2}	IMAX sense voltage (VIN2 – CS2)		17	20	23	
V_{MAX3}	IMAX sense voltage (VIN3 – CS3)		17	20	23	
I_{PK}	Output peak current		–25		–5	mA
I_{SINK}	Output current sink		0.2		10	
I_{FAULT}	Output current sink	Fault shutdown		150		
V_{OL}	Low-level output voltage	Fault shutdown, $I_{O(GATEx)}$ = 10 mA			0.5	V
V_{OH}	High-level output voltage	$I_{O(GATEx)}$ = –4 µA	V_{CPUMP}–1			

linear current amplifier 4

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VMAX4	IMAX sense voltage (VIN4 – CS4)		–75	–150	–225	mV
I_{OL1}	Output leakage current	Fault shutdown	–10		10	µA
I_{OL2}	Output leakage current	Sleep mode	–10		10	

electrical characteristics $V_{I(VIN1)}$ = 12 V, $V_{I(VIN2)}$ = 5 V, $V_{I(VIN3)}$ = 3.3 V, $V_{I(VIN4)}$ = –12 V, T_A = –40°C to 85°C (unless otherwise noted) (continued)

overcurrent comparators 1, 2, 3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OC1}	Overcurrent threshold voltage (VIN1 – CS1)		34	45	56	mV
V_{OC2}	Overcurrent threshold voltage (VIN2 – CS2)		29	40	51	
V_{OC3}	Overcurrent threshold voltage (VIN3 – CS3)		29	40	51	
t_R	Response time		1		5	µs

overcurrent comparator 4

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OC4}	Overcurrent threshold voltage (VIN4 – CS4) relative to VMAX4		–50		–225	mV
t_R	Response time		1		5	µs

undervoltage (UV)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UV1}	Channel 1 undervoltage limit		10.37	10.80	11.23	V
V_{UV2}	Channel 2 undervoltage limit		4.22	4.40	4.58	
V_{UV3}	Channel 3 undervoltage limit		2.78	2.90	3.02	
V_{UV4}	Channel 4 undervoltage limit		-11.23	-10.80	-10.37	

overvoltage (OV)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OV1}	Channel 1 overvoltage limit		12.77	13.20	13.63	V
V_{OV2}	Channel 2 overvoltage limit		5.38	5.60	5.82	
V_{OV3}	Channel 3 overvoltage limit		3.55	3.70	3.85	
V_{OV4}	Channel 4 overvoltage limit		-13.63	-13.20	-12.77	

IRAMP output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CHG}	Source current, charging	$V_{O(IRAMP)}$ = 0.5 V	–46	–58	–68	µA
I_{DSG}	Sink current, discharging	$V_{O(IRAMP)}$ = 0.5 V	1.3	1.8	2.5	

undervoltage lockout (UVLO)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO–L}$	VIN1 UVLO, input rising	$V_{I(VIN2)}$ = $V_{I(VIN3)}$ = $V_{I(VIN4)}$ = 0 V	2.1	2.4	2.9	V
$V_{UVLO–H}$	VIN1 UVLO, input falling		1.90	2.25	2.70	
V_{HYS}	VIN1 UVLO hysteresis		0.05			

BD_SEL# input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			
I_{IH}	High-level input leakage current	$V_{I(BD\_SEL\#)}$ = 5 V		50		µA

electrical characteristics $V_{I(VIN1)}$ = 12 V, $V_{I(VIN2)}$ = 5 V, $V_{I(VIN3)}$ = 3.3 V, $V_{I(VIN4)}$ = –12 V, T_A = –40°C to 85°C (unless otherwise noted) (continued)

HEALTHY# output

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OH}	High–level output (leakage) current	$V_{I(BD\_SEL\#)}$ = 5 V,	V_{OH} = 5 V		1		μA
V_{OL}	Low-level output voltage	$V_{I(BD\_SEL\#)}$ = 0 V,	I_{SINK} = 0.1 mA		0.5		V
I_{OL}	Low-level output (sink) current	$V_{I(BD\_SEL\#)}$ = 0 V,	V_{OL} = 0.5 V	4	10		mA

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	18	I	Analog ground
BD_SEL#	6	I	Logic low enable input for back-end power
CPGND	19	I	Charge pump ground
CPUMP	20	I/O	Charge pump resevoir capacitor connection
CS1	4	I	Channel 1 (12-V) current sense input
CS2	21	I	Channel 2 (5-V) current sense input
CS3	9	I	Channel 3 (3.3-V) current sense input
CS4	16	I	Channel 4 (–12-V) current sense input
GATE1	1	O	Gate drive for Channel 1 (12-V) external pass FET
GATE2	24	O	Gate drive for Channel 2 (5-V) external pass FET
GATE3	12	O	Gate drive for Channel 3 (3.3V) external pass FET
GATE4	13	O	Gate drive for Channel 4 (–12V) external pass FET
HEALTHY#	17	O	Open drain output asserted low for back-end power good
IRAMP	5	O	Current ramp programming pin
PRECHG	8	O	Bias supply of 1V for bus signal precharge
RGND	7	I	Reference ground
VIN1	3	I	Channel 1 supply (12-V) input voltage sense
VIN2	22	I	Channel 2 supply (5-V) input voltage sense
VIN3	10	I	Channel 3 supply (3.3-V) input voltage sense
VIN4	15	I	Channel 4 supply (–12-V) input voltage sense
VS1	2	I	12-V supply back-end voltage sense
VS2	23	I	5-V supply back-end voltage sense
VS3	11	I	3.3-V supply back-end voltage sense
VS4	14	I	–12-V supply back-end voltage sense

DISSIPATION RATING TABLE

PACKAGE	T_A 25°C	DERATING FACTOR	T_A = 85°C
TSSOP (PW)	800 mW	10 mW/°C	200 mW

pin descriptions

AGND: Analog ground reference for the device.

BD_SEL#: Logic low enable input for back-end power. In the CompactPCI® application, this pin ties to the short–pin BD_SEL# input to the plug-in slot. When the input supplies are above the device minimums, and this pin is asserted low the TPS2345 begins the sequential ramp–up of the back-end supplies. Pulling this input high (>2 V) turns off power to the back-end planes, and puts the TPS2345 into low-power sleep mode.

CPGND: Charge pump ground pin for the device.

CPUMP: Charge pump resevoir capacitor connection. An external capacitor of value 0.1 μF to 1 μF must be connected between this pin and CPGND. The capacitor provides charge storage for the internal charge pump for gate drive of the four external N-channel FETs.

CS1, CS2, CS3: These pins tie to the load side of the Channel 1, 2, and 3 current sense resistors, respectively. They are used in conjunction with the VIN1, VIN2 and VIN3 inputs to provide load current magnitude information to each of the positive rail LCAs.

CS4: This pin ties to the more positive side of the Channel 4 current sense resistor (common with the pass FET source). It is used in conjunction with the VIN4 input to provide Channel 4 current magnitude information to the negative rail LCA.

GATE1, GATE2, GATE3, GATE4: Gate drive outputs for the Channel 1 through Channel 4 pass FETs, respectively. The gates are driven according to the supply voltage, enable, sequence programming and load current conditions of the add-in board.

HEALTHY#: Open-drain output asserted low to signal a back-end power good condition. In the CompactPCI® application, this signal is an indication of the board's suitablility to be connected to the CompactPCI® bus. The output is false when back-end power is not enabled, if any of the back-end voltage is not within the factory-programmed tolerances of the undervoltage and overvoltage comparators, or as a result of an overcurrent indication on any supply controller, or a fault time-out on any supply during linear ramp-up.

IRAMP: Current ramp programming pin. A capacitor connected between this pin and ground determines the maximum slew rate of the load current during ramp-up and ramp-down of the three positive back-end voltages. This same capacitor is also used to establish the time limit for ramping each of the supply outputs.

PRECHG: Bias supply of 1 V for bus signal precharge. During plug-in insertion events, this output provides bias supply to precharge the bus signal lines according to the requirements of the CompactPCI® Hot Swap specification.

RGND: Reference ground input for the device.

VIN1: Channel 1 supply (12-V) input voltage sense. This pin is connected to the 12-V power supply input to the add-in card. The supply potential is tested against the undervoltage limits prior to ramping voltage to the back-end 12-V plane. The input supply also serves as the reference potential for the internally generated current limit (IMAX) reference of the Channel 1 LCA. This pin also serves as the VCC supply for the TPS2345.

VIN2: Channel 2 supply (5-V) input voltage sense. This pin is connected to the 5-V power supply input to the add-in card. The supply potential is tested against the undervoltage limits prior to ramping voltage to the back-end 5-V plane. The input supply also serves as the reference potential for the internally generated current limit (IMAX) reference of the Channel 2 LCA. This pin also serves as the supply input for the precharge bias output.

VIN3: Channel 3 supply (3.3-V) input voltage sense. This pin is connected to the 3.3-V power supply input to the add-in card. The supply potential is tested against the undervoltage limits prior to ramping voltage to the back-end 3.3-V plane. The input supply also serves as the reference potential for the internally generated current limit (IMAX) reference of the Channel 3 LCA.

pin descriptions (continued)

VIN4: Channel 4 supply (–12-V) input voltage sense. This pin is connected to the –12-V power supply input to the add-in card. The supply potential is tested against the undervoltage limits prior to ramping voltage to the back-end –12-V plane. The input supply also serves as the reference potential for the internally generated current limit (IMAX) reference of the Channel 4 LCA.

VS1, VS2, VS3: Voltage sense inputs for the positive back-end power busses. These pins connect to the source nodes (load side) of the external pass FETs. After the programmed voltage ramp period for each supply, these inputs are monitored to verify that the load voltages remain within the specified tolerances.

VS4: Voltage sense input for the negative back-end power bus. This pin connects to the drain (load side) of the Channel 4 external pass FET. After the programmed voltage ramp period for the negative supply, this input is monitored to verify that the load voltage remains within the specified tolerance.

functional overview

When an add-in CompactPCI® printed circuit board (PCB) is inserted into a live chassis slot, the discharged supply bulk capacitance on the board can draw huge transient currents from the system supplies. Limited only by the ESR of the bulk capacitors and the impedance of the interconnect, these transients can reach sufficient magnitude to cause immediate damage to connector pins, PCB etch and plug-in and supply components, or cause latent defects reducing long-term reliability. In addition, current spikes can cause glitches on the power busses, causing other boards in the system to reset.

The TPS2345 is designed for use with the connector pin staging and insertion/extraction processes defined in the CompactPCI® Hot Swap Specification, to enable full hot-swap capability in CompactPCI® add-in cards. N–channel MOSFETs in series with each supply input provide isolation between the early power planes and the back-end power planes during insertion and extraction events. Low ohmic-value sense resistors between each input and pass MOSFET feed back current information to the device. The TPS2345 uses load current sensing along with the peripheral slot enable command, BD_SEL#, to determine the appropriate gate drive status for each of the four pass MOSFETs. In this manner, the device provides for the controlled application of power to and removal from the back-end planes during hot swap.

When the add-in PCB is inserted into the slot, the long 5-V, 3.3-V and GND power pins make contact first (see typical application diagram). At this stage of the insertion process, the TPS2345 precharge circuitry becomes active, and biases the I/O pins to a nominal 1.0 V. Next, the medium length pins make contact, which includes the 12-V, –12-V supplies, and the majority of the 5-V and 3.3-V supply pins. The TPS2345 derives VCC power from the 12-V supply; however, the pull-up on the BD_SEL# input pin causes the device to maintain pull-downs on the four gate pins, keeping the pass MOSFETs off. The short BD_SEL# pin is one of the last pins to mate; at that point a logic low on the signal starts the turn-on of power to the back-end loads.

During a ramp-up sequence, the four supply inputs are validated against the pre-programmed undervoltage (UV) and overvoltage (OV) thresholds. As each positive voltage load is enabled, current to the load is ramped at a user-programmable rate, easily set by a capacitor on the current ramp control pin, IRAMP. The supplies are sequenced up in the following order: 12-V, 5-V, 3.3-V and –12-V. The ramp of supply current on each channel is limited to a maximum value, herein referred to as IMAX. The IMAX limit is individually selectable for each channel, by selecting the appropriate value of the sense resistor. If the IMAX current level is attained on any channel during an insertion, charging of that channel's input bulk capacitance completes at that current limit, as required.

functional overview (continued)

As each back-end voltage is ramped, its level is validated to ensure it is within the established UV and OV tolerances at the expiration of a programmable time period, protecting against start-up into faulted loads. The same capacitor at the IRAMP pin which sets the current ramp rate is also used to establish this ramp-up time limit. If all four supplies successfully reach a known good state, the HEALTHY# output signal is pulled low to allow enumeration of the add-in card.

To protect the backplane power bus, the TPS2345 provides an electronic circuit breaker that trips upon detecting an overcurrent event. The detection threshold of an overcurrent event is internally set to approximately two times (2x) IMAX. The –12-V channel also includes a circuit breaker function; its trip threshold is always a minimum of 50 mV above the current-limit sense voltage. If any channel trips the circuit breaker, all supply outputs are rapidly turned off, and remain latched off. Also, the HEALTHY# output becomes high-impedance. The TPS2345 can be reset by cycling either the BD_SEL# input or power to the device.

The low, 20-mV (150 mV on the –12-V channel) nominal sense voltage limit allows the use of low-value sense resistors, or for high-current applications, the use of PC board copper trace. This helps minimize the insertion loss across the hot swap interface. Further insertion loss reduction is achieved via the on-chip charge pump, which ensures maximum gate overdrive on each of the three external pass MOSFETs on the positive supply channels. This feature helps users obtain lower $R_{DS(on)}$ characteristics with their preferred N-channel MOSFETs.

Under a normal PC board shutdown event, the TPS2345 also turns off power in a controlled manner. To initiate a shutdown, BD_SEL# is brought to a logic high during a HEALTHY# state (outputs on and no faults present). The supply outputs are then sequentially ramped off in the reverse order of the ramp-up sequence. After all supply outputs are off, the TPS2345 goes into a low-current sleep mode.

detailed description

The primary circuit blocks of the TPS2345 include internal supply generation, a charge pump, a state machine, programmable ramp generator, precharge circuitry, and a ROM data cell. In addition, each of the four channels contains a gate control block which includes the linear control amplifier (LCA), programmable current source, and the voltage sense circuitry (see Figure 1). The gate drive blocks are virtually identical, except that the Channel 4 block, controlling the negative voltage channel, adds some scaling and level shift circuitry to adjust the polarity of the sense signals to that of the internal circuitry.

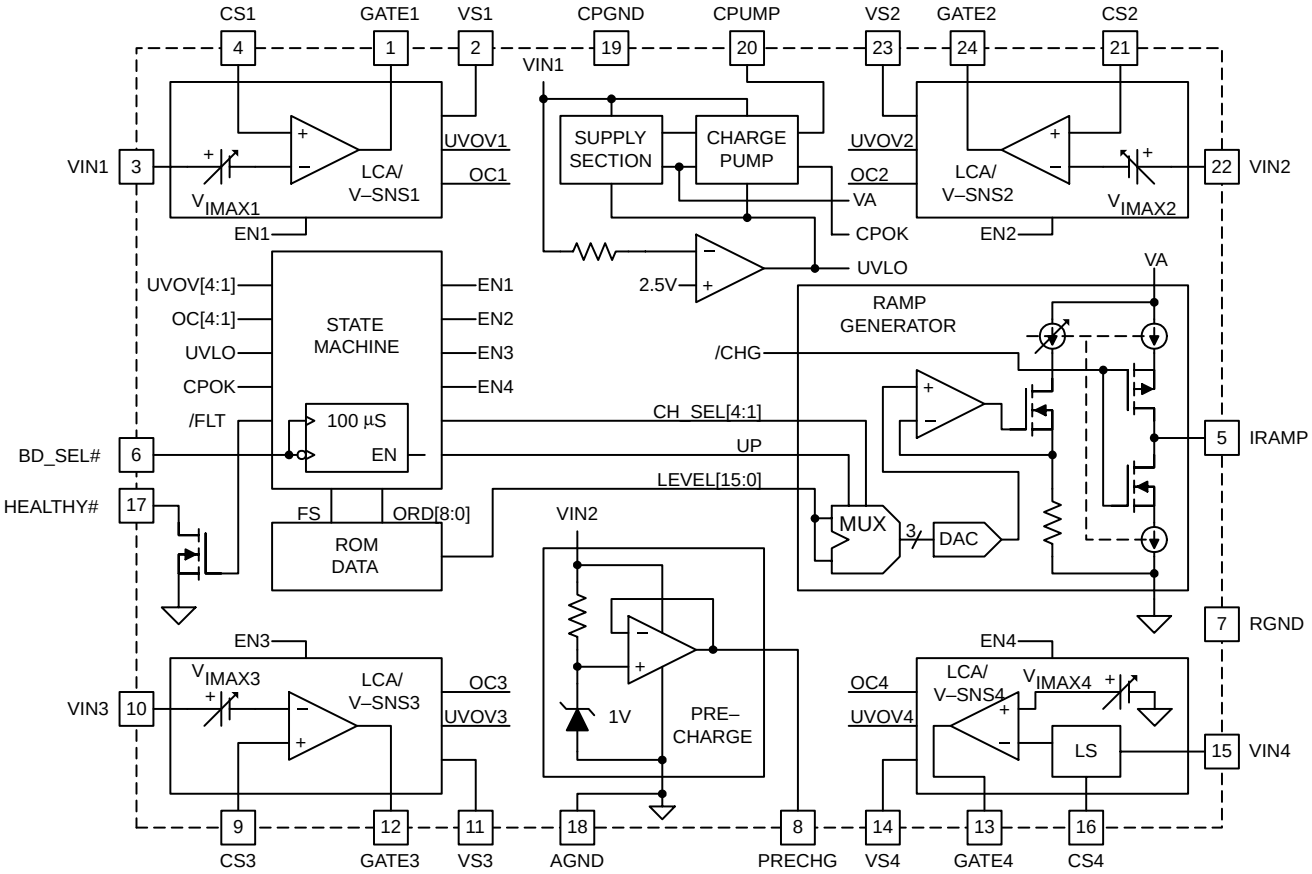


Figure 1. TPS2345 block diagram

The supply generation block contains voltage regulators and references to generate the various bias voltages used internally by the TPS2345. An undervoltage lockout (UVLO) function is used to ensure proper device turn-on once the VIN1 input has attained the UVLO threshold of about 2.5 V. In addition, an on-chip charge pump steps up the VIN1 input to generate the high voltage used by the LCAs to drive the pass MOSFET gates. Burst regulation of the charge pump limits the output to about 20.5 V (peak), with about a 1-V hysteresis. During steady-state load operation, sufficient gate overdrive is ensured to fully enhance the external MOSFETs, while not exceeding the typical 20-V V_{GS} rating of common N-channel MOSFETs, even on the low-voltage channels.

The state machine block contains the logic to control the ramp-up and ramp-down sequencing, ramp generator operation, and fault management. It uses voltage and current monitor outputs, along with the device enable status and programmed order information to determine which channel is to be acted on, whether ramp-up, ramp-down or steady-state operation is required, and the present healthy or faulted states of the back-end supplies. A nominal 100–µS digital filter is applied to the BD_SEL# input to help protect against false triggering in systems not implementing hardware connection control. The filter acts on both high-to-low and low-to-high transitions of the enable input.

detailed description (continued)

The ramp generator consists of a series of multiplexers feeding a digital-to-analog converter (DAC) circuit which sets the magnitude of an internal current source. When active, the current source is used to establish a constant value source or sink current at the IRAMP pin. This current is used to alternately charge and discharge a capacitor connected between IRAMP and ground, generating a series of sawtooth timing pulses. During turn-on of the back-end voltages, the capacitor is charged with a 58-μA current, then subsequently discharged with a 1.8-μA load. A comparator in the ramp generator circuit monitors the IRAMP voltage against two alternating thresholds, such that the voltage charges up to 1.5 V and back down to 0 V. During the rising edge of this waveform, the voltage at IRAMP is used to develop the reference threshold at the inverting input of the active channel's LCA. The other input is connected to the channel's current sense (CSx) input. The LCA slews the GATEx output to maintain the CSx pin at the reference value. Since the CSx voltage is developed as the drop across the external sense resistor due to load current, the current to the load is therefore ramped at a linear rate set by the dV/dt on the IRAMP pin. Therefore, inrush slew rate limiting is easily programmed by the user with the IRAMP capacitor, C_{IRAMP}. For Channel 4, internal device offsets may cause the inrush profile to deviate from the programmed curve, particularly at initial turn-on. However, the maximum sourcing limit imposed by the VMAX4 threshold still applies.

During a load turn-on, the current sense voltage, if required in order to fully charge the back-end plane, can track the IRAMP waveform up to approximately 1.35 V on the IRAMP pin. If the charging current achieves that level, the LCA reference is switched automatically to the fixed IMAX reference. Load charging then continues at that fixed level until complete or until timer expiration, whichever occurs first. For Channels 1, 2 and 3, the IMAX level has been set to 20 mV at the CSx pin, referenced to VINx. For Channel 4, the IMAX level is 150 mV.

The precharge circuitry is powered from the VIN2 supply input, or 5-V for cPCI® systems. Therefore, when the long pins mate during an insertion, or until they break contact during an extraction, the precharge actively biases the bus signal lines to 1.0 V. The precharge block consists of a 1-V reference generator and a unity gain amplifier. The amplifier provides source and sink capability up to 5 mA.

The ROM data cell sets the configuration information for the TPS2345. These parameters include the order of channel sequencing, the magnitude of the charge and discharge currents at IRAMP, and the nominal voltage range of each channel. This information is all pre-programmed at the factory; no programming by the user is necessary.

detailed description (continued)

The basic functional blocks of the LCA/voltage sense circuits is shown in greater detail in Figure 2. The LCA has as its inputs the reference voltage generated by the current sources, and the current sense input. During a supply turn-on, it slews the pass MOSFET gate to force the load current to track the selected source. After load charging completes, and the current decays to the nominal operating level, the LCA drives the GATEx output to its input supply level, the charge pump output voltage.

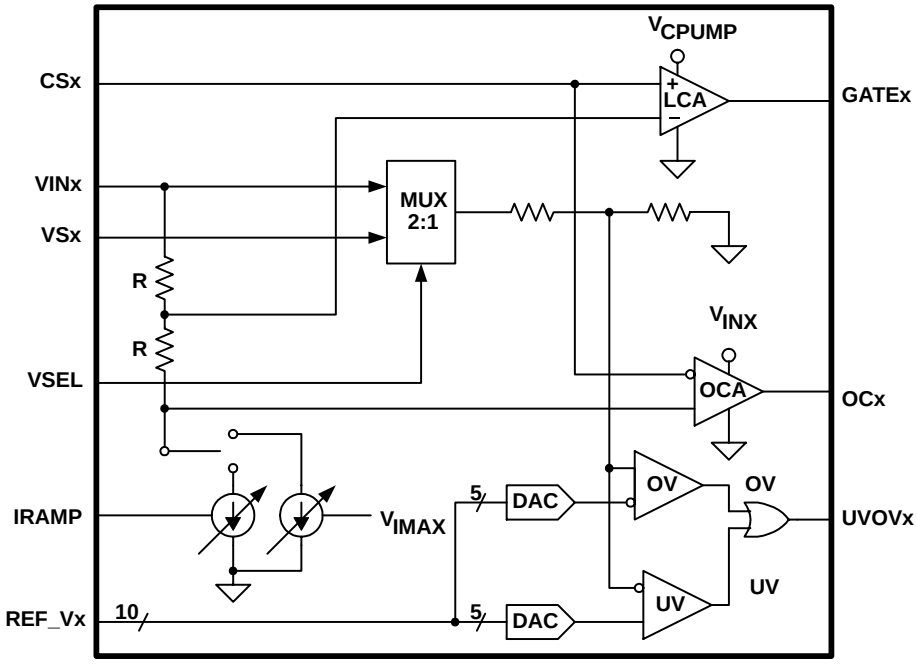


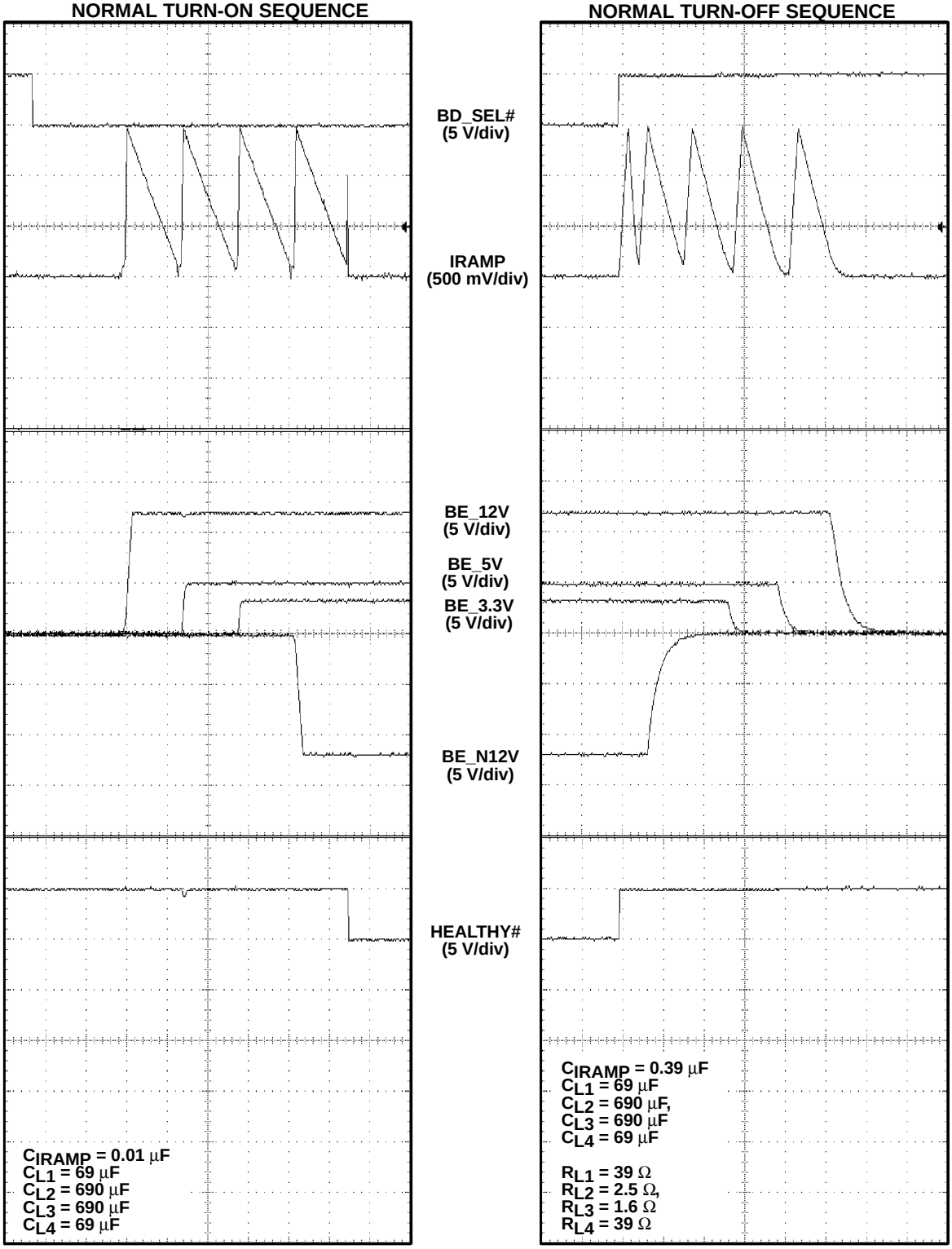
Figure 2. Linear Control Amplifier Block

The supply voltage is monitored by the undervoltage (UV) and overvoltage (OV) comparators. A voltage multiplexer (MUX) selects from either the input supply voltage (VINx) or the load voltage (VSx), and provides that signal to the comparator inputs. Once the Channel 1 supply is above the UVLO threshold, and the BD_SEL# input has been pulled low, but prior to the ramp-up of the first channel, the comparators monitor the input supplies. Any supply outside its UV/OV window causes all pass MOSFETs to be held off. If all inputs are within tolerance, a ramp-up sequence can start, at which time the comparator inputs are switched over to the load, or VSx, voltages. Within the state machine, monitoring of the ORed status of the UV and OV comparators of any channel is enabled at the turn-on of the next channel, or approximately at the leading edge of the next IRAMP pulse.

Finally, a fast overcurrent comparator (OCA in the diagram) also monitors the CSx input. This comparator threshold is set to approximately 2 times the current limit threshold, ($2 \times$ IMAX) for the three positive supplies. In the event of a short-circuit or other fast overcurrent event, the OCA trips, disabling the LCA, and causing additional gate discharge paths to be turned on for a rapid shutdown of the loads.

A 1-μS to 2-μS filter is applied to all overcurrent and voltage faults to guard against nuisance trips. If the duration of a fault condition on any one channel exceeds the filter length, the fault is latched, the open-drain device at the HEALTHY# output is turned off, and all four channels are shut down.

TYPICAL CHARACTERISTICS



t – Time – 5 ms/div

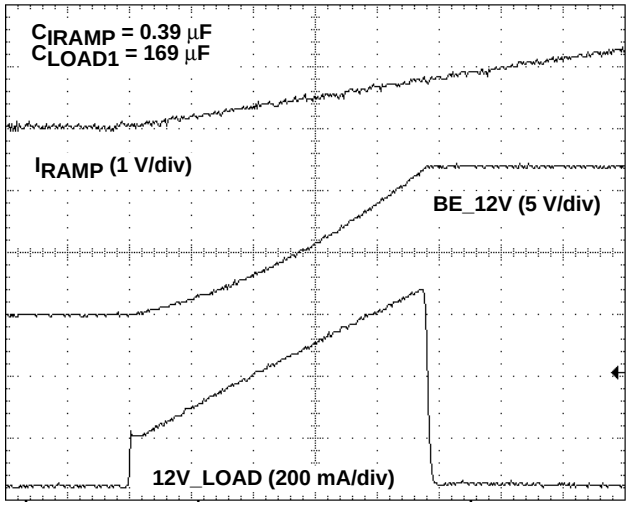
Figure 3

t – Time – 10 ms/div

Figure 4

TYPICAL CHARACTERISTICS

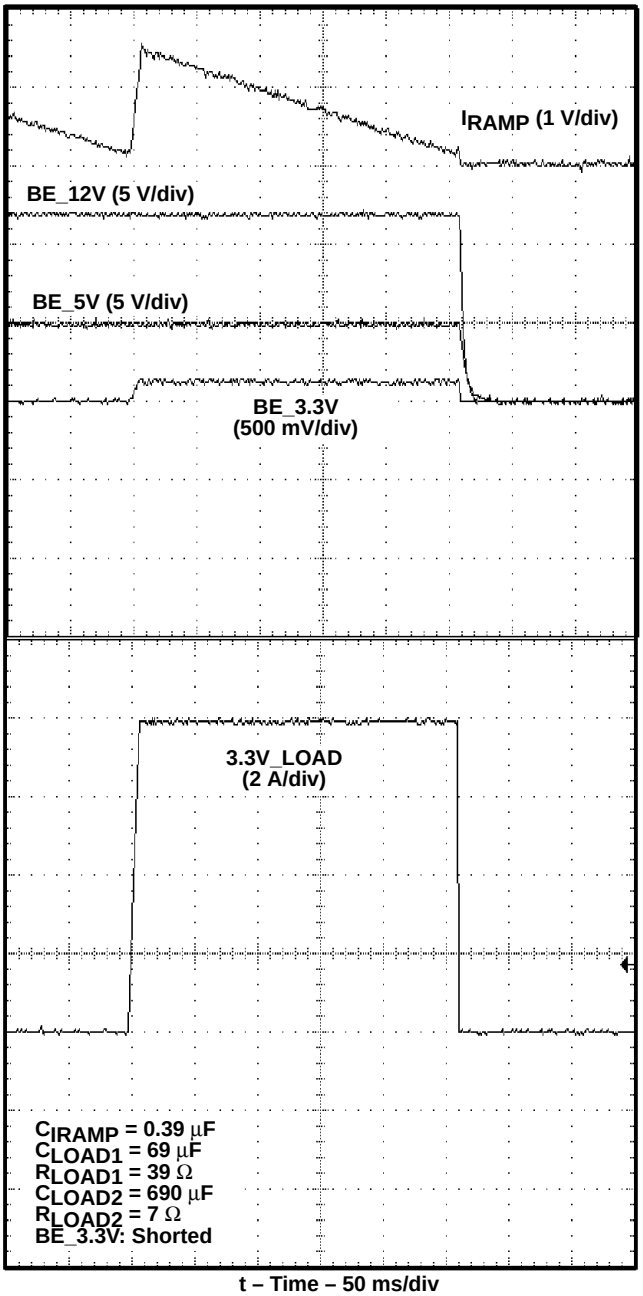
LOAD CURRENT LINEAR RAMP
EXAMPLE: 12-V LOAD



t – Time – 1 ms/div

Figure 5

TURN-ON INTO A SHORT
ON BACK-END 3.3 V



t – Time – 50 ms/div

Figure 6

UNDERVOLTAGE FAULT RESPONSE
5-V FAULT

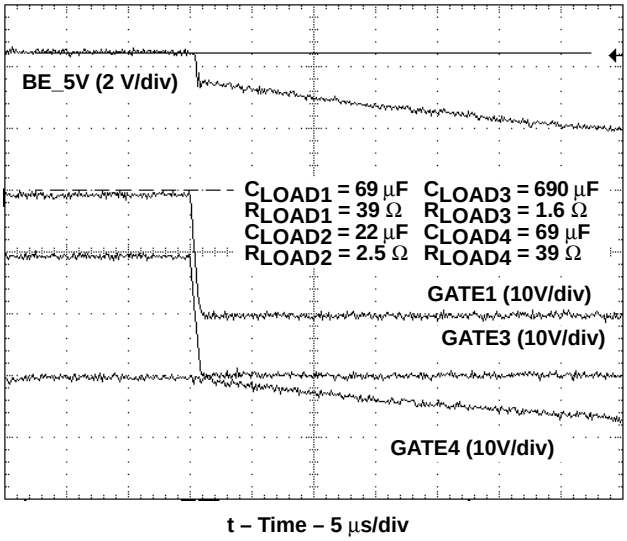


Figure 7

HIGH LEVEL OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE, LCA1

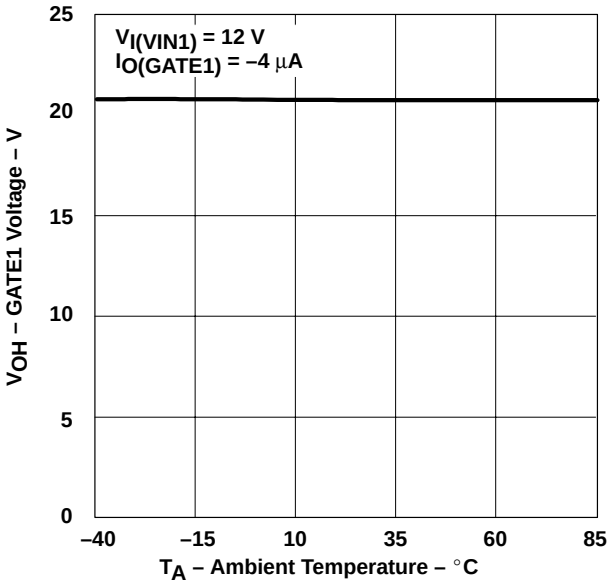


Figure 8

TYPICAL CHARACTERISTICS

HIGH LEVEL OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE, LCA2

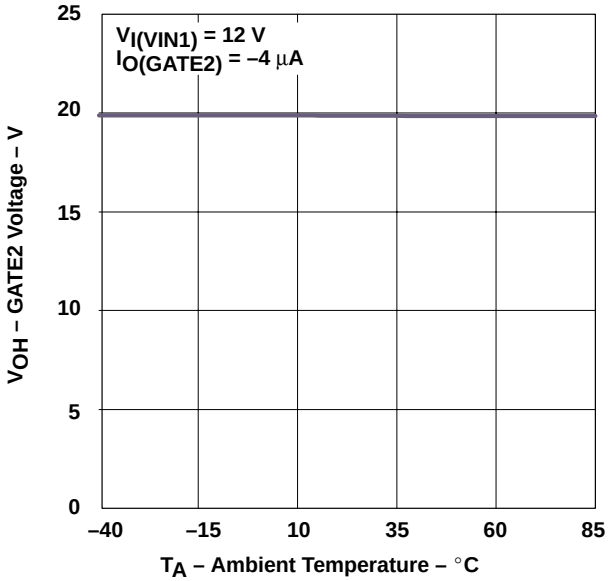


Figure 9

HIGH LEVEL OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE, LCA3

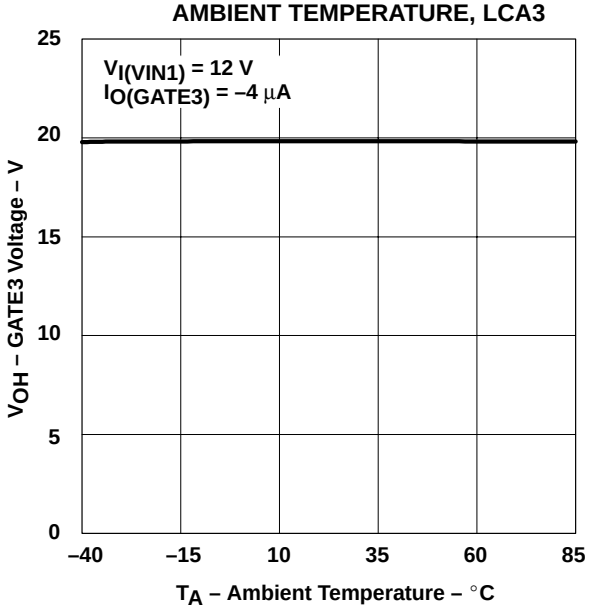


Figure 10

HIGH LEVEL OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE, LCA4

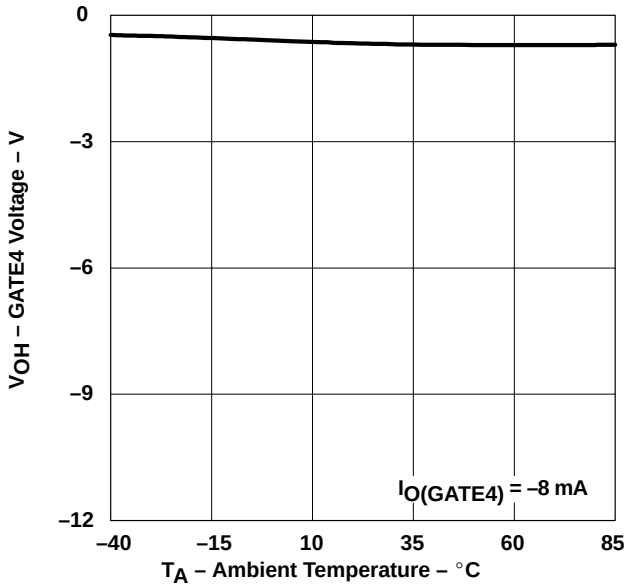


Figure 11

IRAMP OUTPUT CURRENT
vs
AMBIENT TEMPERATURE

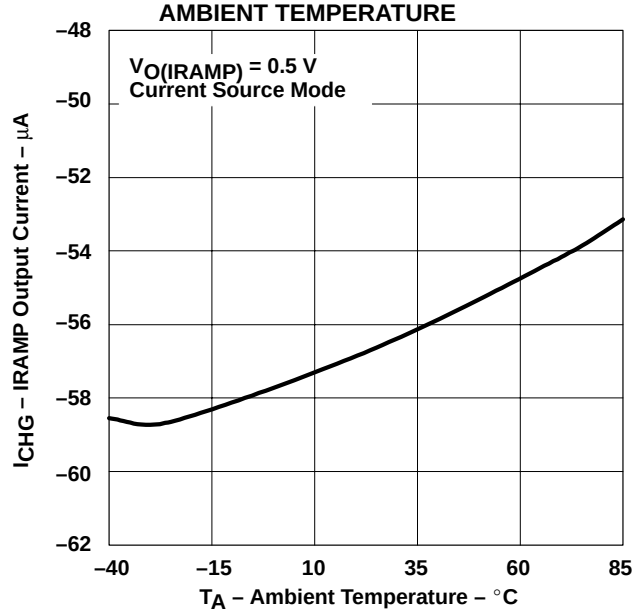


Figure 12

TYPICAL CHARACTERISTICS

IRAMP INPUT CURRENT vs AMBIENT TEMPERATURE

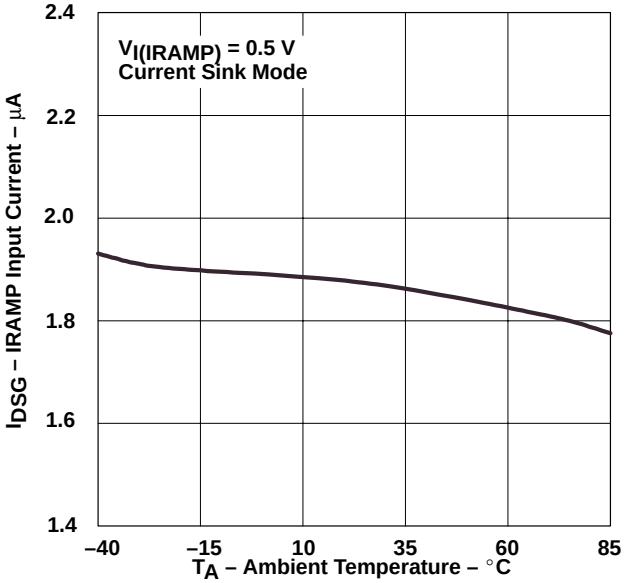


Figure 13

IRAMP MODE TRIP THRESHOLD vs AMBIENT TEMPERATURE

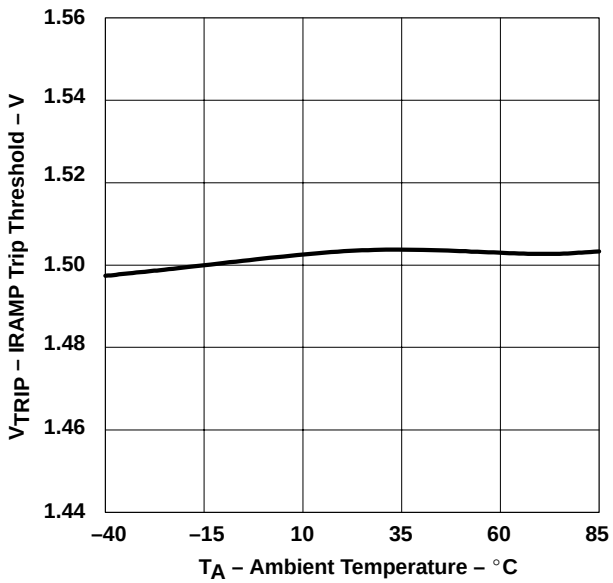


Figure 14

PRECHG OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

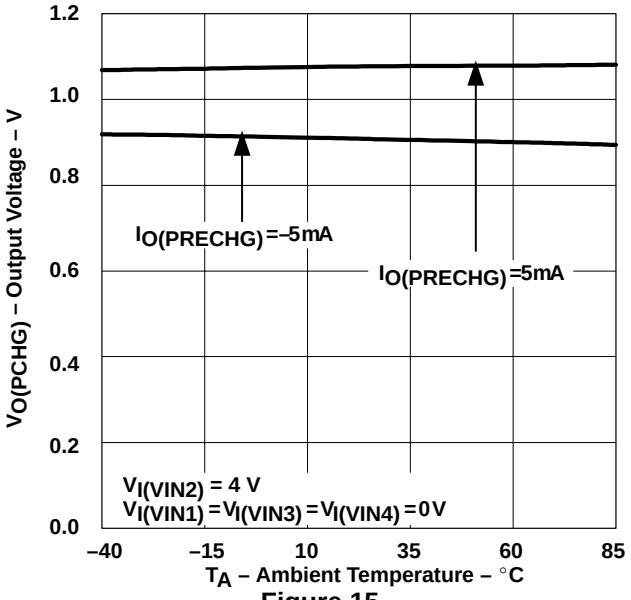


Figure 15

PRECHG OUTPUT VOLTAGE vs SUPPLY VOLTAGE

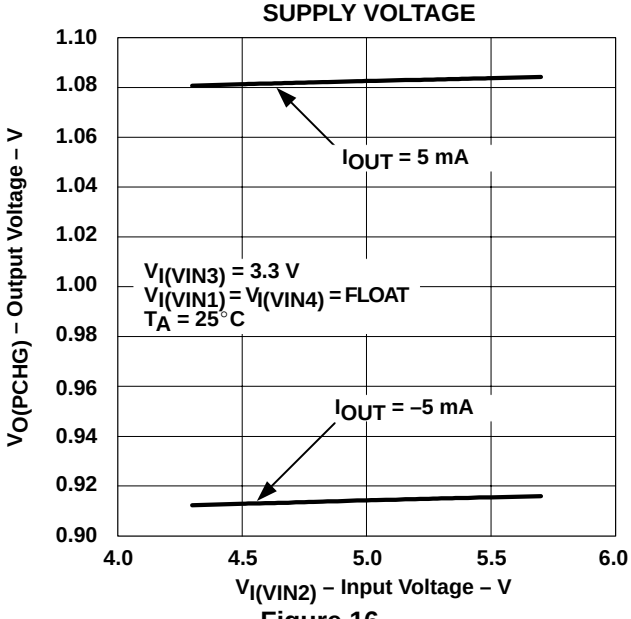


Figure 16

TYPICAL CHARACTERISTICS

PRECHARGE OUTPUT VOLTAGE vs OUTPUT CURRENT, SOURCING

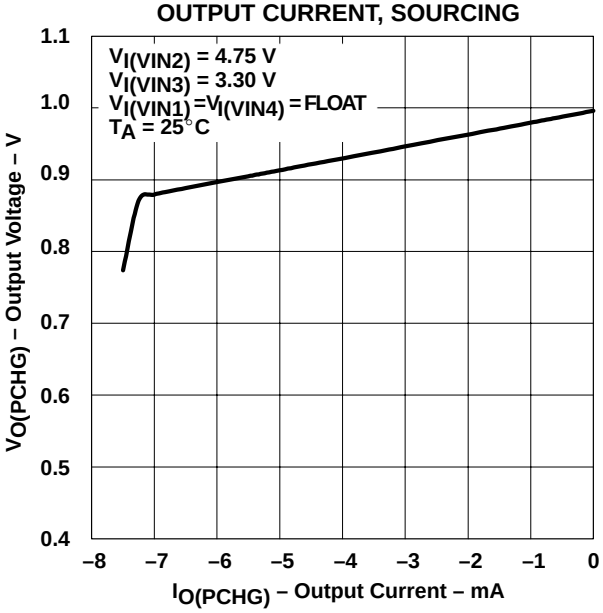


Figure 17

PRECHARGE OUTPUT VOLTAGE vs OUTPUT CURRENT, SINKING

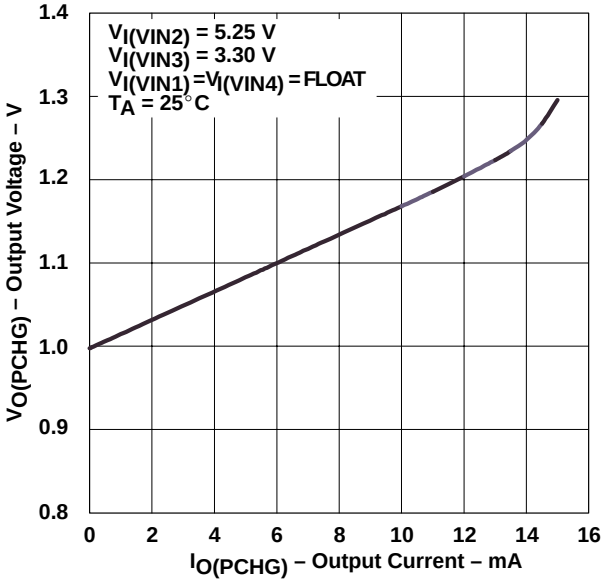


Figure 18

APPLICATION INFORMATION

The connections to set up the TPS2345 for operation in a CompactPCI® plug-in are shown in the typical application diagram.The TPS2345 works in conjunction with four external N-channel MOSFETs to provide isolation of the back-end power planes when disabled, and to provide a low-impedance power path when the load voltages are at the full-input dc potential. For proper operation, each channel of the device must be connected to the appropriate supply as listed in Table 1.

Table 1. TPS2345 Channel to cPCI® Supply Connections

TPS2345 CHANNEL	cPCI® SUPPLY
1	12 V
2	5 V
3	3.3 V
4	–12 V

Sense resistors R1 through R4 connect between the VINx and CSx pins of their respective supplies, and provide load current magnitude information to the TPS2345. To turn on the negative voltage channel, the device pulls the gate of MOSFET Q4 towards ground potential. Resistor R5 provides a gate pull down when the LCA turns off, as the Channel 4 LCA does not drive to the negative rail.

Capacitors C1 through C4 provide decoupling at the plug-in power pins, and are required by the CompactPCI® hot swap specification. For the 5-V and 3.3-V supplies, the specification recommends an average value of between 0.1 μF and 0.2 μF per 10 pins. This capacitance may be distributed along the connector, or provided as a single chip on each supply. Since there are eight 5-V and ten 3.3-V power pins at each backplane slot, two 0.1-μF ceramic capacitors meet this requirement. The ±12-V supplies should also be decoupled as shown. All four capacitors should be placed close to the J1 connector, with trace length less than or equal to 0.6 inch.

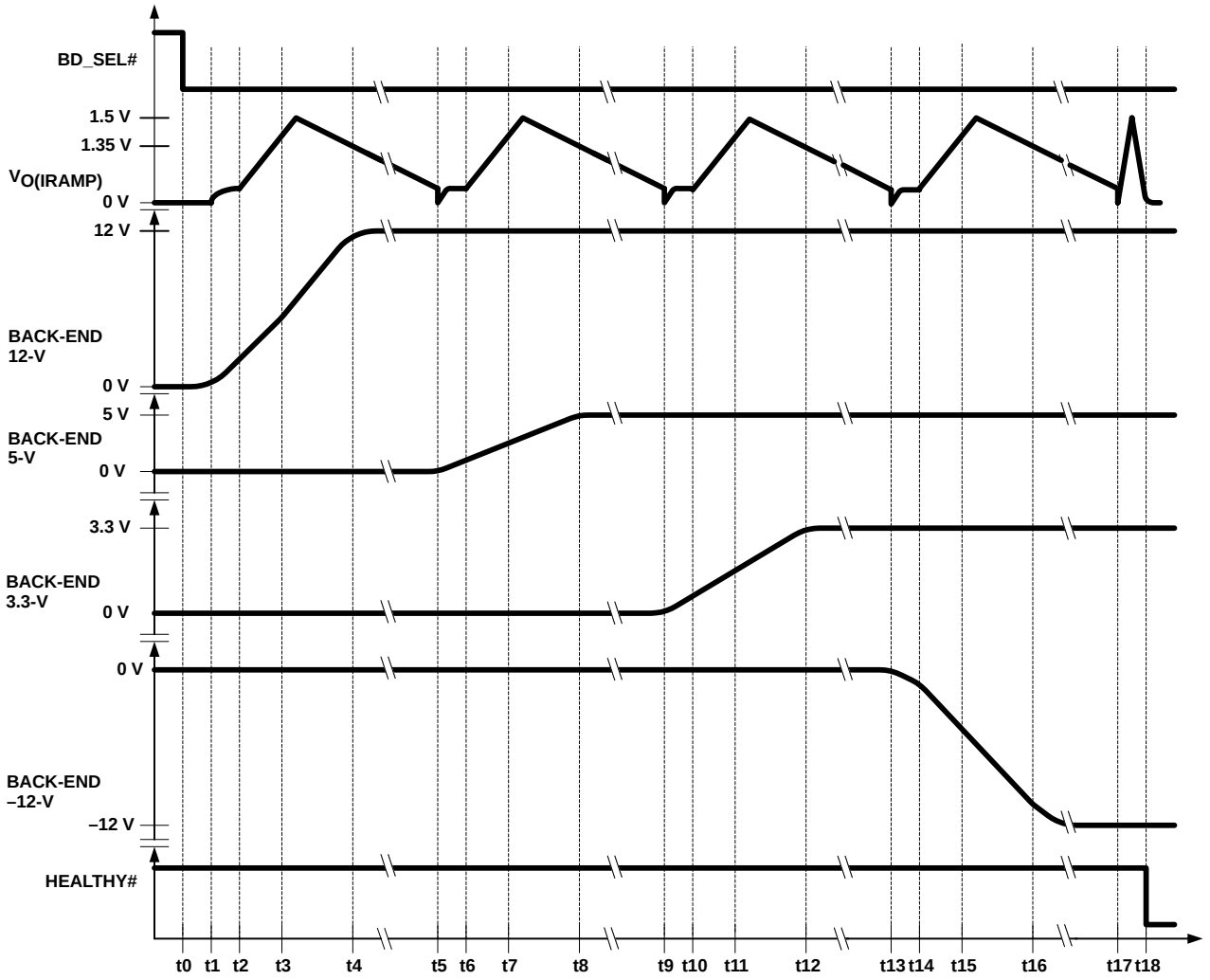
Resistor R7 provides the 1.2-kΩ pull-up on the BD_SEL# pin required by the hot swap specification. The pull-up resistor is shown connected to the early 5-V plane; alternatively, it could be connected to early VIO. Resistor R6 provides a pull-up to early VIO on the HEALTHY# signal; a 10-kΩ resistor should suffice.

A capacitor with a value between 0.1 μF and 1 μF (C6 in the diagram) is required between the CPUMP pin and ground. This capacitor provides charge storage for the on-board charge pump. A 0.1-μF ceramic is sufficient for most applications.

ramp-up sequence

A successful ramp-up of the four cPCI® back-end supplies consists of five pulses on the TPS2345 IRAMP pin. One load voltage is ramped up during each of the first four IRAMP pulses. The fifth pulse enables the fault logic of the last channel (Channel 4) to turn on. This is shown graphically in Figure 19.

APPLICATION INFORMATION



t0: BD_SEL# input brought low to initiate a turn-on sequence.
t1: Channel 1 (12V) gate enabled; IRAMP capacitor starts charging with slow turn-on clamp. Slow charging of load voltage (back-end 12V) begins.
t2: Slow turn-on period ends; linear ramp of current to the load begins.
t3: Constant di/dt period ends; load voltage ramping continues at IMAX rate.
t4: Back–End 12V reaches input DC potential.
t5: Channel 2 (5V) gate is enabled. Slow charging of load voltage (back-end 5V) begins. Fault monitoring on Ch. 1 enabled.
t6: Slow turn-on period ends; linear ramp of current to load begins.
t7: Constant di/dt period ends. Load voltage ramping continues at IMAX rate.
t8: Back–End 5V reaches input DC potential.
t9: Channel 3 (3.3V) gate is enabled. Slow charging of load voltage (back-end 3.3V) begins. Fault monitoring on Ch. 2 enabled.
t10: Slow turn–on period ends; linear ramp of current to the load begins.
t11: Constant di/dt period ends. Load voltage ramping continues at IMAX rate.
t12: Back–End 3.3V reaches input DC potential.
t13: Channel 4 (–12V) gate is enabled. Slow charging of load voltage (back-end –12V) begins. Fault monitoring on Ch. 3 enabled.
t14: Slow turn-on period ends; linear ramp of current to load begins.
t15: Constant di/dt period ends; load voltage ramping continues at IMAX rate.
t16: Back-end –12V reaches input DC potential.
t17: Channel 4 UV/OV fault enable pulse.
t18: HEALTHY# output pulled low.

Figure 19. TPS2345 Ramp-Up Sequence

APPLICATION INFORMATION

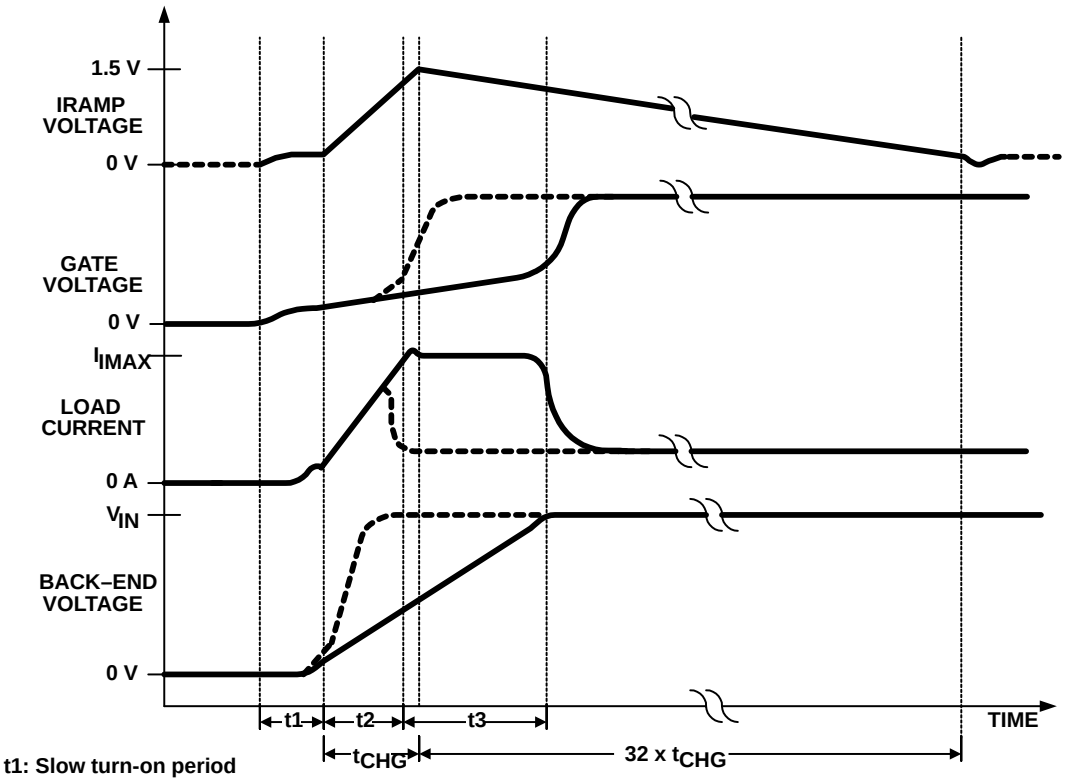
A turn-on sequence is initiated when the BD_SEL# input is brought low (less than 0.8 V), assuming that all four input supplies (at the VINx pins) are within their UV/OV tolerance windows. A voltage fault at any input supply causes all loads to be held off. When BD_SEL# is asserted, the Channel 1 amplifier is enabled, and a 58-μA current source begins charging the IRAMP capacitor to generate the first IRAMP pulse. During the linear rising edge portion of the IRAMP waveform, current is linearly ramped to the 12-V back-end plane. Once the voltage at IRAMP reaches 1.5 V, the source is replaced with a 1.8-μA sink that discharges IRAMP to 0 V. During this discharge period, load charging current, if still required, is limited to IMAX, the current sense voltage (VMAX) divided by the sense resistor value, R_{SNSx}, or IMAXx = VMAXx / R_{SNSx}, where “x” refers to any of the four channels.

At the completion of the first pulse on IRAMP, the TPS2345 moves to the second voltage to be ramped up, Channel 2, enables its LCA and begins generating the second pulse in the IRAMP train. At this time, fault monitoring is enabled on the Channel 1 output. Therefore, if Channel 1 has failed to attain at least the undervoltage threshold potential, a fault is detected, any active channels turned off, and the turn-on sequence aborted. In this manner, the maximum time allowed for ramp-up of any of the channels is the duration of one (1) IRAMP pulse. This protects against indefinite sourcing into faulted loads. The TPS2345 latches off in response to faults, and can be reset either by toggling the BD_SEL# input high and then low again, or by cycling power to the device.

After the Channel 2 ramp pulse, the back–end planes for Channel 3 and Channel 4 are ramped up in similar fashion. Channel 2 fault detection is enabled at the start of the Channel 3 ramp pulse, and so on. Once all four supplies are ramped up, Channel 4 fault detection is enabled on the fifth IRAMP pulse. This last pulse is of relatively short duration, as charge and discharge currents of approximately 256 μA are selected for the UV/OV4 enable pulse. If all four channels reach a known good state, the HEALTHY# output is asserted low.

Each load current waveform, at load turn-on, may have up to three distinct periods, as shown in Figure 20. Initially after being enabled, the ramp generator output voltage is clamped to less than 100 mV. This results in a corresponding clamp on load current of about 7% of the programmed IMAX value (with some variance due to internal device offset). This temporary limit applies during approximately the first 500 μs of output ramping time. The purpose of this slow ramp period is to ensure the LCA is pulled out of saturation, and is closely tracking the CS input, prior to enabling fast charging of the load. During this time, appreciable ramping of the back-end voltage may or may not occur, depending on a number of factors including the IMAX value, the amount of bulk capacitance on the load, and the magnitude and polarity of inherent offsets in the current control loop.

APPLICATION INFORMATION



t1: Slow turn-on period

t2: Linear current ramp (di/dt)

t3: Constant-current load charging

t_{CHG}: IRAMP capacitor charge time, ($1.4 \times C_{IRAMP}/58$)

UDG–02005

Figure 20. Load Current at Startup

Once the slow ramp period has expired, the clamp is removed, and the IRAMP voltage continues to ramp up at a constant rate of:

$$\frac{I_O}{C_{IRAMP}} = \frac{58\ \mu A}{C_{IRAMP}}$$

Since the linear amplifier acts to maintain equal voltages at its inputs (see Figure 2), it slews the GATEx output such that the CSx voltage tracks the internally generated reference at its inverting input. Therefore, the linear voltage ramp at the IRAMP pin results in a linear current ramp to the three positive loads.

APPLICATION INFORMATION

The LCA reference ramp tracks the IRAMP pin voltage up to a level of $V_{O(IRAMP)} \cong 1.35$ V. This corresponds to the maximum sense voltage (VINx – CSx) of 20 mV (150 mV for Channel 4). If charging of the load input bulk capacitance completes during the constant di/dt section of channel turn-on (the set of dashed lines in Figure 20), the load current decays to the steady-state operating level. With decreasing load current, the CSx input is pulled to the VINx potential, and the pass MOSFET gate is driven to the LCA supply rail, fully enhancing the external MOSFET. However, under certain combinations of bulk capacitance, IMAX, and inrush di/dt relative values, the current ramp may reach the IMAX limit. The variable current source is switched out for the constant current source which sets the VMAX reference level (see Figure 2). This defines the third stage of the load current waveform. Load voltage ramping completes at the IMAX level, as shown by the set of solid lines in Figure 20. Again, once the current demand rolls off, the LCA drives the pass MOSFET gate high to fully enhance the MOSFET.

ramp-down sequence

A normal shutdown sequence occurs when the BD_SEL# input is brought high (greater than 2 V) with the output supplies in a healthy state (no overvoltage, undervoltage or overcurrent faults). HEALTHY# is deasserted and the back-end voltages are sequenced off in the reverse order of turn on: –12-V, 3.3-V, 5-V and 12-V (Channel 4, Channel 3, Channel 2 and then Channel 1). The turn off is also controlled by five pulses at the IRAMP pin. The first pulse, which is of short duration, disables the voltage fault monitoring on Channel 4 (–12 V). Starting with the second pulse, each supply is turned off in order. At the start of each pulse at IRAMP, voltage fault monitoring is disabled for the next successive channel to be turned off. The IRAMP capacitor is charged rapidly, up to the 1.5-V threshold, at which point the variable current source in the LCA block is reselected to generate the current limit reference. At the same time, the charging source at IRAMP is replaced with a 58-μA discharge load, such that the IRAMP capacitor is discharged at the same rate used for di/dt control during turn on. This causes the current limit to decrease linearly, so that available load current is forced off no faster than the falling edge at IRAMP. The LCA is disabled, and additional pull-downs applied to the GATEx pin, when either the output voltage has decayed to less than 0.9 V, or the IRAMP waveform has decayed to approximately 0.1 V. Under conditions of light loading during turn off, the bulk capacitance may hold up the back-end voltage even after the MOSFET switch is turned off. In this situation, the TPS2345 waits for load discharge to less than 0.9 V prior to proceeding to the next channel. Channel 4 is the exception to this operation; the VS4 status is not monitored during turn off, and the device sequences to Channel 3 turn-off once the second IRAMP pulse ends.

setting the sense resistor values

Due to the current limiting operation of the internal LCAs, the maximum allowable load current for the application is easily programmed by selecting the appropriate value sense resistors. The LCA acts to limit the CSx voltage (relative to VINx) to the internal reference, which during steady-state operation is VMAX. Therefore, a sense resistor for each channel can be calculated from equation (1).

$$R_{SNSx} = \frac{VMAXx}{IMAXx} \quad (1)$$

where

R_{SNSx} is the the sense resistor value for Channel x,

VMAXx is the IMAX sense voltage limit, and

IMAXx is the Channel x maximum load current.

APPLICATION INFORMATION

When setting the current limits, it is important to consider the device minimum that may be imposed by the TPS2345. Using the values given in the electrical tables, equations (2) through (4) follow from equation (1).

For Channel 1:

$$R_{SNS1} = \frac{16\ mV}{IMAX1} \quad (2)$$

For Channels 2 and 3:

$$R_{SNSx} = \frac{17\ mV}{IMAXx} \quad (3)$$

where:

x = 2 or 3.

For Channel 4:

$$R_{SNS4} = \frac{75\ mV}{IMAX4} \quad (4)$$

To ensure proper operation across the range of anticipated load currents on each channel, the maximum load under normal operating conditions must also be considered. To avoid current-limit operation during steady-state loading, the IMAX level must be set above the expected load. For example, if the 3.3-V (Channel 3) supply of the typical application diagram needs to deliver up to 6.5 A, and a 500-mA margin is desired, using equation (3) yields:

$$R3 = \frac{17\ mV}{7\ A} = 2.43\ m\Omega$$

This value is rounded up to 2.5 mΩ in the schematic. Similarly, for up to 600-mA capability on Channel 1, equation (2) indicates R1 ≅ 25 mΩ. Setting R4 = 250 mΩ, provides some margin over a 250 mA load. Also, these values limit the maximum load within the cPCI® specification limits.

setting the inrush slew rate

The TPS2345 is easily programmed for the desired maximum current slew rate during turn-on and turn-off events. A single capacitor at the IRAMP pin (C5 in the diagram) controls the di/dt for all three positive channels. Once the sense resistor values have been established, the value for C_{IRAMP}, in microfarads, can be determined from equation (5).

For Channels 1, 2, and 3:

$$C_{IRAMPx} = \frac{68}{67.5 \times R_{SNSx} \times \left(\frac{di}{dt}\right)_x} \quad (5)$$

where:

C_{IRAMPx} = the capacitor value indicated to achieve the (di/dt)x limit value,

R_{SNSx} = sense resistor in ohms and

$(di/dt)_x$ = the maximum di/dt rate, in amps/second.

APPLICATION INFORMATION

The CompactPCI® hot swap specification requires the following maximum slew rates for the input supplies (see Table 2).

Table 2. CompactPCI® Hot Swap Slew Rate Specifications

SUPPLY NAME	MAXIMUM SLEW RATE
5 V	1.5 A/ms
3.3 V	1.5 A/ms
12 V	150 mA/ms
–12 V	150 mA/ms

Since the 12-V supplies have the more stringent limit, they are useful for obtaining an initial estimate for the IRAMP capacitor. Using the 12-V supply values, equation (5) produces the result shown in equation (6).

$$C_{IRAMP1} = \frac{68}{67.5 \times (0.025\ \Omega) \times (150\ mA/ms)} \cong 0.27\ \mu F \quad (6)$$

A value of 0.27 μF can be used, or the next available standard value of 0.33 μF provides some margin for capacitor and sense-resistor tolerances. In either case, equation (5) can be rewritten as equation (7), which is used here to verify that the 5-V and 3.3-V slew rates are within specification.

$$(di/dt)_{2,3} = \frac{68}{67.5 \times R_{SNS2,3} \times C_{IRAMP}} \quad (7)$$

where:

$R_{SNS2,3}$ is in ohms,

C_{IRAMP} is in microfarads, and

$(di/dt)_{2,3}$ is given in amps/second.

For a C_{IRAMP} of 0.33 μF, the maximum di/dt for the 5-V and 3.3-V supplies is 1.02 A/ms and 1.22 A/ms, respectively, which is well within the cPCI® specification.

protection against faulted loads

The TPS2345 allows the time period of one IRAMP pulse for each back-end plane's voltage to ramp-up to its minimum level. After this delay period, the device latches off if an undervoltage fault is subsequently detected. This nominal delay time, t_{TIMER}, is set by the constant-current charging and subsequent discharging of C_{IRAMP}, and is therefore determined from equation (8).

$$t_{TIMER} = C_{IRAMP} \times 1.4 \times \left(\frac{1}{58} + \frac{1}{1.8}\right) \quad (8)$$

where:

C_{IRAMP} is in microfarads.

The resultant fault timer period should be sufficient for most applications; however, it is good design practice to verify that the delay is long enough for each load.

APPLICATION INFORMATION

Due to the potential three-phase nature of the load current ramp (refer to Figure 20), the increasing load voltage may also have three distinct periods. The first phase is during the slow turn-on period at the start of each IRAMP cycle. Depending on a number of factors, significant voltage ramping may or may not occur during this time. Also, any appreciable voltage ramp is more likely on the 3.3-V and 5-V loads. For verification of the fault timeout delay, the worst case situation is no appreciable load charging (i.e., a longer overall charge time); therefore it is assumed that no voltage ramp occurs here.

The next phase is the linear load current ramp period. For any device channel x, if the IMAX level is not reached while charging a given load capacitor of C_{Lx}, then the time to reach the input dc level, V_{INx}, is estimated by equation (9).

$$t_{SSx} = \sqrt{\frac{2 \times C_{Lx} \times C_{IRAMP} \times K_X \times R_{SNSx} \times V_{INx}}{58\ \mu A}} \tag{9}$$

where:

K_X = 67.5 for Channels 1, 2, and 3, and

K_X = 7.5 for Channel 4.

For example, assuming the 5-V back-end plane in this application has 220-µF bulk capacitance, the anticipated typical ramp-up time is about 1.6 ms.

During inrush slewing, the load current ramp tracks the voltage ramp on the IRAMP capacitor, up to a voltage of about 1.35 V on the IRAMP pin. Therefore, the time duration of this ramp activity, t_{IRAMP}, is given by equation (10).

$$t_{IRAMP} = \frac{C_{IRAMP} \times (1.25\ V)}{58} \tag{10}$$

where:

C_{IRAMP} is in microfarads.

If, for any channel, the time for soft-start charging of the load voltage is greater than the current ramp period, ($t_{SSx} > t_{IRAMP}$), back-end plane ramp-up completes at the dc IMAX level. In this case, the following procedure can be used to estimate load ramp-up time.

First, equation (11) is used to determine the load voltage level, $v_{Lx}(t)$, attained during the current ramp period.

$$v_{Lx}\left(t_{IRAMP}\right) = \frac{58\ \mu A}{2 \times C_{Lx} \times C_{IRAMP} \times K_X \times R_{SNSx}} \times \left(t_{IRAMP}\right)^2 \tag{11}$$

Once this voltage level is known, it can be used to estimate the additional charging time required at constant current to reach the input dc potential, t_{CCx}. This time is calculated from equation (12).

$$t_{CCx} = \frac{C_{Lx} \times \left(V_{INx} - V_{Lx}\left(t_{IRAMP}\right)\right)}{IMAXx} \tag{12}$$

The sum of t_{IRAMP} and t_{CCx} can then be used to estimate the total load ramp-up time for Channel x.

APPLICATION INFORMATION

precharge circuit

The PRECHG pin can be used to generate the 1-V bias voltage which precharges the CompactPCI® bus signals during hot swap events. The pin's output stage has both source and sink capability, enabling it to pull lines up from 0 V or down from V(I/O) as needed. Typically, each I/O line requiring precharge is isolated from the PRECHG source with a minimum 10-kΩ resistor (R_P in the typical application diagram). Depending on the signaling level of a particular system (5 V or 3.3 V), other requirements for precharge resistor value and disconnection may apply. Numerous manufacturers currently offer integrated bus switches that may be useful when disconnection is desired or required. A stub resistor (R8) is inserted in each I/O line as shown, which helps provide some series damping. The value of this resistor is specified as 10 Ω ±5%, placed within 0.6 inch of the connector.

generating LOCAL_PCI_RST#

The LOCAL_PCI_RST# signal used to initialize the plug-in's PCI device in CompactPCI® systems is easily generated from the TPS2345's HEALTHY# output using as few as two logic gates. A suggested solution is shown in Figure 21. The circuit functions such that LOCAL_PCI_RST# is asserted whenever back-end power is not healthy, regardless of the status of PCI_RST#. Texas Instruments and several other manufacturers produce a series of single-gate devices in small footprint, 5-pin packages. Table 3 lists some of the options available within three of the technologies available from TI: AHC, AHCT, and LVC. The applicable device numbers are shown sorted according to signaling environment and package type. Chip-scale packaging may also be available for the LVC types.

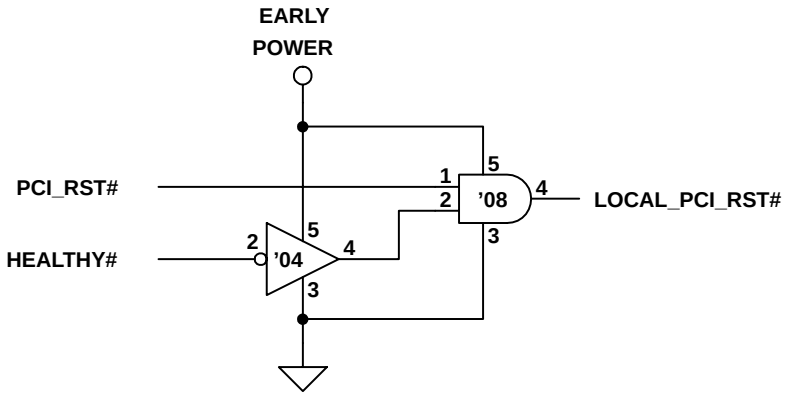


Figure 21. LOCAL_PCI_RST# Circuit

Table 3. Texas Instruments Little Logic Device Options

SIGNALING ENVIRONMENT	DEVICE	PACKAGED DEVICES	
		SOT–23 (DBV)	SC–70 (DCK)
5V	'04	SN74AHCT1G04DBVR	SN74AHCT1G04DCKR
	'08	SN74AHCT1G08DBVR	SN74AHCT1G08DCKR
3.3V	'04	SN74AHC1G04DBVR	SN74AHC1G04DCKR
	'08	SN74AHC1G08DBVR	SN74AHC1G08DCKR
	'04	SN74LVC1G04DBVR	SN74LVC1G04DCKR
	'08	SN74LVC1G08DBVR	SN74LVC1G08DCKR

APPLICATION INFORMATION

protecting the TPS2345 from voltage transients

Parasitic inductance associated with the power distribution network can cause large voltage spikes on the supply rails if the current is suddenly interrupted by the TPS2345 during a fault condition. It is important to protect the TPS2345 against such spikes to avoid device damage. There are several practices that provide sufficient protection.

- Clamp the voltage at the supply pins of the TPS2345 with Zener diodes. Since the absolute maximum voltage rating of the device is 15 V, this is most important on the 12-V and –12-V rails. The typical application diagram shows the connection of these devices (D1 and D2) in the circuit. The diodes should be placed close to the TPS2345, with short trace lengths back to the VINx and GND pins. The maximum breakdown of these devices must be less than 15 V to properly protect the TPS2345. Lower voltage Zeners can also be placed on the 5-V and 3.3-V pins if desired, but the steady-state operating level of these pins provides more margin from damage levels. In addition, it may be necessary to protect the sense inputs on the 12-V and –12-V back-end planes, VS1 and VS4, depending on the PCB characteristics.
- Use dedicated PCB planes for the four supplies and ground nodes and maximize the trace width of high-current runs to minimize inductance associated with the power distribution. This is recommended on both the backplane and plug-in modules.

layout considerations

To optimize the performance of the TPS2345, care should be taken to use good layout practice with the parts placement and etch routing of the hot swap circuit components. This includes any protection devices as well as the sense and pass elements. Protection devices should be located close to the hot swap controller, and trace-lengths back to their respective pins kept to a minimum. If a decoupling capacitor is used on the VIN1 supply, it also should be placed close to the part.

Mount the charge pump reservoir capacitor (C6 in the application diagram) close to the TPS2345, with minimal trace lengths back to the CPUMP and CPGND pins.

For proper operation, the three ground pins of the TPS2345 must be connected together near the device. The ground leads of the ramp and charge pump capacitors, protection diodes, and any decoupling capacitors should also tie into this node close to the part. This junction should be routed separately back to the J1 connector, where it can tie into the PCB GND node, as opposed to tying into the ground plane elsewhere in the high-current return path.

Use wide traces when connecting the sense resistors and power FETs into their respective current paths. When feeding these connections through from an internal power plane, use multiple vias to reduce the overall impedance of the current path. This helps reduce insertion loss across the hot swap interface, and improve the thermal performance of the PCB. Additional copper plane used on the land patterns of these devices can significantly reduce their thermal impedance, reducing temperature rise in the module and improving overall reliability of the power devices.

Connections to the sense resistors for the VINx and CSx device pins should be made with good Kelvin connections to optimize the accuracy of the current-limit thresholds and slew-rate control. This is especially important for the 5-V and 3.3-V sense connections. Because typical load levels on these supplies are so high, up to 10 A, board trace resistance between elements in the supply current paths becomes significant. The two sense traces for each supply should connect symmetrically to the sense resistor land pattern, in close proximity to the element leads, and not upstream or downstream from the device. Trace routing back to the TPS2345 should be fairly well balanced. Figure 22 illustrates two recommendations for the current sense layout.

APPLICATION INFORMATION

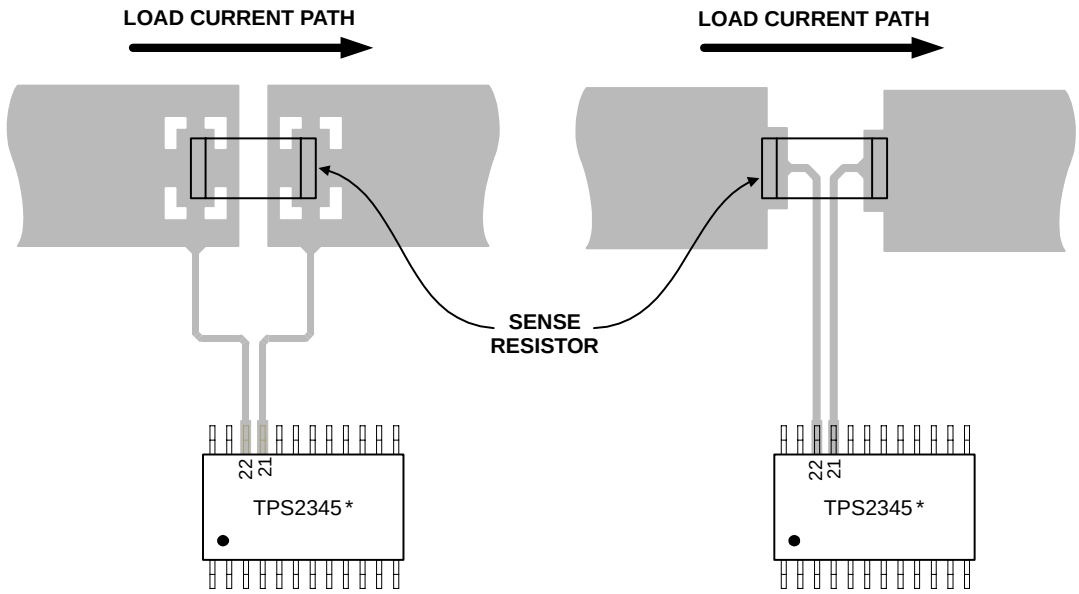


Figure 22. Recommended Layout for SMD Chip-Sense Resistor for 5-V Rail

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2345PW	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
TPS2345PWG4	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
TPS2345PWR	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
TPS2345PWRG4	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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