



# THE DATASHEET OF CD4029BCN



## CD4029BC Presettable Binary/Decade Up/Down Counter

### General Description

The CD4029BC is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1", the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0". Advancement is inhibited when either or both of these two inputs is at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both  $V_{DD}$  and  $V_{SS}$ .

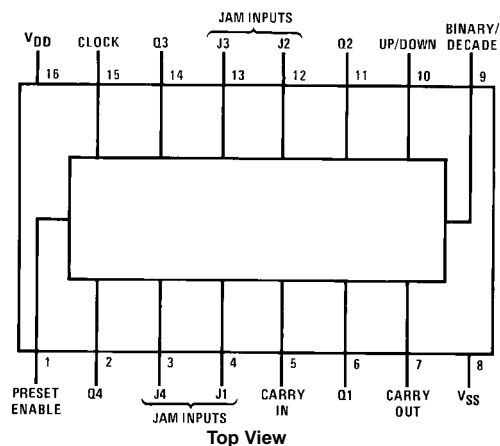
### Features

- Wide supply voltage range: 3V to 15V
- High noise immunity:  $0.45 V_{DD}$  (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- Parallel jam inputs
- Binary or BCD decade up/down counting

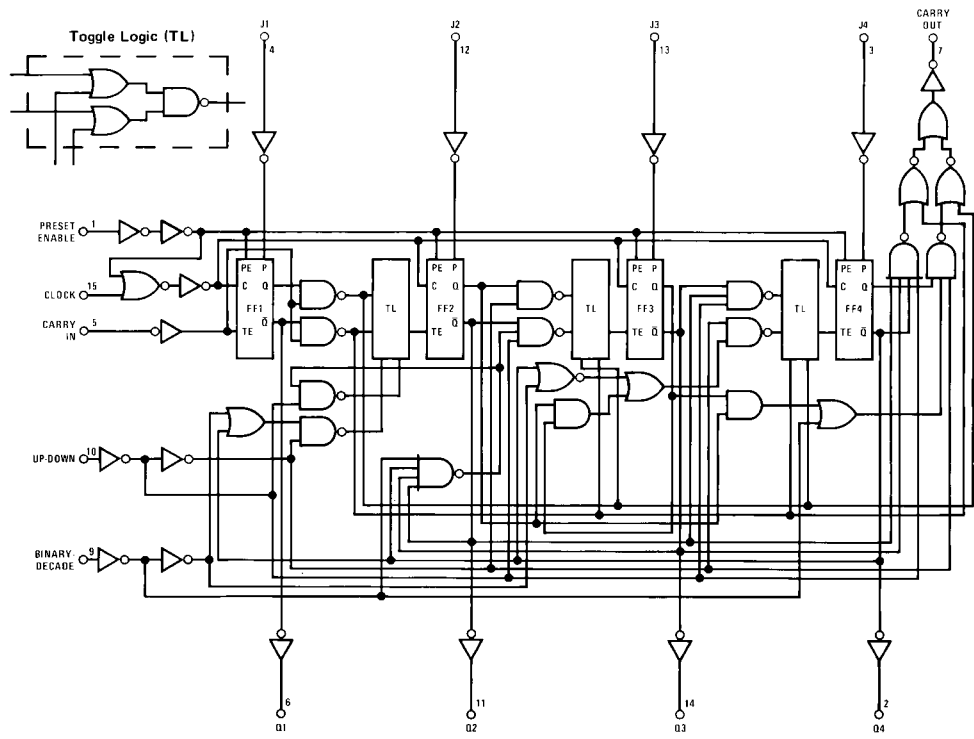
### Ordering Code:

Order Number	Package Number	Package Description
CD4029BCWM	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4029BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4029BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

### Connection Diagram



### Logic Diagram



<b>Absolute Maximum Ratings</b> (Note 1)		<b>Recommended Operating Conditions</b> (Note 2)	
(Note 2)			
DC Supply Voltage ( $V_{DD}$ )	-0.5V to +18 $V_{DC}$	DC Supply Voltage ( $V_{DD}$ )	3V to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD} + 0.5 V_{DC}$	Input Voltage ( $V_{IN}$ )	0V to $V_{DD} V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C	Operating Temperature Range ( $T_A$ )	-55°C to +125°C
Power Dissipation ( $P_D$ )		<b>Note 1:</b> "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.	
Dual-In-Line	700 mW	<b>Note 2:</b> $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature ( $T_L$ )			
(Soldering, 10 seconds)	260°C		

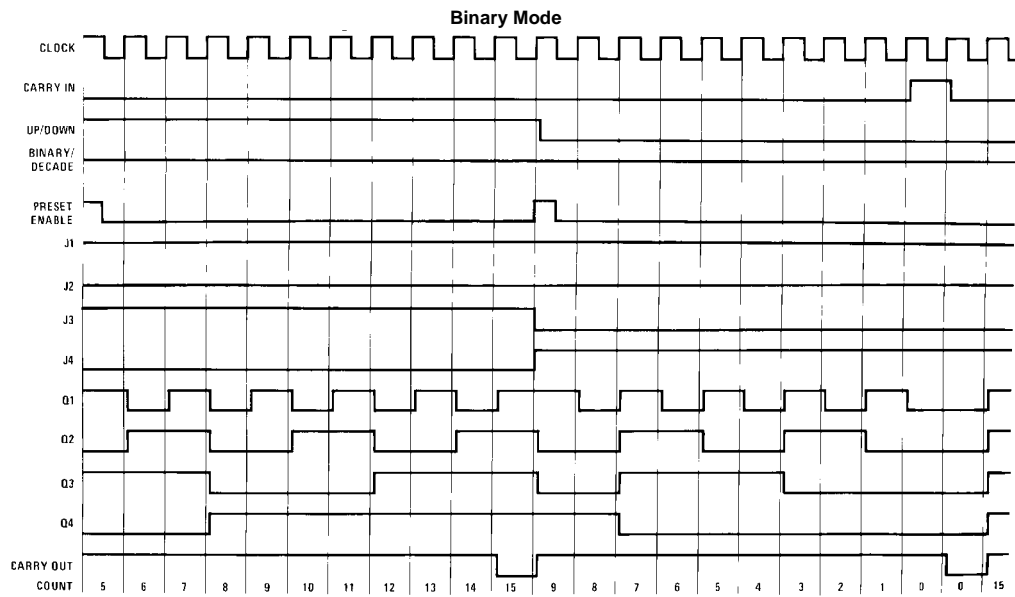
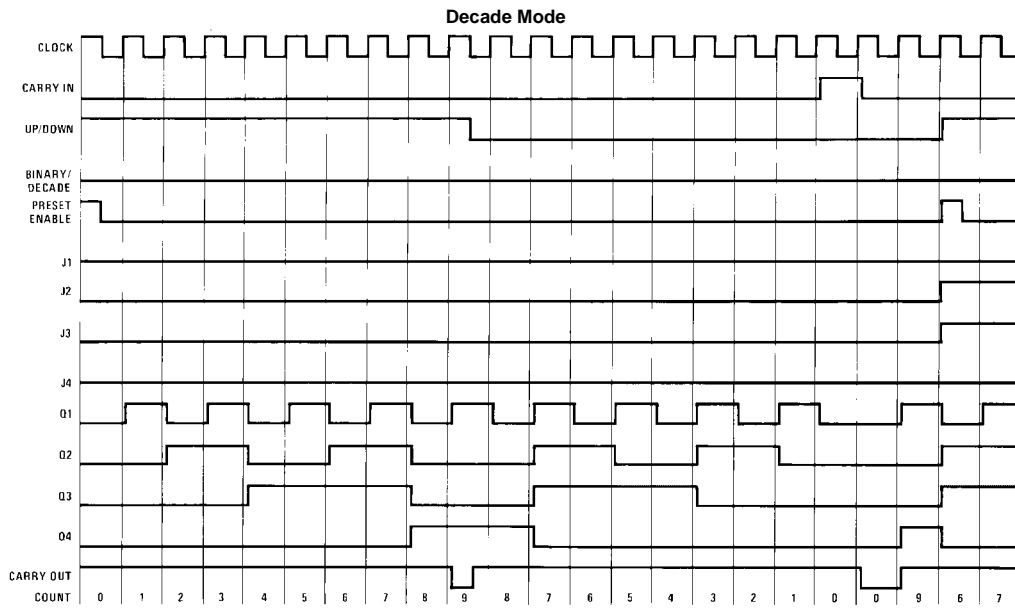
**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		5 10 20			5 10 20		150 300 600	$\mu A$
$V_{OL}$	LOW Level Output Voltage	$ I_{O}  < 1 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V
$V_{OH}$	HIGH Level Output Voltage	$ I_{O}  < 1 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95	5 10 15		4.95 9.95 14.95		V
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1V$ or 9V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V		1.5 3.0 4.0			1.5 3.0 4.0		1.5 3.0 4.0	V
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1V$ or 9V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0			3.5 7.0 11.0		V
$I_{OL}$	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4		mA
$I_{OH}$	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.64 -1.6 -4.2		-0.51 -1.3 -3.4	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.1 0.1		$-10^{-5}$ $10^{-5}$	-0.1 0.1		-1.0 1.0	$\mu A$

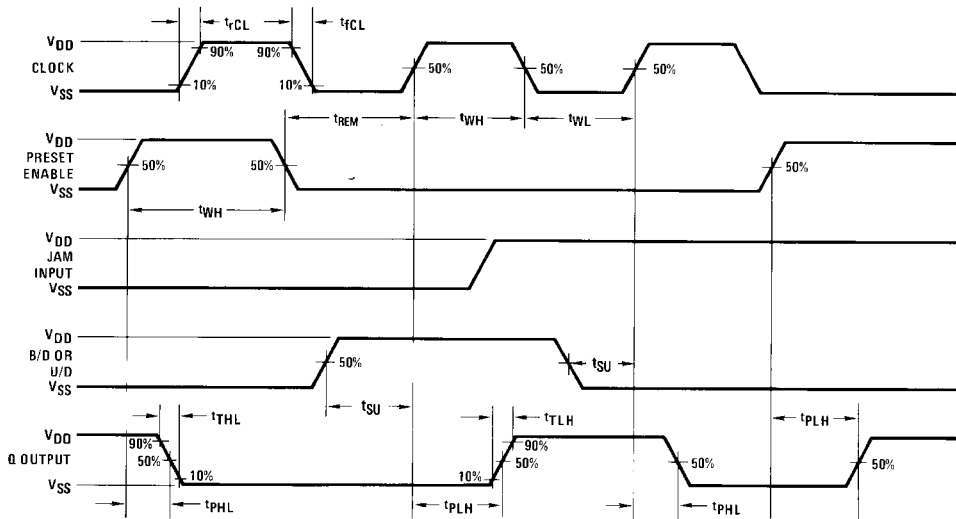
**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

AC Electrical Characteristics (Note 4)						
$T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , $R_L = 200\text{ k}$ , Input $t_{rCL} = t_{fCL} = 20\text{ ns}$ , unless otherwise specified						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CLOCKED OPERATION</b>						
$t_{PHL}$ or $t_{PLH}$	Propagation Delay Time to Q Outputs	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 85 70	400 170 140	ns
$t_{PHL}$ or $t_{PLH}$	Propagation Delay Time to Carry Output	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		320 135 110	640 270 220	ns
$t_{PHL}$ or $t_{PLH}$	Propagation Delay Time to Carry Output	$C_L = 15\text{ pF}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		285 120 95	570 240 190	ns
$t_{THL}$ or $t_{TLH}$	Transition Time/Q or Carry Output	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns
$t_{WH}$ or $t_{WL}$	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		160 70 55	320 135 110	ns
$t_{rCL}$ or $t_{fCL}$	Maximum Clock Rise and Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	15 10 5			$\mu\text{s}$
$t_{SU}$	Minimum Set-Up Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		180 70 55	360 140 110	ns
$f_{CL}$	Maximum Clock Frequency	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	1.5 3.7 4.5	3.1 7.4 9		MHz
$C_{IN}$	Average Input Capacitance	Any Input		5	7.5	pF
$C_{PD}$	Power Dissipation Capacitance	Per Package (Note 5)		65		pF
<b>PRESET ENABLE OPERATION</b>						
$t_{PHL}$ or $t_{PLH}$	Propagation Delay Time to Q output	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		285 115 95	570 230 195	ns
$t_{PHL}$ or $t_{PLH}$	Propagation Delay Time to Carry Output	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		400 165 135	800 330 260	ns
$t_{WH}$	Minimum Preset Enable Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		80 30 25	160 60 50	ns
$t_{REM}$	Minimum Preset Enable Removal Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		150 60 50	300 120 100	ns
<b>CARRY INPUT OPERATION</b>						
$t_{PHL}$ or $t_{PLH}$	Propagation Delay Time to Carry Output	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		265 110 90	530 220 180	ns
$t_{PHL}$ , $t_{PLH}$	Propagation Delay Time to Carry Output	$C_L = 15\text{ pF}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 85 70	400 170 140	ns
<b>Note 4:</b> *AC Parameters are guaranteed by DC correlated testing.						
<b>Note 5:</b> $C_{PD}$ determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application note, AN-90.						

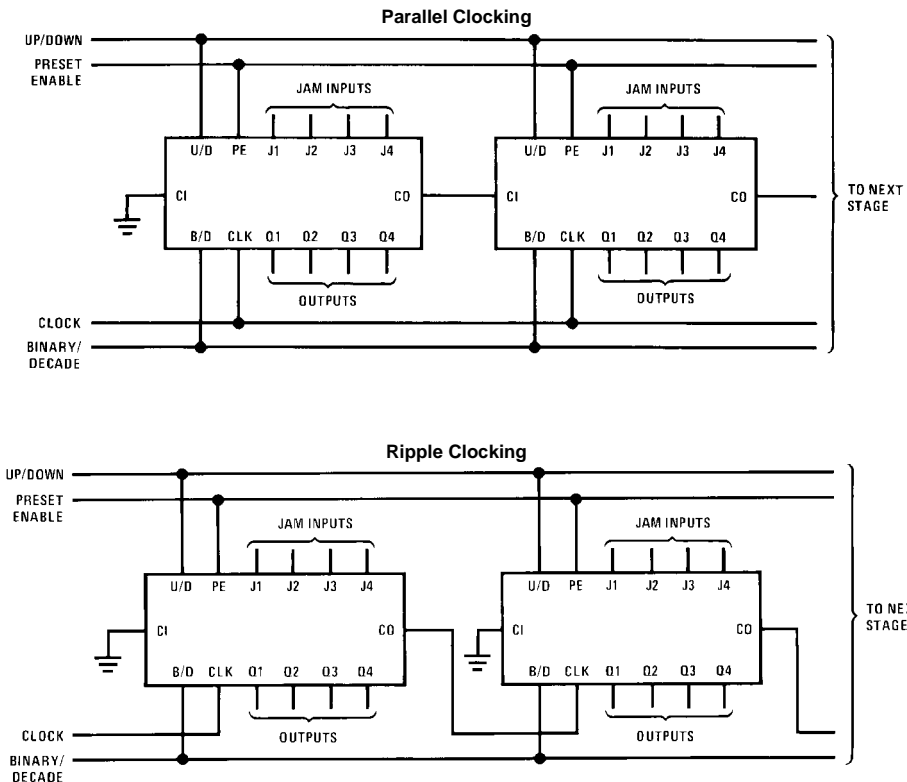
Logic Waveforms



### Switching Time Waveforms

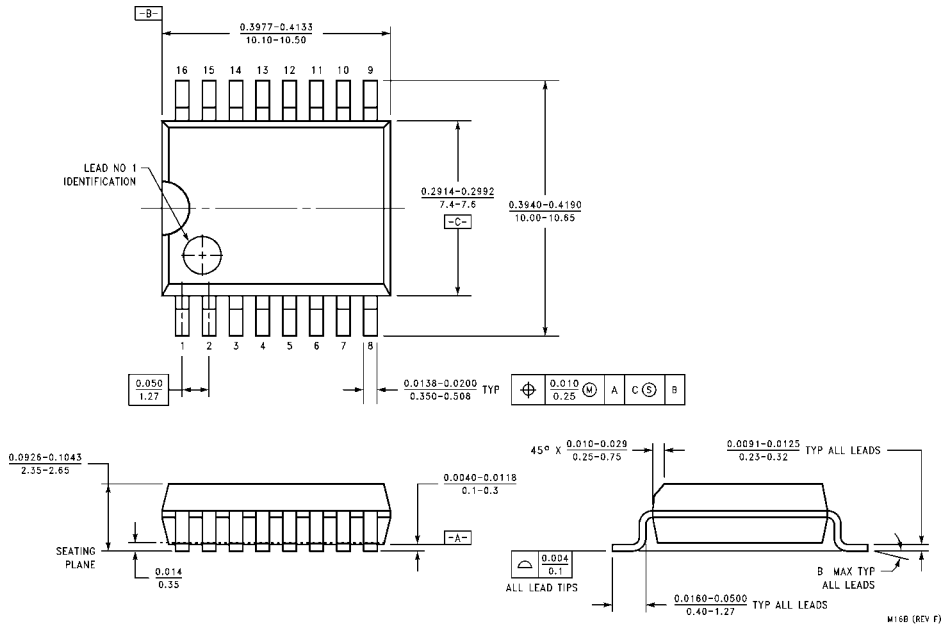


### Cascading Packages



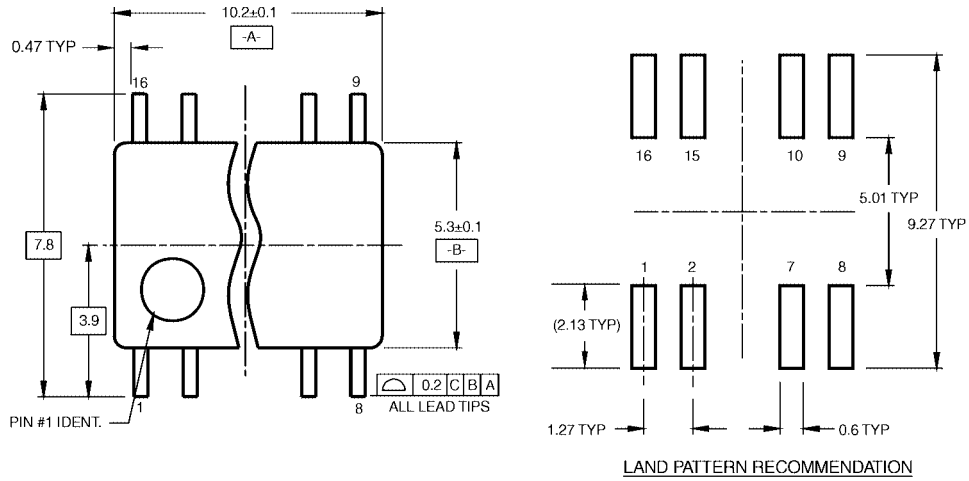
Carry out lines at the 2nd or later stages may have a negative-going spike due to differential internal delays. These spikes do not affect counter operation, but if the carry out is used to trigger external circuitry the carry out should be gated with the clock.

**Physical Dimensions** inches (millimeters) unless otherwise noted



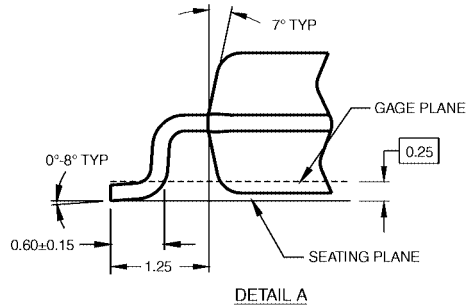
**16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M16B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1





**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**



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